A Seven-Level VSI With a Front-End Cascaded Three-Level Inverter and Flying-Capacitor-Fed H-Bridge

Tirupathi Abhilash, Kirubakaran Annamalai, *Senior Member, IEEE*, and Somasekhar Veeramraju Tirumala, *Member, IEEE*

***Abstract*—Multilevel inverters (MLIs) are playing a pivotal role in the power sector with potential applications, such as interfacing renewable energy sources with the grid and several industrial drive applications. MLIs with a smaller number of switching devices are more promising due to their compact size, reduced cost, and higher efficiency compared with their traditional counterparts. This paper, therefore, presents a new three-phase seven-level inverter. This topology is a combination of two cascade-connected two-level voltage-source inverters (VSIs) and H-bridge cells with flying capacitors (FCs). This paper presents the operating principle and the balancing technique for the dc-link capacitors and FCs. The generation of various output voltage levels and the limitation of the sinusoidal pulsewidth modulation control for FC voltage balancing is also presented. The number of components in the proposed circuit configuration and their voltage ratings are considerably lower compared with the recently proposed topologies. The behavior of the proposed circuit configuration is first assessed with simulation studies and is then tested with a laboratory prototype. The simulation and experimental results validate the effectiveness of the proposed topology and the voltage balancing technique.**

***Index Terms*—Capacitor voltage balancing, flying capacitor, medium voltage, multilevel inverter, three-level inverter.**

I. Introduction

CONTEMPORARY research on multilevel inverters (MLIs) aims to improve power circuit configurations to obtain higher efficiency, reliability, spectral performance, and operability from high-voltage dc input. To this end, attempts are being made to reduce the device count, as it would directly influence the aspects of cost, efficiency, and reliability. With MLIs, the higher output voltage is derived from voltage sources and power semiconductor switching devices of lower voltage ratings. MLIs also synthesize stepped output voltage waveforms, which are close to the sinusoidal wave increasing the spectral quality.

MLIs are likely to be used extensively for large capacity power generation using renewable energy sources [1]–[3]. The lower voltage and power ratings of photovoltaic and fuel cells can easily be connected in series and parallel to increase the power and voltage levels for the grid-connected applications. MLIs also facilitate to handle large dc-link voltages with reduced device stress and reduced harmonics for high- and medium-voltage applications.

The most significant topologies pertaining to MLIs are the following:

i) neutral point clamped (NPC),
ii) flying capacitor (FC), and
iii) cascaded H-bridge (CHB) inverters [4]–[8].

These topologies are well suited for medium- and high-voltage applications. However, these topologies have restricted applicability for relatively lower ratings due to their inherent drawbacks, such as the requirement of more clamping diodes and FCs in NPC and FC converters, respectively. The FC topology can be used for higher power levels with the aid of auxiliary voltage balancing circuits or modified control schemes. The requirement of separate dc sources for each H-bridge in CHB leads to more components for the increased number of levels and also leads to complexity in control. In order to balance the dc-link capacitor voltages, an active front-end boost converter with an additional balancing circuit is presented in [9]. Recently, a novel six-level inverter using two-level cell and three-level FC cell is proposed in [10]. However, it demands additional circuitry to provide unequal dc-link capacitor voltages leading to higher component count, bulkiness, and reduced efficiency.

Many novel symmetrical, asymmetrical, and hybrid converters have been reported in the literature to overcome the limitations of the conventional topologies [11]–[13]. Among these, asymmetrical MLIs with unequal voltages give higher output levels compared with the symmetrical configurations. However, these topologies demand more dc sources compared with NPC and FC inverters. Replacing these dc sources with capacitors, and natural balancing in voltage control will reduce the overall size and cost of the system. However, these topologies result in poor response during the transient conditions. A five-level inverter topology, which overcomes these limitations, is presented

Manuscript received June 21, 2018; revised October 18, 2018; accepted June 24, 2019. Date of publication August 4, 2019; date of current version October 18, 2019. Paper 2018-IPCC-0676.R1, presented at the 2019 IEEE International Conference on Environment and Electrical Engineering and 2019 IEEE Industrial and Commercial Power Systems Europe, Genova, Italy, Jun. 10–14, approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. *(Corresponding author: Kirubakaran Annamalai.)*

The authors are with the Department of Electrical Engineering, National Institute of Technology Warangal, Warangal 506004, India (e-mail: abhigate4ever@gmail.com; kiruba81@nitw.ac.in; sekhar@nitw.ac.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIA.2019.2933378

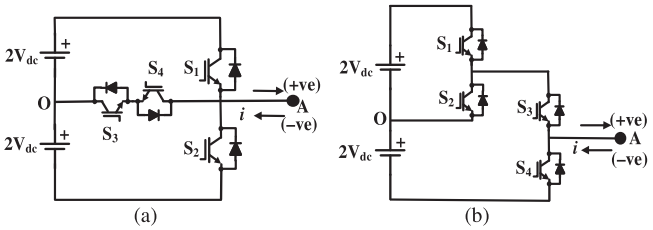


Fig. 1. Three-level inverters. (a) T-type topology. (b) Cascaded three-level inverter topology.

in [14], which consists of a three-level (3L) active NPC (ANPC) converter with FC along with voltage balancing technique. Another Phase-shifted pulsewidth modulation (PWM) with a proportional controller is developed for a three-phase five-level FC-MLI to balance the FC voltages during the transient states [15]. However, the selection of the size of the FC and control strategy plays a crucial role in this topology, to ensure the quality of the output.

Modular multilevel inverter configurations are relatively new entrants into the arena of three-phase applications. It is not only possible but is also desirable to operate a modular multilevel inverter with multiple dc sources (one per cell) in applications, such as HVDC. However, the need for separate dc sources in each two-level cell could be a limiting factor for modular multilevel configurations for low- and medium-power applications [16]. A new configuration of a T-type three-level inverter and 7L-ANPC for three-phase applications are reported in [17] and [18] with the merits of low conduction losses and high efficiency. Recently, a hybrid three-phase seven-level inverter was proposed in [19] with the combination of T-type converter and H-bridge inverter, which is also referred to as hybrid seven-level converter (H7LC). In this circuit configuration, the T-type converter in each phase requires two devices (S_1 and S_2), which must be rated to block the voltage of $4V_{\rm dc}$ (the switching devices, which connect the pole point to the positive as well as the negative dc rails), as shown in Fig. 1(a). Similarly, a modified hybrid topology, which is derived from the T-type converter, is reported in [20]. The advantage of this configuration is that the blocking voltage is reduced to half as compared with the T-type topology. Reduction in dc-link blocking voltage will significantly reduce the rating of the devices and the losses considerably. However, it demands more switch count. These limitations clearly spell out the motivation to improvise the existing hybrid multilevel inverter topologies. It can also be noticed that the development of various circuit configurations is based on three major factors, namely

1) reduction in device count,
2) balancing of the dc-link and/or the FC voltages,
3) avoidance of extra components for balancing circuits.

Realization of these objectives results in lesser weight, volume, cost, and higher efficiency of the configurations.

In this paper, a new three-phase hybrid cascaded seven-level inverter is proposed with the inherent benefits of a reduced number of power semiconductor switching devices and a *single dc source*. The proposed topology uses a cascaded three-level inverter, as shown in Fig. 1(b), which provides a common dc link that is combined with an H-bridge containing FC.

The proposed structure has four advantages compared with the H7LC and the other three conventional circuits (NPC, FC, and CHB), which are as follows:

1) the need of only one high-voltage switch of $4V_{\rm dc}$ rating, i.e., S_4 in each phase (compared with two in the T-type);
2) reduced component count of 24 compared with 36 switches of NPC, FC, and CHB;
3) higher efficiency compared with all these topologies; and
4) reduced dc-link voltage compared with the conventional circuits.

Moreover, the balancing of the dc link and the FC voltages is ensured in the proposed MLI.

This paper also presents a detailed discussion on the control strategy that is employed for balancing the voltages across the dc-link capacitors and FCs. Furthermore, a comparison is made with other recently proposed topologies to show the effectiveness of this circuit configuration in terms of the reduced parts count and the voltage rating of the switching devices. The performance of the proposed topology for different modulation indices with *R–L* load is assessed with the aid of simulation studies. The simulation studies are validated by a laboratory prototype.

II. Proposed Topology and Operating Principles

A. Novel Seven-Level Hybrid Converter

Fig. 2 depicts the proposed three-phase hybrid cascaded multilevel inverter. The proposed topology is capable of generating a seven-level inverter output voltage with reduced switching devices. This configuration, which employs a common dc link, is built by connecting an H-bridge cell with an FC at the output of the cascaded three-level inverter structure proposed in [21], [36], and [37].

Each of the common dc-link capacitors C_{d1} and C_{d2} are charged to a voltage of $2V_{\rm dc}$, whereas each of the FCs C_a, C_b, and C_c connected in H-bridges are charged to a voltage of $V_{\rm dc}$. These capacitors, with the appropriate operation of the switching devices, generates seven levels in pole voltages V_{XO} (X = A, B, C) in the range of $-3V_{\rm dc}$ to $+3V_{\rm dc}$. The cascaded three-level structure, shown in Fig. 3, generates voltage levels of $-2V_{\rm dc}$, 0, and $+2V_{\rm dc}$ across $V_{\rm A'O}$, which are input to the H-bridge cell. The H-bridge cell generates voltage levels of $-V_{\rm dc}$, 0, and $+V_{\rm dc}$ across $V_{AA'}$. Hence, the resultant pole-voltage V_{AO} consists of symmetrical seven levels, i.e., $-3V_{\rm dc}$, $-2V_{\rm dc}$, $-V_{\rm dc}$, 0, $V_{\rm dc}$, $2V_{\rm dc}$ and $3V_{\rm dc}$. The load terminals A, B, and C in each phase are connected to a Y-connected *R–L* load, which forms a neutral point N, as shown in Fig. 2. The proposed topology is implemented with only one dc source at the dc link with a voltage of $4V_{\rm dc}$, and the FC voltages are balanced by using the redundant switching states without any front-end source. A separate control strategy is developed for balancing the dc-link capacitor voltages.

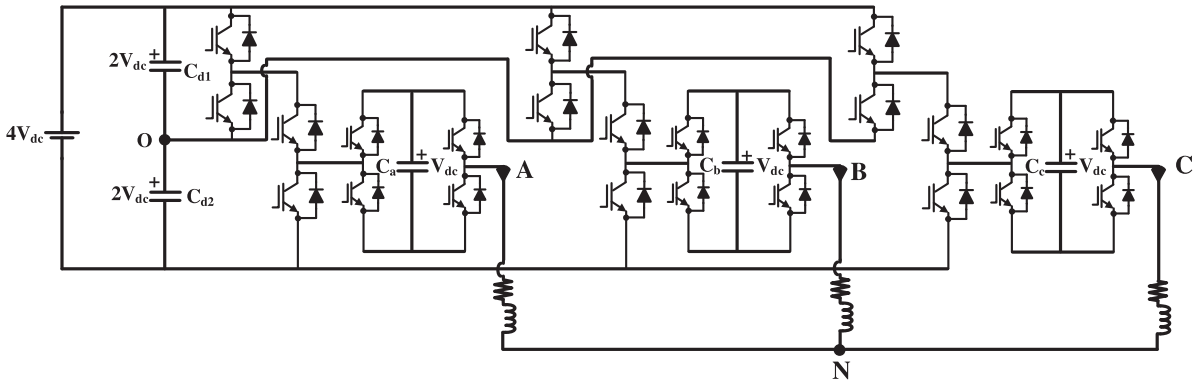


Fig. 2. Proposed topology.

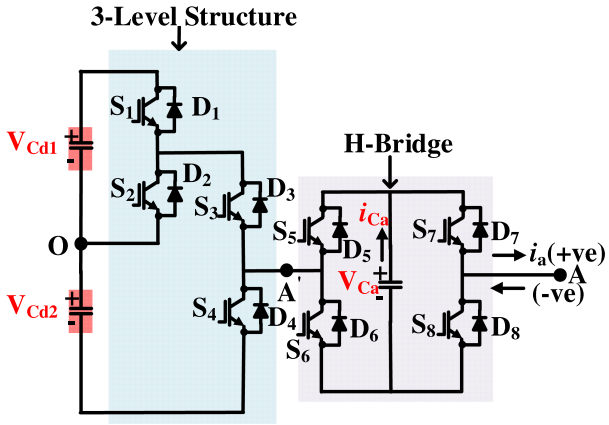


Fig. 3. Single-phase diagram of the proposed seven-level inverter.

Fig. 3 illustrates the phase-A of the proposed seven-level inverter. Switches S_1, $S_2, \ldots$, S_8 are the power MOSFETs. D_1, $D_2, \ldots$, D_8 are the body diodes or antiparallel diodes of the switches S_1, $S_2, \ldots$, S_8, respectively. It may be noted that the voltage ratings of the switches are not identical in the proposed topology. The switching devices, which constitute the H-bridge, (i.e., S_5, S_6, S_7, and S_8) require to be rated for $V_{\rm dc}$. Three switches (S_1, S_2, and S_3) should have a voltage rating of $2V_{\rm dc}$, whereas switch S_4 is to be rated for a voltage of $4V_{\rm dc}$. This means that in the 3-phase configuration (see Fig. 2), 12 switches are rated for$V_{\rm dc}$, 9 switches are rated for $2V_{\rm dc}$, and 3 are rated for. The decrease in modulation index (m_a) will vary the output pole voltages from seven levels to five levels and further to three levels. The blocking voltage of the switches depends on the type of the topology and the magnitude of the dc-link voltage. Therefore, the blocking voltage of the switches is completely independent of m_a. The following section describes the methodology of operating these switching devices to generate various voltage levels.

B. Operating Modes

The working principle of the proposed topology is explained through the following seven modes of operation for various output voltage levels. Fig. 4 presents these modes along with the details concerning the conducting devices and the direction of the load current (i_A).

Mode 0 [$V_{AO} = 0$]: In this mode, at zero output voltage, S_2 and S_3 are continuously gated along with the sets of either S_5 and S_7 or S_6 and S_8. To facilitate a better utilization of the switching devices, the combinations of S_5 and S_7 and S_6 and S_8 are gated during positive and negative half-cycles, respectively. The conduction of either a switch or its antiparallel diode is decided by the direction of i_A.

In the case of the positive zero crossing of the pole voltage, $V_{AO} = 0^+$, and if i_A is positive (+ve), D_2, S_3, D_5, and S_7 conduct, as shown in Fig. 4(i). However, for a lagging operation, i_A would be negative (–ve) when $V_{AO} = 0^+$. In such a case, the conducting devices would be D_7, S_5, D_3, and S_2. Similarly, for negative zero crossing i.e., $V_{AO} = 0^-$ and i_A is +ve; the path for the current is through D_2, S_3, S_6, and D_8. But for lagging loads, i_A is generally +ve when $V_{AO} = 0^-$. Hence, the conducting devices are S_8, D_6, D_3, and S_2. This clearly shows that the proposed power circuit configuration is capable of handling all the four quadrants in the $V_{AO} - i_A$ plane.

Mode-1 $[V_{AO} = V_{dc}]$*:* In this mode of operation, voltage balancing of the FC is to be ensured to generate the level of $+V_{\rm dc}$ without distortion. Hence, the switch S_3 is continuously triggered.

Case 1: If S_2, S_6, and S_7 are gated, $V_{AO} = V_{Ca}$. Assuming that C_a is initially charged to $V_{\rm dc}$ (as the polarity shown in Fig. 3), then $V_{AO} = V_{\rm dc}$. Here, the use of the FC reduces the need of additional dc source in each phase, which is an advantage of the proposed system. However, a proper switching sequence should be adopted to balance the capacitor voltages during the charging and discharging modes of operation. When i_A is +ve, C_a discharges; the conducting devices are: D_2, S_3, S_6, and S_7. When i_A is –ve, C_a charges through the conducting devices D_7, D_6, D_3, and S_2.

Case 2: If S_1, S_5, and S_8 are gated, then $V_{AO} = V_{Cd1} - V_{Ca}$. Assuming that C_{d1} and C_a are initially charged to $2V_{\rm dc}$ and $V_{\rm dc}$ (as the polarity shown in Fig. 3), then the output voltage becomes $V_{AO} = V_{\rm dc}$. The capacitor C_a gets charged when i_A is +ve, and the conducting devices are S_1, S_3, D_5, and D_8. The

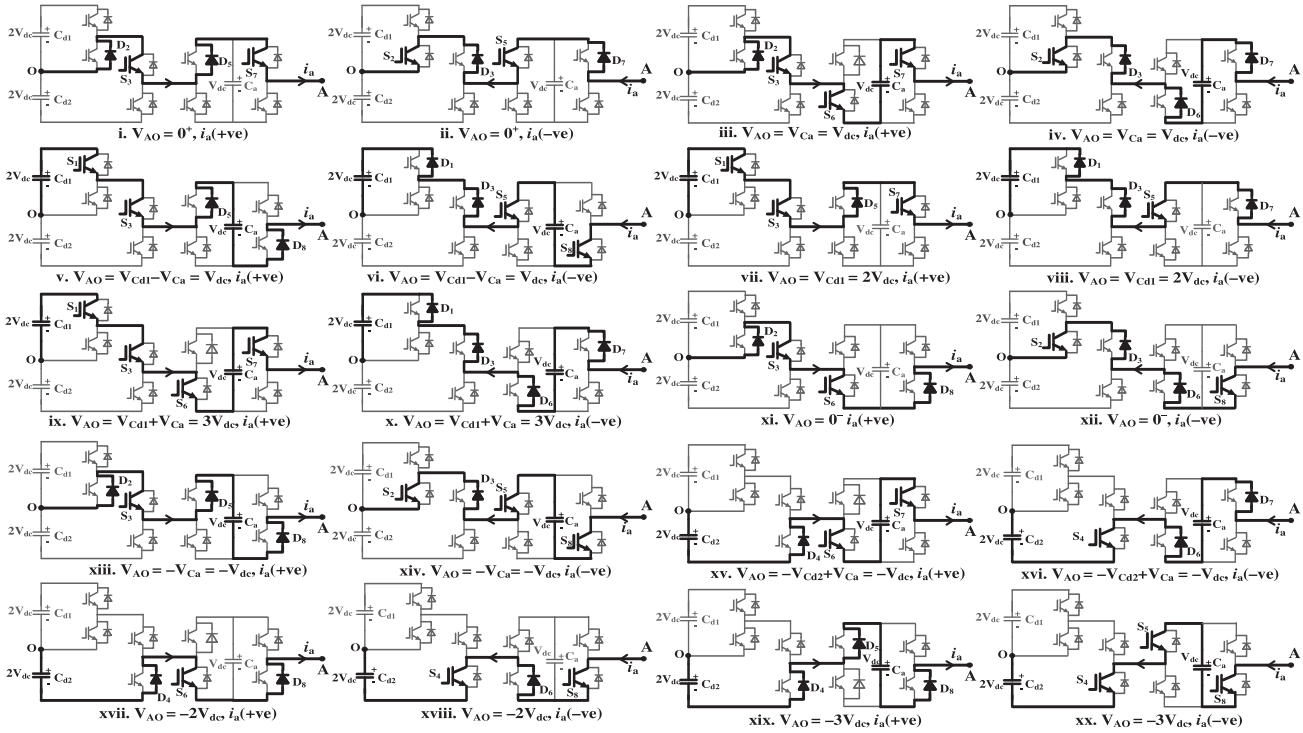


Fig. 4. Different modes of seven-level operation of phase-A.

capacitor C_a gets discharged when i_A is –ve, and the conducting devices are S_8, S_5, D_3, and D_1. Thus, in this mode of operation, by continually switching among case 1 and case 2, the FC voltage can be maintained at the level of $V_{\rm dc}$.

Mode-2 $[V_{AO} = 2V_{dc}]$*:* In this mode of operation, the FC is made to float and is therefore called the *Floating Mode*. The switches S_1, S_3, S_5, and S_7 are continuously triggered, as a consequence of which, the load is directly clamped to the dc-link capacitor C_{d1}. This makes $V_{AO} = V_{Cd1} = 2V_{\rm dc}$. It may be noted that the devices S_1, S_3, D_5, and S_7 conduct when i_A is +ve. Similarly, the devices D_7, S_5, D_3, and D_1 conduct when i_A is –ve.

Mode-3 $[V_{AO} = 3V_{dc}]$ In this mode, the discharging of the FC is addressed. Switches S_1, S_3, S_6, and S_7 are continuously triggered to produce $V_{AO} = V_{Cd1} + V_{Ca}$. Also, either the sets of devices S_1, S_3, S_6, and S_7 or D_7, D_6, D_3, and D_1 conduct for the positive and the negative load currents, respectively. The positive current discharges the FC, whereas the negative current charges it. Since $3V_{\rm dc}$ is the peak voltage level, the current is usually positive, which results in the discharging of the FC.

Mode-4 $[V_{AO} = -V_{dc}]$*:* This mode is similar to mode 1, and the process of charging and discharging are addressed in the following case 1 and case 2.

Case 1: If S_2, S_3, S_5, and S_8 are gated, $V_{AO} = -V_{Ca}$. Assuming that the capacitor C_a is initially charged to $V_{\rm dc}$ (as the polarity shown in Fig. 3), then $V_{AO} = -V_{\rm dc}$. Assuming that i_A is +ve, C_a charges; the conducting devices are D_2, S_3, D_5, and D_8. When i_A is –ve, C_a discharges through the conducting devices S_8, S_5, D_3, and S_2.

Case 2: If S_4, S_6, and S_7 are gated, $V_{AO} = V_{Ca} - V_{Cd2}$. Assuming that the capacitors C_{d2} and C_a are initially charged to $2V_{\rm dc}$ and $V_{\rm dc}$, respectively (as the polarity is shown in Fig. 3), then $V_{AO} = -V_{\rm dc}$. When i_A is +ve, C_a discharges; the conducting devices are D_4, S_6, and S_7. When i_A is –ve, C_a charges, and the conducting devices are D_7, D_6, and S_4. Thus, by toggling among these two cases, it is possible to maintain the FC voltage at a level of $V_{\rm dc}$.

Mode-5 $[V_{AO} = -2V_{dc}]$*:* Again, this mode is the *floating mode* for the FCs. In this mode of operation, switches S_4, S_6, and S_8 are continuously triggered, and the load is clamped to the dc-link capacitor C_{d2} to produce $V_{AO} = -V_{Cd2} = -2V_{\rm dc}$. It may be observed that the devices D_4, S_6, and D_8 conduct when i_A is +ve, whereas the devices S_8, D_6, and S_4 conduct when i_A is –ve.

Mode-6 $[V_{AO} = -3V_{dc}]$*:* In this mode, the FC discharges and is therefore called as FC *discharging mode*. In this mode of operation, $V_{AO} = -(V_{Cd2} + V_{Ca})$ and the switches S_4, S_5, and S_8 are gated. The devices D_4, D_5, and D_8 conduct when i_A is +ve. Similarly, the devices S_8, S_5, and S_4 conduct when i_A is –ve.

Table I presents the switching sequences for the generation of all of the seven levels. The digits "1" and "0" represent the switching states of ON and OFF, respectively. The pole voltage measured between phase-A and dc neutral point-O is equal to V_{AO}. In this configuration, the FC voltage balancing is carried out with the use of available redundant switching states at $V_{\rm dc}$ and $-V_{\rm dc}$ levels. The charging and discharging modes are decided by the direction of current and the employment of the

TABLE I
EFFECT OF THE SWITCHING STATES OF THE SEVEN-LEVEL INVERTER ON FC OF PHASE-A

V_{A0} (V)	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	i_A	(a)	(b)	(c)
$3V_{dc}$	1	0	1	0	0	1	1	0	>0	D	4	V_4
									<0	C		
$2V_{dc}$	1	0	1	0	1	0	1	0	--	N.E	4	V_3
	0	1	1	0	0	1	1	0	>0	D	4	V_2
V_{dc}									<0	C		
	1	0	1	0	1	0	0	1	>0	C	4	V_1
									<0	D		
0^+	0	1	1	0	1	0	1	0	--	N.E	4	V_0
0^-	0	1	1	0	0	1	0	1				
$-V_{dc}$	0	1	1	0	1	0	0	1	>0	C	4	V_5
									<0	D		
	0	0	0	1	0	1	1	0	>0	D	3	V_6
									<0	C		
$-2V_{dc}$	0	0	0	1	0	1	0	1	--	N.E	3	V_7
$-3V_{dc}$	0	0	0	1	1	0	0	1	>0	C	3	V_8
									<0	D		

Note. C, charging; D, discharging; N.E., no effect.
*(a)—status of C_a.
**(b)—number of ON switches/phase
***(c)—switching state.

redundant switching states. If a given switching state charges the FC, then its redundant state has the tendency of discharging it. However, for the switching states V_0, V_3, and V_7, the FC voltage will not be affected due to the diversion of current paths. From Table I, it may be observed that a maximum of 12 (i.e., 4×3) devices, out of 24, conduct in any given mode. One may, therefore, expect a higher efficiency with the proposed topology on account of lower conduction losses of the switching devices.

III. MODULATION TECHNIQUE AND DC-LINK CAPACITOR VOLTAGE BALANCING

A. PWM Technique

The selection of a PWM scheme also plays an important role in the performance of an MLI. Among various Sine-triangle PWM methods, the level-shifted in-phase disposition (LSIPD) sinusoidal PWM (SPWM) [22], [23] technique is adopted in the present study, which can result in the lowest harmonic content [24]. Fig. 5 illustrates the schematic diagram of LSIPD-SPWM. The gate pulses are generated by using a fundamental sine wave and six LSIPD carrier waves, and the corresponding output pulses for each voltage level for one complete cycle is given in Fig. 5. With the help of an field-programmable gate array (FPGA), the required pulse pattern is generated to produce the seven-level output.

B. DC-Link Capacitor Voltage Balancing and the Design of DC-Link Capacitors

The balancing of the dc-link capacitor voltages is very important to improve the quality of the output. The given single $4V_{\rm dc}$ dc supply is split into two $2V_{\rm dc}$ across the capacitors (C_{d1} and C_{d2}). In order to balance the dc-link capacitor voltages (V_{Cd1} and V_{Cd2}), a simple controller is developed, and its offset error is added with the reference fundamental signals. Fig. 6

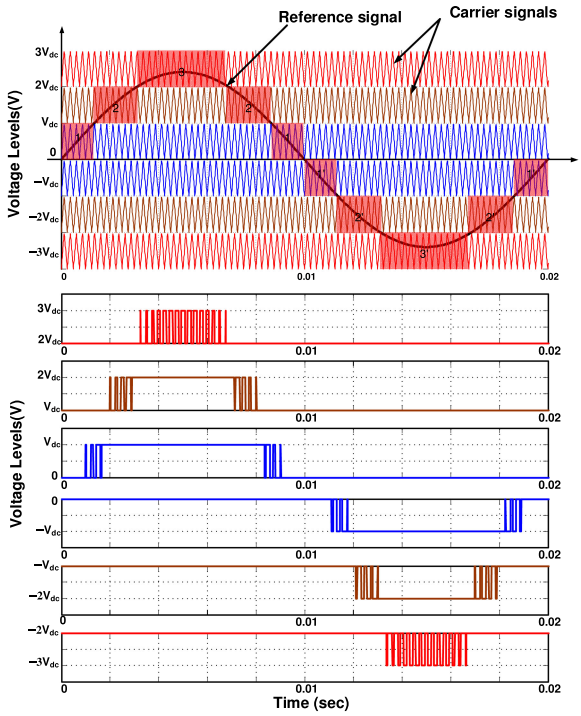


Fig. 5. LSIPD-SPWM scheme for seven-level generation.

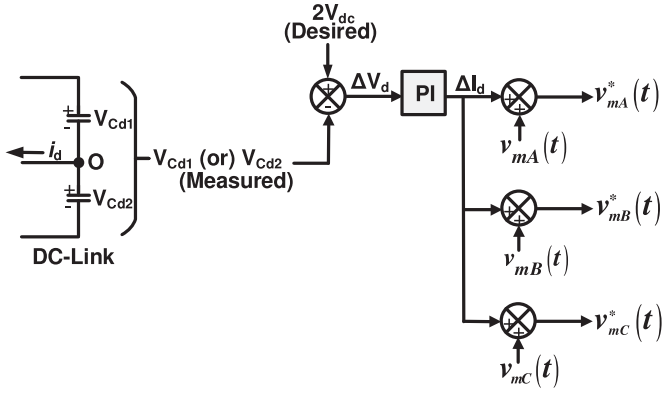


Fig. 6. DC-link capacitor voltage control.

depicts the developed control strategy to balance the dc-link capacitor voltages. It can be noticed that this controller can be implemented with the measurement of the voltage across one of the dc-link capacitors to maintain the desired voltage magnitude of $2V_{\rm dc}$. Suppose, if $V_{Cd1} < 2V_{\rm dc}$, then the error ΔV_d is positive, which charges the top capacitor C_{d1} and discharges C_{d2} until V_{Cd1} become $2V_{\rm dc}$. Otherwise, if ΔV_d is negative, then it discharges the top capacitor C_{d1} and charges C_{d2}. Here, the relationship between ΔV_d and ΔI_d can be derived as per the expressions reported in [32] and [33] as follows:

$$C_{d1}\frac{\Delta V_{Cd1}}{\Delta t} - C_{d2}\frac{\Delta V_{Cd2}}{\Delta t} = i_d. \quad (1)$$

Furthermore, this expression can be written in the form of s-domain ($C_{d1} = C_{d2} = C_d$) as follows:

$$\frac{C_d}{2} s \Delta V_d(s) = i_d(s). \tag{2}$$

Finally, the transfer function for the control of dc-link capacitor voltages is

$$G_d(s) = \frac{\Delta V_d(s)}{i_d(s)} = \frac{2}{C_d s}. \tag{3}$$

It can be noticed that the controller is a first-order integrator, and the value of cutoff frequencies depends on the size of the dc-link capacitor. This current error is combined with the three-phase modulating signals $v_{mX}(t)$, as shown in Fig. 6, to generate the new reference signals ($v^*_{mX}(t)$) and, thus, capable to improve the stability of the dc-link capacitor voltages relatively. Furthermore, the dc-link capacitors are designed using the following expression given in [34] and [35]

$$C_{d1} = C_{d2} = \frac{(P_O/V_S)}{2 \times \omega_m \times \Delta V_S \times V_S} \tag{4}$$

where P_O is the output power (W), ω_m is the angular fundamental frequency (rad/s), V_S is the total dc-link voltage (V), and ΔV_S is the % ripple voltage.

IV. FC Voltage Balancing and FC Design

A. Analysis of FC Voltage Balancing

The mathematical analysis related to the LSIPD-SPWM for the voltage balancing of the FCs is well addressed in [19]. The total charge variation on an FC can be estimated for half of the fundamental cycle and is given as follows:

$$Q_{Ca} = \cos\phi \cdot I_{\mathrm{AM}} \cdot \frac{T_{\omega_m}}{2\pi} \left(\frac{V_{\mathrm{AM}}}{V_{Ca}} \left(-\frac{\pi}{2} + 2\arcsin\left(\frac{V_{Ca}}{V_{\mathrm{AM}}}\right)\right) + 2.\sqrt{1 - \left(\frac{V_{Ca}}{V_{\mathrm{AM}}}\right)^2} \right) \tag{5}$$

where

Q_{Ca}	total charge variation in phase-A FC;
ϕ	load power factor (PF) angle;
I_{AM}	amplitude of phase-A current;
T_{ω_m}	time period of the fundamental wave;
V_{AM}	amplitude of phase-A voltage;
V_{Ca}	phase-A FC voltage.

From the above-mentioned expression, it can be understood that the charge variation on the FCs is directly related to load PF and the ratio of V_{AM} and V_{Ca}, where they, respectively, denote phase-A output voltage and FC voltage. When $\cos\phi = 0$, the voltage of C_a is naturally balanced, because of the active power supplied by C_a is zero. In other conditions, Q_{ca} must be greater than zero to maintain the capacitor voltage balancing.

The modulation index (m_a) is defined as

$$m_a = \frac{V_{\mathrm{AM}}}{3 \times V_{Ca}}. \tag{6}$$

In order to estimate the maximum limits of m_a, a new expression is derived from (5) and (6), without considering the impact of PF, as follows:

$$K = I_{\mathrm{AM}} \cdot \frac{T_{\omega_m}}{2\pi} \left(3m_a \left(-\frac{\pi}{2} + 2\arcsin\left(\frac{1}{3m_a}\right)\right)\right) + 2 \cdot \sqrt{1 - \left(\frac{1}{3m_a}\right)^2}. \tag{7}$$

Here, the parameter $K = \frac{Q_{Ca}}{\cos\phi}$ is positive when $m_a \leq 0.81$. For the values of $m_a > 0.81$, K becomes negative, which implies that $Q_{Ca} = -\cos\phi$. The negative sign indicates that the discharging rate of the FCs is more, which results in unbalancing of the FC voltages. Therefore, the maximum value of m_a under LSIPD-SPWM is limited to 0.81.

As mentioned before, the voltage balancing of the FCs depends on the switching sequence selection. The voltage balancing of the FCs calls for a well-organized switching sequence. If the proposed topology is operated for five-level operation, during $V_{AO} = V_{\mathrm{dc}}$ and $-V_{\mathrm{dc}}$, there are two switching states, one switching state charges the FC and other discharges it. Hence, both charging and discharging states are effectively utilized to maintain the FC voltage constant. FC voltage balancing is quite difficult when the proposed topology is operated for seven levels, because of only one possible switching state at the peak voltage ($3V_{\mathrm{dc}}$ and $-3V_{\mathrm{dc}}$) levels and during this state, FC discharges. The nominal range of m_a for the seven-level operation of the proposed converter is $0.7 < m_a < 1$. In order to produce seven-level pole voltage output and to balance the FC voltages, m_a is to be limited.

B. Analysis of FC Voltage Ripple

The modulation index is categorized into two different ranges based on the FC voltage ripple as follows:

1) If $0.7 < m_a < 0.81$*:* The FC in each phase will experience a maximum voltage ripple of 5.5 V for unity PF (UPF) load and 3.2 V for 0.56 lagging PF load, which is quite acceptable for proper operation of the circuit. The dependence of the peak value of the fundamental component of phase-A voltage (V_{AN1M}) and phase-A current (I_{AM}), total harmonic distortion (THD), and phase-A FC voltage ripple (ΔV_{Ca}) on m_a are recorded in simulation and are listed in Table II.

2) If $m_a > 0.81$*:* As indicated by the earlier mathematical analysis (3), it is not possible to ensure the balancing of the FC voltages when $m_a > 0.81$ for UPF loads. It can be observed from Table II that when $m_a > 0.81$, ΔV_{Ca} is increasing rapidly. This deteriorates the quality of output voltages using the LSIPD-SPWM modulation technique. In other words, the proposed power circuit configuration suffers from the same disadvantage as the one proposed in [19]. Fig. 7 illustrates the variation of the FC voltage ripple for corresponding changes in m_a from UPF to 0.4lag PF loads.

From Fig. 7, it may be observed that when m_a is 0.82, the voltage ripple in the FCs is 11 V for UPF operation, and the total dc-link voltage is 540 V. Fig. 7 also indicates that the ripple in the FC voltage is going to increase further, as m_a is increased beyond 0.81. To prevent this from happening, m_a should not be

TABLE II
VARIATION OF FC VOLTAGE RIPPLE W.R.T M_a AND PF

m_a	V_{ANIM} (V)	%THD of V_{AN}	I_{AM} (A)	UPF (R=70Ω) ΔV_{Ca} (V)	0.8 PF Lag (R=55Ω, L=0.13H) ΔV_{Ca} (V)	0.56 PF Lag (R=38Ω, L=0.17H) ΔV_{Ca} (V)	0.4 PF Lag (R=27Ω, L=0.19H) ΔV_{Ca} (V)
0.7	283	16	4	0.5	0.5	0.4	0.3
0.75	303	14	4.3	2	1.8	1.4	1.1
0.8	323	13	4.6	4.8	3.7	2.8	2
0.81	327	13	4.7	5.5	4	3.2	2.4
0.82	331	12	4.8	11	5	3.4	2.6
0.83	335	12	5	25	5.1	3.7	2.7

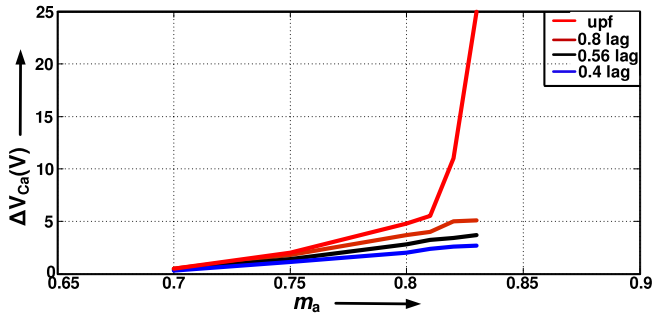
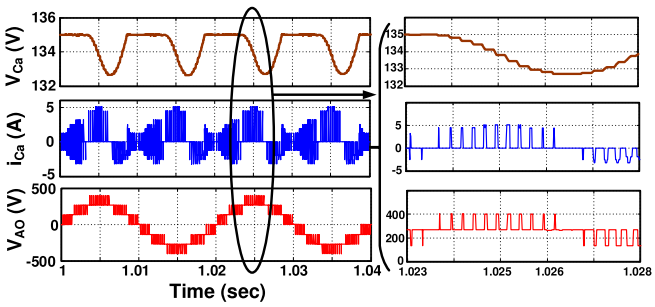
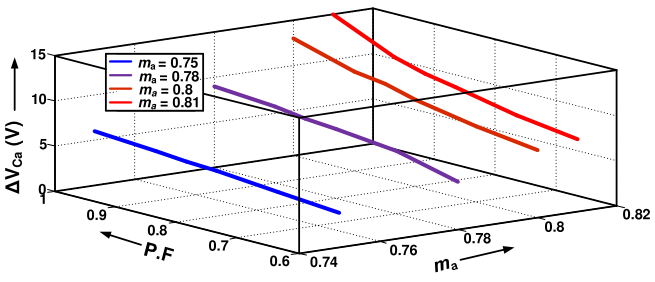


Fig. 7. Variations of FC voltage ripple in phase-A w.r.t m_a at different PFs.



(a)



(b)

Fig. 8. (a) Simulation results of FC voltage, FC current, and pole voltage of Phase-A. (b) Three-dimensional representation of the relationship between FC voltage ripple, PF, and m_a.

increased beyond 0.81. This could limit the dc-link utilization of the proposed power circuit configuration.

Furthermore, Fig. 8(a) depicts the corresponding simulation results to prove the theoretical analysis presented above. It can be noticed that FC voltage ripple occurs during peak voltage levels. Fig. 8(b) shows the variation of the FC ripple voltage, and PF for the corresponding changes in the modulation index. It is observed that the ripple voltage of the FC increases with increase in load PF or m_a or both. The increase in PF results in the increase in charge variation, according to (5). On the other hand, due to the absence of redundant switching states at higher values of m_a, FC voltage ripple increases.

C. Design of FCs

Recently, a new asymmetric MLI topology for five-level was reported in [25]. This topology is the cascade connection of a full-bridge and half-bridge submodules. In this circuit, the FC in the half-bridge is balanced naturally due to the fact that it discharges and charges during positive and negative half-cycles. However, the FC voltage ripples and output voltage distortion are more due to the absence of redundant switching states.

The drop in FC voltage in each phase of the proposed configuration occurs mostly during peak voltage levels, i.e., $3V_{\rm dc}$ or $-3V_{\rm dc}$. Therefore, the voltage drop during peak levels is considered in sizing of the FCs. Hence, the FCs are designed based on the expression reported in [26], which is given as follows:

$$C_x = \frac{I_x}{\Delta V_{Cx} \times f_{sw}} \tag{8}$$

where $x = a,\ b,$ and $c,\ I_x$ is the peak value of load current, $f_{\rm sw}$ is the switching frequency, and ΔV_{cx} is the ripple voltage.

V. COMPARISON OF THE PROPOSED TOPOLOGY WITH VARIOUS MLI CONFIGURATIONS

Table III presents a comprehensive comparison of the proposed power circuit configuration with the recently proposed topologies and the conventional topologies. In some aspects, the proposed inverter shows considerable advantages of reduced switches, capacitors, and their ratings. It can also be noticed that the need for $4V_{\rm dc}$ switches is only three, as aforementioned in Section I. This ensures that the voltage rating of the devices reduced to half and a considerable reduction in the power losses, which results in higher efficient operation as compared with the other MLIs.

TABLE III
COMPARISON OF THE PROPOSED TOPOLOGY WITH VARIOUS TOPOLOGIES

Components	Voltage rating	NPC [27]	FC [28]	CHB [29]	[18]	[30]	[19]	[25]	[9]	[13]	[14]	[16]	Proposed
Switches	$4V_{dc}$	--	--	--	--	--	6	--	--	--	--	--	3
	$3V_{dc}$	--	--	--	12	12	--	--	--	12	--	--	--
	$2V_{dc}$	--	--	--	--	6	6	12	2	--	12	--	9
	V_{dc}	36	36	36	12	12	12	12	40	21	18	36	12
	$0.5V_{dc}$	--	--	--	--	--	--	--	--	12	--	--	
Clamping diodes	$5V_{dc}$	6	--	--	--	--	--	--	6	--	--	--	--
	$4V_{dc}$	6	--	--	--	--	--	--	6	--	--	--	--
	$3V_{dc}$	6	--	--	--	--	--	--	6	--	--	--	--
	$2V_{dc}$	6	--	--	--	--	--	--	8	--	--	--	--
	V_{dc}	6	--	--	--	--	--	--	10	--	--	--	--
Flying Capacitors	$5V_{dc}$	--	3	--	--	--	--	--	--	--	--	--	--
	$4V_{dc}$	--	3	--	--	--	--	--	--	--	--	--	--
	$3V_{dc}$	--	3	--	--	3	--	--	--	--	--	--	--
	$2V_{dc}$	--	3	--	--	3	--	--	--	--	--	--	--
	V_{dc}	--	3	--	--	3	3	6	--	--	6	18	3
Inductors	--	--	--	--	--	--	--	--	4	--	--	6	--
DC-link Capacitors	V_{dc}	--	6	--	9	--	--	--	6	--	--	--	--
	$2V_{dc}$	--	--	--	--	--	2	--	--	--	2	--	2
Independent DC sources	V_{dc}	6	--	9	--	--	--	--	--	9	--	--	--
	$2V_{dc}$	--	--	--	--	--	--	3	2	--	--	--	--
	$3V_{dc}$	--	--	--	3	--	--	--	--	--	--	1	--
	$4V_{dc}$	--	--	--	--	--	1	--	--	--	1	--	1
	$6V_{dc}$	--	1	--	--	1	--	--	--	--	--	--	--
Total component count		72	58	45	36	40	30	33	90	54	39	61	30

TABLE IV
SYSTEM PARAMETERS

Parameter	Simulation	Experimental
DC-link Voltage ($4V_{dc}$)	540 V	160 V
FC Voltage (V_{dc})	135 V	40 V
DC-link Capacitance	1000 µF	500 µF
Flying Capacitance	1000 µF	500 µF
Output Power (P_O)	3 kW	650 W
Switching frequency (f_{sw})	4 kHz	4 kHz
Fundamental Frequency (f_m)	50 Hz	50 Hz

VI. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the feasibility of the proposed three-phase seven-level inverter is verified through simulation and experimental studies. In simulation studies, the model is developed by considering 540 V dc-link voltage and 135 V FC voltage to produce 400 V(L–L) ac output voltages.

The control pulses are developed using the LSIPD-SPWM technique. A switching frequency of 4 kHz is considered for both simulation and experimental works. Furthermore, a laboratory prototype model is developed to test the proposed configuration. The power circuit is consists of IRFP460 MOSFETs, and the control signals are generated using MATLAB/Xilinx system generator blocks with DIGILENT SPARTAN-6 (XC6SLX45) FPGA processor. The performance of the model is studied for an *R–L* load at various modulation indices. The detailed simulation and experimental parameters are given in Table IV.

A. Simulation Results

First, the simulation study is carried out for a 3-kW, 400-$V_{\rm rms}$(L–L) in MATLAB/SIMULINK environment. The proposed model is tested for modulation indices of 0.45 and 0.8 to produce the five-level and seven-level inverter output voltages, respectively. The performance of the dc link and FC voltage controllers is also tested. Figs. 9(a)–(c) and 10(a)–(c) show the inverter output results consisting of the pole voltages, line voltages, phase-A voltage, and current for two different values of m_a (i.e., 0.45 and 0.8, respectively). Figs. 9(e) and 10(f) illustrate the harmonic spectra of these synthesized inverter output pole-A voltage waveform for an m_a of 0.45 and 0.8, respectively. It can be observed that the THD value decreases from 42.8% to 24.12% for the changes in m_a from 0.45 to 0.8, respectively, due to the increase in voltage levels in the output.

Similarly, Figs. 9(d) and 10(d) present the steady-state response of the FC voltages for the aforementioned values of the modulation indices. Fig. 10(e) shows the response of dc-link capacitor voltages with and without the balancing controller. Initially, the voltages $V_{\rm Cd1}$ and $V_{\rm Cd2}$ are unbalanced from $t = 0$ to $t = 0.5$ s. When the controller is ON at t equals 0.5s, the voltages across capacitors are balanced to 270 V. It can be noticed that the dc-link capacitor voltages and the FC voltages are well balanced and maintained at 270 and 135 V, respectively. Figs. 9(f)–(h) and 10(g)–(i) illustrate the harmonic spectra of line voltage (V_{AB}), phase voltage (V_{AN}), and load current (i_A) at two different modulation indices of 0.45 and 0.8, respectively. It is observed that all of the dominant harmonics have been nullified in the line and phase voltages, and the harmonic levels in the load current waveform are very low, which are less than 1%. Hence, the proposed topology and the control strategy are effective and suitable for medium power applications.

B. Experimental Results

Fig. 11 shows the developed laboratory prototype based on Spartan-6 FPGA to verify the effectiveness of the proposed topology for different modulation indices. The hardware setup is built-in the laboratory for a lower scale dc-link voltage and FC voltage of 160 and 40 V, respectively. The 3-Ø, Y-connected *R–L* load of $R = 26\ \Omega$ and $L = 10$ mH is used in the experimentation.

Fig. 12(a)–(c) illustrates the response of pole voltages, line voltages, phase-A voltage, and corresponding load current for an m_a of 0.45. Fig. 12(d) illustrates the phase-A FC voltage w.r.t load change approximately from 2 to 4 A (peak). It can be observed that the FC voltage ripple is quite low and maintained constant for different loads.

Similarly, the experimental study is carried out at an m_a of 0.8, and their results are shown in Fig. 13(a)–(i). The seven-level inverter output waveforms of pole voltages, line voltages, phase-A voltage, and the sinusoidal output phase current are in good agreement with the simulation results. In this case also the developed control scheme succeeds to balance the FC voltages for load changes approximately from 5 to 3 A (peak), as shown in Fig. 13(d). The dc-link capacitor voltages V_{Cd1} and V_{Cd2} w.r.t load change are shown in Fig. 13(e). Fig. 13(f) depicts the performance of the dc-link voltage balance controller. It can be noticed that the top capacitor voltage (V_{Cd1}) is charged to 130 V and V_{Cd2} is discharged to 30 V, without the controller. Both the capacitor voltages are balanced to 80 V, immediately once the controller comes into the operation. This shows that the controller is highly reliable in balancing the dc-link capacitor voltages.

Finally, Figs. 12(e)–(h) and 13(g)–(j) illustrate the harmonic spectra and THD values of the seven-level pole-A output voltage, line-voltage, phase-A voltage, and line current. It can be noticed

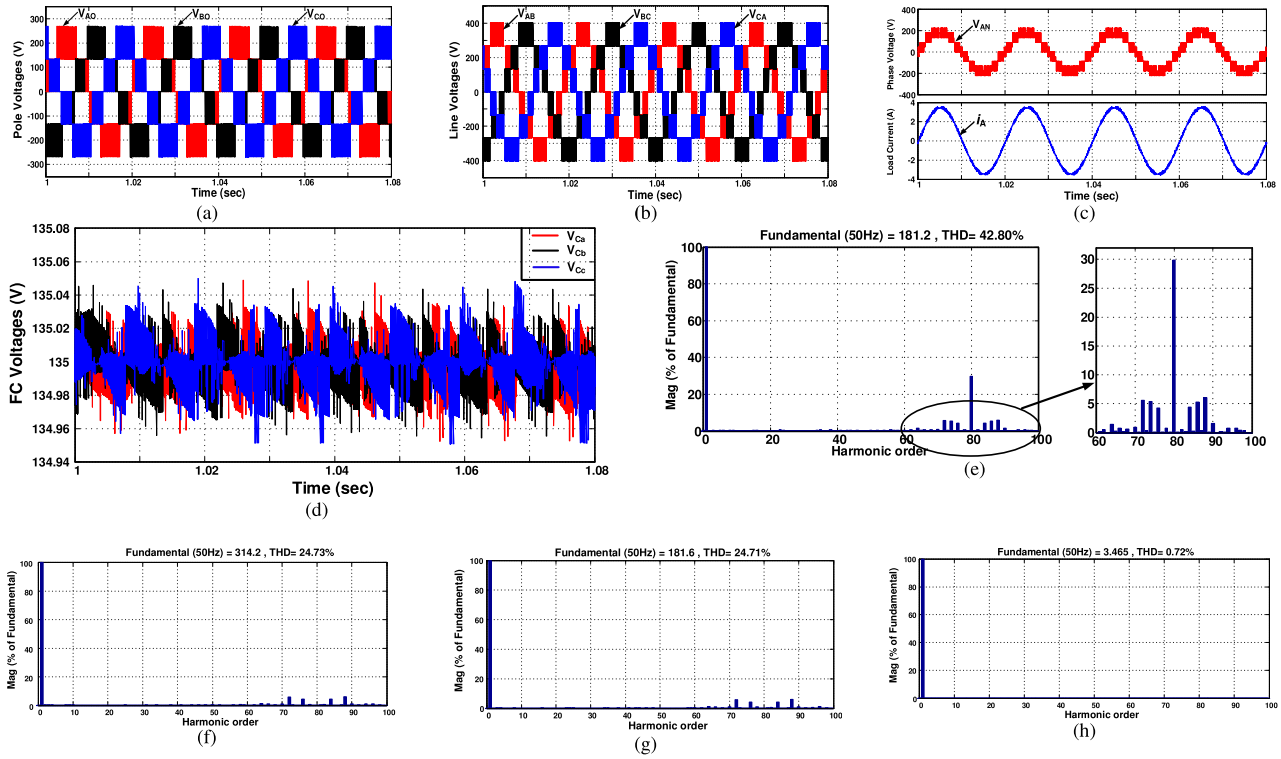


Fig. 9. Simulation results at $m_a = 0.45$. (a) Pole voltages. (b) Line voltages. (c) Phase-A voltage and current. (d) Steady-state FC voltages of all the three phases. FFT analysis of (e) pole voltage (V_{AO}), (f) line voltage (V_{AB}), (g) phase voltage (V_{AN}), and (h) load current (i_A).

that the %THD of voltage (V_{AO}) decreases from 49.46% to 27.46% due to the increase in voltage levels in the output. Moreover, the order of the dominating harmonic components exactly matches between the simulation and experimental results. It is to be noted that the magnitudes of %THD in experimental results are slightly higher than simulated results due to the selection of lower size capacitors. The nearest agreement between the simulation and experimental results validates the proposed power circuit configuration.

The dynamic performance of the converter and the control algorithm is tested by applying different transient disturbances. Figs. 14(a) and (b) depicts the transient response of the proposed configuration for a step change in m_a, which is applied at an arbitrary instant of time. It is observed from Fig. 14(a) that the pole voltage and load current after the step change in m_a are settled to their final values within the duration of one fundamental cycle. Fig. 15(a) and (b) illustrates the response of FC voltages and dc-link capacitor voltages for a step change in m_a. It can be noticed that the dc-link capacitor voltages are well balanced and FC voltages are maintained constant. However, a slight increase in FC voltage ripples is observed during higher loading conditions at $m_a = 0.8$. Figs. 16 and 17 show the pole voltage and load current waveforms for a step change in switching frequency $(f_{\rm sw})$ and fundamental frequency (f_m), respectively. These experimental results demonstrate the effectiveness of the proposed topology, control strategy, and the balancing techniques in steady-state and transient conditions.

C. Charging Process and balancing dynamics of the FCs

The FCs in each phase are charged from the dc supply. Initially, the FC voltages are zero; required switching states that charge the FCs are selected according to the control algorithm, which exploits the property of redundant switching states. The charging time of the FCs depends on the value of m_a, for the given values of $f_{\rm sw}$ and *R–L* load parameters. The plot that demonstrates the voltage balancing dynamics (i.e., the charging process of the FC) of the FC is shown in Fig. 18.

It can be noticed from Fig. 18(a) that the voltage balancing rate is relatively slow at $m_a = 0.1$, which is due to the reduced magnitude of the load current. As the value of m_a increases to 0.45 in Fig. 18(b), the rate of voltage balancing is faster. However, the ripple in the FC voltage, in this case, is higher compared with the case of $m_a = 0.1$. Fig. 18(c) shows the charging process of FC at $m_a = 0.8$. It can be observed that the voltage balancing rate is slow and the ripple is slightly high, due to the absence of redundant switching states at peak voltage levels.

D. Testing Under Nonlinear Loads

The proposed 3-Ø, seven-level inverter is tested for a nonlinear load consisting of a 3-Ø full-bridge diode rectifier that is connected to an *R–L* load of 26 Ω and 10 mH and compared with the linear load for better illustration, as shown in Fig. 19. The line voltages (V_{AB}) and line current (i_A) for linear and nonlinear loads are shown in Fig. 19(a) and (b). It can be seen that the line current becomes nonsinusoidal due to continuous switching

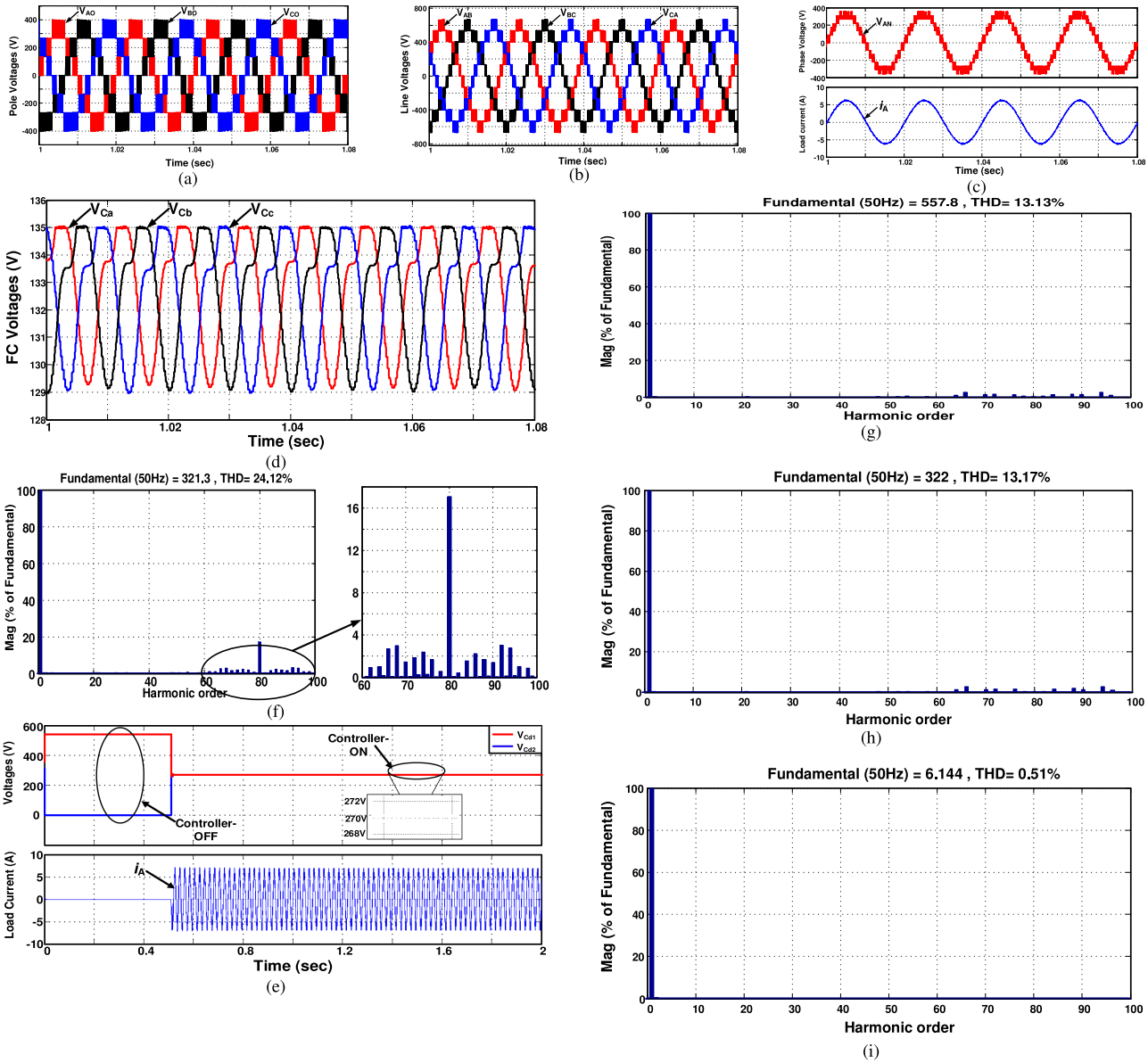


Fig. 10. Simulation results at $m_a = 0.8$. (a) Pole voltages. (b) Line voltages. (c) Phase-A voltage and current. (d) Steady-state FC voltages of all the three phases. (e) DC-link capacitor voltages during without and with controller. FFT analysis of (f) pole voltage (V_{AO}), (g) line voltage (V_{AB}), (h) phase voltage (V_{AN}), and (i) load current (i_A).

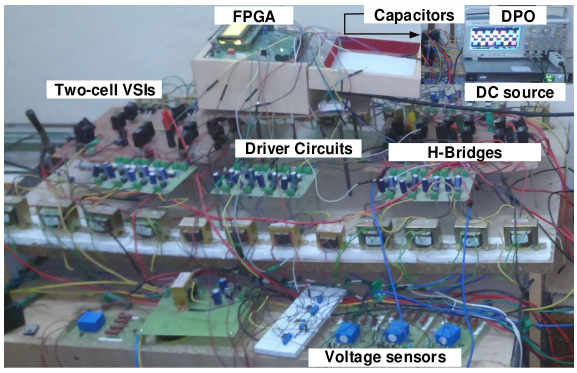


Fig. 11. Experimental setup.

of the diodes in the rectifier, which is shown in Fig. 19(b), as compared with the sinusoidal load current shown in Fig. 19(a). Hence, the proposed topology is also suitable in applications where nonlinear loads are present.

E. Efficiency Calculation

The efficiency of the proposed topology, NPC, FC, and H7LC MLIs is evaluated for a 3-kW, 400$V_{\rm rms}$ (L–L), $f_{\rm sw}$ of 4 kHz, and m_a of 0.8. However, from the design aspects, the NPC and FC inverters are capable to operate at a maximum m_a of unity. Therefore, a dc-link voltage of 650 V is needed in the NPC and the FC MLIs to match 400$V_{\rm rms}$ output for efficiency calculation.

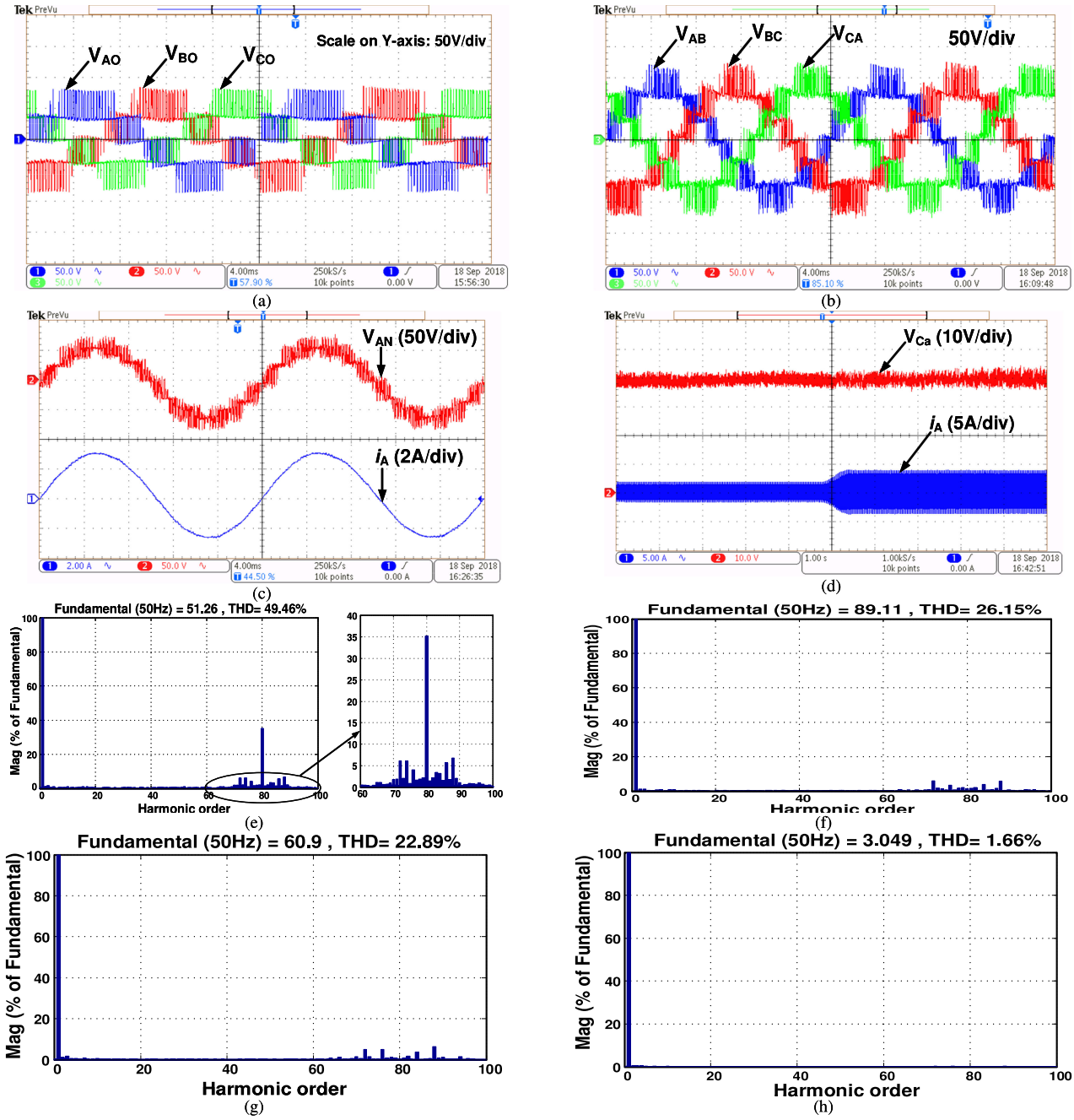


Fig. 12. Experimental results at $m_a = 0.45$. (a) Pole voltages, (b) line voltages, and (c) phase-A voltage and current; time scale (4 ms/div). (d) Voltage across FC (C_a) w.r.t load change; time scale (1 s/div). FFT analysis of (e) pole voltage (V_{AO}), (f) line voltage (V_{AB}), (g) phase voltage (V_{AN}), and (h) load current (i_A) (from comma-separated values (CSV) file).

Fig. 20 shows the variation of efficiency for different loads. It can be noticed that the proposed topology has a higher efficiency of 96% as compared with NPC, FC, and H7LC MLIs. Moreover, the proposed converter gives slightly higher efficiency as compared with the H7LC MLI [19]. This is mainly due to reduced device ratings, and, therefore, the losses mentioned earlier. In order to evaluate the efficiency, different ratings of semiconductor devices were selected as per the blocking voltage and the peak current of each switch. The efficiency calculation is computed in MATLAB software by considering all the device parameters given in the manufacturer's data sheet. Table V shows the list of various ratings of semiconductor devices selected for the proposed topology.

The losses incurred by various MOSFET devices are estimated using the expressions given in [31]. Furthermore, Fig. 21 illustrates the distribution of the losses in various switches of phase-A at full load with a constant m_a of 0.8.

Where

Pcon,d conduction losses of anti-parallel diode in a switch;

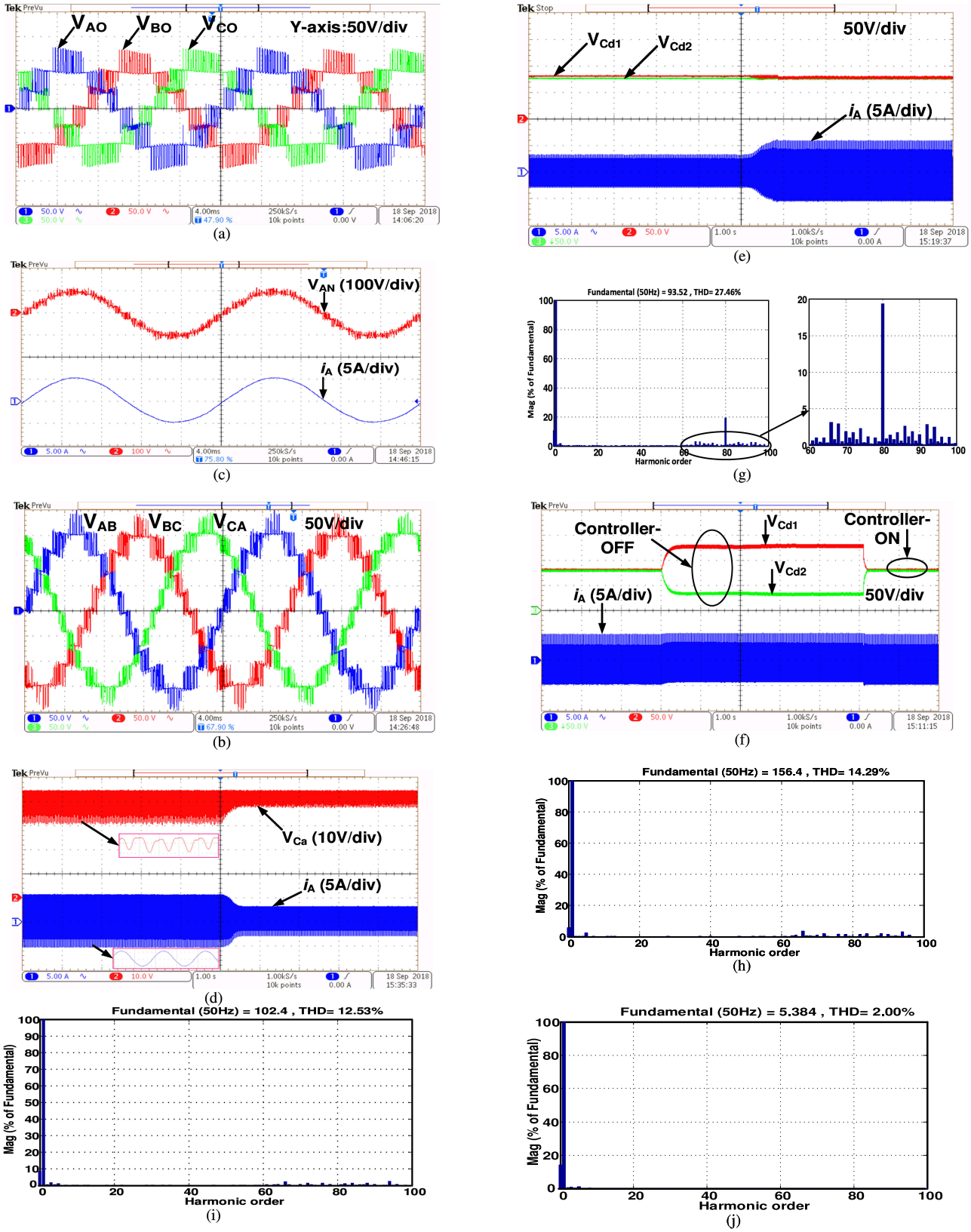
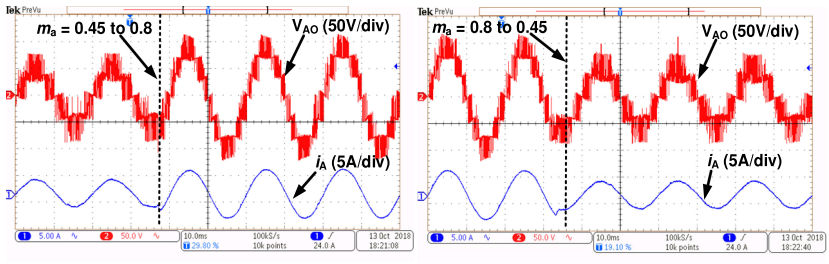
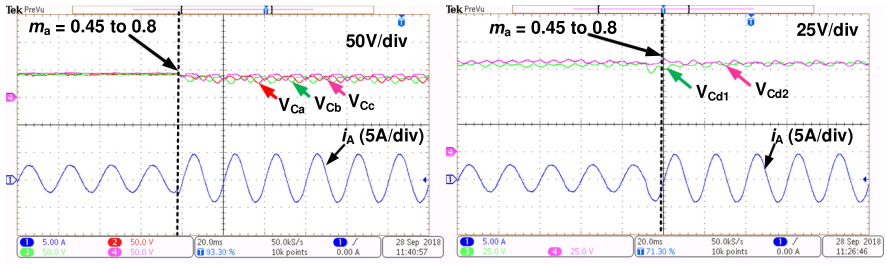


Fig. 13. Experimental results at $m_a = 0.8$. (a) Pole voltages, (b) line voltages, and (c) phase-A voltage and current; time scale (4 ms/div). (d) Voltage across FC (C_a) w.r.t load change, (e) voltage across dc-link capacitors w.r.t load change, (f) voltages across dc-link capacitors and current (i_A) during the controller ON and OFF; time scale (1 s/div). FFT analysis of (g) pole voltage (V_{AO}), (h) line voltage (V_{AB}), (i) phase voltage (V_{AN}), and (j) load current (i_A) (from CSV-file).



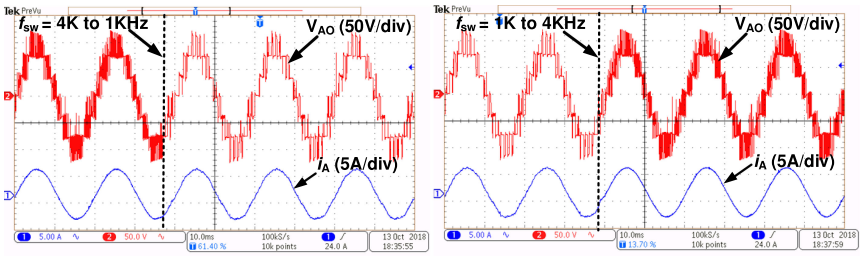
(a) (b)

Fig. 14. Waveforms of pole voltage (V_{AO}) and load current (i_A) when m_a changes from (a) 0.45 to 0.8 and (b) 0.8 to 0.45; time scale (10 ms/div).



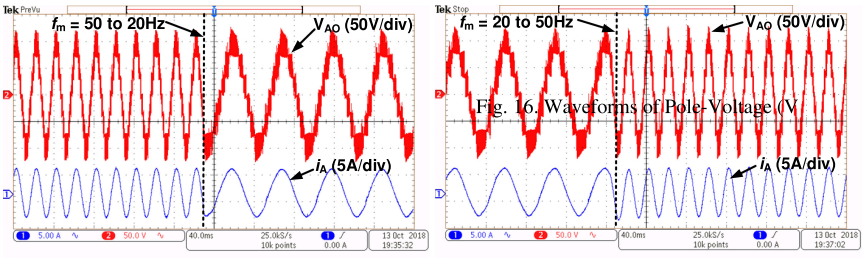
(a) (b)

Fig. 15. Waveforms of (a) FC voltages and load current (i_A) and (b) DC-link capacitor voltages and load current (i_A), when m_a changes from 0.45 to 0.8; time scale (20 ms/div).



(a) (b)

Fig. 16. Waveforms of pole voltage (V_{AO}) and load current (i_A) when $f_{\rm sw}$ changes from (a) 4 k to 1 kHz and (b) 1 k to 4 kHz; time scale (10 ms/div).



(a) (b)

Fig. 17. Waveforms of pole voltage (V_{AO}) and load current (i_A) when f_m changes from (a) 50 to 20 Hz and (b) 20 to 50 Hz; time scale (40 ms/div).

Psw,d switching losses of anti-parallel diode in a switch;
Pcon,sw conduction losses of a switch;
Psw,sw switching losses of a switch.

It can be noticed that the conduction losses of switches are considerably higher as compared with the switching losses. It can be reduced further by the proper selection of the switches, with lower values of $R_{\rm DS}$(on).

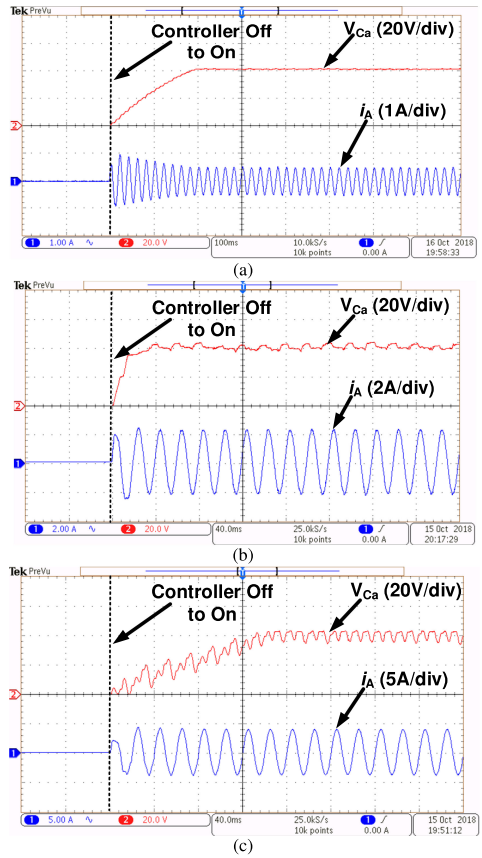


Fig. 18. Charging process and the voltage balancing rate at (a) $m_a = 0.1$; time scale (100 ms/div), (b) $m_a = 0.45$, and (c) $m_a = 0.8$; time scale (40 ms/div). The load resistance (R) $= 26\ \Omega$ and the load inductance (L) $= 10$ mH for all the cases.

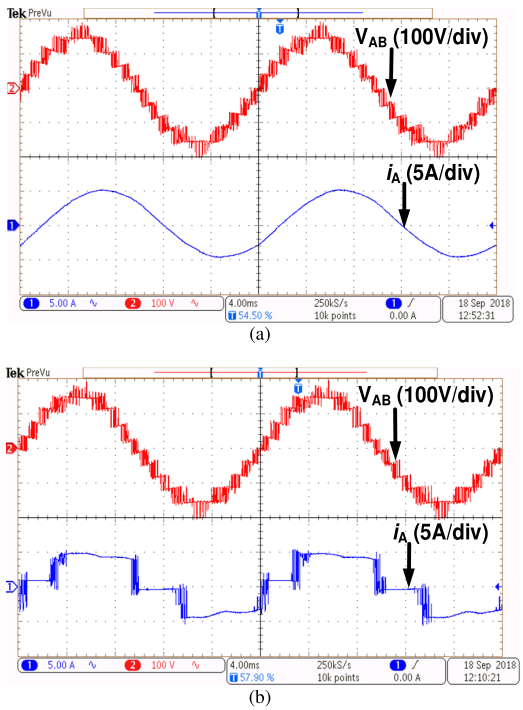


Fig. 19. Experimental results of line voltage and line current for a (a) linear load and (b) nonlinear load; time scale (4 ms/div).

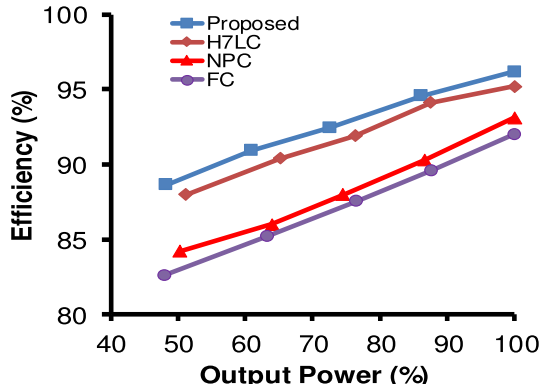


Fig. 20. Variation of efficiency w.r.t output power in various topologies.

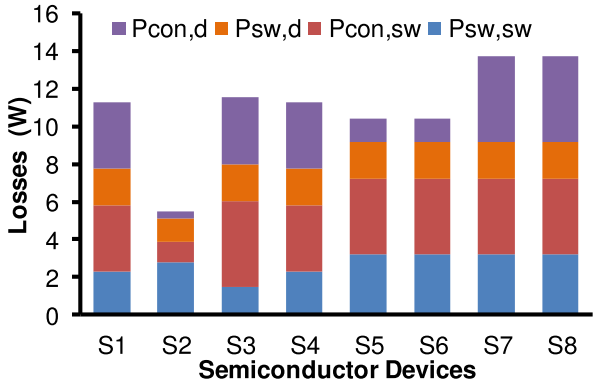


Fig. 21. Distribution of semiconductor losses in various switches of phase-A.

TABLE V
SELECTION OF SEMICONDUCTOR DEVICES

Switches	Required Ratings		Device Number	Device Parameters		
	V_{DS} (V)	I_D (A)		V_{DS} (V)	I_D (A)	$R_{DS(on)}$ (mΩ)
S_1, S_3	270	8	BSC13DN30NSF	300	16	130
S_2	270	5	BSC13DN30NSF	300	16	130
S_4	540	8	STFH24N60M2	650	18	190
S_5, S_6, S_7 and S_8	135	8	MTP20N15E	150	20	130

Note. V_{DS}, drain to source blocking voltage; I_D, maximum allowable drain current; R_{DS} (ON), ON-state drain to source resistance.

VII. CONCLUSION

A new power circuit configuration for a three-phase, seven-level inverter with a *single* dc source is presented in this paper. This topology is developed with a three-level inverter and a full-bridge FC circuit, with reduced component count and device ratings as compared with the conventional MLIs and the T-Type hybrid seven-level inverter. The LSIPD-SPWM control scheme is implemented to balance the FC voltages for different loading conditions with reduced complexity. A separate dc-link voltage balancing control scheme is also presented. The proposed model is demonstrated for different modulation indices, dynamic loading conditions, and nonlinear loads. To assess the proposed power circuit vis-à-vis the other recently proposed topologies, a

comparative study is also carried out. The comparative studies reveal that the proposed topology shows advantages in terms of the reduced component count and the voltage rating of the switching devices. It also shows higher efficiency compared with NPC, FC and H7LC MLIs.

REFERENCES

[1] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded H-Bridge multilevel PV inverter with distributed MPPT for grid-connected applications," *IEEE Trans. Ind. Appl.*, vol. 51, no. 2, pp. 1722–1731, Mar./Apr. 2015.

[2] F. Wu, X. Li, F. Feng, and H. B. Gooi, "Modified cascaded multilevel grid-connected inverter to enhance European efficiency and several extended topologies," *IEEE Trans. Ind. Inform.*, vol. 11, no. 6, pp. 1358–1365, Dec. 2015.

[3] M. Coppola, F. Di Napoli, P. Guerriero, D. Iannuzzi, S. Daliento, and A. Del Pizzo, "An FPGA-based advanced control strategy of a gridtied PV CHB inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 806–816, Jan. 2016.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[5] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters," in *C onf. R ecord 1993 IEEE Ind. Appl. Conf. 28th IAS Annu. Meet.*, 1993, pp. 965–970.

[6] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[7] F. Z. Peng and J. S. Lai, "Multilevel cascade voltage-source inverter with separate DC source," U.S. Patent 56 422 75A, Jun. 24, 1997.

[8] K. Corzine and Y. Familiant, "A new cascaded multilevel H-bridge drive," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 125–131, Jan. 2002.

[9] R. Abdullah, N. A. Rahim, S. R. Sheikh Raihan, and A. Z. Ahmad, "Five-level diode-clamped inverter with three-level boost converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5155–5163, Oct. 2014.

[10] Q. A. Le and D. Lee, "A novel six-level inverter topology for medium-voltage applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7195–7203, Nov. 2016.

[11] S. A Gonzalez, M. I. Valla, and C. F. Christiansen, "Five-level cascade asymmetric multilevel converter," *IET Power Electron.*, vol. 3, no. 1, pp. 120–128, Jan. 2010.

[12] A. Taghvaie, J. Adabi, and M. Rezanejad, "A multilevel inverter structure based on a combination of switched-capacitors and DC sources," *IEEE Trans. Ind. Inform.*, vol. 13, no. 5, pp. 2162–2171, Oct. 2017.

[13] S. Sabyasachi, V. B. Borghate, R. R. Karasani, S. K. Maddugari, and A. H. M. Suryawanshi, "Hybrid control technique-based three-phase cascaded multilevel inverter topology," *IEEE Access*, vol. 5, pp. 26912–26921, Dec. 2017.

[14] S. R. Pulikanti and V. G. Agelidis, "Hybrid flying-capacitor-based active-neutral-point-clamped five-level converter operated with SHE-PWM," *IEEE Trans. Ind. Electron.* vol. 58, no. 10, pp. 4643–4653, Oct. 2011.

[15] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage-balancing method using phase-shifted PWM for the flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4521–4531, Sep. 2014.

[16] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[17] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.

[18] Ji. Yipeng and G. Chen, "A novel three-phase seven-level active clamped converter using H-bridge as a level doubling network," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 479–484.

[19] H. Yu, B. Chen, W. Yao, and Z. Lu, "Hybrid seven-level converter based on T-type converter and H-bridge cascaded under SPWM and SVM," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 689–702, Jan. 2018.

[20] S. Xu, J. Zhang, X. Hu, and Y. Jiang, "A novel hybrid five-level voltage-source converter based on T-type topology for high-efficiency applications," *IEEE Trans. Ind. Appl.*, vol. 53, no. 5, pp. 4730–4743, Sep./Oct. 2017.

[21] V. T. Somasekar and K. Gopa kumar, "Three-level inverter configuration cascading two two-level inverters," *IEE Proc.-Electric Power Appl.*, vol. 150, no. 3, pp. 245–254, May 2003.

[22] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[23] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE 29th Power Electron. Spec. Conf.*, 1998, pp. 172–178.

[24] P. N. Enjeti, P. D. Ziogas, and J. F. Lindsay, "Programmed PWM techniques to eliminate harmonics: A critical evaluation," *IEEE Trans. Ind. Appl.*, vol. 26, no. 2, pp. 302–316, Mar./Apr. 1990.

[25] S. K. Chattopadhyay and C. Chakraborty, "A new asymmetric multilevel inverter topology suitable for PV applications with varying irradiance," *IEEE Trans. Sustain. Energy*, vol. 8, no. 4, pp. 1496–1506, Oct. 2017.

[26] N. Sandeep and R. Y. Udaykumar, "Operation and control of an improved hybrid nine-level inverter," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5676–5686, Nov./Dec. 2017.

[27] X. Yuan and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *IEEE Trans. Power Electron.*, vol. 15, no. 4, pp. 711–718, Jul. 2000.

[28] M. F. Escalante, J. C. Vannier, and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 809–815, Aug. 2002.

[29] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 25–33, Jan. 2009.

[30] S. A. Rahul *et al.*, "A hybrid seven level inverter topology with a single DC supply and reduced switch count," in *Proc. 17th Eur. Conf. Power Electron. Appl.*, 2015, pp. 1–10.

[31] H. Chen, H. Kim, R. Erickson, and D. Maksimovic, "Electrified automotive powertrain archietcture using composite DC–DC converters," *IEEE Trans. Power. Electron.*, vol. 32, no. 1, pp. 98–116, Jan. 2017.

[32] Y. Wang, Y. Hu, and G. Chen, "A novel modulation scheme and a DC-link voltage balancing control strategy for T-Type H-bridge cascaded multilevel converters," *J. Power Electron.*, vol. 16, no. 6, pp. 2099–2108, Nov. 2016.

[33] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[34] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.* vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[35] A. Kirubakaran, "Xilinx FGPA-based single phase seven-level inverter with single input DC voltage source," *J. Circuits, Syst. Comput.*, vol. 26, no. 12, pp. 1–20, May 2017.

[36] T. Abhilash, A. Kirubakaran, and V. T. Somasekhar, "A novel three-phase seven-level inverter," in *Proc. IEEE Int. Conf. Innov. Power Adv. Comupt. Technol.*, 2017, pp. 1–5.

[37] T. Abhilash, A. Kirubakaran, and V. T. Somasekhar, "A seven-level hybrid inverter with DC-link and flying capacitor voltage balancing," in *Proc. 19th IEEE Int. Conf. Environ. Elect. Eng.*, 2019, pp. 1–5.

Tirupathi Abhilash received the B.Tech. degree in electrical and electronics engineering from A.S.C.E.T Engineering College, Nellore, India, in 2009, and the M.Tech. degree in power electronics & drives from S.V.P.C.T., Tirupati, India, in 2012. He is currently working toward the Ph.D. degree at the Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India.

His research interests include hybrid multilevel inverters for medium-voltage applications and voltage balancing techniques.

Kirubakaran Annamalai (SM'18) was born in Kanchipuram, India, in 1981. He received the B.E. degree in electrical and electronics engineering from Madras University, Chennai, India, in 2002, the M.E. degree in power system from Annamalai University, Chidambaram, India, in 2004, and the Ph.D. degree in electrical engineering from the Maulana Azad National Institute of Technology, Bhopal, India, in 2011.

He was a Lecturer with the Department of Electrical & Electronics Engineering, Thirumalai Engineering College *(*Affiliated to Anna University*),* Kanchipuram, India, from 2004 to 2006. From 2010 to 2012, he was an Associate Professor with the School of Electrical Engineering, VIT University, Vellore, India. Since 2012, he has been an Assistant Professor with the Electrical Engineering Department, National Institute of Technology Warangal, Warangal, India. His research interest includes fuel-cell-based distributed generation, photovoltaic systems, multilevel inverters, and grid interface.

Prof. Annamalai's biography is listed in *Marquis Who's Who in the World 2012 & 2013*.

Somasekhar Veeramraju Tirumala (M'11) received the graduate degree from Regional Engineering College Warangal (presently the National Institute of Technology), Warangal, India, in 1988, the postgraduate degree from the Indian Institute of Technology, Bombay, Mumbai, India, in 1990, and the Doctoral degree from the Indian Institute of Science, Bangalore, India, in 2003.

He was an R&D Engineer with M/s Perpetual Power Technologies, Bangalore, India, and as a Senior Engineer with M/s Kirloskar Electric Co. Ltd., Mysore, India, during 1990–1993. He joined the Faculty of Electrical Engineering, National Institute of Technology, Warangal, India, in 1993, where he is currently a Professor. His research interests include multilevel inversion with open-end winding induction motors, ac drives, and PWM strategies.