A Novel Two-Stage Hybrid T-type Five-Level Transformerless Inverter

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***Abstract*— This paper presents a new two-stage hybrid T-type five-level inverter for 1-φ grid connected photovoltaic applications (PV). The new topology comprises three-level boost converter (3LBC) and hybrid T-type five-level inverter. The 3LBC balances the capacitor voltages by employing simple control algorithm and also improves power conversion efficiency by lowering voltage stress. The sinusoidal level shifted pulse width modulation (SLS-PWM) scheme is used to operate the inverter at different power factor conditions without affecting the transitions in common mode voltage (CMV). Moreover, the leakage current produced by the parasitic capacitance of the PV panel is minimized by providing common mode path to the inverter. Furthermore, it also minimizes the voltage rating of the power semiconductor switches, total harmonic distortion and the filter size. Simulation results are presented to validate the capabilities of the proposed inverter.**

Keywords—Transformerless multilevel Inverter, Common mode voltage, Sinusoidal pulse width modulation, Total harmonic distortion.

I. INTRODUCTION

Environmentally friendly renewable energy sources are gaining popularity to satisfy the power demands while having low impact on the ecosystem. Among all the renewable energy sources, photovoltaic (PV) power generation has gained much more importance due to its rooftop implementation ability in medium and small power scales connected to the 1-φ grid. A line frequency transformer (LFT) is often used to feed power into the grid both for voltage boosting and galvanic isolation. However, the cost and size of the overall system increases with reduction in efficiency [1]-[2]. Therefore, many researchers have focused on transformerless operation, but it will introduce the issue of leakage current due to parasitic capacitance of the PV source with respect to ground.

The value of the parasitic capacitance typically ranges between few tens of nanofarads to microfarad per kilowatt based on the environmental conditions and technology employed in PV cell manufacturing. To model this capacitance, an equivalent capacitance is connected across the positive or negative terminals of the PV source to ground. The voltage that appears across these capacitances causes flow of leakage current into the system. The leakage current flow affects power quality, introduces electromagnetic interference (EMI) and endangers operator's safety [3]-[4]. Therefore, it is essential to address the issue of leakage current in the absence of LFT and it should be below the DIN VDE 0126 1-1 grid standards for PV power generation.

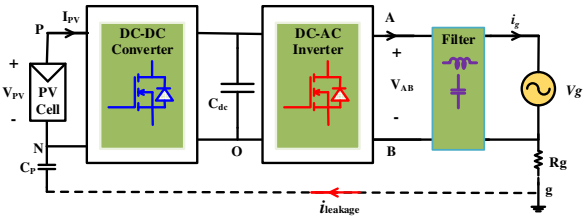

Fig. 1. Typical two-stage transformerless PV inverter.

Several topologies have been presented in the literature [5], to address the issue of leakage current. But, very few inverters are associated with multilevel operation. Multilevel inverters have significant advantages like high quality of power output lowering the total harmonic distortion (THD), reduced losses with the reduction in voltage stress of the switches, reduced filter size and increased modularity [6]. It is advantageous to have such benefits in PV power generation systems along with reduction in leakage current. However, these topologies require a large number of series connected PV panels to serve the voltage requirements of grid; inverters with such configurations are known as single-stage inverters. The series connected PV panel topologies have several demerits such as poor maximum power point tracking (MPPT), imbalance in the power sharing of PV panels, and lower operational safety. Therefore, two-stage PV power generation system is the best alternative to limit the above mentioned shortcomings as shown in Fig. 1 [7].

There are topologies presented in the literature, which are capable of limiting the leakage current either by modifying pulse width modulation (PWM) technique or by changing the inverter structure with no boosting [8]-[10]. Zhan Zang et. al proposed a high-efficient two-stage five-level micro inverter in [11]. High frequency transformer (HFT) and more switching devices are employed to provide galvanic isolation and to boost DC voltage in the front-end converter respectively. Therefore, the overall system size and cost of the inverter will increase. Jun-Seok Kim et. al proposed a two-stage high efficient five-level grid connected PV inverter in [12], leakage current of the inverter is a little high because high amplitude grid frequency variations are present in the total common mode voltage. Therefore, the researchers were inclined to develop a new five-level two-stage inverter topology which is capable of boosting and facilitating minimum leakage current by providing common mode conducting path to the inverter. In addition, the switch count and size of the filter is not increased. The proposed inverter circuit is also suitable for non-unity power factor operations of the grid without affecting the behavior of common mode voltage.

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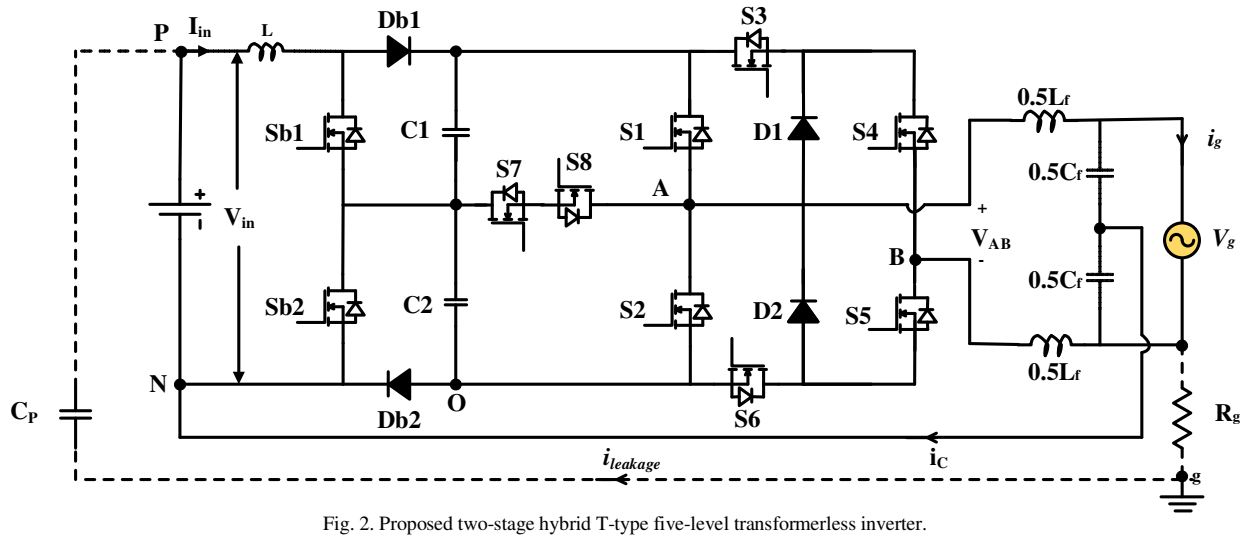


Fig. 2. Proposed two-stage hybrid T-type five-level transformerless inverter.

II. Proposed Two-Stage Hybrid T-Type Five-Level Inverter

The schematic arrangement of the proposed two-stage five-level inverter configuration is depicted in Fig. 2. It comprises three level boost converter (3LBC) converters and a hybrid T-type five-level transformerless inverter. The 3LBC produces balanced DC-link capacitor voltages by employing a simple control circuit. The proposed hybrid T-type inverter produces five-level output voltage by using sinusoidal level shifted pulse width modulation (SLS-PWM) scheme, which enables the inverter to operate at all power factors without affecting the common mode voltage (CMV). Further, the LCL filter provides common mode path to the inverter to limit the magnitude of leakage current.

A. 3-Level boost converter

The proposed 3LBC is derived from three-level DC-DC converter given in [13]. The front-end 3LBC is depicted in Fig. 3, it comprises one inductor L, two DC-link capacitors C1 and C2, two switches Sb1 and Sb2. Depending on switching states the 3LBC have four modes of operation; Mode 2 and Mode 3 occur, when either Sb1or Sb2 is turned ON. Mode 1 and Mode 4 occur, when Sb1 and Sb2 are both turned ON or OFF respectively. It is noticed that there are two operating regions based on the value of duty ratio D. In region 1, R1 (0<D<0.5) allows the converter to operate in Mode 1, Mode 2 and Mode 3. In region 2, R2 (0.5<D<1) allows the converter to operate in Mode 1, Mode 3 and Mode 4. Therefore, operating modes of the 3LBC depend on the value of D.

The control pulses for the switches Sb1 and Sb2 are generated with simple proportional-integral (PI) controller as shown in Fig. 3, where the error sensed by the DC-link capacitors is compared and fed to the PI controller. The PI controller provides change in duty ratio ΔD, which can balance the DC-link capacitors.

$$V_{dc} = \frac{V_{in}}{1-D} \tag{1}$$

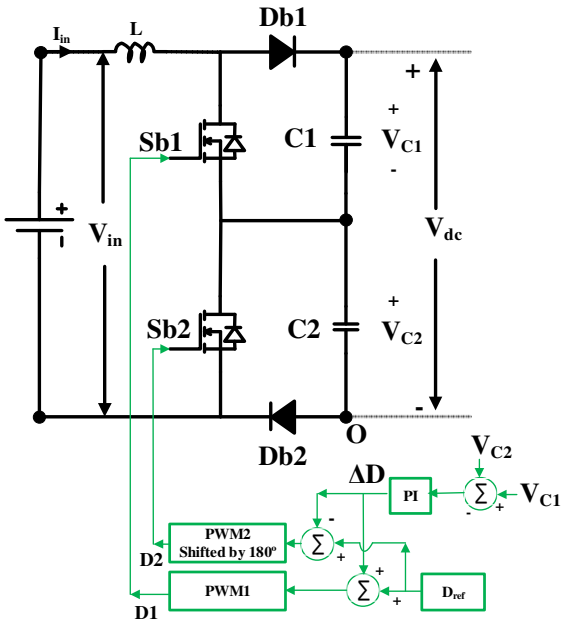


Fig. 3. Block diagram of 3LBC with PI control.

Further, it is passed through the PWM circuit to generate the control pulses Sb1 and Sb2. Eq. (1) gives the relation between input voltage and DC-link voltage. Where, V_{in} and V_{dc} indicate the input voltage and total DC-link voltage respectively.

B. Hybrid T-type five-level inverter

The proposed hybrid T-type five-level inverter is derived from the T-type inverter given in [14]. It comprises single-phase T-type inverter with S1, S2, S7 and S8 and a neutral point clamping (NPC) branch with D1, D2, S3, S4, S5 and S6. Operation of the proposed topology consists of five states. State 1 and State 2 correspond to V_{dc} and $V_{dc}/2$, State 3 corresponds to zero voltage level of the inverter in both positive and negative half cycles of the grid, State 4 and State 5 correspond to $-V_{dc}/2$, $-V_{dc}$ respectively.

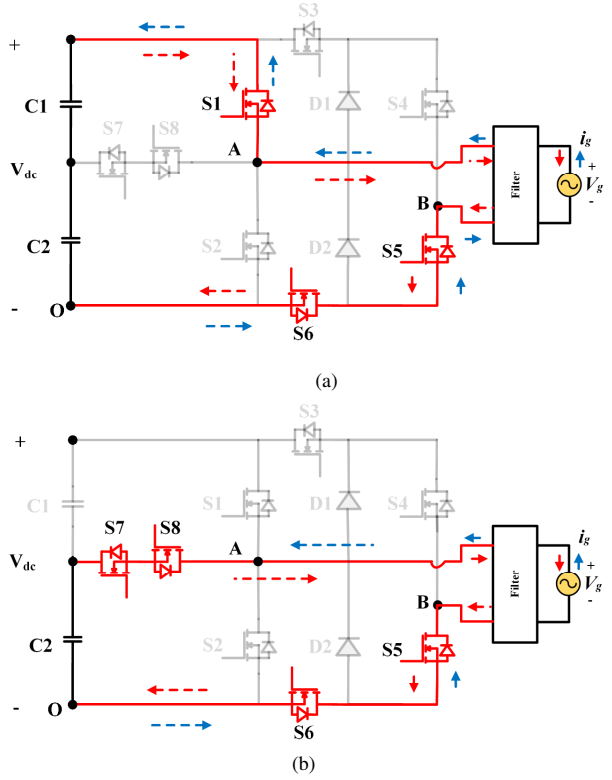


Fig. 4. Operating states of the inverter (a) $V_{AB}= V_{dc}$; (b) $V_{AB}= Vdc/2$

State 1: In this state, $V_{AB}= (V_{C1}+V_{C2})$, and the current flows either from 3LBC to grid or vice-versa as shown in Fig. 4(a). When, the current flows from 3LBC to grid, switches S1, S5 and S6 are in conduction. If the current flows from grid to 3LBC, body diodes of the switches S1, S5 and S6 are in coduction. Throughout this state DC-link capacitor are in series and they are connected in parallel to the grid.

State 2: In this state, $V_{AB}= V_{C2}$, and the current flows either from 3LBC to grid or vice-versa as shown in Fig. 4(b). When current flows from 3LBC to grid, switches S5, S6, S7 and body diode of S8 are in conduction. If the current flows from grid to 3LBC, switch S8 and body diodes of the switches S5, S6 and S7 are in conduction. Throughout this state DC-link capacitor C2 connected parallel to the grid.

State 3: In this state, $V_{AB}= 0$ which provides free wheeling path in the positve as well as negative half cycles of the grid. Switches S4, S5, S7, S8, D1 and D2 are turned-ON as shown in Fig. 5. Grid current freewheels through the above said switches and diodes based on the current direction. Throughout this state 3LBC is isolated from the grid and the potentials V_{AO} and V_{BO} are clamped to the mid-point of DC-link capactiors. Therefore, the amplitude of CMV is reduced.

State 4: In this state, $V_{AB}= -V_{C1}$ and the current flows either from grid to 3LBC or vice-versa as shown in Fig. 6(a). When current flows from grid to 3LBC, switches S3, S4, S8 and body diode of S7 are in conduction. If the current flows from 3LBC to grid, switch S7 and body diodes of the switches S3, S4 and S8 are in conduction. Throughout this state DC-link capacitor C1 is connected parallel to the grid.

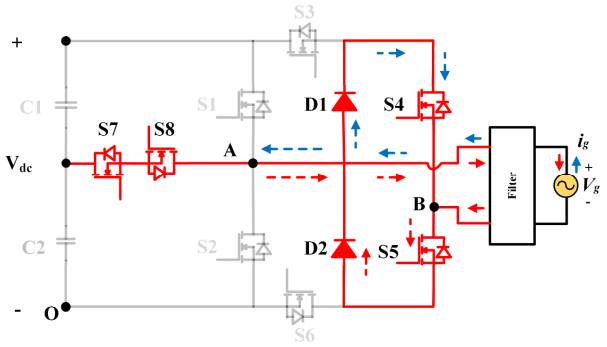


Fig. 5. Operation of the inverter in freewheeling state.

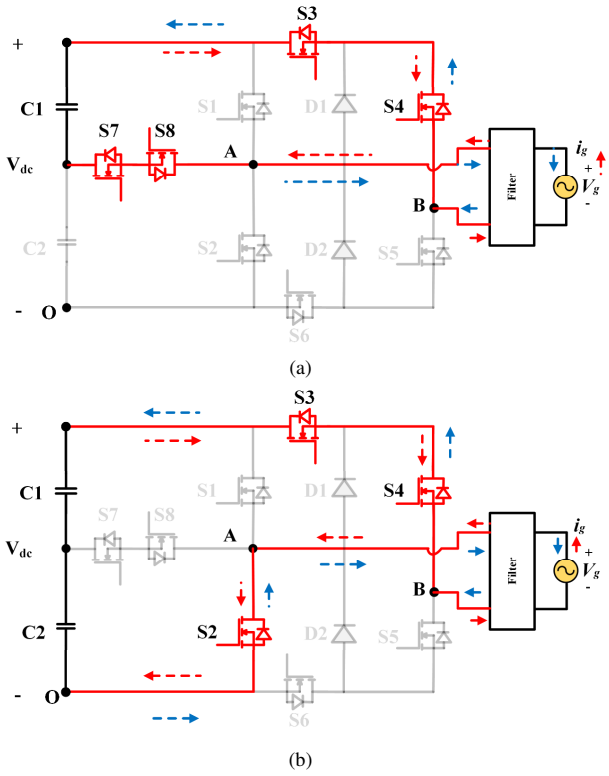


Fig. 6. Operating states of the inverter (a) $V_{AB}= -V_{dc}/2$; (b) $V_{AB}= -V_{dc}$.

State 5: In this state, $V_{AB}= -(V_{C1}+V_{C2})$, and the current flows either from grid to 3LBC or vice-versa as shown in Fig. 6(b). When, the current flows from grid to 3LBC, switches S2, S3 and S4 are in conduction. If the current flows from 3LBC to grid, body diodes of the switches S2, S3 and S4 are in conduction. Throughout this state DC-link capacitor are in series and they are connected parallel to the grid.

Therefore, the proposed hybrid T-type five-level inverter is capable of producing levels in the output at different power factor conditons of the grid, which enhances the reactive power control of the inverter.

III. Pulse Genration

SLS-PWM scheme is employed to produce control pulses for inverter. Fig. 7 shows the implementation of various SLS-PWM switching states of the inverter for five-level output voltage realization. (Table. I).

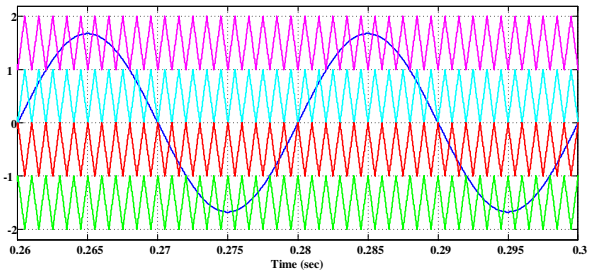


Fig. 7. Waveforms of SLS-PWM.

TABLE I. SWITCHING LOGIC OF THE INVERTER

	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*
V_{dc}	1	0	0	0	1	1	1	0
0.5 V_{dc}	0	0	0	0	1	1	1	1
0	0	0	0	1	1	0	1	1
-0.5 V_{dc}	0	0	1	1	0	0	1	1
-V_{dc}	0	1	1	1	0	0	0	1

It is observed that switches S1 & S2 are conducting only in the top levels of output voltage. S3 and S6 are conducting in the negative and positive cycles except zero level, respectively. S4 and S5 are conducting in the negative and positive half cycles of the grid respectively. S7 and S8 are conducting according to the selection of voltage level. Usually, switches S4, S5 and D1, D2 are enough to provide zero state, but it will float the terminal voltages of the inverter, which causes imbalance in the CMV due to junction capacitances of the switches. Therefore, to clamp the CMV at $V_{dc}/2$ switches S7 and S8 are also in conduction during zero state. Moreover, this provides path for current in any direction to realize non-unity power factor operations of the grid with similar CMV behavior. Furthermore, due to absence of complementary action in the inverter switches, dead-time related issues are eliminated for the proposed inverter.

IV. CMV ANALYSIS

The leakage current flow from the grid to PV source is one of the major issues in transformerless inverter applications. To analyze the effect of variations in the CMV on leakage current, an equivalent circuit is derived from Fig. 2 by considering only the common mode behaviour. There is no effect of the differential mode behaviour of the inverter on leakage current [15], hence it is ignored in the equivalent circuit shown in Fig. 8.

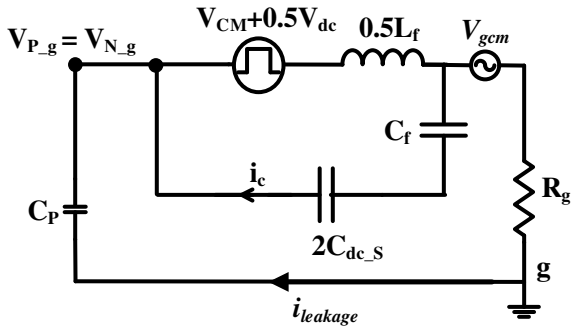


Fig. 8. Common mode equivalent circuit.

$V_{AO}(\omega)$ and $V_{BO}(\omega)$ are the terminal voltages of the inverter with respect to terminal 'O' as shown in Fig. 1. $V_{CM}(\omega)$, $V_{DM}(\omega)$ are the common mode and differential mode voltages of the inverter and they are given in Eq. (2) and Eq. (3) respectively. V_{P_g} and V_{N_g} are the voltages across PV parasitic capacitances. From the equivalent circuit shown in Fig. 8; it is noticed that, an LC circuit is formed between the grid and PV terminals, therefore high frequency components in the CMV are attenuated with a factor $A(\omega)$. The simplified expression for V_{P_g} is given in Eq. (4), where 'ω' and 'ω_r' the switching and resonant frequency components in rad/sec respectively.

$$V_{CM}(\omega) = \frac{V_{AO}(\omega) + V_{BO}(\omega)}{2} \tag{2}$$

$$V_{DM}(\omega) = V_{AB}(\omega) = V_{AO}(\omega) - V_{BO}(\omega) \tag{3}$$

$$V_{P\_g} = \frac{-V_{CM}(\omega)}{A(\omega)} - 0.5V_{dc} - 0.5V_{ripple} + V_{gcm} \tag{4}$$

$$A(\omega) = 20\log\left(\left|1 - \frac{\omega^2}{\omega_r^2}\right|\right)$$

$$i_{leakage} = C_P \frac{dV_{P\_g}}{dt} \tag{5}$$

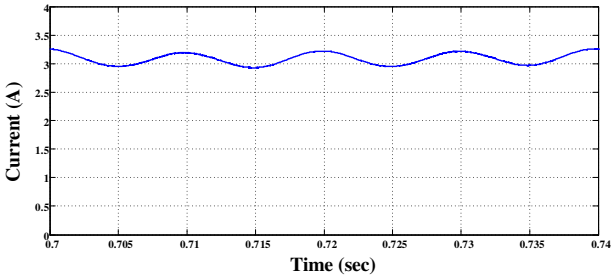
Low frequency components have low affect on the V_{P_g}, hence they are ignored [16]. From Eq. (5), the magnitude of leakage current depends on the value of C_P and variations in CMV. Variations in CMV are attenuated by the LC network which leads to minimized leakage current flow from the grid to PV panel and is well below the grid standards. Moreover, this solution does not affect the active and reactive power flow to the grid.

V. SIMULATION RESULTS

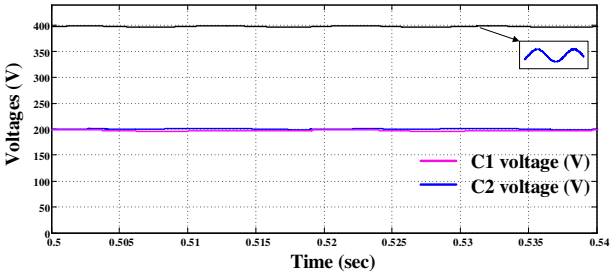
To validate the proposed two-stage configuration, simulations are carried out using MATLAB/SIMULINK software with the parameters given in Table II. To show the leakage current flow in PV parasitic capacitance due to variations in CMV, an equivalent capacitor is modelled and connected across the terminals of DC source as depicted in Fig. 2. Simulation results of 3LBC are given in Figs. 9(a) and 9(b). Fig. 9(a) shows the input inductor current, which is in continuous conduction mode. Fig. 9(b) shows the DC-link capacitor voltages along with total DC-link voltage of 3LBC operating with 0.5 duty ratio.

TABLE II. PARAMETERS USED IN THE SIMULATION

S. No	*Parameters*	*Value*
1	Input voltage	200 V
2	Inductor L, L_f	1 mH, 4 mH
3	Capacitors C1, C2, C_f	1 mF, 1 mF, 6 μF
4	AC output voltage	230V, 50 Hz
5	Switching frequency f_s	10 kHz
6	Output power	900W
7	C_P and R_g	10 nF, 100Ω
8	Modulation index (M_a)	0.94



(a)



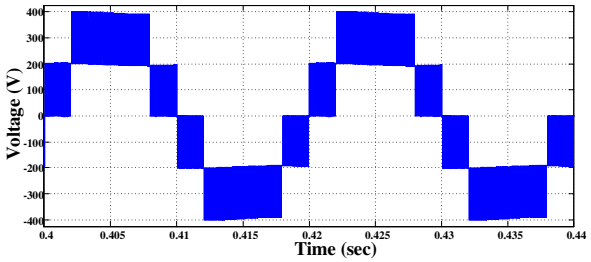
(b)

Fig. 9. Simulations results of the 3LBC (a) input current; (b) Total DC-link voltage and DC-link capacitor voltages.

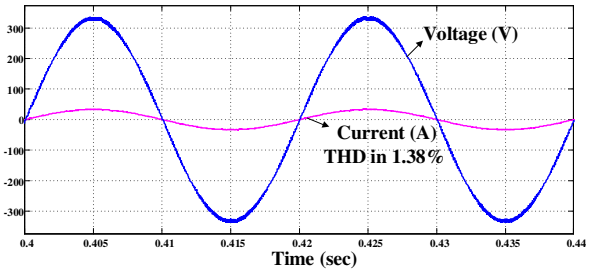
It confirms that the balancing of DC capacitors is achieved with the control algorithm as explained in Section III. The balanced DC voltage produced by the 3LBC is fed to the five-level hybrid T-type inverter for obtaining output voltage levels.

Further, a filter circuit is employed to filter out the unwanted harmonics which are flowing into the grid; and the corresponding results are given in Fig. 10. Fig. 10(a) shows the five-level output voltage of the hybrid T-type five-level inverter. Figs. 10(b), (c) and (d) show the filtered voltage and current waveforms at unity, lagging and leading power factor conditions respectively. The total harmonic distortion (THD) of the load current for unity power factor operation is computed in MATLAB/SIMULINK software by using FFT analysis in the "powergui" block and it shown in Fig. 11. From the above results the level voltage is not disturbed at any loading condition and the current THD is within the standards of IEEE1547. Therefore, it is evident that the proposed topology is quite efficient in operation with reactive power control of the grid.

Furthermore, to show the CMV behavior of the proposed configuration Fig. 12 is presented. The terminal voltage V_{AO}, V_{BO} and common mode voltage waveforms are given in Fig. 12(a). By observing the PV terminal voltage V_{N_g} in Fig. 12(b), it is confirmed that the common mode path introduced by the LC filter effectively limits the variations in the CMV. The calculated value of rms leakage current is 5.24 mA for the specifications given in Table II, which is well below 200 mA as per German DINVDE0126-1-1 grid standards and it is shown in Fig. 12(c). Therefore, this validates the effectiveness of the proposed topology and its modulation technique about reduction of leakage current.



(a)



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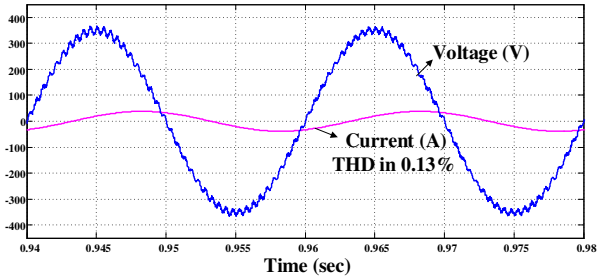
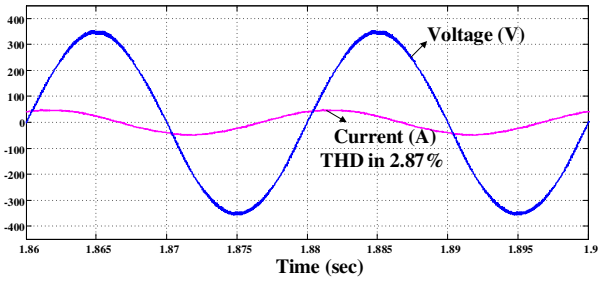


(c)



(d)

Fig. 10. Simulations results of the five-level hybrid T-type inverter (a) level voltage; Output voltage and current at (b) unity power factor; (c) lagging power factor; (d) leading power factor.

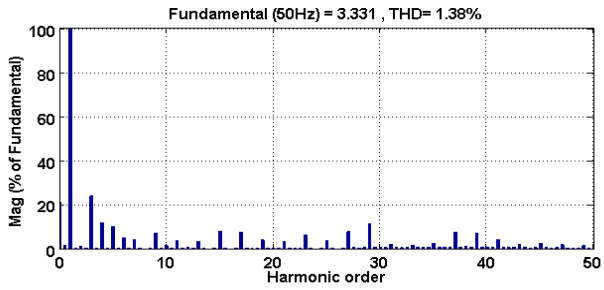
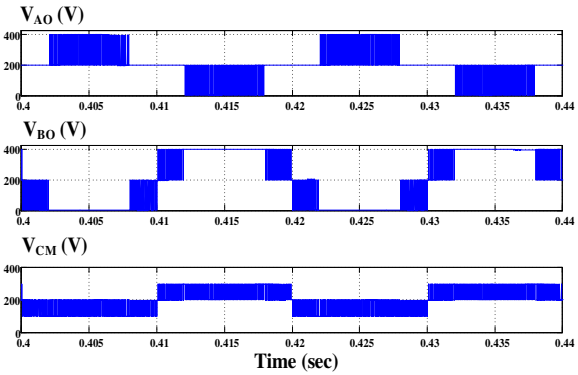
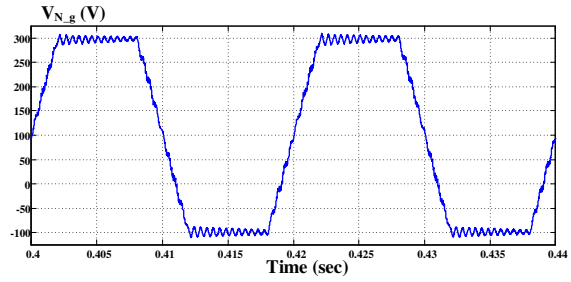


Fig. 11. FFT spectrum of load current.



(a)



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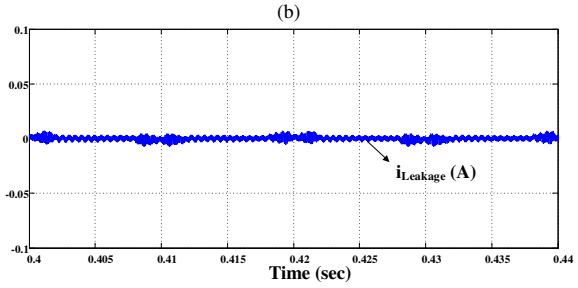

(c)

Fig. 12. Simulation results of (a) V_{AO}, V_{BO} and V_{CM}; (b) $V_{N\text{-}g}$; (c) Leakage current ($i_{leakage}$).

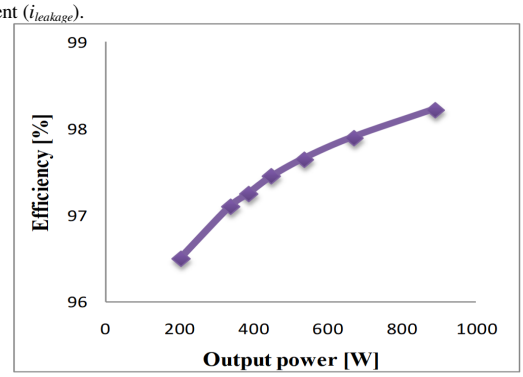

Fig. 13. Efficiency curve.

Finally, efficiency versus output power curve of the proposed two-stage system is depicted in Fig. 13, which is evaluated using PSIM thermal module [17]. Data sheets of FCA76N60N MOSFET and RUR1S1560S diode are used for estimating switching and conduction losses of switches as per the parameters given in Table. II.

VI. Conclusion

In this paper, a novel two-stage hybrid T-type five-level inverter configuration is presented, which provides boosting and limits the leakage current in the transformerless PV inverters. The 3LBC balances the DC- link capacitors by using simple control algorithm, which reduces the control complexity of the inverter. The proposed inverter topology and its SLS-PWM technique provides path to the current at different power factor conditions without affecting the CMV behavior. Moreover, the leakage current flowing from grid to PV source is limited by introducing common mode path to the inverter using LC filter and it is well below the grid standards. Simulation results are presented to support the above mentioned claims. Experimentation is underway to validate the proposed configuration, and those results will be presented in the later version of the paper.

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