Modified Structure of Sepic Based Single-Phase Five-Level T-Type Inverter for Photovoltaic Applications

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Abstract*: In this paper, a modified structure of two-stage sepic based five-level T-type inverter is presented for photovoltaic applications. The proposed topology consists of a frond-end sepic converter cascaded with full bridge T-type inverter through a high-frequency transformer. The proposed topology owns the merits of high boost output voltage level, modularity, reduced device parts, and better quality of supply. Therefore, a detailed operation of the proposed topology and the level generations using sine pulse width modulation are presented. Finally, the performance of the proposed topology is validated through Matlab simulation and experimental prototype model results.

Keywords* : SEPIC inverter, Multilevel inverter, Field programmable gate array (FPGA), total harmonic distortion (THD).

I. INTRODUCTION

Photovoltaic (PV) system is getting more attention in the past ten years due to the availability of large resource of sun energy, depleting nature of fossil fuels and environmentally friendly nature. The cost of the PV panel installation is also decaying in the last few years due to technology development. However, the issues of power fluctuations during climate changes, common-mode voltage and leakage current due to parasitic components on the integration of PV systems motivate the researchers to develop a suitable power electronic interface and simple control.

In this context, an adequate number of single-stage DC/AC inverters and two-stage consisting of DC/DC converters cascaded with DC/AC inverters have been developed to convert PV output voltage into a suitable form of energy for standalone/grid connection with their own merits and demerits. However, the use of single-stage DC/AC full-bridge converter is always buck in nature and demands large DC-link voltage. Therefore, the conventional boost converter is introduced in front of the DC/AC inverter which forms two-stage configuration. But, it has limited high output voltage gain due to an increase in energy losses and poor efficiency at a higher duty cycle. Therefore, the sepic converter is considered for the study which has advantages of step-up and step-down operation; cascading to the high-frequency transformer leads to further increase in voltage gain. In this way, a high gain can be achieved by the proposed topology.

On the other hand, multilevel inverters (MLIs) with reduced parts count topologies have become popular. MLIs offer the advantages of reduced device ratings, lower electromagnetic interference, and high power quality. Besides there is a considerable reduction in the size of the filter compared to conventional Two-level inverter. Moreover, the recent literature reveals that the output voltage quality is improved by the reduction in total harmonic distortion for the increase in output levels[1-3]. However, the complexity of the circuit is raised for increased output levels with the demand for more switching devices and driver units. Therefore, a five-level z source based MLI is proposed in [4]. Cascaded H-Bridge (CHB) is the most popular one among the various MLIs. But, it demands more independent DC sources and semiconductor devices for the increase in level. Alternatively, asymmetric MLIs are getting popular with CHB configurations for increased output voltage levels with the same switches using different ranges of DC sources. Recently, a transistor clamped five-level inverter with reduced devices is proposed for multi-string PV applications in [5-6] without compromise in the increase in output level and devices counts. The same inverter is cascaded for more output levels in [7]. This is achieved using a frond end multi-winding transformer with three-phase rectifier units for three-phase induction motor applications. However, the boosting is achieved only with a transformer design and is bulky. Some of the recently proposed flying capacitor based MLIs [8] and other MLIs with modified configuration with H-bridge circuit [9] are found to perform better for five-level operation with a better quality of output waveforms. But, these configurations demand more switching devices than usual.

Therefore, in this paper, a five-level inverter consisting of a full bridge DC/AC inverter connected to an auxiliary circuit cascaded with the sepic converter through a high-frequency transformer is presented [11]. The main advantage of the proposed topology is that high voltage boosting can be achieved with simple control. The complete operation of the proposed configuration is presented. Further, a detailed comparison of the various five-level inverters is presented to show the merit of the proposed topology.

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Moreover, simulation work has been carried out in Matlab software and an experimental prototype model is also developed to validate the results.

II. PROPOSED CONFIGURATION

Fig. 1 depicts the proposed modified structure of sepic based five-level T-type inverter for photovoltaic applications. It consists of various parts of sepic dc/dc converter, HF transformer, Full bridge DC/AC inverter and auxiliary circuits. The proposed configuration is more useful for single-phase applications. The five-level inverter is a modular structure and the levels can be extended by clamping the DC-link voltage with additional auxiliary circuits. The detailed operation of each part is as follows;

A. SEPIC Converter

The single-ended primary inductor converter (SEPIC) is constructed using two inductors, one capacitor and a single switch. The main advantage of this converter is it can be operated at less than, greater than or equal to the input voltage by adjusting the duty cycle. Besides one of the inductors is utilized as the primary winding of the HF transformer. This results in a reduction in the volume and size of the system.

Fig. 2 depicts the simple circuit configuration of the SEPIC converter. The voltage transfer gain(M) of the converter can be derived using the following formulae by applying volt-sec balance equations.

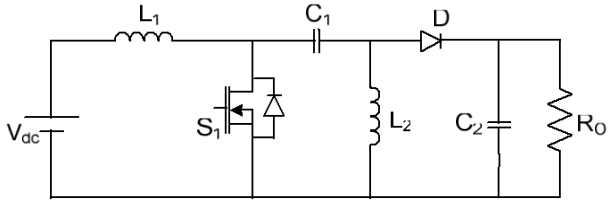


Fig. 2. SEPIC Converter.

$$M = \frac{V_o}{V_{dc}} = \frac{D}{1-D} \quad (1)$$

where V_{dc} is the input dc voltage, V_o is the output voltage and D is the duty cycle.

Moreover, The selection of inductor (L) and capacitor (C) also decides the response of the converter and also cost of the system. The larger size of L & C is more expensive and more internal resistance.

So proper value of L & C selected based on the ripple content and system capacity. Here the input inductor and capacitor can be selected using the following expression [12];

$$\frac{V_o}{V_{in}} = \frac{D}{(1-D)} \quad (1)$$

$$L = \frac{DV_{in}}{f_s \Delta I_L} \quad (2)$$

$$C = \frac{DV_{dc}}{Rf_s \Delta V_C} \quad (3)$$

B. Multilevel Inverter

The single-phase five-level T-type inverter with the reduced number of switches on a single DC source and an auxiliary circuit is shown in Fig. 3. The source voltage is split into two half over the DC-links using two capacitors. The positive half cycle and the negative half cycle is obtained with the use of a full bridge circuit; wherein the auxiliary circuit is used to generate levels such as V_{dc} and $2V_{dc}$. The switching states and corresponding output voltage levels are given in Table I. It can be noticed that only two switches are conducting for each level generation, which results in higher efficiency of the inverter topology.

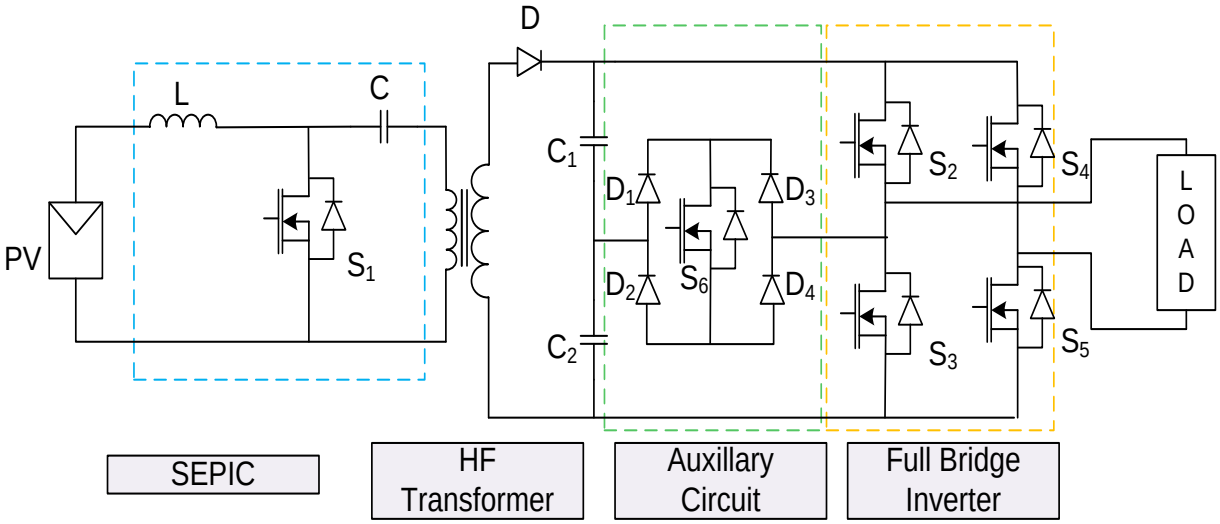


Fig. 1. Proposed SEPIC based single phase seven-level inverter[11].

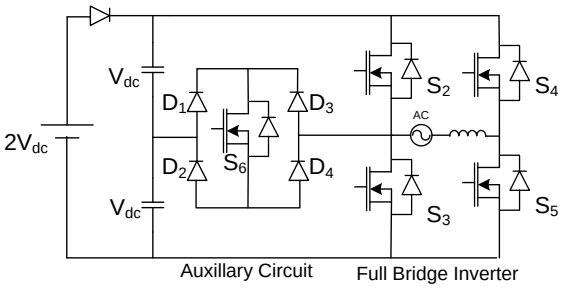


Fig. 3. Five-level inverter

Table- I: Switching states and Corresponding Output Voltage Levels

S_2	S_3	S_4	S_5	S_6	V_o	Number of conducting switches
1	0	0	1	0	$2V_{dc}$	2
0	0	0	1	1	V_{dc}	2
0	1	0	1	0	0	2
0	0	1	0	1	$-V_{dc}$	2
0	1	1	0	0	$-2V_{dc}$	2

III. CONTROL ALGORITHM

Simple sine pulse width modulation technique is used to generate the control signals for the five-level as shown in Fig. 4. A high-frequency carrier is compared with the level shifted modulated sine waveform to produce the switching signals for switches S_1 to S_5. It can be noticed that the switching pulses S3 and S4 are complementary and operate at a fundamental switching frequency; wherein other switches are operating at the higher switching frequency. Whereas, the modulation index M_a decides the output voltage level. It should be maintained between 0-1 for linear control in output voltage. M_a >1 leads to over modulation which results in higher harmonics in the output phase voltages.

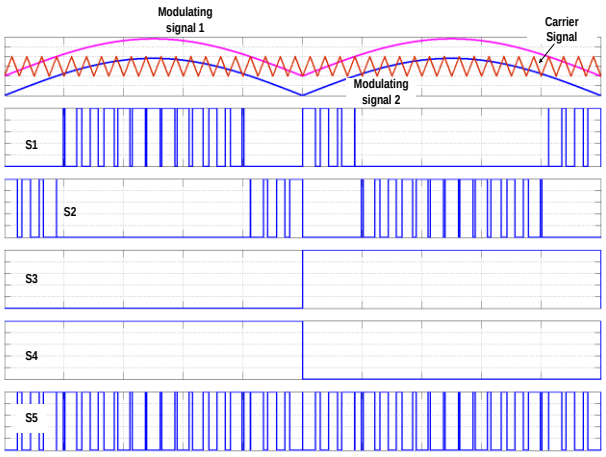


Fig. 4. Control pulses generation for five-level inverter.

IV. COMPARISON OF VARIOUS FIVE-LEVEL INVERTER

In this session, a detailed comparison is made with the recently proposed five-level inverters in the literature along with conventional CHB topology to show the merit of the proposed T-type structure using the auxiliary circuit. From Table II it can be noticed that the proposed MLI configuration demands less number of switches and better regulation of DC-link voltage and the voltage level can be enhanced by adjusting the duty cycle of the sepic converter. In the case of CHB and flying capacitor-based MLIs, it is difficult to enhance the voltage unless changes in the source voltages occur.

Table II: Comparison of recently proposed Five-Level Inverters

Topology	Number of DC Sources	Number of Switches	DC link Voltage regulation
CHB	2	8	No
Ref. [8]	1	8	No
Ref. [9]	1	8	No
Ref. [10]	1	6	Yes
Proposed	1	5	Yes

V. RESULTS AND DISCUSSION

In this session, the proposed topology is verified through Matlab simulation and experimental prototype model. The parameters considered for the simulation and experimental studies are given in Table III. Fig. 5 depicts the simulated waveforms of the input voltage, dc-link capacitor voltages, five-level inverter output voltage and their corresponding load currents respectively. It can be noticed that the input voltage is maintained constant and boosted to an output voltage of 150V by SEPIC converter and further stepped up to 300V with HF transformer. The voltage across the capacitors is maintained at 150V to generate five-level output voltage waveform. It can be noticed that the output voltage is always maintained constant during load transitions from 3A to 8A peak to peak at 1 sec. By employing a suitable controller the output voltage can be regulated for both step changes in load as well as input voltage changes. Fig. 6 illustrates the measured frequency spectrum of both inverter five-level output voltage and load current waveforms. The %THD of the output current is within IEEE standard limits. This shows that the proposed configuration is well suited for PV applications**.** Further, an experimental setup is developed using IRF460 Mosfet and the control signals are generated each semiconductor devices using fpga Xilinx Matlab blocks are shown in Figs. 7 and 8 respectively. It can be noticed that the experimental results are made for scaled down voltage of 25V/div due to limitations of the available facilities in the laboratory. The measured five-level output voltage waveform and their corresponding load current as shown in Fig. 9. Moreover, the patterns of experimental results have good agreement with the simulation results. This validates the effectiveness of the proposed topology is more suitable for PV applications.

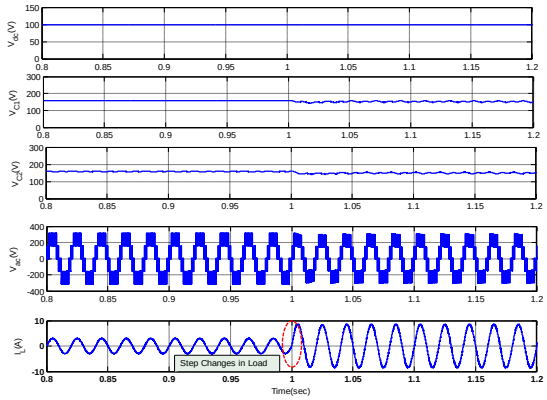
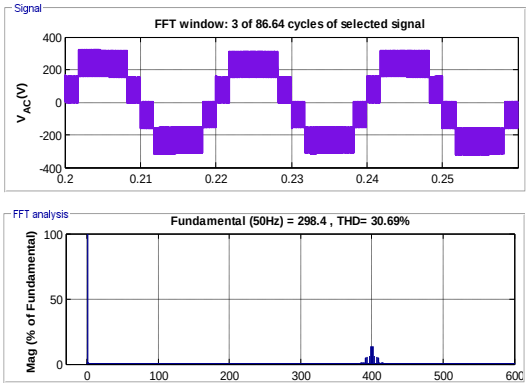
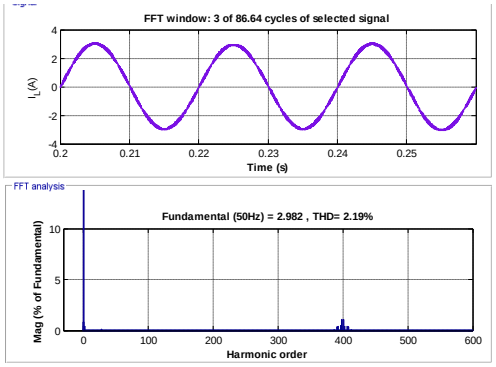


Fig. 5. Input voltage, output voltages, inverter output voltage and load current.



(a)



(b)

Fig. 6. FFT spectrum of (a) Inverter output voltage and (b) Load current.

Table III: Specifications of the parameters

Parameters	Values
Input dc voltage V	100 V
Inductor L	500 μH
Capacitors C, C_1 & C_2	100F, 2000F, 2000F
LCL Filter	1mH, 1F
Switching Frequency of the SEPIC converter	50 kHz
Switching Frequency of the five-level inverter	40 kHz
RL Loads	100Ω, 10mH; 50Ω, 10mH

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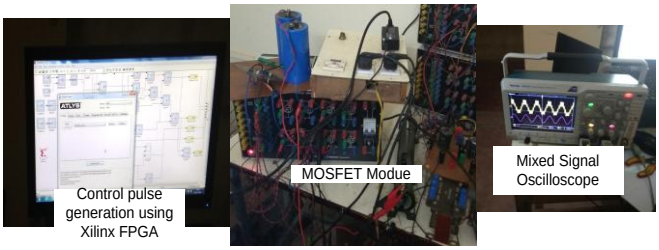
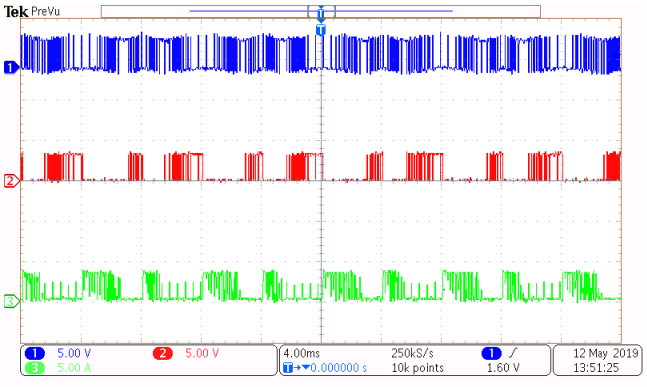
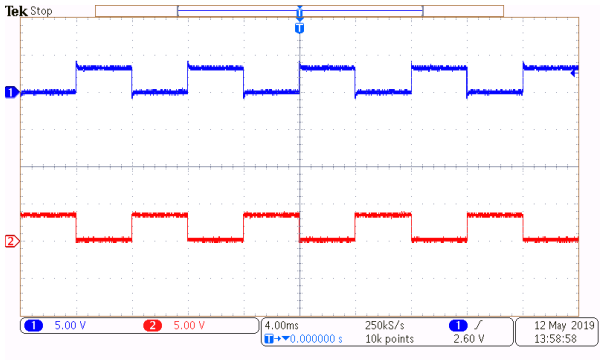


Fig. 7. Experimental setup.



(a)



(b)

Fig. 8. Switching Pulses

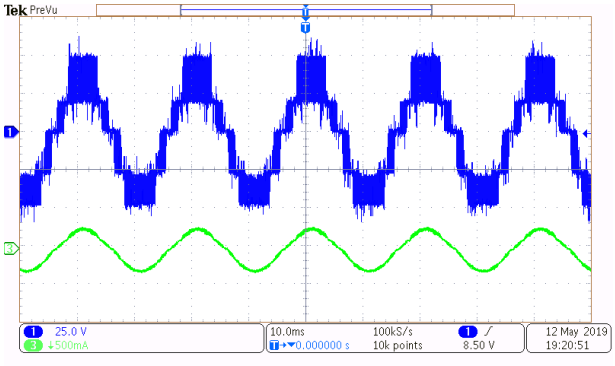


Fig. 9. Inverter output voltage and load current.

VI. CONCLUSION

In this paper, a modified structure of sepic based five-level inverter is presented for photovoltaic applications. The paper also addresses the complete operating and switching control schemes developed for the proposed configuration. Simulation work is carried out in Matlab software and tested for load changes to observe their performance. The %THD of the voltage and current waveforms are also measured and within the IEEE limits. A detailed comparison of different five-level inverters presented to show the merit of the proposed configuration. Further experimental results validate the simulation results that the proposed topology is eminently suited for PV applications.

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