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RESEARCH ARTICLE

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FPGA-based implementation of single-phase seven-level quasi-Z-source inverter

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Summary

In this paper, a new single-phase seven-level quasi-Z-source (qZs) inverter with reduced switch count for multistring photovoltaic applications is proposed, which is capable of supplying both direct current (dc) and alternating current (ac) loads simultaneously. The proposed configuration is derived from a combination of qZs networks and asymmetrical seven-level inverter. The front-end qZs converter boosts the input voltage obtained from the dc sources to the desired value, whereas the asymmetrical seven-level inverter performs dc-ac conversion with reduced switch count and provides better efficiency. The steady-state performance of the model is evaluated in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) of operation. In addition, the dynamic performance of the model is tested for the load as well as input voltage changes. A simple proportional-integral (PI) controller is implemented in FPGA Spartan-6 Processor using Xilinx system generator blocks. An experimental prototype is also developed to validate the feasibility of the proposed topology. Finally, a brief comparative assessment is formulated with other topologies to show the merits of the proposed structure.

KEYWORDS

multilevel inverter, power losses, quasi-Z-source (qZs) network, total harmonic distortion (THD)

1 | INTRODUCTION

The dwindling supply of fossil fuels and increasing global environmental concerns have been addressed by enhancing energy generation from renewable energy sources. Among all renewable sources, photovoltaic (PV) is a promising candidate and has gained a lot of attention in recent years due to the reasonable cost of investment, eco-friendly nature, and large generation capacity. The PV installation cost has come down in recent years. However, the development of suitable power conditioners plays a key role in extracting maximum power from PV during intermittent conditions of temperature and irradiation changes.

The evolution of Z-source inverters[1] (ZSIs) in the area of power electronics has seen a significant rise in the last decade due to its wide range of applications in major areas like uninterruptible power supply (UPS), facts, hybrid electrical vehicles,[2] and distributed generation (DG). The limitations of voltage source inverters (VSIs) and current source inverters (CSIs) are addressed through flexible control of output voltage by allowing overlap of switches for a part of switching cycle, which eliminates the need of dead band between the switches, thus reducing the waveform distortion and enhancing reliability. In addition, it provides single-stage power conversion with buck-boost capability, thus improving the efficiency of the system compared with two-stage conversion due to reduced component count. However,

the inverter suffers from discontinuous input current profile in boost mode. To address this problem, quasi-Z-source (qZs) inverter (qZSI) is developed, which inherits the same features of ZSI. In addition, it provides low voltage stress across C_2, thus reducing its size while providing continuous input current and common grounding between source and load.[3,4] Hence, qZSI is becoming popular among all Z-source-based topologies. A comprehensive survey on different Z-source topologies and their advancements is reported in Siwakoti et al.[5]

In contemporary, multilevel inverter (MLI) is becoming popular for low-voltage and low-power applications. It offers significant advantages of lower device ratings, low dv/dt, low total harmonic distortion (THD), and reduced filter size. Some well-known and popular topologies are neutral-point-clamped MLIs (NPC MLIs), flying capacitor MLIs (FC MLIs), and cascaded H-bridge MLIs (CHB MLIs). Among these, CHB is most preferred due to its modularity feature.[6] Moreover, several topologies are developed in recent years in terms of reduced component count, capacitor voltage balancing, control complexity, and the number of direct current (dc) sources. However, the switch count remains a major constraint in developing new topologies. Despite the various advantages, the output gain of MLI is buck in nature, which is a limitation. This necessitates a suitable power conditioner to be upgraded with MLI in order to improve input voltage regulation as well as output voltage gain. Therefore, MLI is upgraded with impedance source network with features of improved output voltage gain, enhanced reliability, enhanced input voltage regulation, and quality output waveforms for the increase in levels.

A single-phase Z-source-based three-level (3L) NPC inverter[7] is reported, which requires two Z-source networks and a common neutral point. This structure is further extended for three-phase applications with single ZSI.[7] The Z-source-based diode-clamped inverter is reported for four- and five-level operations.[8,9] However, the discontinuous input current pattern is a major concern for all these topologies. An improvised single-phase 3L NPC qZSI[10] topology using a single dc source with reduced capacitor voltage stress and continuous input current is presented. A Z-source-based 7L inverter[11] with reduced switch count is reported, which is derived from a combination of Z-source networks and multilevel dc-link inverter. A 7L qZSI CHB configuration is reported for PV applications in Sun et al.[12] Moreover, in recent years, some modified configuration of qZs-based cascaded MLIs was introduced to improve the voltage gain for five-level operation.[13-15] However, these topologies were associated with problems of more dc sources and passive components for more output voltage levels. Husev et al[16] address the various configurations of impedance-based MLIs proposed in recent years. From the literature, it is noticed that most of the topologies are NPC- and CHB-based impedance networks, which demand more fast recovery diodes and semiconductor devices for increased output voltage levels, which increase the overall cost and size of the system.

Therefore, a new structure of single-phase qZs-based seven-level inverter is proposed with the features of reduced switch count, simple control, and high efficiency.[17] Moreover, the proposed topology is modular, provides better output voltage regulation, and is highly suitable for multistring-based PV applications. The performance of the proposed topology is studied with the boundary condition between CCM and DCM for different loads under the steady state in Section 2. The merits of the proposed structure are highlighted in Section 3 with a comparison of recently proposed topologies. Section 4 presents the complete method of control pulse generation using MATLAB Xilinx system generator blocks. The simulation and experimental results are reported in Section 5. Moreover, the dynamic performance of the model is also evaluated for step changes in input voltage and load. Finally, Section 6 presents the concluding remarks.

2 | SYSTEM CONFIGURATION

Figure 1 shows the proposed qZs-based seven-level inverter topology for multistring PV applications. It consists of a qZs-based dc-dc network as a basic unit interfaced with an asymmetrical seven-level inverter configuration. The number of input dc sources depends on the number of strings connected. Here, the qZs dc-dc networks act as a front-end power conditioning unit to process the input voltages of V_{pv1} and V_{pv2}, which are obtained from PV array. This voltage is boosted to the desired value by regulating the shoot-through duty cycle D_o of switches S_1 and S_2. Both the strings can be operated independently, which facilitates better ease of control, and it further provides the provision of extension by adding an extra string with corresponding changes in asymmetrical inverter due to its modularity feature. The performance and voltage gain of the qZs converter is also determined by the type of filters such as C filter or LC filter. A C filter is preferred as it offers better voltage gain, and the dc bus voltages V_1 and V_2 are fed to the seven-level inverter for realizing the seven-level output. This seven-level inverter enables optimum performance by enhancing the voltage and current profile, reduced filter size, and low electromagnetic interference (EMI) due to the increased number of levels.

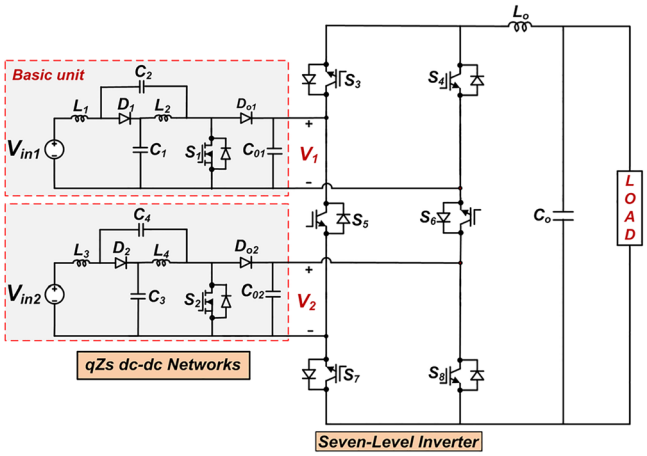

FIGURE 1 Proposed single-phase seven-level quasi-Z-source-based inverter [Colour figure can be viewed at wileyonlinelibrary.com]

2.1 | qZs dc-dc converter

Quasi-Z-source dc-dc converter performs both boosting and output voltage regulation, which is fed from various uncontrolled input DG sources. Figure 2A illustrates the qZs converter, which comprises impedance LC network, one switch for regulating the output voltage, and an LC filter for obtaining constant dc bus voltage. The performance of the qZs network is evaluated under DCM and CCM operation. The mode of operation and its characteristics are determined by the circuit parameters such as inductance L, load current I_o, operating frequency f, and input voltage V_{in}.

2.2 | Analysis of qZs converter in CCM

Figure 2C,D shows the corresponding circuits of the qZs network under shoot-through states and active states. In general, the total operating period T is basically divided into two states, ie, (a) active-state T_1 and (b) shoot-through-state T_0.

$$T = T_0 + T_1 \tag{1}$$

This can be also expressed as

$$\frac{T_0}{T} + \frac{T_1}{T} = D_0 + D_1 = 1, \tag{2}$$

where D_0 is the shoot-through duty cycle and D_1 is the active-state duty cycle.

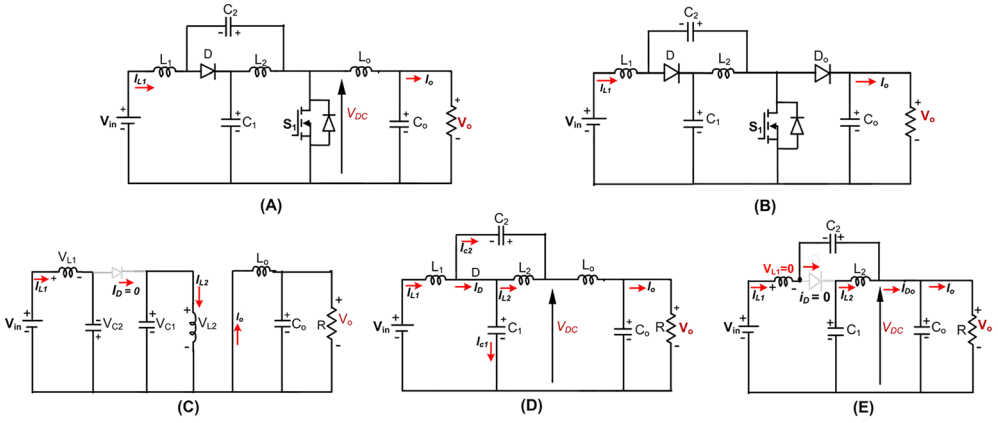

FIGURE 2 (A) Quasi-Z-source (qZs) direct current–direct current (dc-dc) converter with LC filter; (B) qZs dc-dc converter with C filter; equivalent circuits during (C) shoot through; (D) active state; (E) discontinuous state [Colour figure can be viewed at wileyonlinelibrary.com]

The maximum output dc voltage of the qZs network[18] is

$$V_{\mathrm{DC\ (max)}} = V_{c1} + V_{c2} = \frac{1}{1-2D_0} V_{\mathrm{in}}. \tag{3}$$

The attenuated filtered output voltage that is fed to the dc load and MLI is given by

$$V_0 = V_{c1} = \frac{1-D_0}{1-2D_0} V_{\mathrm{in}}. \tag{4}$$

Further, the analysis is extended for qZs dc-dc network with C filter as depicted in Figure 2B. The analysis remains the same as discussed above, but the voltage gain changes due to the diode.

$$V_0 = V_{\mathrm{DC\ (max)}} = \frac{1}{1-2D_0} V_{\mathrm{in}} \tag{5}$$

From (4) and (5), it can be noted that qZs converter with C filter enables better output voltage gain when compared with the qZs converter with LC filter for a particular value of duty cycle. However, a large capacitance is required to alleviate the 2ω ripple oscillations in the output dc-link voltage. Hence, CCM operation is demonstrated using qZs converter with C filter in simulation and experimentation. Figure 3 illustrates the typical waveforms of inductor currents, diode current, dc-link voltage, capacitor voltages, and inductor voltages of the qZs converter operating in CCM and DCM for one switching cycle.

2.3 | Analysis of qZs converter in DCM

In the qZs converter, the DCM operation occurs relatively at lower loading conditions. However, it depends mainly on the switching frequency, value of inductance, and loading conditions. This operation may lead to instability in operation, over boost effect of the output voltage, and cause damage of components when operating at small loads. Hence, this mode of operation needs special attention regarding the design of components and selection of switches.[19] The analysis based on DCM is as follows.

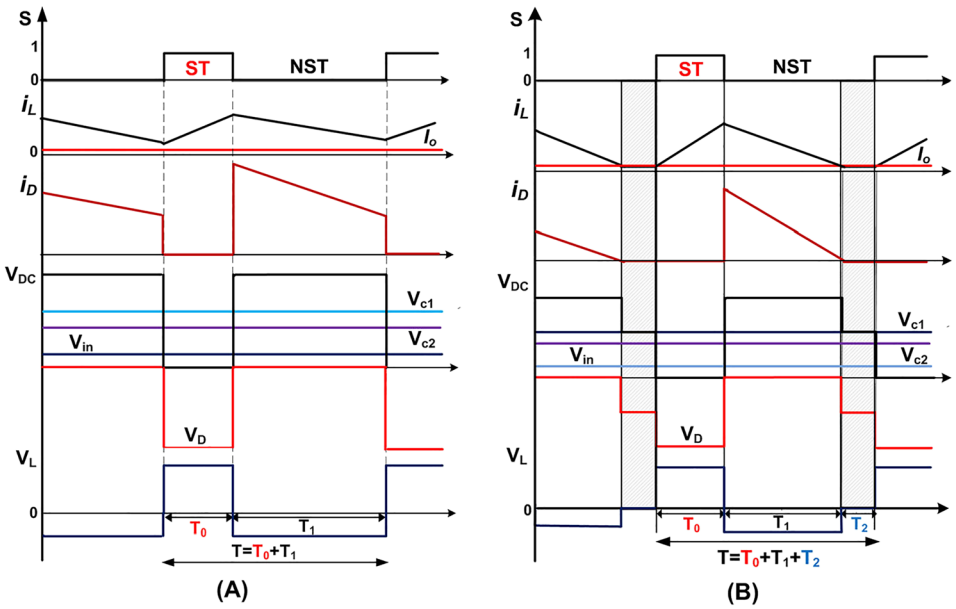

FIGURE 3 Typical voltage and current waveforms of the quasi-Z-source (qZs) converter: (A) continuous conduction mode (CCM) and (B) discontinuous conduction mode (DCM) [Colour figure can be viewed at wileyonlinelibrary.com]

The operating period T is divided into active-state T_1, shoot-through-state T_0, and discontinuous conduction–state T_2.

$$T = T_0 + T_1 + T_2 \tag{6}$$

This can be also expressed as

$$\frac{T_0}{T} + \frac{T_1}{T} + \frac{T_2}{T} = D_0 + D_1 + D_2 = 1, \tag{7}$$

where D_0 is the shoot-through duty cycle, D_1 is the active-state duty cycle, and D_2 is the discontinuous-state duty cycle, respectively.

In DCM mode of operation, the active-state T_1 and shoot-through-state T_0 are similar to CCM operation. The operation varies slightly during the discontinuous conduction–state T_2 only. From Figure 3B, it can be observed that the inductor current drops to $\frac{1}{2}I_0$ when the diode is off and the inductor voltage is 0. The dc-link voltage drops to the value of V_0.

Assuming an ideal qZs converter, the expression used to calculate the load voltage is given in Vinnikov et al.[20]

$$V_0 = V_{c1} = \frac{1 - D_0 - D_2}{1 - 2D_0 - D_2} V_{\text{in}}, \tag{8}$$

$$I_L = \frac{I_o}{2} + \frac{V_{L2.}T_0}{2.L.T}(T_0 + T_1) = \frac{I_0}{2} + \frac{V_o D_o^2}{2.L.f}\left(\frac{2V_o - V_{\text{in}}}{V_o - V_{\text{in}}}\right), \tag{9}$$

where f, L, and V_{L2} are the switching frequency, inductance, and voltage across the inductor L_2, respectively. It is observed from Equations (8) and (9) that the change in mode from CCM to DCM leads to increase in output voltage.

Considering a lossless system, balancing the input and output powers,

$$V_{\text{in}} I_L = V_o I_o. \tag{10}$$

From Equations (8) and (9), it can be written as

$$\frac{2.V_o.D_o^2}{V_o - V_{\text{in}}} = \frac{2.I_o.L.f}{V_{\text{in}}}. \tag{11}$$

By introducing a coefficient,

$$\gamma = \frac{2.I_o.L.f}{V_{\text{in}}}. \tag{12}$$

Finally, the modified dc output voltage equation form (11) in DCM is

$$V_o = \frac{\gamma}{\gamma - 2D_o^2} V_{\text{in}}. \tag{13}$$

The output voltage in DCM is decided by the coefficient γ.[21] Hence, the over boost effect can be compensated by properly regulating the operating frequency f, inductance L, and load current I_o. At this juncture, it would be appropriate to derive the boundary condition, at which no DCM occurs from Equation (13),

$$\gamma > 2D_o^2, \tag{14}$$

$$L > \frac{D_o^2}{I_o.f} V_{\text{in}}. \tag{15}$$

Equations (14) and (15) should be satisfied to prevent instability and abnormal operation of the qZs networks. Figure 4A shows the variation of voltage gain versus γ of the qZs networks for different values of duty cycle D_0. This

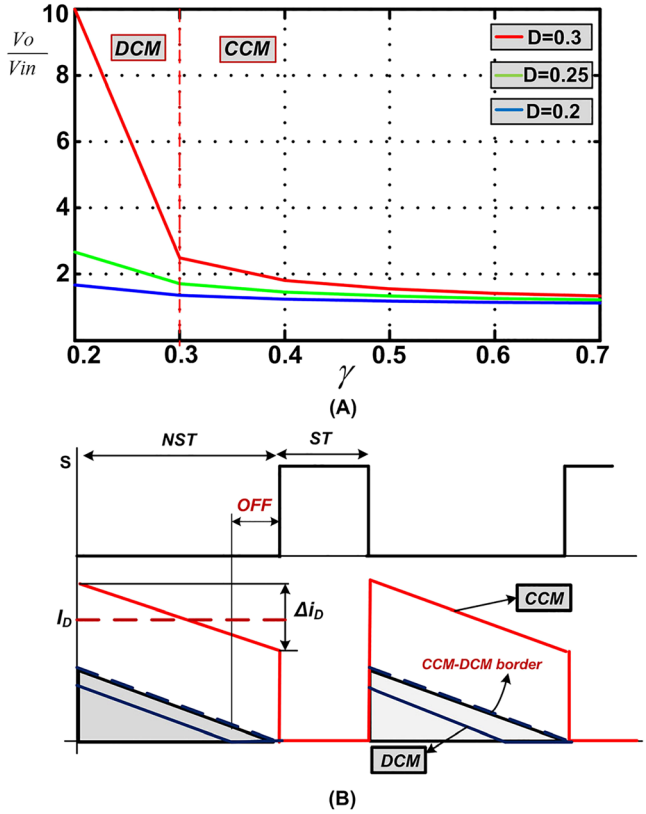

FIGURE 4 A, Voltage gain vs γ under continuous conduction mode (CCM) and discontinuous conduction mode (DCM). B, Current through diode and CCM-DCM border operation [Colour figure can be viewed at wileyonlinelibrary.com]

shows that higher voltage gain is achieved for a particular duty cycle in DCM. There is no significant increase in gain for the increase in γ, and it also reduces efficiency due to the increase in losses. However, the higher coefficient of γ is selected for CCM, especially for higher loads and increased frequency operation.

2.4 | Boundary condition between CCM and DCM

The boundary between CCM and DCM modes can be estimated from the diode current waveform I_D as shown in Figure 4B. During the shoot-through state, the diode is in off condition, while the diode current in the non-shoot-through (NST) state in CCM depends on the input current. The transition between CCM and DCM is clearly evident from the CCM-DCM border[22] given in Figure 4B. In DCM, the diode becomes off during discontinuous-state T_2.

The condition for the converter to operate in CCM can be expressed as follows:

$$I_D > \frac{\Delta i_D}{2}. \tag{16}$$

Assuming that the system is under CCM mode, during the NST,

$$\Delta i_D \approx \Delta i_L. \tag{17}$$

From the analysis, the average value of diode current can be expressed in terms of inductor current I_L as

$$I_D \approx I_L(1 - D_o). \tag{18}$$

During the NST state, Δi_L can be expressed as

$$\Delta i_L = \frac{V_L(1 - D_o)}{Lf_s}. \tag{19}$$

Analyzing the voltage across inductor V_L during NST,

$$\Delta i_L = \frac{D_o V_{\text{in}}(1-D_o)}{(1-2D_o)Lf_s}. \tag{20}$$

From Equations (5), (10), and (20), the inequality relation (16) can be used for deriving the critical resistance,

$$R_{\text{crit}}$$

$$R_{\text{crit}} = \frac{2Lf_s}{(1-2D_o).D_o}. \tag{21}$$

Considering $L = 0.5$ mH, $f_s = 10$ KHz, and $D_o = 0.25$,

$$R_{\text{crit}} = \frac{2\times 0.5\times 10^{-3}\times 10^3}{(1-2\times 0.25)\times 0.25} = 80\ \Omega, \tag{22}$$

where R_o is the alternating current (ac) load resistance. If $R_o > R_{\text{crit}}$, the system operates in DCM; otherwise, the system operates in CCM. This is applicable for any value of duty cycle for a constant switching frequency and the corresponding inductance.

2.5 | Design of passive components

The values of inductance and capacitance of the qZs network are designed so as to mitigate the double frequency (2ω) ripple[12] in the input current and dc-link voltage,[23] respectively, during shoot-through-state D_0T and can be expressed as

$$L \geq \frac{x_c{}^*V_{\text{in}}{}^*(1-2D)}{4\omega\, x_L MI_o\cos\varnothing}, \quad C \geq \frac{(1-2D)(1+x_L\cos\varnothing)MI_o}{2x_c\omega V_{\text{in}}}. \tag{23}$$

Assuming the acceptable input current ripple to be x_L%, which is defined as

$$x_L\% = \frac{\Delta i_L}{I_L}\times 100. \tag{24}$$

Assuming the acceptable voltage ripple to be x_C%, which is defined as

$$x_c\% = \frac{\Delta V_c}{V_c}\times 100. \tag{25}$$

Considering x_L=20%, $x_c = 3\%$, $D_o = 0.25$, $I_o = 5$ A, $f_s = 10$ kHz, $V_{\text{in}} = 30$ V, $M = 0.9$, $\varnothing = 0$, where I_o represents the peak value of output current and $\varnothing$ represents the impedance angle. The values of inductance and capacitance are computed to be around 0.398 mH and 477 μF, respectively. Hence, an inductance value of 0.5 mH and capacitance value of 500 μF are considered in this study.

The dc bus capacitor is selected so as to keep the voltage deviations across the dc bus within specified limits. The net power flowing into the dc bus capacitor can be expressed as follows:

$$P_{\text{bus}} = P_{\text{qzs}} - \frac{V_o I_o}{2}(1-\cos 2\omega t). \tag{26}$$

Using the maximum change in the stored energy of the capacitor, the value of the dc bus capacitor C_o can be derived from the following relation[24]:

$$V^2_{\text{bus,max}} = V^2_{\text{bus,min}} + \frac{2P_{\text{qzs}}}{\omega C_o}. \tag{27}$$

Considering the maximum voltage deviation, $\nabla V_{\text{bus}} = V_{\text{bus,max}} - V_{\text{bus,min}} = 10$ V, and P_{qzs} is the total output power of the qZs units.

The value of dc bus capacitance C_o is computed to be around 1000 μF and can be expressed as

$$C_o = \frac{C_{o1} \times C_{o2}}{(C_{o1} + C_{o2})}. \tag{28}$$

Hence, the values of the dc bus capacitances C_{o1} and C_{o2} are chosen as 2000 μF in order to keep the voltage deviations within limits.

2.6 | Seven-level inverter

In this configuration, packed U cells[25] (PUCs)–based MLI is adopted for synthesizing the seven-level output voltage.[26] It is found to be superior due to lower semiconductor devices, size, cost, and switching losses compared with its equivalent CHB, NPC, and FC MLIs. However, it requires switches of different voltage rating and isolated dc sources for its realization. The PUC is constructed in string form by cascading various semiconductor devices in the ratings of 1, 2, 3 V,

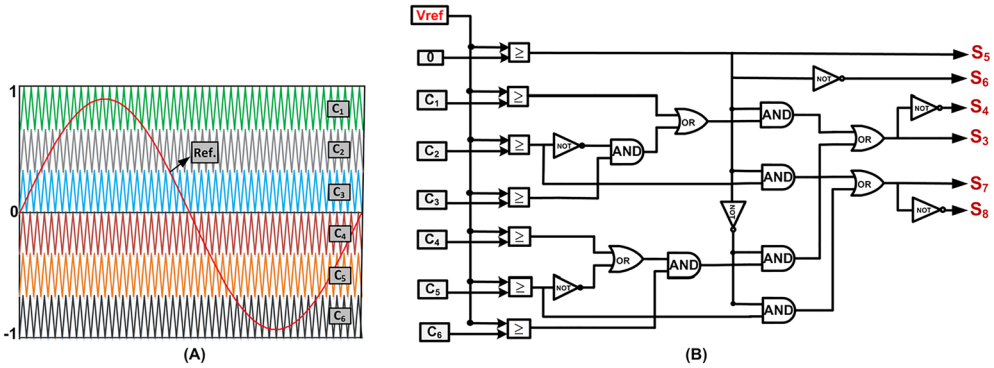

FIGURE 5 A, Multicarrier sinusoidal pulse width modulation (PWM). B, Switching scheme for seven-level inverter [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Comparison of various 7L qZs MLIs

Components	CHB qZSI[12]	Cascaded qZSI[11]	Transformer-Based qZSI[27]	Proposed Inverter
DC sources	3	3	1	2
Inductors	6	6	2	4
Capacitors	6	6	2	6
Diodes	3	3	1	4
Switches	12	10	12	8
HF transformers	-	-	3	-
Galvanic isolation	No	No	Yes	No

Abbreviations: CHB, cascaded H-bridge; DC, direct current; HF, high frequency; MLI, multilevel inverter; qZs, quasi-Z source; qZSI, quasi-Z-source inverter.

TABLE 2 Voltage stress across the switches

Topology	Voltage Stress												TBV
Switches	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
CHB qZSI[12]	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	12 V_{dc}
Cascaded qZSI[11]	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	3 V_{dc}	3 V_{dc}	3 V_{dc}	3 V_{dc}	-	-	18 V_{dc}
Transformer-based qZSI[27]	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	12 V_{dc}
Proposed inverter	V_{dc}	2 V_{dc}	V_{dc}	V_{dc}	3 V_{dc}	3 V_{dc}	2 V_{dc}	2 V_{dc}	-	-	-	-	15 V_{dc}

Abbreviations: CHB, cascaded H-bridge; qZSI, quasi-Z-source inverter; TBV, total blocking voltage.

and so on for increased output voltage levels. The increase in output voltage level also depends on the suitable combinations of cascading the input sources. Here, two strings are utilized to produce the seven-level output waveform. The control scheme based on multicarrier sine pulse width modulation and switching logic is depicted in Figure 5A,B. However, any imbalance in dc bus voltages will lead to unequal voltage levels, which results in waveform distortion. Therefore, dc bus voltages should be maintained constant by adjusting the shoot-through duty cycle of the respective qZs networks for variations in input voltage and load.

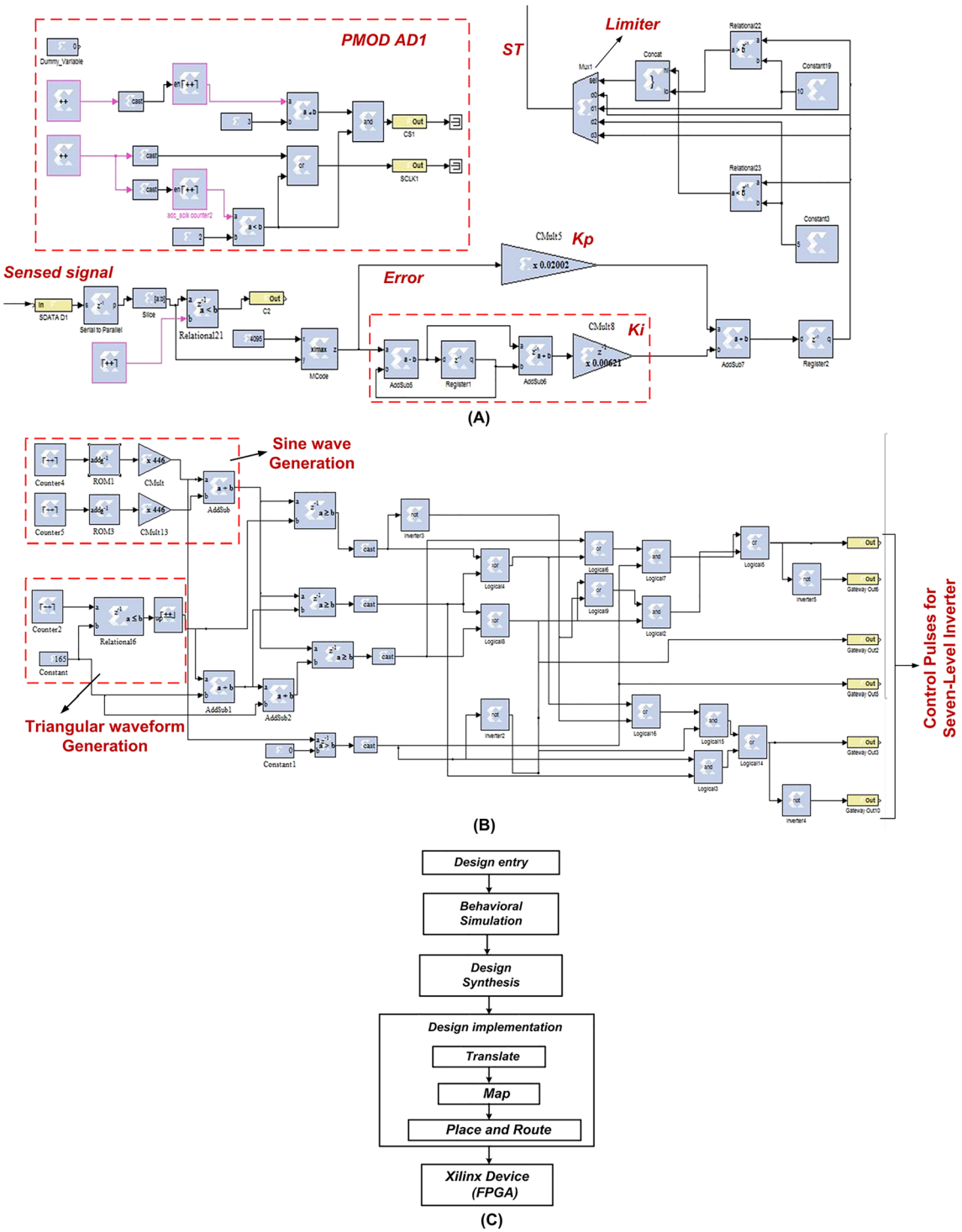

FIGURE 6 A, Proportional-integral (PI) controller implementation. B, Control pulses for seven-level inverter. C, Field programmable gate array (FPGA) design flow [Colour figure can be viewed at wileyonlinelibrary.com]

3 | COMPARISON OF SEVEN-LEVEL QZS INVERTER TOPOLOGIES

In this section, a detailed comparison of various seven-level qZs inverter is constructed in Table 1 to elaborate the features of components and their benefits. It can be noticed that the proposed inverter requires two dc sources, reduced switch count (eight switches), and lower inductor count when compared with CHB qZSI and cascaded qZSI. Although the transformer-based qZSI utilizes only one dc source and lower passive component, it requires three high-frequency transformers, which increase the size, weight, and cost of the inverter, and is suitable only for low-power applications.

Voltage stress is another important parameter, which decides the performance of the configuration. Hence, the voltage stress of each semiconductor devices and the total blocking voltage (TBV) of each configuration in terms of dc-link voltage V_{dc} are presented in Table 2. The proposed inverter requires higher voltage-rated switches for S_5 to S_8 when compared with CHB qZSI. However, these semiconductor devices operate at a fundamental frequency, which results in reduced losses. Moreover, the output levels can be enhanced by adding the number of strings with corresponding changes in asymmetrical MLI with lower increment in switching devices compared with other qZs MLIs.

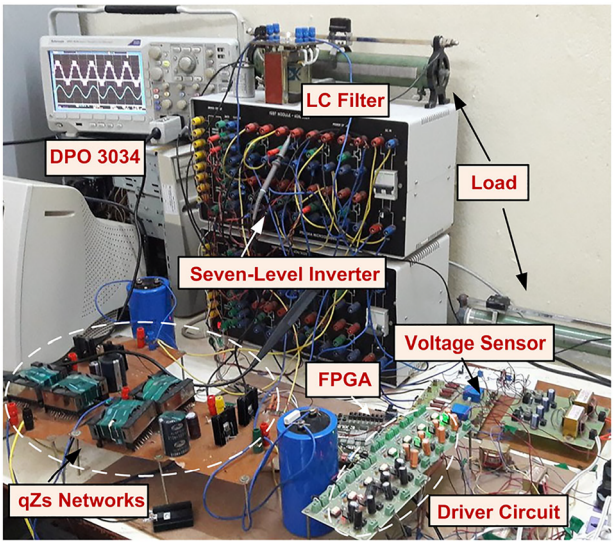

FIGURE 7 Experimental setup of the proposed inverter [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 3 System parameters used for simulation and experimentation

Parameters	Values
Input DC voltages (V_{in1} and V_{in2})	25-40 and 50-80 V
Inductors L_{1i}, L_{2i}, r_L	0.5 mH, 0.092 Ω
Capacitors C_{1i}, C_{2i}, r_c	500 μF, 0.12 Ω
Filter capacitor C_o, r_{c0}	2000 μF, 0.12
Filter inductor L_f, capacitor C_f	4 mH, 25 μF
Switching frequency of qZs network, f_s	10 kHz
Switching frequency of MLI	3 kHz
Fundamental frequency	50 Hz
Modulation index, m_a	0.9
AC load	60 Ω (CCM); 120 Ω (DCM)

Abbreviations: AC, alternating current; CCM, continuous conduction mode; DC, direct current; DCM, discontinuous conduction mode; MLI, multilevel inverter; qZs, quasi-Z source.

4 | PWM GENERATION USING XILINX FPGA BLOCKS

In earlier days, the development of the controller using analogue ICs is quite complex and bulky. Advancement in digital controllers enabled researchers to adopt them for their user-friendly nature, fast processing operation, and reliability. Integration of controller with MATLAB enables easy implementation for testing various circuits in real time using digital signal *processor* (DSP) and field programmable gate array (FPGA) processors in recent years. However, one of the major difficulties faced in DSP is the implementation of level-shifted multicarrier triangular waveforms and its comparison with fundamental sine waveform for MLI operation. The FPGA overcomes this drawback, and it is easy to implement complex control schemes with Xilinx system generator blocks in MATLAB software.[28] In some of the modern system, the features of both DSP as controller and FPGA for the sensing signals and level generation are used.

Figure 6 shows the control scheme developed in MATLAB using Xilinx tools for the proposed topology. In general, the counter block generates sawtooth and triangular waveforms either by selecting up/up-down mode operation. Here, the maximum count period is limited by the number of bits selection. For example, the counter is enabled for the free running value of 256 counts for 8-bit operation. However, the designer can limit/select suitable count periods based on their demands. The ROM block is used to generate the sine signal based on selecting an appropriate count period, and frequency can also be regulated. The generated sine wave is compared with the level-shifted triangular waveforms, and the control pulses are generated by using the relational and logical blocks. The gateway out is used to assign proper I/O as per the pin assignment given in Atlys Spartan-6 user manual. Further, the system generator simulates and generates the corresponding VHDL code for the developed model in MATLAB. The control logic can be realized in FPGA for any power electronic converter. Figure 6C shows the design flow of FPGA using Xilinx tools.

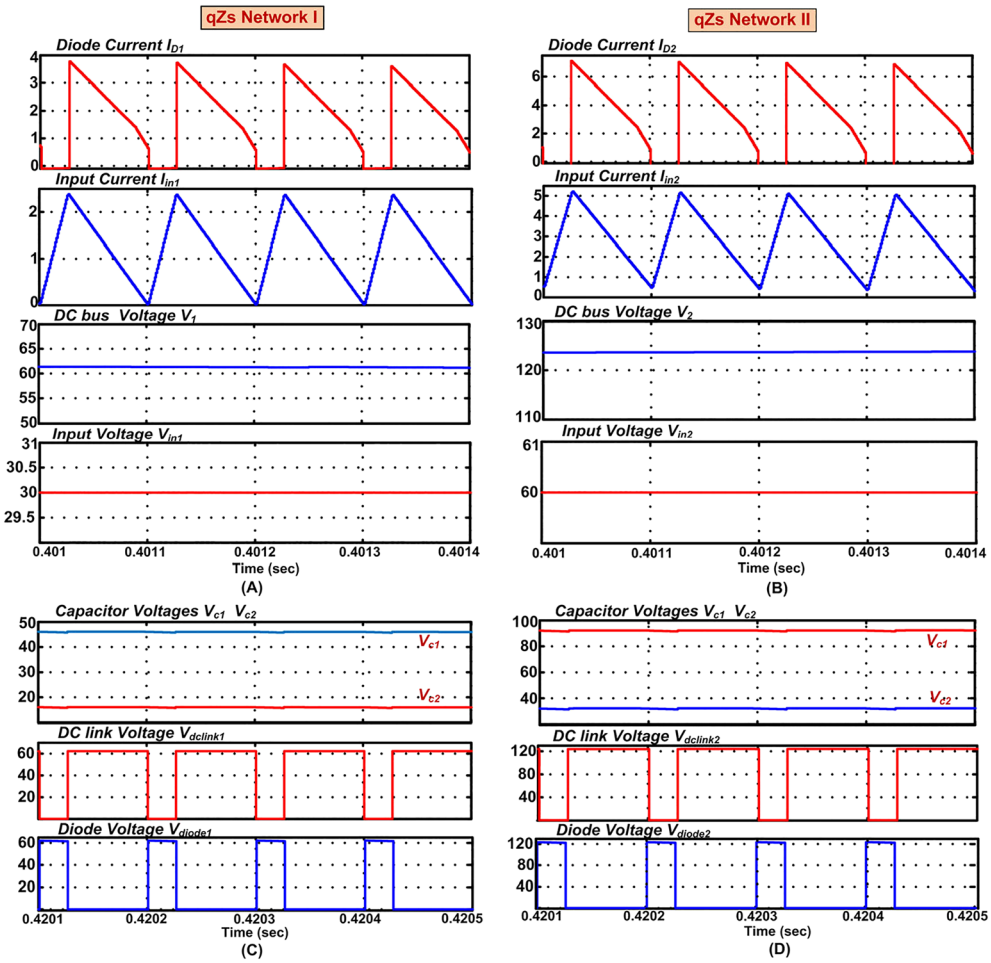

FIGURE 8 Simulation results in continuous conduction mode (CCM): input voltage, input current, diode current, and direct current (dc) bus voltage of (A) quasi-Z-source (qZs) network I and (B) qZs network II capacitor voltages and dc-link voltage and diode voltage of (C) qZs network I and (D) qZs network II [Colour figure can be viewed at wileyonlinelibrary.com]

5 | RESULTS AND DISCUSSION

In this section, the performance of the model is verified from the simulation and experimental results under the same conditions. The simulation is performed in MATLAB software, and a prototype model is constructed as a proof of concept based on the available components in the laboratory as shown in Figure 7, and their specifications are given in

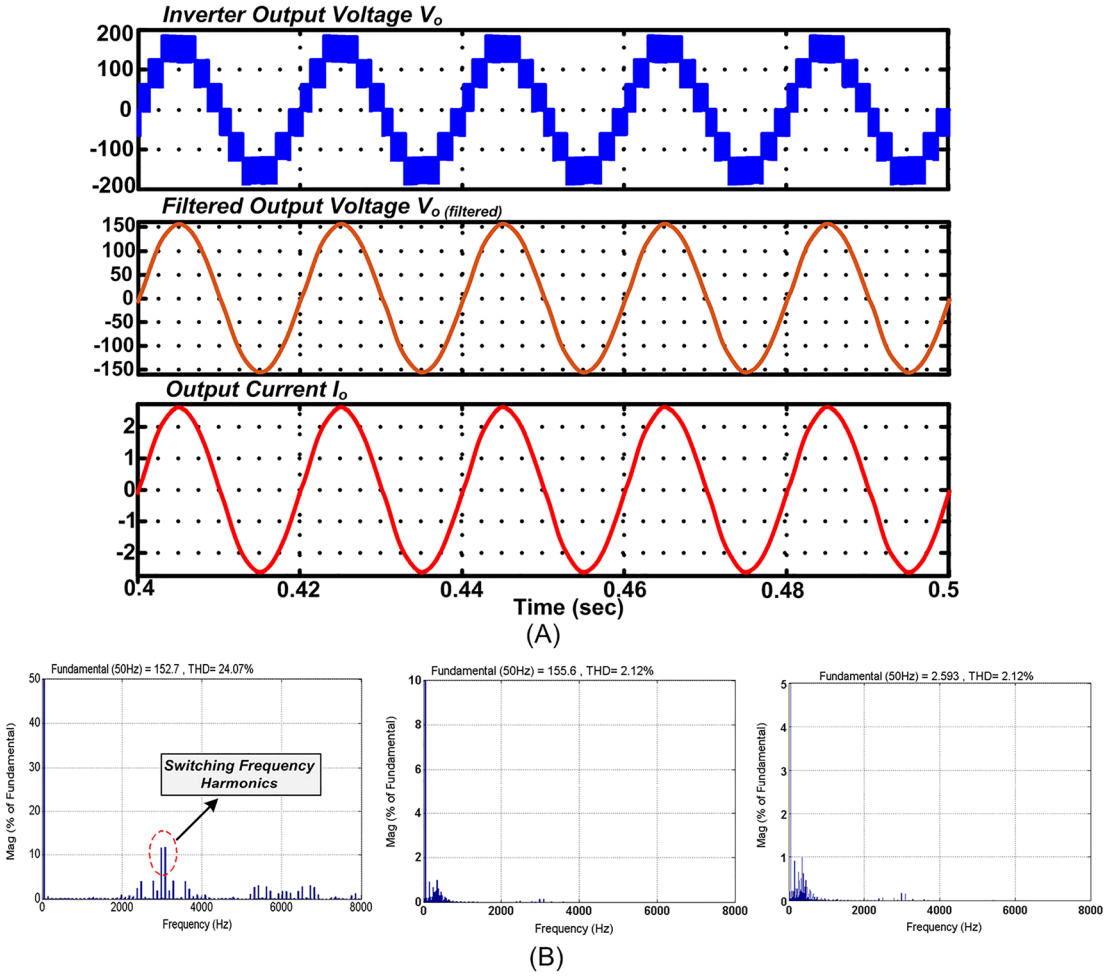

FIGURE 9 Simulation results in continuous conduction mode (CCM). A, Output voltage V_o, V_o (filtered), output current I_o. B, Harmonic spectrum of output voltage V_o, V_o (filtered), output current I_o [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 4 Harmonics of output voltage

Harmonics h	$m_a = 0.9$	$m_a = 0.8$
Fundamental	165.7	147.6
3	0.944	0.723
5	0.249	0.148
7	0.116	0.059
9	0.132	0.162
11	0.18	0.177
THD (%), $\boldsymbol{V_o}$	21.89	23.76
THD (%), $\boldsymbol{V_{o,f}}$	0.77	0.64
THD (%), $\boldsymbol{I_o}$	0.77	0.64

Abbreviation: THD, total harmonic distortion.

Table 3. Moreover, in simulation, the nonidealities of the passive components are matched with the experimentation conditions as it plays a major impact in determining the mode of operation. Initially, the steady-state performance of the model is tested for input voltages V_{in1} and V_{in2} of 30 and 60 V, respectively, and shoot-through duty cycle D_o of 0.25 to produce a desired value of 110-V rms ac output. It should be noted that the model can be operated at different input voltages and different duty cycles as well.

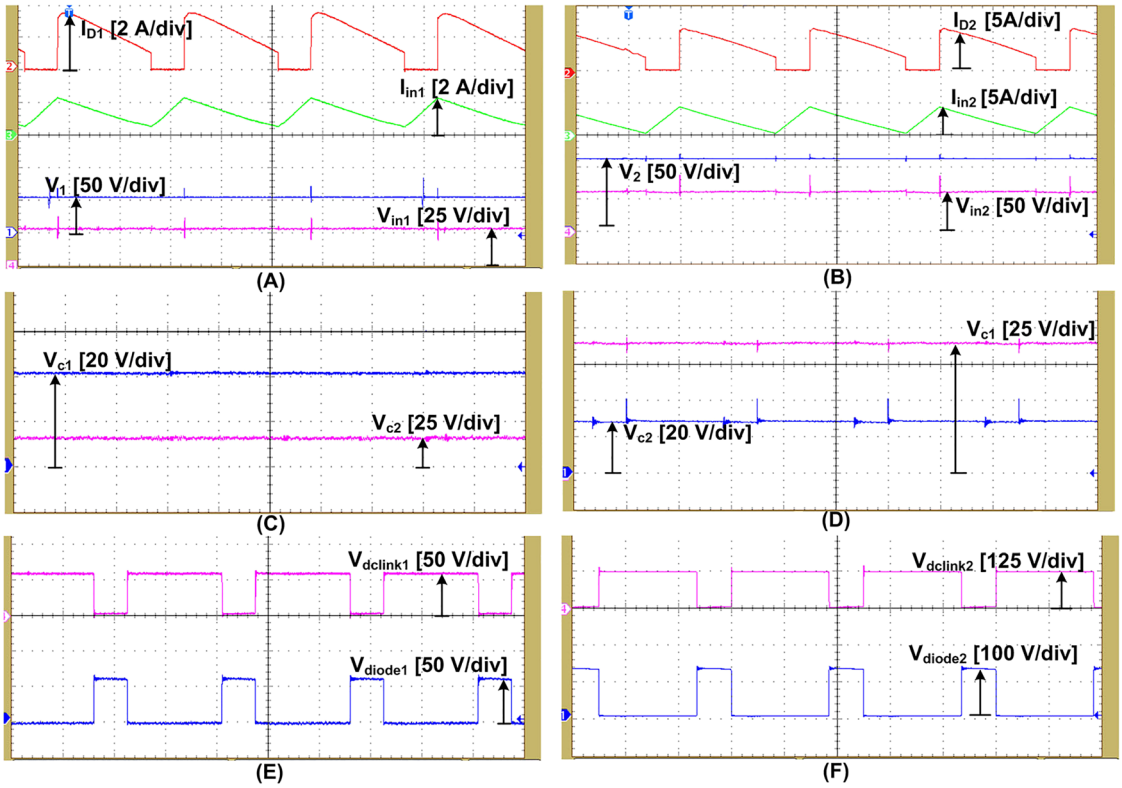

FIGURE 10 Experimental results in continuous conduction mode (CCM): input voltage, input current, diode current, and direct current (dc) bus voltage of (A) quasi-Z-source (qZs) network I and (B) qZs network II; capacitor voltages (C) qZs network I and (D) qZs network II; and dc-link voltage and diode voltage of (E) qZs network I and (F) qZs network II [Colour figure can be viewed at wileyonlinelibrary.com]

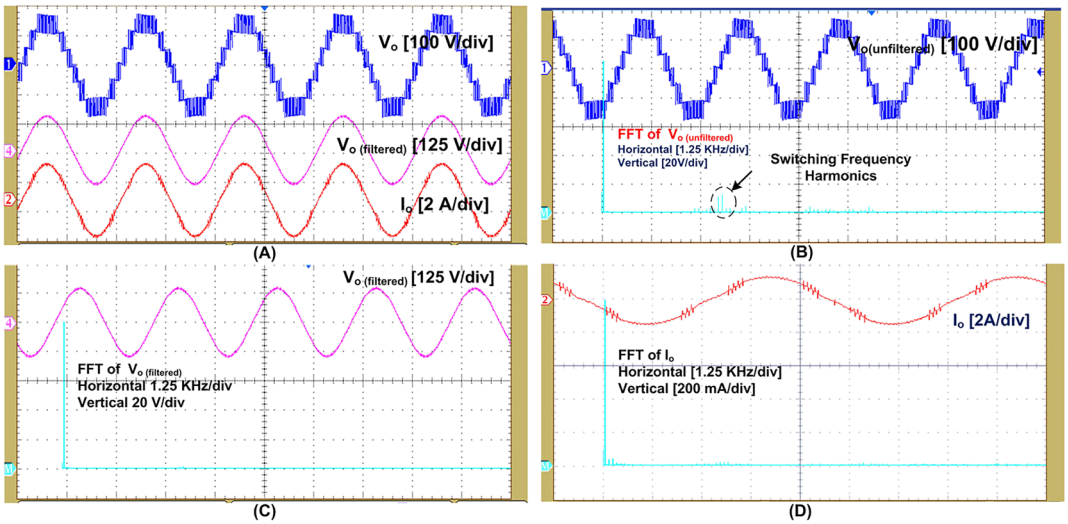

FIGURE 11 Experimental results in continuous conduction mode (CCM). (A) Output voltage V_o, V_o (filtered), output current I_o. Harmonic spectrum of (B) inverter output voltage and (C) filtered output voltage, (D) output current [Colour figure can be viewed at wileyonlinelibrary.com]

Spartan-6 FPGA processor is used to generate the control pulses based on MATLAB Xilinx system generator blocks. The power circuit is constructed using IRF640N MOSFET, Schottky diode MBR20200CT for qZs network I and II, and IGBT module with CT60-AZ for seven-level inverter. The driver circuit uses TLP250 optocoupler, which drives the switches and provides isolation from the power circuit. Two regulated dc sources are used as input voltage sources for testing the model, and Tektronix DPO 3034 is used to capture the experimental results. In order to demonstrate the CCM and DCM operation, the model is tested under two different loading conditions, while keeping the other parameters such as switching frequency and inductance value unchanged. The proposed model is capable of supplying both dc and ac loads. However, the model is tested only in the presence of ac load to simplify the analysis.

5.1 | Continuous conduction mode

In order to verify the CCM operation, the topology is tested for a load of 60 Ω (less than the critical resistance). The typical waveforms of the input voltage, input current, diode current, and dc bus voltage for qZs networks I and II are shown in Figure 8A,B. The input current and the diode current waveforms of both the networks validate the CCM operation. It can be observed that the input current increases linearly during the shoot-through state and decreases during the active state. The dc bus voltages V_1 and V_2 are maintained constant due to the presence of C filter. The capacitor voltages, dc-link voltage, and diode voltages of qZs networks I and II are shown in Figure 8C,D. The capacitor voltages are boosted to around 45 and 15 V, respectively, in qZs network I, while the capacitor voltages are boosted to around 90

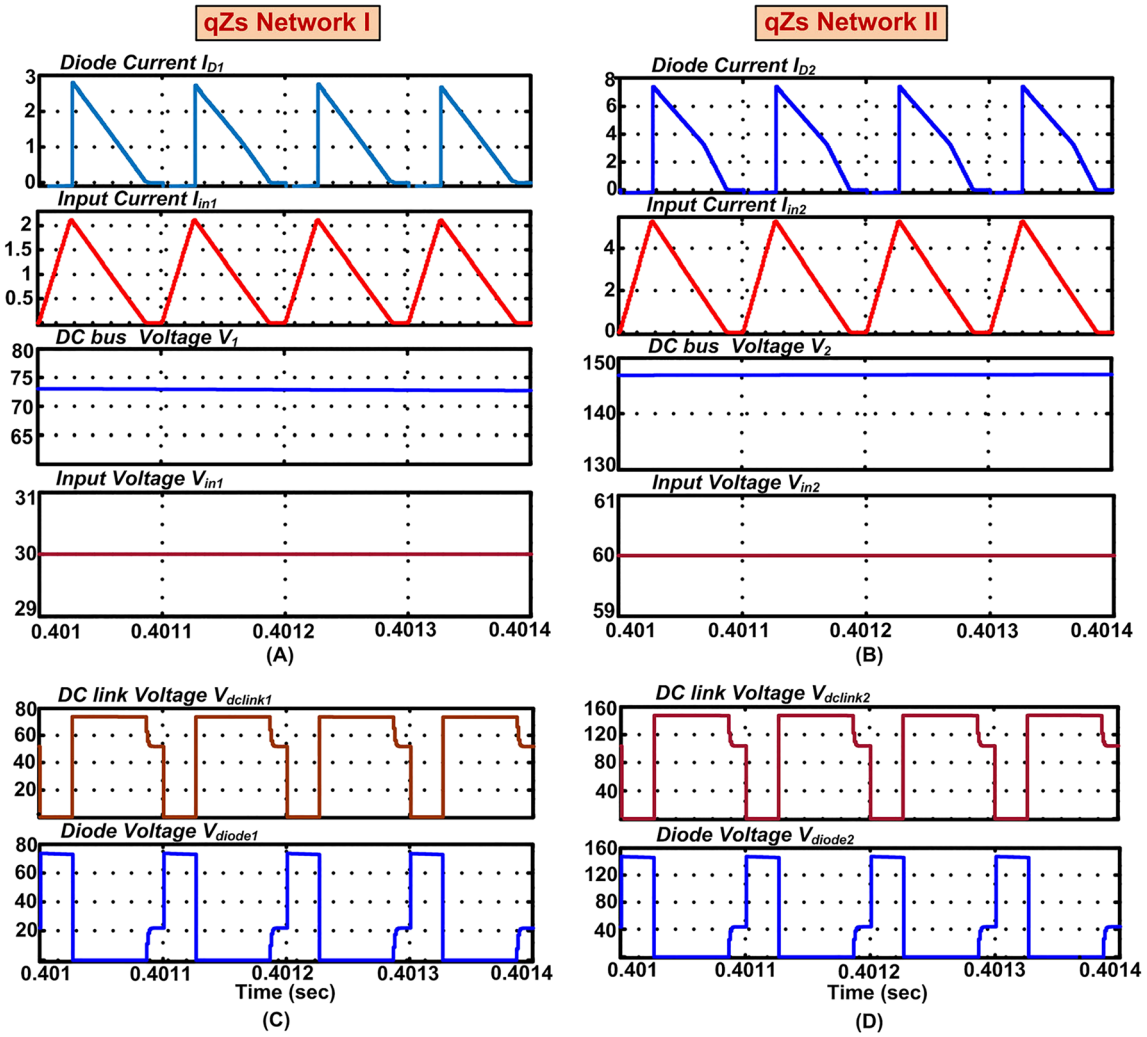

FIGURE 12 Simulation results in discontinuous conduction mode (DCM) input voltage, input current, diode current, and direct current (dc) bus voltage of (A) quasi-Z-source (qZs) network I and (B) qZs network II and dc-link voltage and diode voltage of (C) qZs network I and (D) qZs network II [Colour figure can be viewed at wileyonlinelibrary.com]

and 30 V, respectively, in qZs network II. It can be noticed that the dc-link voltage and diode voltage are pulsating in nature.

Figure 9A depicts that the response of seven-level inverter output voltages, load current, and their respective harmonic spectrums is shown in Figure 9B. It can be noticed that the presence of dominant harmonics at the higher frequency reduces the size of the filter. The THD of the seven-level inverter output voltage is around 24%, which gets reduced to around 2% by the use of LC filter. Table 4 represents the amplitude of harmonics of seven-level inverter output voltage for different modulation indices of 0.9 and 0.8.

Figures 10A-F and 11A-D depict the corresponding experimental results of the model under the same conditions. It is evident that the experimental results are in compliance with the simulation results. However, a slight deviation in values is credited to the parasitic resistance associated with the conducting wires and various components in the model.

5.2 | Discontinuous conduction mode

Further, the model is demonstrated for discontinuous mode of operation with a load of 120 Ω (greater than critical resistance). Figure 12A,B illustrates that the qZs converters I and II completely operate in DCM, which is evident from the diode and input currents waveforms. The dc-link voltages and diode voltages of both the qZs networks I and II are shown in Figure 12C,D, which shows the reduction in dc-link voltage during T_2 state. Figure 13A-E shows the corresponding experimental results, and it can be clearly observed that the dc-link voltage is increased in DCM. It can be seen that the output voltage is elevated when compared with CCM. The over-boost effect can be observed with increased loading conditions. The output voltage is elevated, and the levels are asymmetric in nature, which is attributed to DCM operation. It can be observed that all experimental and simulated waveforms are in close agreement with each other.

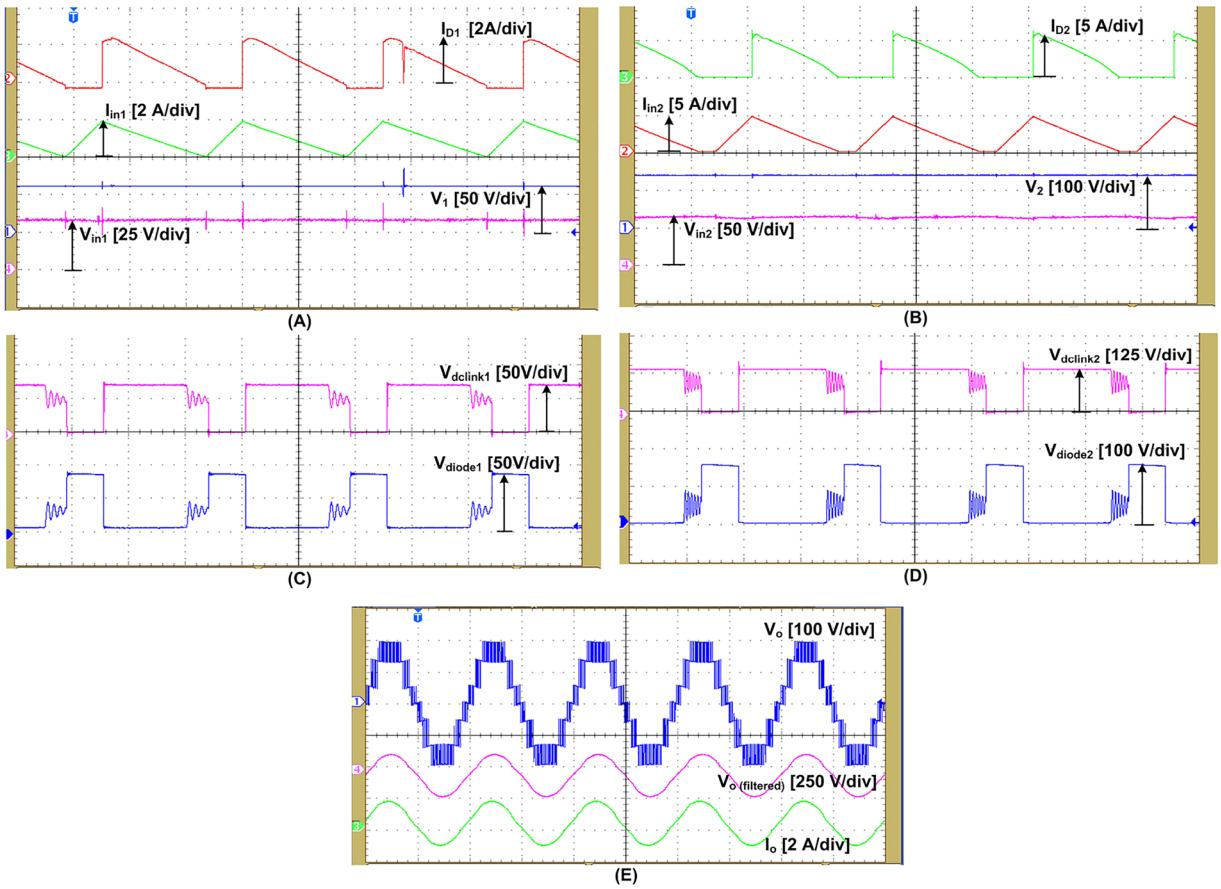

FIGURE 13 Experimental results in discontinuous conduction mode (DCM): input voltage, input current, diode current, and direct current (dc) bus voltage of (A) quasi-Z-source (qZs) network I and (B) qZs network II; dc-link voltage and diode voltage of (C) qZs network I and (D) qZs network II; (E) output voltage V_o, V_o (filtered), output current I_o [Colour figure can be viewed at wileyonlinelibrary.com]

5.3 | Dynamic response

Figure 14 depicts the closed-loop control block diagram of the proposed qZs-based seven-level inverter based on FPGA implementation. Two sensors are used to measure the dc bus voltages of both qZs networks, ie, V_1 and V_2, and the error signal is fed to the simple proportional-integral (PI) controllers to maintain the desired dc bus voltages by adjusting the shoot-through duty cycle. Here, the system is developed for voltage references of 60 and 120 V for both dc busses for an output of 110-V rms at the inverter output. A limiter is also used to ensure that the shoot-through period is within the design values of [0.1-0.3].

Here, the dynamic response of the dc bus voltage V_1 is first evaluated for an input voltage V_{in1} changes from 25 to 40 V and from 40 to 32 V, while keeping the other input voltage V_{in2} constant at 60 V. Similarly, the study is carried out for input voltage V_{in2} changes from 50 to 70 V and from 70 to 60 V, while keeping the other input voltage V_{in1} constant at 30 V. Figure 15A,B illustrates the response of dc bus voltages of qZs networks for input voltage changes. It is evident that the dc bus voltages V_1 and V_2 are maintained constant with wide variation in input voltage. Figure 15C,D shows the output voltage response when the load is changed from 120 to 60 Ω and from 60 to 120 Ω, respectively. The output voltage is well regulated despite the change in loading by 50% and operating between the two modes. This ensures the effectiveness of the model and achieves fast dynamic response within two switching cycles, which validates the performance of the controller.

5.4 | Efficiency calculation

The efficiency of the proposed circuit configuration is computed by considering various losses of the qZs converter. The overall loss comprises conduction and switching loss of the switch and losses due to passive components of diode, inductors, and capacitors of the qZs network, which is computed from the expressions given in Erickson and Maksimovic[29]

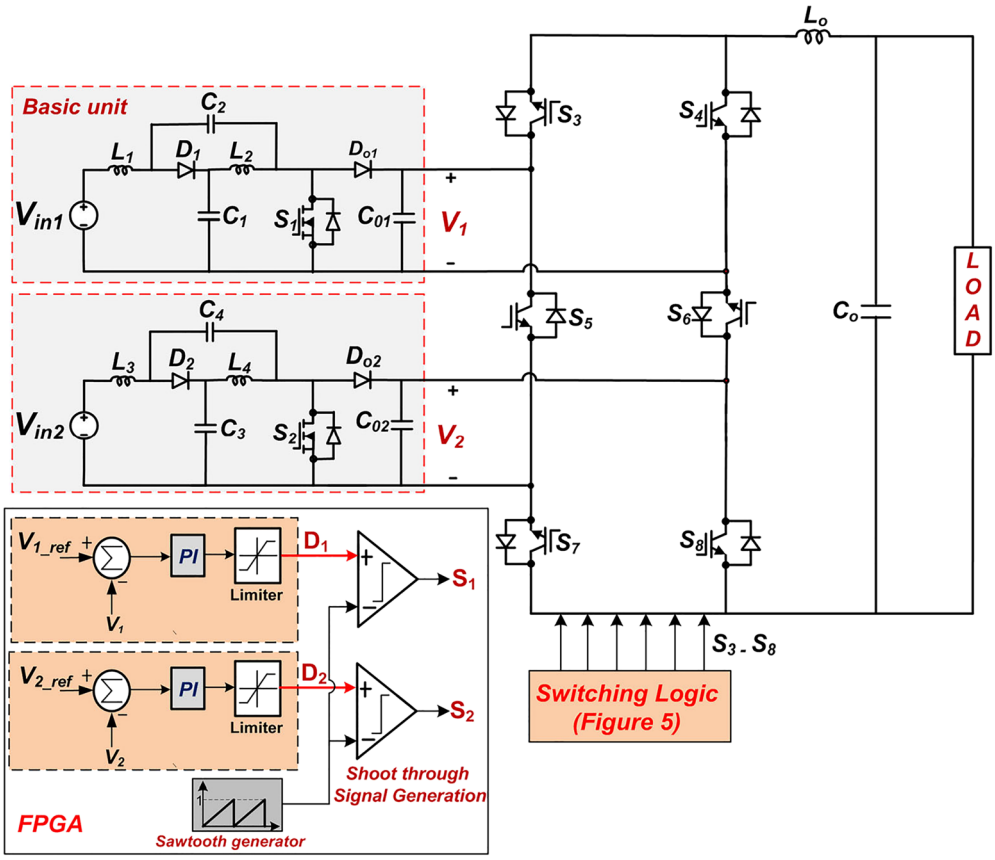

FIGURE 14 Closed-loop control block diagram of the proposed quasi-Z-source (qZs)–based seven-level inverter [Colour figure can be viewed at wileyonlinelibrary.com]

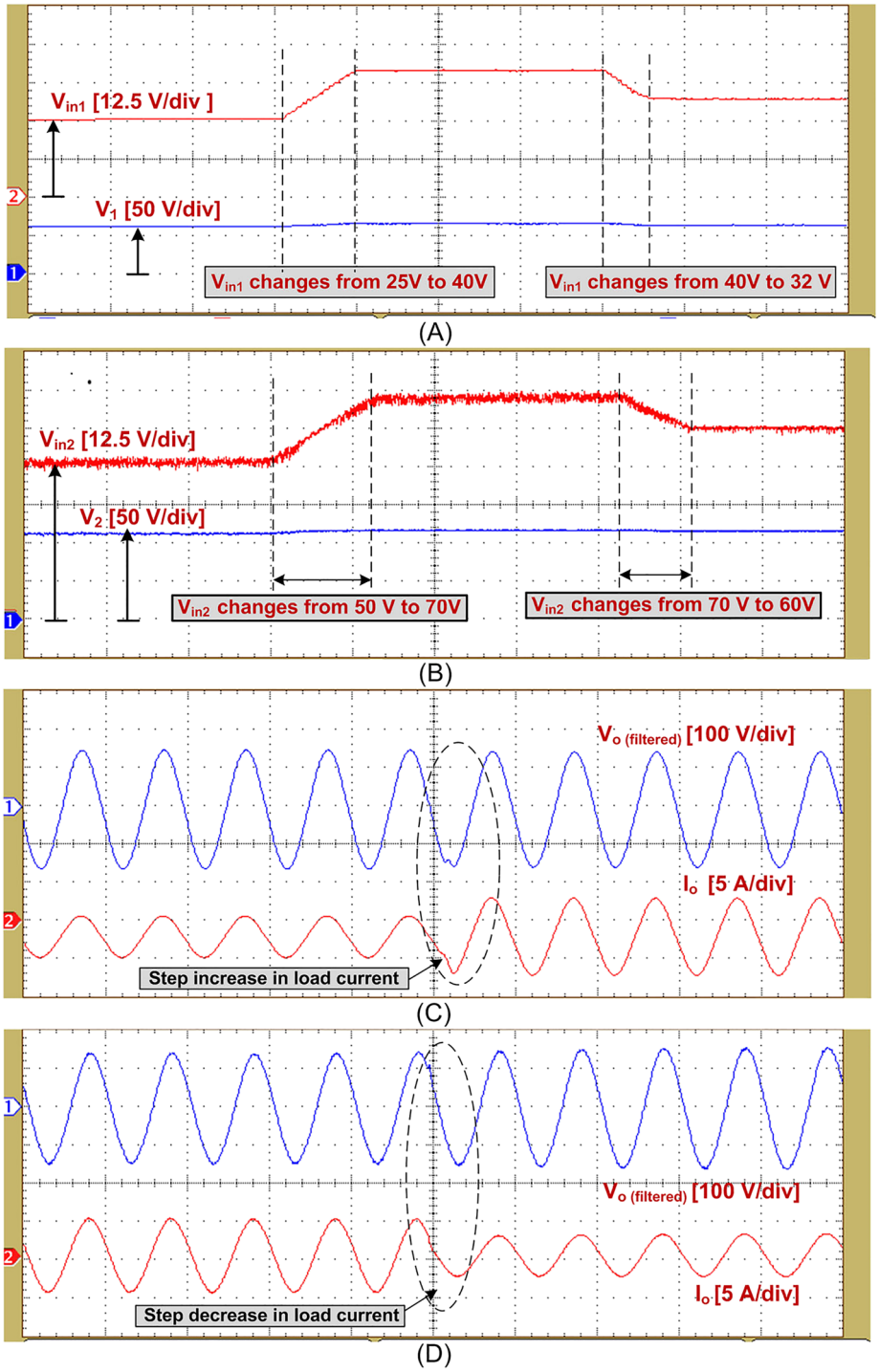

FIGURE 15 Experimental results for (A) changes in input voltage V_{in1}; (B) changes in input voltage V_{in2}; (C) step change in load from 120 to 60 Ω; and (D) step change in load from 60 to 120 Ω [Colour figure can be viewed at wileyonlinelibrary.com]

and Patidar and Umarikar.[30] The conduction loss and switching loss of the seven-level inverter are computed independently from expressions given in Ji and Wang.[31]

$$\text{Efficiency } (\%) = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \times 100\% \tag{31}$$

Figure 16A clearly illustrates the power loss distribution across various components for a total load of 200 W at 0.25 duty cycle. From the loss analysis, it can be noted that qZs diode accounts for most of the losses; hence, efficiency can be

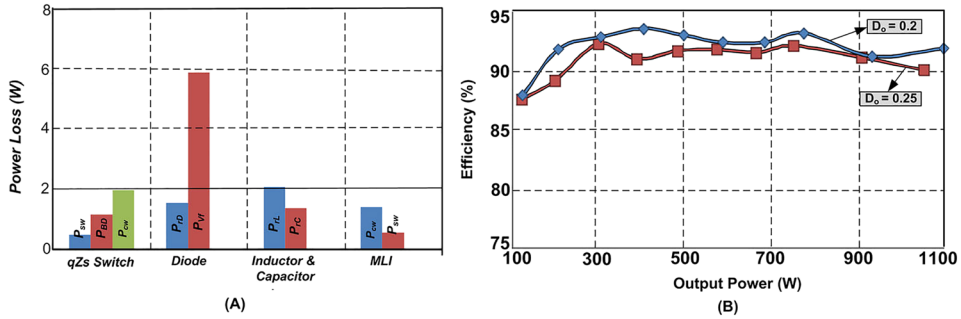

FIGURE 16 A, Power loss of various components. B, Efficiency curve [Colour figure can be viewed at wileyonlinelibrary.com]

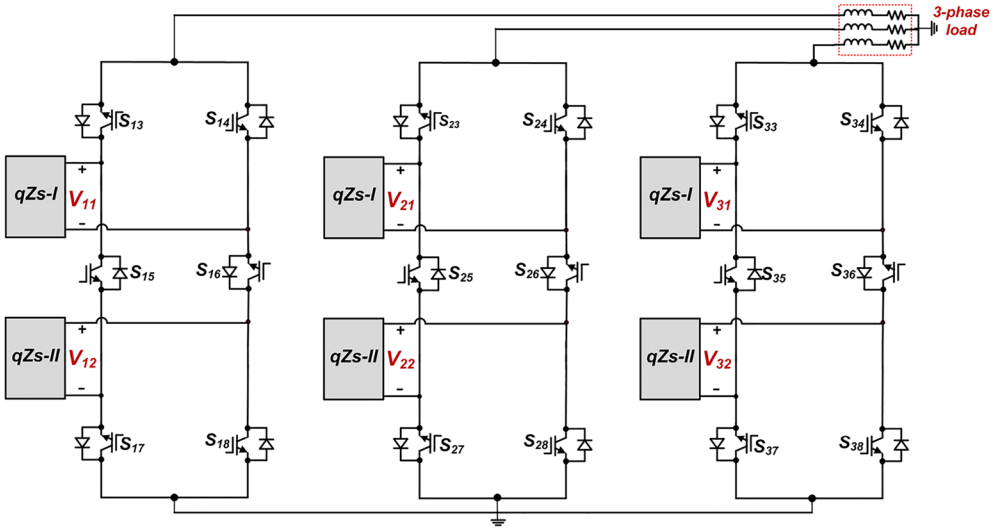

FIGURE 17 Three-phase derivative of the proposed inverter [Colour figure can be viewed at wileyonlinelibrary.com]

further improved by replacing qZs diode with semiconductor devices.[32] Figure 16B shows the measured efficiency curve using PSIM thermal module for two different shoot-through duty cycles of 0.2 and 0.25. It is evident that higher efficiency is obtained at lower shoot-through duty cycle. As shoot-through duty cycle increases, there will be increased current in the boost mode, which leads to increased losses and reduction in efficiency.

5.5 | Extension of the proposed inverter

In this paper, a qZs-based seven-level inverter is proposed for single-phase applications. However, it can also be extended to the medium power three-phase multistring PV applications by utilizing six qZs converters and three PUC configurations as shown in Figure 17.

6 | CONCLUSION

A new single-phase seven-level qZSI is proposed for multistring PV applications. The proposed topology offers significant features of reduced switches, fewer dc sources, shoot-through immunity, and better output quality of supply. The operating boundary conditions of proposed topology under CCM and DCM are evaluated for different loading conditions. The dynamic performance of the proposed configuration is verified with simple PI controllers during load changes as well as input voltage changes. A low-scale prototype model is developed, and their control schemes are

implemented using Xilinx FPGA blocks. Finally, it is noticed that both the simulation and experimental results show similar performance and validate the theoretical assumptions and calculations.

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