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RESEARCH ARTICLE

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A new configuration of seven-level quasi Z-source–based isolated inverter for renewable applications

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Summary

In this paper, a new configuration of seven-level quasi Z-source (qZs)–based isolated inverter is introduced in the family of Z-source–based multilevel inverters (MLIs). The proposed topology is an upgrade of qZs inverter and asymmetrical seven-level inverter with significant advantages of high boost gain, reduced device count, and higher efficiency. In addition, the front-end qZs converter provides wide input voltage regulation for eco-friendly photovoltaic (PV) as well as fuel cell–based standalone/grid-connected applications. The use of high-frequency transformer blocks the leakage current from PV panels to the local load/grid, and the seven-level inverter produces high quality sinusoidal output waveform, which reduces the filter size. Therefore, the working principle of the proposed configuration is tested in simulation, and an experimental verification is performed to validate the effectiveness of the model. A proportional-integral (PI) controller is designed in field-programmable gate array (FPGA) using Xilinx blocks, and the dynamic response of the model is evaluated for changes in input voltage and step changes in load. Moreover, a brief comparative assessment of proposed configuration with existing seven-level qZs-MLI is also presented.

KEYWORDS

isolated quasi-Z source inverter, multilevel inverter, pulse-width modulation, shoot-through

1 | INTRODUCTION

Recent advancements in Z-source–based converters have witnessed tremendous growth in terms of usage in potential applications such as eco-friendly photovoltaic (PV)/fuel cell–based generations to meet the increasing power demands, flexible alternating current transmission system (FACTS) devices, energy storage, and electric vehicles and wind energy conversion systems.[1] Z-source–based converters have emerged as a viable alternative among other converters because of the obvious advantages of wide output voltage regulation with inherent buck-boost capability. This improves the overall efficiency in single-stage conversion compared with the dc-dc converter–based two-stage conversion. The Z-source

List of symbols and abbreviations: B, boost factor; C_1, C_2, capacitances of the qZs network; CHB, cascaded H-bridge; D_0, shoot-through duty cycle; I_L, average inductor current; I_C, average capacitor current; L_1, L_2, inductances of the qZs network; M, modulation index; MLI, multilevel inverter; N_P, number of turns of transformer primary winding; N_{S1}, N_{S2}, number of turns of transformer secondary windings; PV, photovoltaic; PWM, pulse-width modulation; V_{DC}, dc-link voltage; V_{PV}, pv voltage; i_{PV}, pv current; TBV, total blocking voltage; T, switching period; qZSI, quasi z-source inverter; ZSI, z-source inverter

inverter (ZSI) alleviates the shortcomings of traditional voltage source and current source inverters by adding an impedance network comprising two inductors and two capacitors in the form of X-shape.[2] This introduction of impedance network eliminates the failure of inverter due to misgating in the absence of dead band between the switches in a leg, and thus reduces the waveform distortion. The output voltage is regulated by varying the duty cycle D_0 by allowing the switches of a phase or all the phases to turn on for the duration of switching cycle.

A review of different shoot-through control techniques is reported.[3] The conventional pulse-width modulation (PWM) techniques are slightly modified to incorporate the shoot-through in zero states without altering the active states to enable the desired output voltage. However, optimal placement of shoot-through state is mandatory, as it has prominence in assessing the input current ripple, number of commutations of the switches, switching loss minimization, and soft switching capability and efficiency.[4] In this context, an improved control scheme is investigated,[5] which reduces the overall switching commutations by switching at zero voltage (ZVS) features for simple control and higher efficiency. Both the legs are utilized for shoot-through operation, which reduce the current stress among the switches. However, the upper and bottom switches operate at different frequencies f_s and $2f_s$, respectively, which increase the losses. In this paper, this control technique is modified such that all the switches operate at equal switching frequency (f_s) to reduce the switching loss.

Quasi Z-source inverter[6] (qZSI) is becoming popular for renewable applications because of the advantages of continuous input current and reduced capacitor C_2 voltage stress and size compared with ZSIs. Recently, multilevel inverters (MLIs) have been extended for low-power applications as well because of the significant advantages of low dv/dt, low stress across the switches, better voltage and current profile, and reduction of filter size. The three popular topologies, namely, cascaded H-bridge (CHB), neutral-point clamped (NPC), and flying capacitor (FC), are widely used in industrial applications. Among these, CHB is most preferable because of its modularity feature and absence of clamping diodes and FC voltage balancing problems. A lot of research has been carried out in MLIs[7] to address the issues of switch count, reduction in capacitors, diodes, capacitor balancing, ease of control, and number of dc sources. Despite various advantages offered by MLIs, one of the major limitations is the limited output voltage gain. This necessitates a proper upgrade of MLIs with suitable power conditioners that provide better voltage regulation and output quality. Here, Z-source–based converter is chosen as the power conditioner to integrate with MLI.

Integration of impedance source network with MLI provides better solution in renewable applications where reliability is of major concern. Impedance-source–based multilevel converters have gained attention in recent years, as they offer voltage buck-boost capability, better input voltage utilization, and high gain, in addition to the features obtained from the MLI topologies. In this context, a single-phase three-level NPC converter[8] using two Z-source networks is presented, which requires two sources and two impedance networks, and the neutral point is commonly grounded. Further improvements have been made in this topology based on single-source, single Z-source network and extended to three-phase systems. This idea is further extended to multilevel diode clamped ZSI.[9-12] However, all these topologies suffer because of discontinuous current profile.

A single-phase NPC qZSI based on double qZs network topology is addressed[13] for three-level operation. Some topologies have been proposed based on NPC with coupled inductors impedance network[14] to address the issue of pure dc link in ZSI and qZSI. A three-level NPC inverter based on LC switching[15] is reported, in which the passive component count is reduced. A seven-level inverter-based Z-source network[16]is presented by a combination of Z-source with cascaded half-bridge MLI with reduced switches. A new qZs-based cascaded five-level inverter is derived[17] from the above topology by the addition of switched inductor cell in the qZs network with coupled inductors to improve the voltage gain. The qZSI-based CHB inverter[18] for PV applications is addressed for seven-level operation. However, this requires more number of isolated dc sources and passive component count. A five-level boost inverter using two quasi-switched boost networks[19] is presented with reduced passive component. A family of novel single-phase modified qZSI-based MLI[20] is introduced, which utilizes only one leg for shoot-through and the other leg for voltage inversion. It improves the harmonic spectrum when compared with traditional qZSI. A single-phase modified qZSI hybrid three-level inverter[21] is reported with higher voltage gain using two inductors. In turn, this basic unit is cascaded with another unit in combination with H-bridge to produce a five-level output. A comprehensive overview of some of the existing Z-source MLIs[22] is reported.

From the literature, it is evident that most of the Z-source–based MLI topologies are constructed from upgrading impedance source–based converter with NPC and CHB, which demands more component count for multilevel output realization. Also, integration of existing qZs-MLI to large-scale grid-connected PV systems is associated with large leakage current due to the absence of isolation and grounding. Therefore, this necessitates the high-frequency (HF) isolation between the input PV and the grid, which enables the reduction of leakage current, dc current injection into the grid, and the provision of grounding the PV panel to enhance the system reliability and safety. In this context, a front end isolated qZSI-CHB[23] is introduced. A transformer-based ZSI-CHB[24] is reported with single Z-source network

for seven-level output realization. However, these topologies are bulky and suitable for medium voltage applications. This motivates the authors to develop a qZs-MLI for low power applications.

Therefore, a new configuration of seven-level qZs-based isolated inverter[25] intended for renewable applications is presented. The working principle and control technique of the proposed configuration is presented in Section 2. Section 3 presents the detailed comparison of various qZs-based seven-level inverters. Section 4 describes the mathematical model of PV with maximum power point tracking (MPPT) and dc-link voltage balancing control. Further, Section 5 presents the simulation results in grid-connected and stand-alone mode. The experimental verification and power loss calculation are discussed in Section 6, and the conclusion is presented in Section 7.

2 | SYSTEM DESCRIPTION

Figure 1 shows the proposed seven-level qZs-based inverter with HF galvanic isolation for grid-connected PV applications. The major parts of the circuit consists of front-end qZSI, an HF transformer with multiple secondary windings, diode rectifier unit, and a six-switch seven-level inverter. The qZSI boosts the input voltage V_{PV} to attain the desired dc-link voltage by inserting proper shoot-through duty cycle D_O across the full bridge inverter. The HF transformer enables the necessary galvanic isolation between the input PV source and the grid and also provides second stage of boosting based on the turns ratio. A multi-winding transformer with turns ratio of 1:2 is considered and cascaded with diode rectifier units followed by capacitors to provide stable dc bus voltages V_1 and V_2. Further, it is interfaced with asymmetrical seven-level inverter to generate the desired output voltage of 230 V for renewable applications. The significant features of the proposed topology are as follows:

(1) The qZSI enables high boosting output voltage, continuous input current operation for PV panels with reduced ripple to the sources, and additional step-up operation of HF transformer.
(2) The use of HF transformer introduces extra control degree, which improves the system performance and also provides output voltage regulation.
(3) It is capable to accommodate wide variations in input voltage because of its intermittent nature and is well-suited for PV applications.
(4) Reduced parts count MLI is used for realizing seven-level output voltage, which reduces the overall system size and cost and provides higher efficiency.
(5) Galvanic isolation eliminates the problems associated with leakage current while interfacing PV array with the grid.

2.1 | Analysis of qZSI network with HF transformer

The qZs converter enables buck-boost operation based on the input voltage generated from the distributed energy sources by inserting the corresponding shoot-through duty cycle D_o. During D_oT, the inductor stores the energy, and the energy transfer from source to load is zero. During$(1 - D_o)T$, the energy is transferred from the source to load.[25] The capacitor voltages V_{c1} and V_{c2} are expressed as

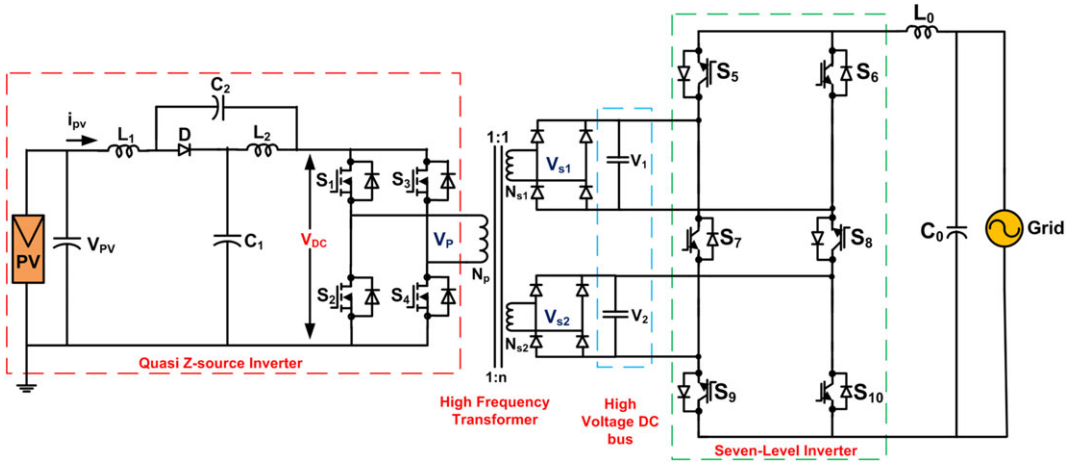

FIGURE 1 Seven-level quasi Z-source–based isolated inverter for grid-connected photovoltaic (PV) system

$$V_{c1} = \frac{(1 - D_o)V_{pv}}{1 - 2D_o}, \quad V_{c2} = \frac{D_o V_{pv}}{1 - 2D_o} \ . \tag{1}$$

Hence, the dc-link voltage can be expressed as

$$V_{dc} = V_{c1} + V_{c2} = B.V_{pv} = \frac{V_{pv}}{1 - 2D_o}. \tag{2}$$

The dc-voltage gain in the primary winding (N_P) of the transformer is

$$\frac{v_p}{V_{pv}} = \frac{1}{1 - 2D_o}. \tag{3}$$

The dc-voltage gain in the secondary windings N_{S1} and N_{S2} is

$$\frac{v_{S1}}{V_{pv}} = \frac{1}{1 - 2D_o}, \qquad \frac{v_{S2}}{V_{pv}} = \frac{n}{1 - 2D_o}, \tag{4}$$

where n is the number of secondary windings.
The dc bus voltages V_1 and V_2 can be represented as

$$V_1 = \frac{V_{pv}}{1 - 2D_o}, \qquad V_2 = \frac{n.V_{pv}}{1 - 2D_o}. \tag{5}$$

Finally, the output voltage V_O can be determined based on the duty cycle and turns ratio as

$$V_0(\text{rms}) = \frac{m_a.n.V_{pv}}{1 - 2D_0}. \tag{6}$$

2.2 | Shoot-through control technique

The control technique for the generation of control signals with shoot-through insertion is shown in Figure 2. Here, the saw tooth waveforms are shifted and utilized for the generation of PWM signals and shoot-through states. The saw tooth waveforms T and T_{50} are compared with a value M equal to modulation index to generate the control pulses for the top switches S_1 and S_3. The saw tooth waveforms T_{25} and T_{75} are compared with a control variable ST to generate the corresponding shoot-through, which are inserted alternatively at an instant through an OR gate to generate the control pulses for bottom switches. Thus, shoot-through is inserted in only one leg at an instant, thus reducing the switching loss. However, this improves the current stress among the switches during shoot-through state. This control technique can be utilized for low power applications where the current flowing through the switches is relatively low. All the switches are operated at switching frequency f_s equalizing switching losses, which improves the overall efficiency of the qZs inverter. The shoot-through states are distributed uniformly on either side of the active state, thus reducing the input current ripple. The switching cycle consists of six switching states, out of which the shoot-through states occurs twice. The switching scheme corresponding to each switching state is given in Table 1.

2.3 | Selection of passive components L and C

The inductance value is chosen so as to mitigate the oscillations in the input current due to low-frequency ripple during shoot-through state D_oT. During D_oT, the current increases linearly, and the voltage across the inductor is positive,

$$V_L = L \ \frac{\Delta i_L}{D_o T}. \tag{7}$$

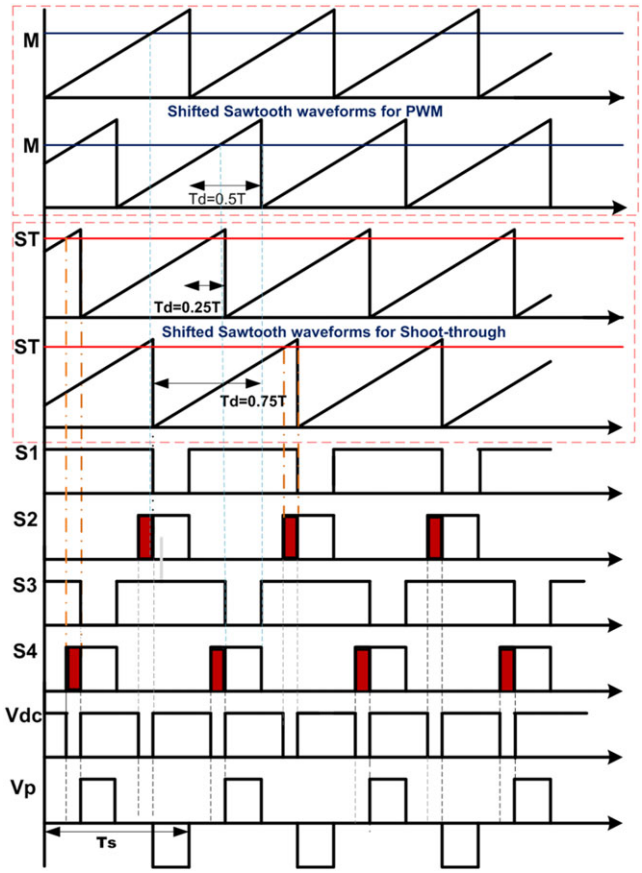

FIGURE 2 Pulse-width modulation (PWM) control technique

TABLE 1 Switching scheme

State	S_1	S_2	S_3	S_4	Output Voltage
Zero	1	0	1	0	0
ST	1	0	1	1	0
Active	1	0	0	1	$+V_{dc}$
Zero	1	0	1	0	0
ST	1	1	1	0	0
Active	0	1	1	0	$-V_{dc}$

Assuming the acceptable input current ripple to be $x_L\%$, which is defined as

$$x_L\% = \frac{\Delta i_L}{I_L} \times 100, \tag{8}$$

the inductance can be computed as

$$L_1 = L_2 = \frac{(V_{\text{in}} + V_{\text{c2}})D_{\text{o}}\text{T}}{x_L I_L}. \tag{9}$$

From (1) and considering x_L=20%, $D_o = 0.25$, $I_L = 10A$, $f_{\text{s}} = 10$ KHz, and $V_{\text{in}} = 60$ V, the computed inductance value is

$$L_1 = L_2 = \frac{V_{\text{in}}(1 - D_{\text{o}}).D_{\text{o}}}{x_L.I_L(1 - 2D_{\text{o}})f_{\text{s}}} \approx 1.125 \text{ mH} . \tag{10}$$

Hence, an inductance value of 1.2 mH is chosen for the study. Similarly, the value of the capacitance is selected so as to mitigate the oscillations due to the low-frequency voltage ripple and maintain constant dc-link voltage. During$(1 - D_{\text{o}})$ T, the capacitors C_1 and C_2 are in series, hence the current flowing through the capacitor during the non-shoot-through $(1 - D_{\text{o}})T$ can be expressed as

$$i_c = C\frac{\Delta V_c}{(1 - D_{\text{o}})T}. \tag{11}$$

The capacitance can be computed by

$$C_1 = C_2 = \frac{2.\ \frac{I_L.D_0}{1 - D_0} \times (1 - D_0)T_{\text{s}}}{\Delta(V_{c1} + V_{c2})}. \tag{12}$$

Assuming the acceptable voltage ripple to be x_C%, which is defined as

$$x_c\% = \frac{\Delta V_c}{V_c} \times 100. \tag{13}$$

From (2), (12), and (13), considering the boost factor $B = 2$, $I_L = 10$ A, $D_{\text{o}} = 0.25$, $V_{\text{in}} = 30$ V, $x_c = 0.01$, and $f_{\text{s}} = 10$ kHz.

The capacitance can be computed as

$$C_1 = C_2 = \frac{2.I_L.D_0}{B.x_c.V_{\text{in}}f_{\text{s}}} \approx 830\,\mu\text{F}. \tag{14}$$

Hence, a capacitance value of 1000 μF is selected for both C_1 and C_2 with different voltage ratings.

2.4 | Asymmetrical seven-level inverter

The asymmetrical seven-level inverter is based on the packed U-cells[26,27] configuration. It is superior compared with its equivalent CHB topology in terms of switch count and reduced average switching power loss. This topology is utilized for seven-level output realization. However, it requires switches of different voltage blocking capacity and isolated dc sources to be in arithmetic progression. The number of strings decides the input dc sources, which can be in binary or trinary form. Here, two-strings are considered to construct an asymmetrical MLI with binary arrangement of input sources V and 2 V and to synthesize the seven-level output. The stable dc bus voltages, V_1 and V_2, are generated from the diode rectifier units, which are fed to the seven-level inverter. The dc sources were connected in such a way as to synthesize all possible algebraic combinations of the input voltages. Figure 3A,B demonstrates the level-shifted PWM and corresponding switching scheme for the seven-level inverter operation.

3 | COMPARISON OF PROPOSED WITH EXISTING QZS-MLI TOPOLOGIES

Table 2 shows the comparison in terms of number of active and passive components required for the proposed topology with existing seven-level CHB-qZSI, seven-level cascaded qZSI, and seven-level transformer-based qZSI. It can be noticed that the proposed inverter demands less number of dc sources, passive components, and switching devices when compared with other topologies. The inductor frequency remains the same for all the topologies. Also, the proposed topology demands only one HF transformer as compared with the transformer-based qZSI, which reduces the overall size and cost of system. The limitations of the proposed topology are the requirement of additional diodes with use of rectifier circuit. However, proper selection of rectifier integrated circuits (ICs) with low forward voltage drop leads to reduced losses with better rectification. The galvanic isolation incorporated in the proposed inverter further enhances the reliability, especially in PV-based applications. Table 3 shows the voltage stress across switches and total blocking voltage (TBV) of the proposed inverter with other topologies. Here, the voltage stress is similar for switches S_1 to S_6

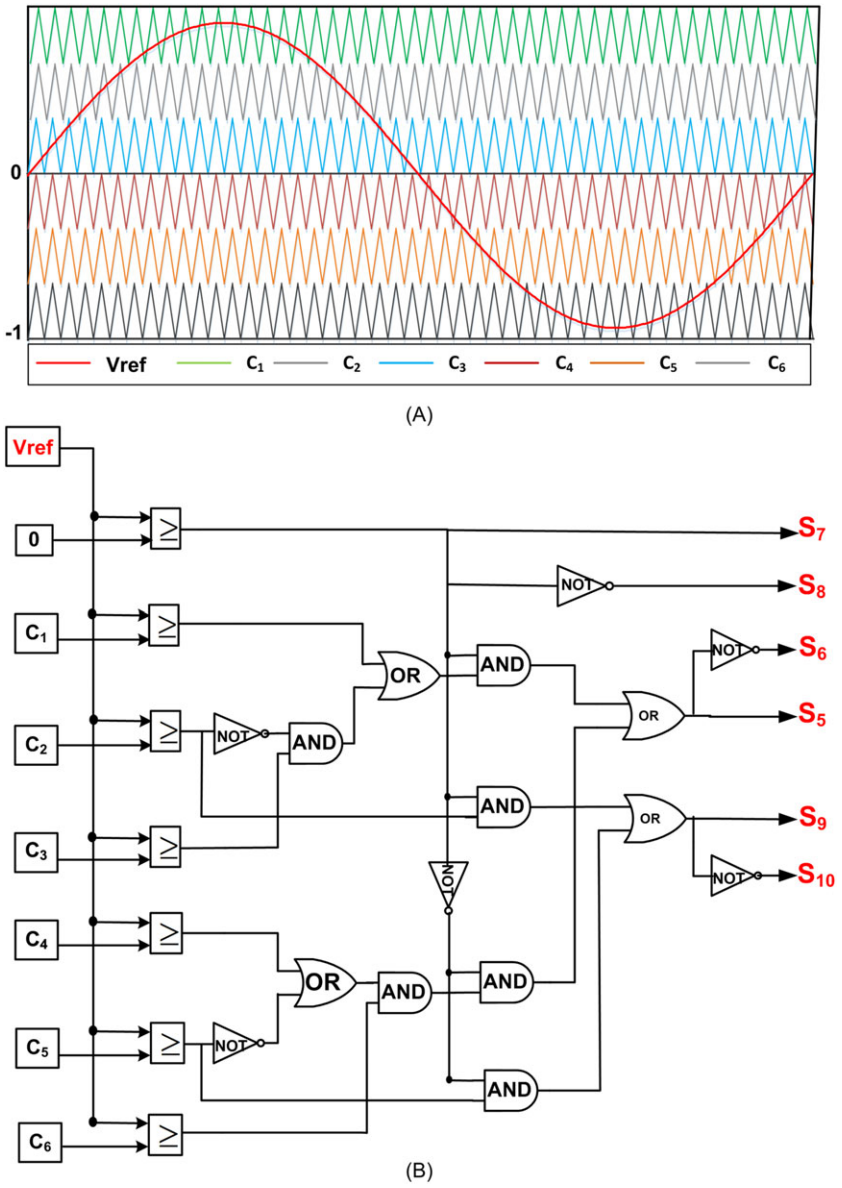

FIGURE 3 A, Level shifted sine pulse-width modulation (PWM) and B, switching schemes for seven-level inverter

TABLE 2 Comparison of proposed with existing seven-level qZSI-MLI

Components	Proposed Inverter	CHB-qZSI[23]	Cascaded qZSI[21]	Transformer-Based qZSI[24]
DC sources	1	3	3	1
Inductors	2	6	6	2
Capacitors	4	6	6	2
Diodes	9	3	3	1
Switches	10	12	10	12
HF transformers	1	-	-	3
Inductor frequency	$2f_s$	$2f_s$	$2f_s$	$2f_s$
Galvanic isolation	Yes	No	No	Yes

Abbreviations: CHB, cascaded H-bridge; HF, high frequency; MLI, multilevel inverter; qZSI, quasi Z-source inverter.

for all the topologies. Particularly, the switches S_7 to S_{10} has higher voltage stress compared with CHB-qZSI. However, it leads to more number of semiconductor devices. Moreover, the number of levels can be increased by using multiple secondary windings with slight increase in switching devices as compared with other qZSI-MLIs.

TABLE 3 Voltage stress across all switches

Item	Topology	Voltage Stress												TBV
Switches		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
Voltage stress	CHB-qZSI[18]	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$12V_{dc}$
	Cascaded-qZSI[16]	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	$3V_{dc}$	---	---	$18V_{dc}$
	Transformer-based qZSI[24]	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$12V_{dc}$
	Proposed inverter	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	$3V_{dc}$	$3V_{dc}$	$2V_{dc}$	$2V_{dc}$	---	---	$16V_{dc}$

Abbreviations: CHB, cascaded H-bridge; qZSI, quasi Z-source inverter; TBV, total blocking voltage.

4 | MATHEMATICAL MODELING OF PV AND ITS CONTROL

4.1 | Modeling of PV array

The characteristics of the PV cell is built using the following expression given in Sun et al.[18] In order to obtain increased voltage and power level, the modules are constructed in series as well as parallel combinations.

$$I_{pv} = N_p I_p - I_s\left(\exp\left[\left(\frac{q}{nKT_o}\right)\left(\frac{V}{N_s}\right)\right] - 1\right) - \frac{V}{R_{sh}}, \tag{15}$$

where V_{pv} and I_{pv} are the voltage and current, respectively, obtained from the PV string, N_p and N_s are the series and parallel number of cells connected, respectively, n is the diode ideality factor, K is Boltzmann constant, q is the electron charge, I_s is the reverse saturation current, and R_{sh} is the shunt resistance of the cell.

Here, the PV module is constructed based on the commercially available Solarex MSX-60 PV module.[28] The simulated family of I-V and P-V characteristics curves of the PV string under different irradiance levels modeled in MATLAB environment is shown in Figure 4. The model parameters given in the datasheet are listed in Table 4. It

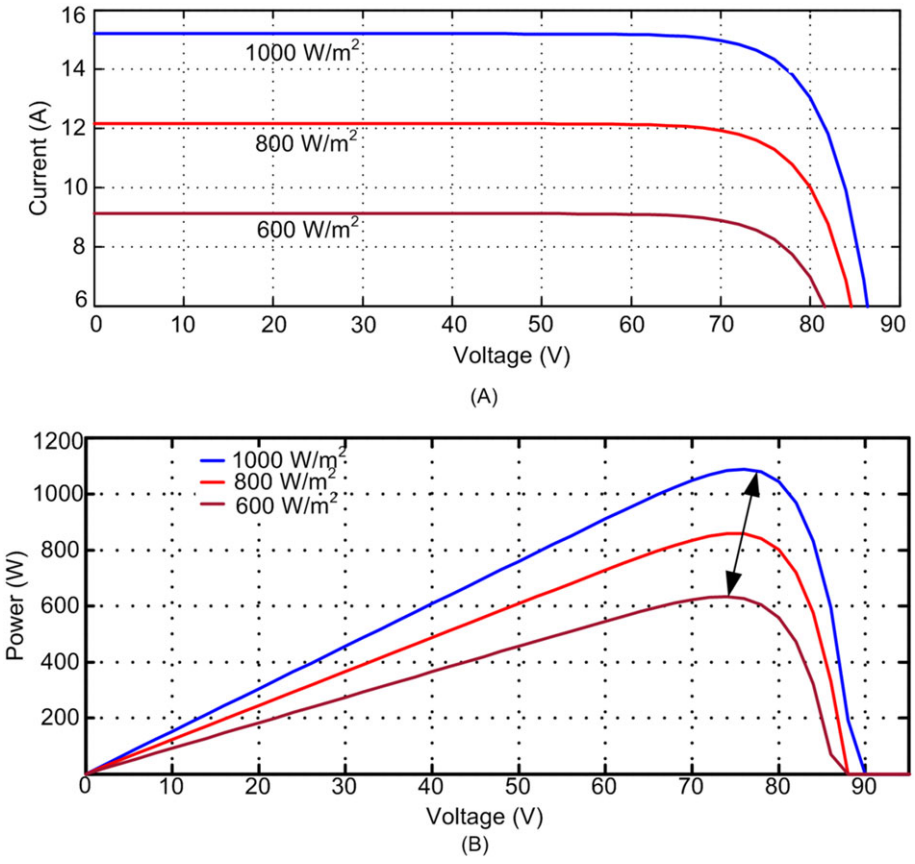

FIGURE 4 Family of I-V and P-V characteristics of solarex MX-60

TABLE 4 Parameters of the photovoltaic array model

Parameters	Values
Open circuit voltage, V_{oc}	21.1 V
Short-circuit current, I_{sc}	3.8 A
Voltage at maximum power, V_{mp}	17.1 V
Current at maximum power, I_{mp}	3.5 A
Number of panels connected in series, N_s	4
Number of panels connected in series, N_P	4
Maximum power of the panel P_{max}	60

can be observed that an increase in irradiance results in a corresponding change in power output. Moreover, the development of a suitable controller plays an important role in maximum power extraction from the PV.

4.2 | PV voltage control with MPPT

Figure 5 shows the block diagram of the PV voltage control with MPPT. The PV voltage V_{pv} and PV current I_{pv} are the inputs to the MPPT block. Various MPPT algorithms are available for the generation of reference voltage signal V^*_{pv}. However, the Perturb and observe algorithm (P&O) is adopted because of its simplicity and better tracking capability.[29] A simple proportional-integral (PI) controller is used to track the reference signal V^*_{pv} and the shoot-through duty cycle D_o generation to extract the maximum power for changes in irradiation and temperature. A limiter and gain K is provided to ensure the range of D_o within the limits of [0.1-0.3]. The control variable ST is utilized by the switching scheme to generate the control signals for qZSI.

4.3 | DC-link voltage and output current control

The scheme implemented for the control of dc-link voltage and output current is shown in Figure 6. The reference dc-link voltage V^*_{dc} is set at its desired value, and the dc-link voltage error is utilized by the PI controller to determine

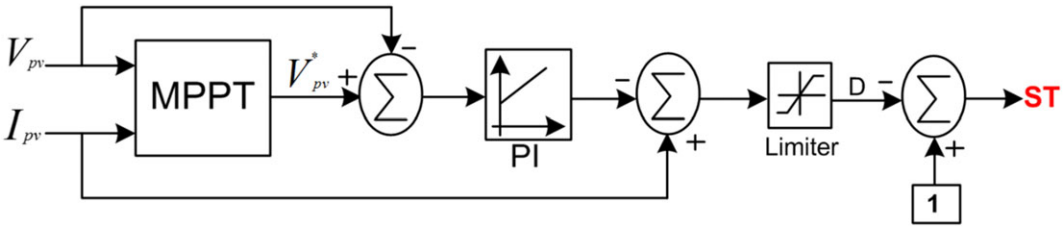

FIGURE 5 Photovoltaic (PV) voltage control with maximum power point tracking (MPPT)

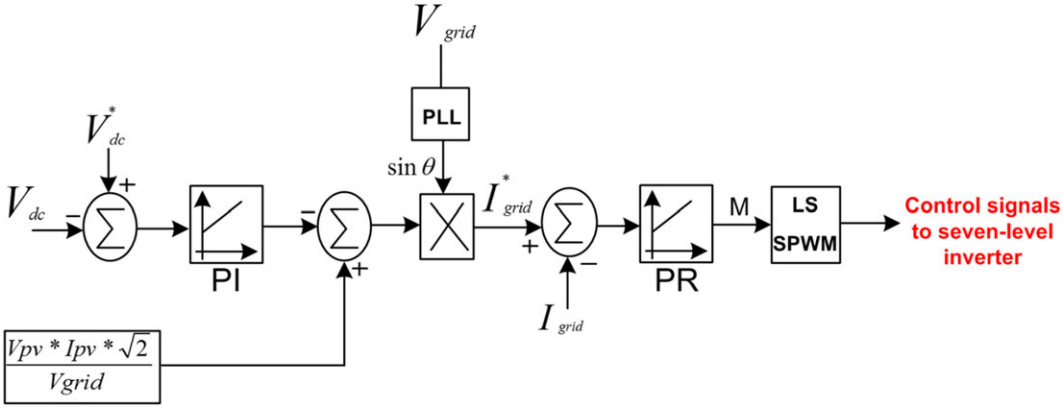

FIGURE 6 DC-link voltage and output current control

the reference grid current I^*_{grid}.[30] The phase-locked loop (PLL) generates the output frequency of the grid; the current error, which is fed to the PR controller, generates the modulating signal and improves the dynamic steady-state performance. This modulating signal is utilized by the level shift sinusoidal pulse-width modulation (LS-SPWM) to generate the control signals for the seven-level inverter.

5 | SIMULATION RESULTS

Initially, the model is tested in MATLAB environment in order to verify the performance of the proposed grid-connected qZs-MLI topology. Table 5 shows the detailed specifications of various components selected for both simulation and experimentation. This will enable easy validation of the proposed topology and dynamic response of the shoot-through control. Moreover, the on-state resistances of the switches, diode's forward drop voltage, and the internal parasitic resistances of passive components such as inductors and capacitors are also considered for the simulation study.

Figure 7A depicts the simulation waveforms of input voltage, input current, and dc-link voltage. Similarly, the measured voltage across the capacitors V_{c1} and V_{c2} of the qZs network and the dc bus voltages V_1 and $V_2$are shown in Figure 7B. It is noticed that the capacitor voltage V_{c1} is boosted to a value of 56 V and V_{c2} to a value of 8 V under steady state. The dc bus voltages V_1 and V_2 are equal to 63 V and 126 V, respectively, under steady state, with low-frequency ripple amplitude of 1 V. These values are slightly reduced because of the nonidealities of the components being considered. Figure 7C illustrates the response of seven-level output voltage, filtered output voltage, and output current waveforms. Figure 7D shows the measured harmonic spectrum of the seven-level output voltage, filtered output voltage, and the output current waveforms. It can be observed that the dominating harmonics occur around the switching frequency of 3 kHz, which reduces the size of the filter. The seven-level inverter output voltage total harmonic distortion (THD) is around 24%, while the %THD of filtered output voltage and output current waveforms are only 0.85% and well within the limits of IEEE standards.

Moreover, the dynamic performance of the proposed topology is evaluated in grid-connected mode with PV and simple P&O MPPT algorithm under varying irradiances in MATLAB environment. The Solarex MSX-60 PV module is considered for the study. Figure 8 illustrates the simulated response of various measured parameters of PV modules along with the *ST* duty cycle for changes in irradiance. Initially, the irradiation is maintained at 1000 W/m^2, the module voltage is maintained constant at 76 V, and the PV system power is around 1050 W, as shown in Figure 8.

The irradiation is decreased in step to 800 W/m^2 at 0.3 second, which leads to significant reduction in PV module current and PV module power. However, the MPPT block regulates the shoot-through duty cycle in order to extract the maximum power. The PV voltage decreases slightly during the transient state and retains voltage at maximum power V_{mp} value under steady state. The power under steady state is about 800 W at 0.5 second; the irradiation is increased in step to its initial level. It can be observed that the MPPT along with PI controller regulates the shoot-through duty cycle accordingly, and all the parameters retain its original values. Figure 9 shows the seven-level inverter output voltage, the grid voltage, and grid current during the variation in irradiation at 0.3 second. It can be observed that the output voltage is maintained constant despite the variations in grid current.

TABLE 5 Simulation and experimentation parameters

Parameters	Values
Output voltage, V_{out}	230 Vrms
Inductors (L_1,L_2)	1.2 mH
Capacitors (C_1,C_2)	1000 μF
Filter inductor L_f,capacitor C_f	4 mH, 25 μF/230 V
Switching frequency of qZs network, f_s	10 kHz
Switching frequency of MLI	3 kHz
Fundamental frequency	50 Hz

Abbreviations: MLI, multilevel inverter; qZs, quasi Z-source.

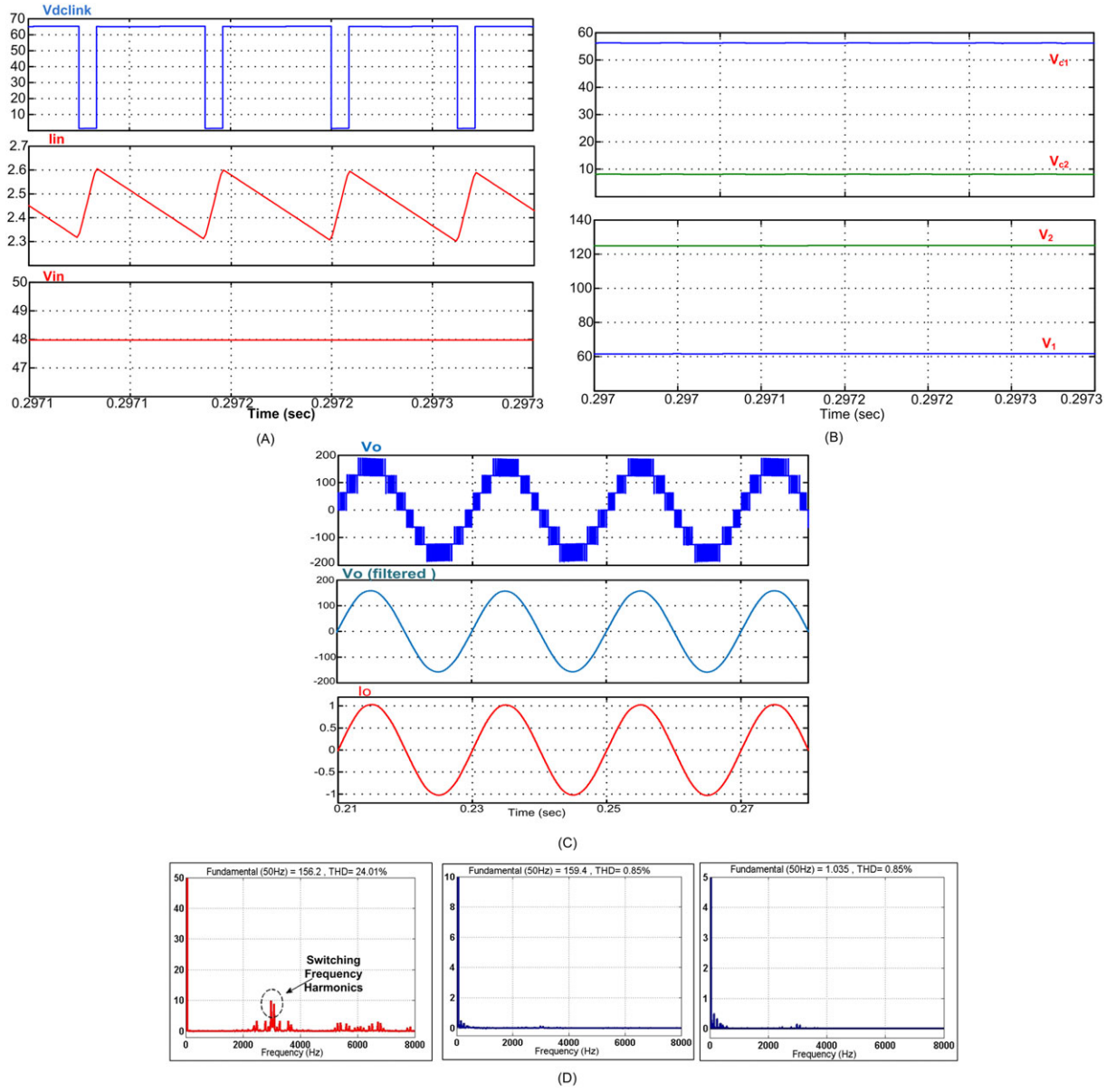

FIGURE 7 Simulation results: A, input voltage, input current, dc-link voltage; B, capacitor voltages and dc bus voltages; C, seven-level inverter output voltage, filtered output voltage, and current; D, harmonic spectrum of output voltage, output voltage (filtered), and output current

6 | EXPERIMENTAL VERIFICATION

A prototype model is built as proof-of-concept to demonstrate the working principle of the topology. Figure 10 depicts the developed experimental prototype setup in the laboratory, and the selected parameters are given in Table 5. The power circuit of qZSI is built using IRF640N MOSFETs, and the readily available insulated-gate bipolar transistor (IGBT) module with CT60AM-18F is used for realization of MLI. The values of inductances L_1 and L_2 are selected as 1.3 mH, and capacitances C_1 and $C_2$are 1000 μF. The switching frequency is taken as 10 kHz for the qZSI network, while the switching frequency of the seven-level inverter is considered as 3 kHz. One Schottky diode MBR20200CT and two diode rectifiers KBJ1510 are also used. The values of filter inductance and capacitance are 4 mH and 25 μF/230 V. An Atlys Spartan 6 LX45 FPGA processor is used for the generation of control pulses. The control pulses are generated using MATLAB Xilinx system generator blocks. Further, TLP250 optocoupler driver ICs are preferred to step-up the field-programmable gate array (FPGA) output control pulses and also to isolate the driver from power circuits. The input voltage V_{in} is varied from 40 V to 60 V, while the output voltage V_o is maintained constant at 110 Vrms. The experimental results are captured using Tektronix DPO 3034 with the help of differential voltage probe TMDP0200 and current probe TCP 0030.

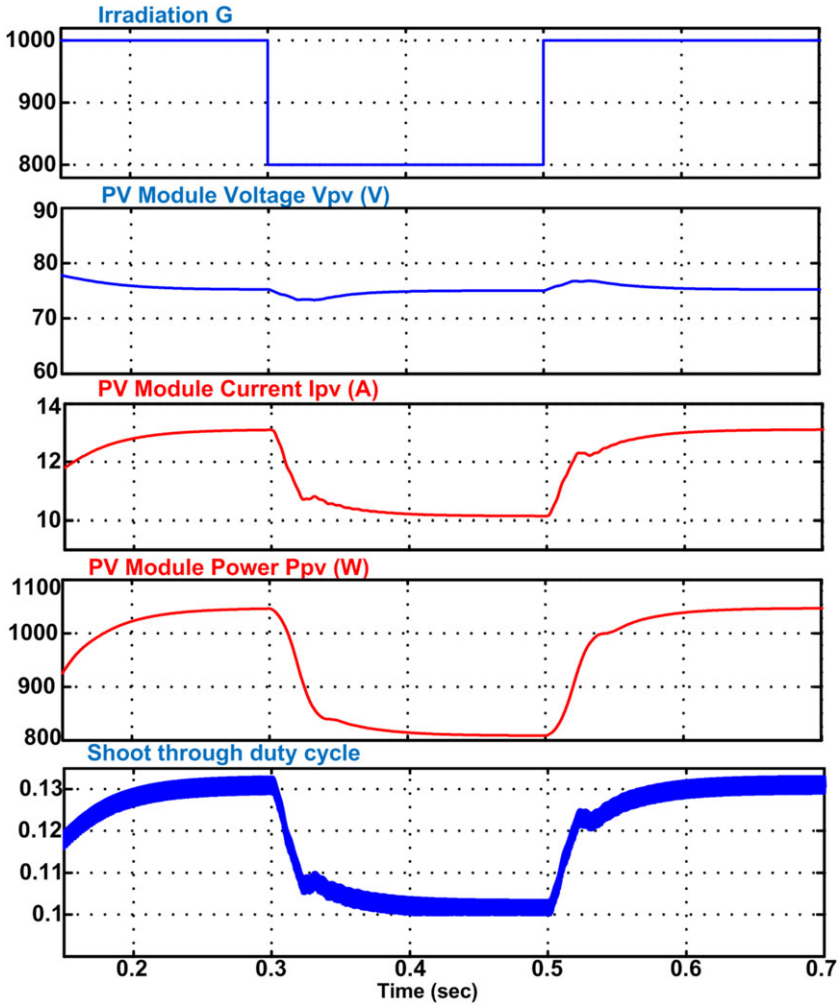

FIGURE 8 System dynamic response, irradiance, photovoltaic (PV) module average voltage, PV module average current, PV module average power, and shoot-through duty cycle

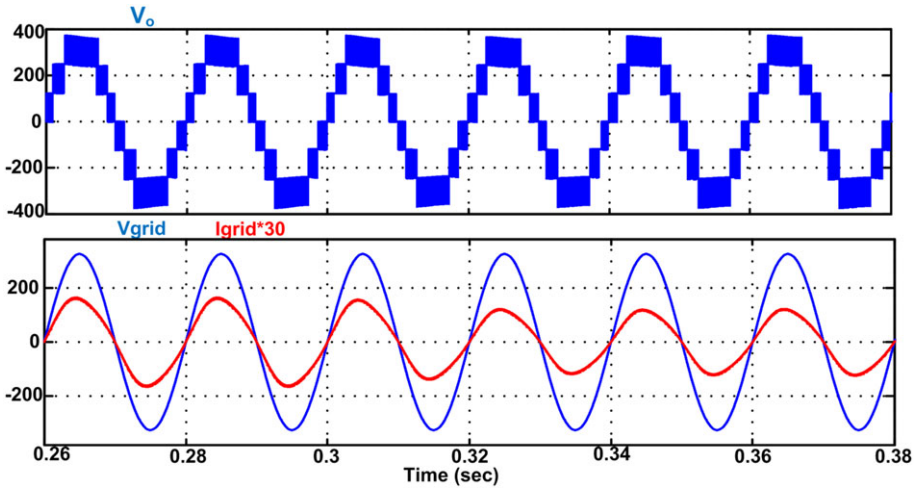

FIGURE 9 Simulation results of inverter output voltage, grid voltage, and grid current

6.1 | Open loop response

Initially, the open loop response of the experimental setup is tested for an input voltage of 48 V, shoot-through duty cycle of 0.13, and for a load of 150 Ω. Figure 11A shows the voltage and current stresses of the top switch S_3 and the bottom switch S_4, respectively, to demonstrate the soft switching capability. It is evident that S_3 switches on at zero voltage, and S_4 switches off at zero current, thus incorporating the feature of ZVS turn on and ZCS turn off.

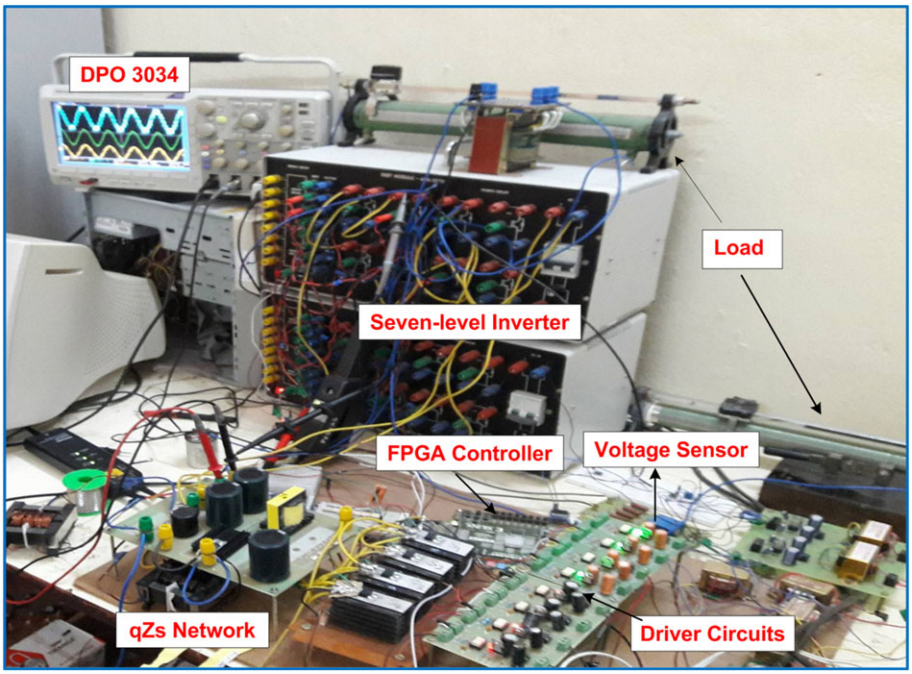

FIGURE 10 Experimental setup of the proposed model

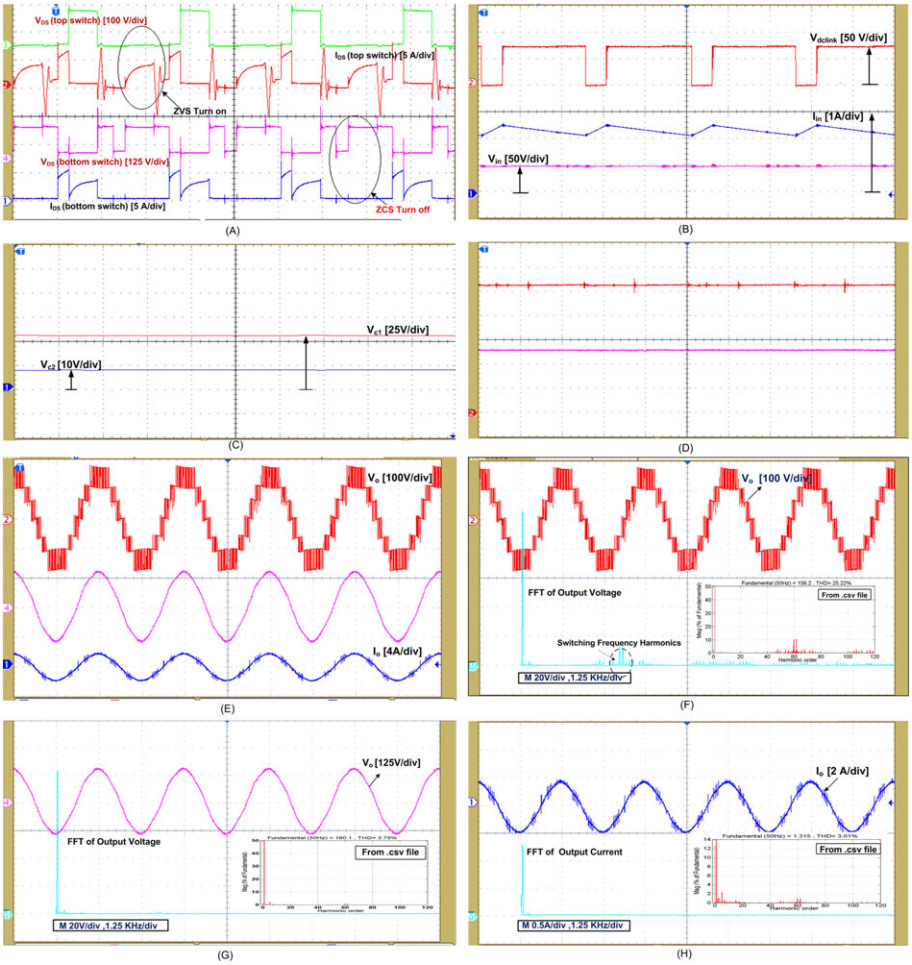

FIGURE 11 Experimental results: A, voltage and current stress of top and bottom switches; B, input voltage, input current, and dc link voltage ; C, capacitor voltages; D, dc bus voltages; E, seven-level inverter output voltage, filtered output voltage, and current; experimental fast Fourier transform (FFT) spectrum of F, seven-level output voltage ; G, filtered output voltage; H, output current

Figure 11B illustrates the input voltage V_{in}, input current I_{in},and dc link voltage V_{dclink}. The dc-link voltage is pulsating in nature. It can be seen that during the shoot-through period, the input current increases linearly, which stores the energy in the inductors. The energy gets transferred to the load in the non-shoot-through period; hence, the input current decreases linearly. Figure 11C shows the measured voltages of 15 V and 63 V across the capacitors C_1 and C_2 of the qZSI, respectively. Figure 11D shows the stable dc bus voltages of 63 V and 126 V, which are fed to the MLI. Figure 11E shows the output voltage V_o before and after LC filter along with the filtered output current I_o. The measured output voltage is 110 Vrms.

The quality of the waveform can be evaluated from the THD present in it. The experimental fast Fourier transform (FFT) spectra and THD of the seven-level Inverter output voltage, filtered output voltage, and output current are extracted from the MATLAB computation of .csv file and are added to the respective FFT spectrum obtained from DPO 3034 as shown in Figures 11F-H. It can be observed that the introduction of LC filter effectively eliminates the dominating harmonics around the switching frequency and reduces the %THD in the output voltage from 25.22% to 3.78%, and the load current is also around 3%, within the IEEE-519 limits.

6.2 | Dynamic response

A simple PI controller is realized in FPGA using Xilinx system generator blocks to control the peak dc-link voltage. The measurement of peak dc-link voltage requires two individual voltage sensors for computing V_{c1} & V_{c2}. However, from the model, it can be observed that the peak dc-link voltage is equal to dc bus voltage V_1. Therefore, the dc bus voltage V_1 is selected as the control parameter, which needs to be controlled, as it requires only one voltage sensor. Further, the voltage signal is scaled down to required level and fed into the FPGA through PMOD AD1 for analog to digital conversion. The reference value of the peak dc bus voltage V_{1ref} is set equal to 125 V in order to obtain 110 Vrms ac output. The error is computed and then fed to the PI controller, which produces the output control variable D_o as follows:

$$D_o = \left(K_p + \frac{K_i}{s}\right)(V_{1ref} - V_1). \tag{16}$$

The PI controller regulates the shoot-through duty cycle by reducing the dc bus voltage error $(V_{1ref} - V_1)$. A limiter is provided to ensure the shoot-through duty cycle range within [0.1-0.25], whereas the modulation index is fixed at 0.75. Further, the control variable ST is regulated accordingly for intermittent variations in input voltage and load. The logic implemented for the generation of control pulses using Spartan-6 FPGA is shown in Figure 12.

In order to test the dynamic performance of the model, the system is tested in two different conditions, ie, (a) changes in input voltage and (b) step change in load. Figure 13A shows the response of qZs network during changes in input voltage from 40 to 60 V and from 60 to 48 V for a constant loading condition. It can be noticed that the dc link voltage is maintained constant throughout the operation during input voltage changes. Further, the model is tested for step increase in load by 40% and also for 55% decrease in load, and their corresponding experimental results are given in

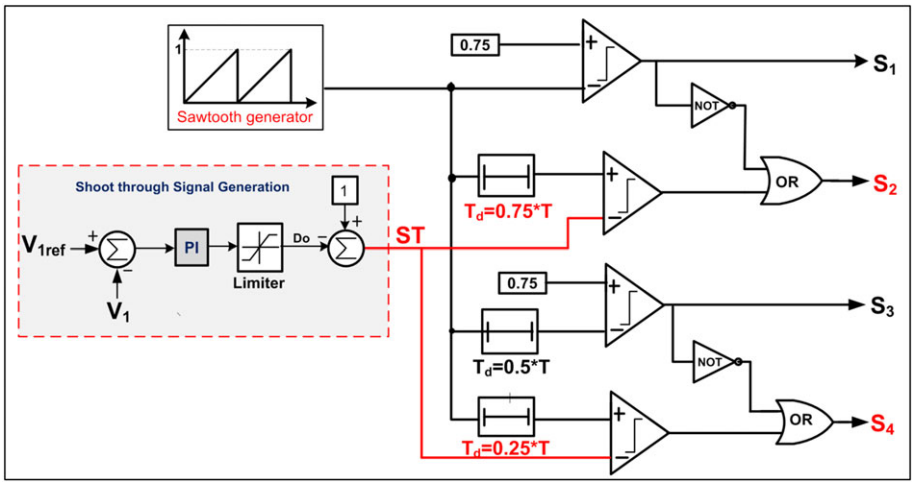

FIGURE 12 Generation of control pulses using field-programmable gate array (FPGA)

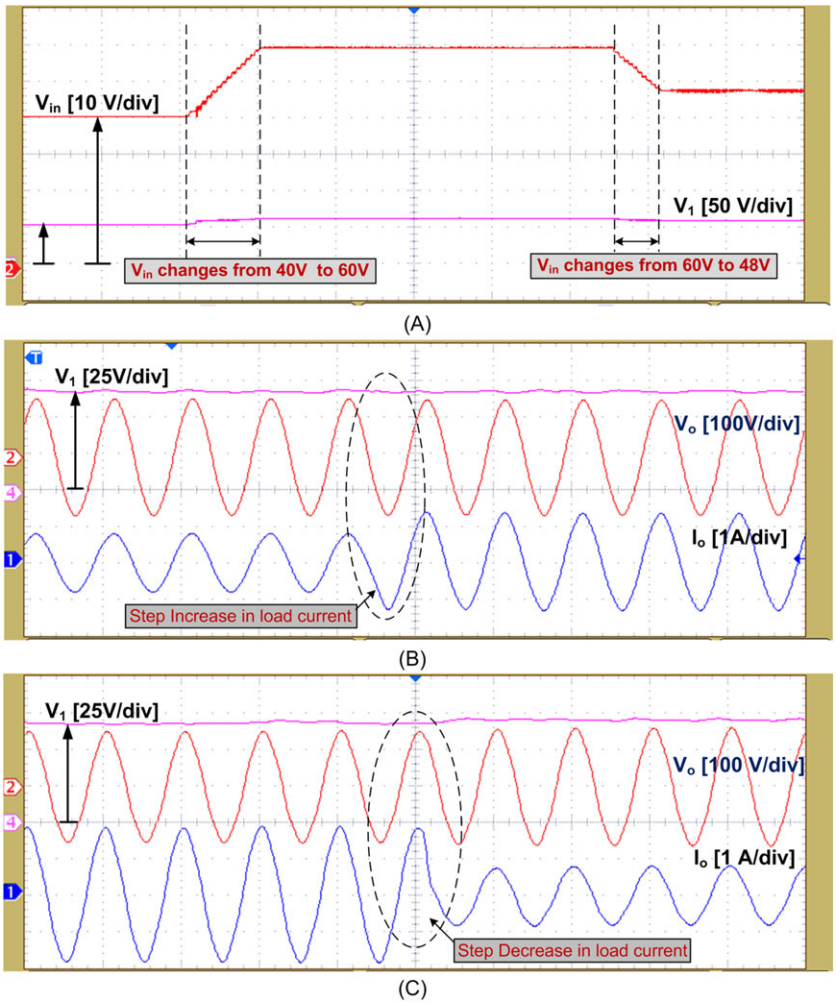

FIGURE 13 Experimental results: A, change in input voltages; B, increase in load current by 40%; and C, decrease in load current by 55%

Figures 13B,C, respectively. In both the cases, the filtered output voltage and dc bus voltage V_1 are maintained almost constant for step changes in load. It is clearly evident that the model exhibits fast dynamic response, within one cycle of operation for wide variation in input voltage as well as load, which validates the effectiveness of the controller.

Furthermore, the developed topology is tested for an increased output voltage of 230 Vrms for step changes in input voltage and changes and loading conditions. Figure 14A illustrates the measured inverter output voltage, filtered output voltage, and output current for an input voltage of 70 V. Figure 14B shows response of dc bus voltage V_1 for changes in input voltages from 80 to 95 V and from 95 to 85 V at different intervals under constant loading conditions. Similarly, Figure 14C shows the response for different loading conditions. It can be noticed that the output voltage remains unchanged for changes in input voltage and/or loads. This shows the effectiveness of the developed system and its suitability to accommodate intermittent power changes in PV systems and fuel cell applications.

6.3 | Power loss, efficiency, and %THD

It can be noticed that the developed model is tested for which the qZSI and HF shares equal amount of boosting gain apart from the galvanic isolation. The gain of qZSI can be enhanced by increasing the shoot-through duty cycle. However, to achieve better efficiency of the proposed topology, the D_o is limited to 0.25, otherwise it leads to more switching losses. Also, the selection of devices is important to estimate the actual efficiency of the system. Therefore, the following devices are considered for the calculation of efficiency: IRFP4668PbF MOSFET switches, IGB50N60T IGBT switches, MBR30300CT Schottky diodes, and KBJ1510 rectifier diodes. Figure 15A illustrates the efficiency curve of the proposed configuration calculated for 1 kW output power. The efficiency is estimated analytically to be around 94% for an output power of 1 kW.

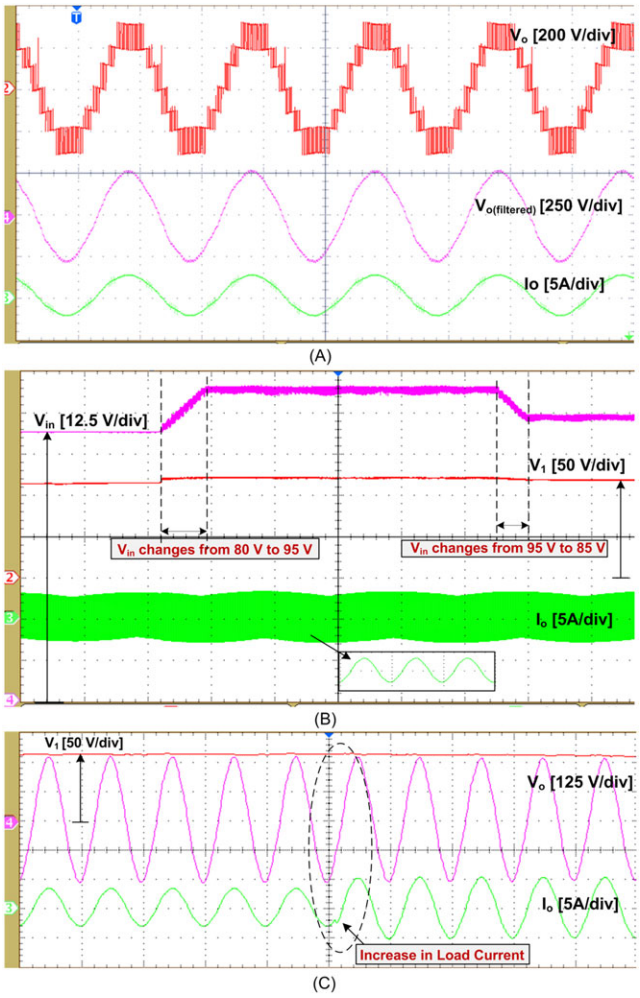

FIGURE 14 Experimental results: A, seven-level inverter output voltage, filtered output voltage, and current; B, for changes in input voltage; and C, for step change in load

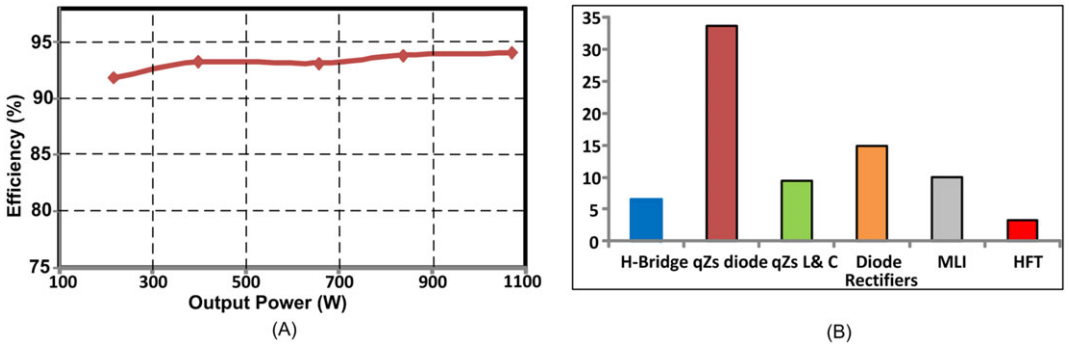

FIGURE 15 A, Efficiency curve; B, power loss distribution at 1 kW output

Furthermore, Figure 15B illustrates the power loss distribution among various components of the system at an output power of 1 kW. The percentage power loss incurred by various components is given in Figure 16B. The loss incurred in inductors, capacitors of qZs network, and dc bus capacitors due to the parasitic resistance is calculated based on the expression given.[31] The conduction and switching losses of the seven-level inverter is computed.[32,33] Also the core loss and winding loss of HFT is calculated.[34] It can be observed that major loss of around 44% occurs in qZs network. So, the overall efficiency of the proposed topology can be improved further by replacing the diode with an active switch in qZs network.

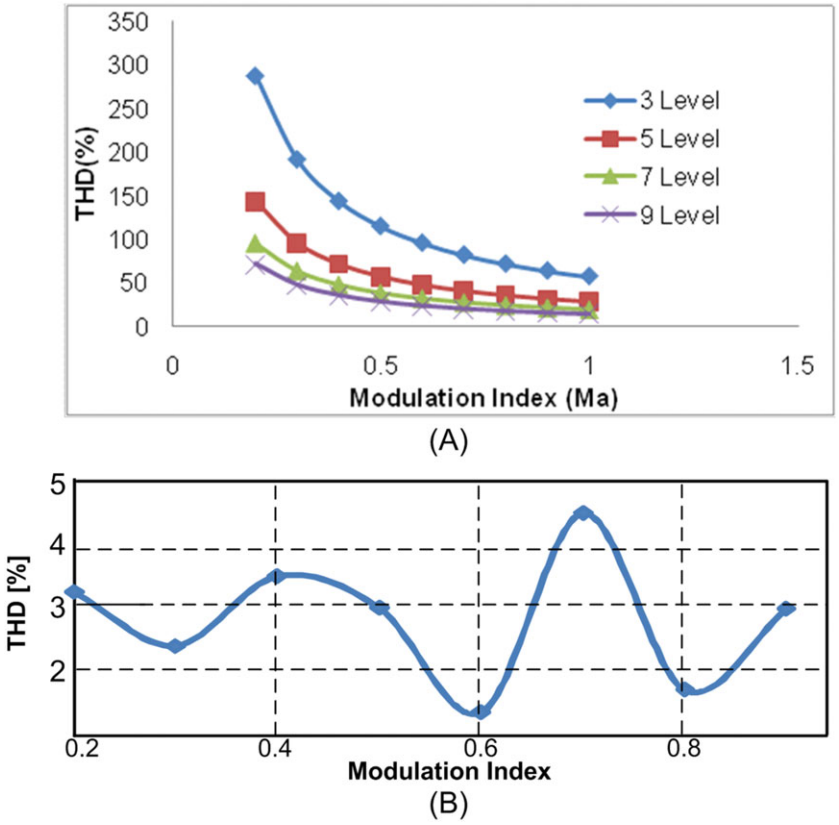

FIGURE 16 Total harmonic distortion (THD) of A, inverter output voltage and B, filtered output voltage

Figure 16A illustrates the measured THD of inverter output for different values of modulation index, Ma = 0.2, 0.4, 0.6, 0.8, and 1, and for various level generations. It can be noticed that higher levels in the output leads to lower %THD, which result to reduction in size of the filter components. Figure 16B shows that the %THD of filtered output voltage is within the 5% limits of IEEE 519 standards.

7 | CONCLUSION

A new seven-level qZs-based isolated inverter is presented, suitable for PV and fuel cell–based distribution generations. This topology provides better input voltage regulation, high efficiency, and high quality sinusoidal output voltage and output current with low filter size. The performance of the model is compared with existing qZs-based MLI topologies in terms of component count and voltage stress. A prototype model is developed and tested for different conditions of input voltage variations and step changes in load. The simulation and experimental results confirm and validate the effective performance of the model.

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REFERENCES

1. Moghadasi N, Esmaeli A, Soleymani S, Mozafari B. Quasi-Z-source matrix converters to be used in PMSG-based WECS: modeling, control and comparison. *Int Trans Elect Energ Syst*. 2018;28(6):e2544.

2. Peng FZ. Z-source inverters. Wiley Encyclopedia of Electrical and Electronics Engineering 2017,:1-11.
3. Siwakoti YP, Peng FZ, Blaabjerg F, Loh PC, Town GE. Impedance source network for electric power conversion—Part II:review of control. *IEEE Trans Power Electron*. 2015;30(4):1887-1907.
4. Wang S-C, Liu Y-H, Cheng Y-S, Peng B-R. A novel modulation technique with interleaved-and-shifted shoot-through state placement for quasi-Z-source inverters. *Int J Ccirc Theor Appl*. 2018;46(2):343-363.
5. Siwakoti YP, Town G. Improved modulation technique for voltage fed quasi-Z-source DC/DC converter. In Proc APECE, 2014,:1973-1978.
6. Anderson J, Peng FZ. Four Quasi-Z-Source Inverters. *Proc. IEEE PESC,* 2008: 2743-2749.
7. Ge B, Abu-Rub H, Malinowski M, Al-Haddad K. Multilevel converter/inverter topologies and applications. In: *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*. Wiley; 2014.
8. Loh PC, Gao F, Blaabjerg F, Feng SYC, Soon NJ. Pulsewidth-modulated Z-source neutral-point-clamped inverter. *IEEE Trans Ind Appl*. 2007;43(5):1295-1308.
9. Loh PC, Lim SW, Gao F, Blaabjerg F. Three-level Z-source inverters using a single LC impedance network. *IEEE Trans Power Electron*. 2007;22(2):706-711.
10. Gao F, Loh PC, Blaabjerg F, Teodorescu R. Modulation schemes of multi-phase three level Z-source inverters. Proc IEEE PESC, 2007,:1905-1911.
11. Strzelecki R, Adamowicz M, Wojciechowski D. Buck-boost inverters with symmetrical passive four-terminal networks. *Proc*CPE, 2007,: 1-9.
12. Li T, Cheng Q. Structure analysis and sliding mode control of new dual quasi-Z-source inverter in microgrid. *Int Trans Electr Energ Syst*. 2018;e2662.
13. Husev O, Roncero-Clemente C, Romero-Cadaval E, Vinnikov D, Stepenko S. Single phase three-level neutral-point-clamped quasi-Z source inverter. *IET Power Electron*. 2015;8:1-10.
14. Mo W, Loh PC, Blaabjerg F, Wang P. Trans-Z-source and neutral-point-clamped inverters. *IET Power Electron*. 2015;8(4):1-7.
15. Manoranjan S, Sivakumar K. A three level LC-switching based voltage boost NPC inverter. *IEEE Trans Ind Electron*. 2017;64:2876-2883.
16. Banaei MR, Dehghanzadeh AR, Salary E, Khounjahan H, Alizadeh R. Z-source-based multilevel inverter with reduction of switches. *IET Power Electron*. 2012;5(3):385-392.
17. Babaei E, Zarbil MS, Sabahi M. A new structure of quasi-Z-source-based cascaded multilevel inverter. *J Circuits, Syst Comp*, 2017; 26:1-26.
18. Sun D, Ge B, Yan X, et al. Modeling, impedance design and efficiency analysis of quasi-Z source moduel in cascaded phtotovoltaic power system. *IEEE Trans Ind Electron*. 2014;61(11):6108-6117.
19. Nguyen MK, Tran TT. Quasi cascaded H-bridge five-level boost inverter. *IEEE Trans Ind Electron*. 2017;64(11):8525-8533.
20. Husev O, Strzelecki R, Blaabjerg F, Chopyk V, Vinnikov D. Novel family of single-phase modified impedance-source buck-boost multilevel inverters with reduced switch count. *IEEE Trans Power Electron*. 2016;31(11):7580-7591.
21. Ho AV, Chun TW. Single-phase modified quasi-Z-source cascaded hybrid five-level inverter. *IEEE Trans Ind Electron*. 2018;65(6):5125-5134.
22. Liu Y, Abu-Rub H, Ge B, Blaabjerg F, Elabban O, Loh PC. Z-Source Multilevel Inverters. In: *Impedance Source Power Electronic Converters*. Chichester, West Sussex, UK: Wiley; 2016:194-224.
23. Liu Y, Ge B, Abu-Rub H, Zhang H, Balog RS. Comparison of SiC and GaN devices for front-end isolation of quasi-Z-source cascaded multilevel photovoltaic inverter. *IEEE Energy Conv Congrass Expo*. 2016;1-6.
24. Banaei MR, Dehghanzadeh AR, Fazel A, Oskouei AB. Switching algorithm for single Z-source boost multilevel inverter with ability of voltage control. *IET Power Electron*. 2013;6(7):1350-1359.
25. Rahul JR, Kirubakaran A. Single-phase quasi-Z-source based isolated DC/AC converter. *IEEE 6th Int. Conf. on Power Systems* 2016:1-4.
26. Ounejjar Y, Al-Haddad K, Gregoire LA. Packed U-cells multilevel converter topology: theoretical study and experimental validation. *IEEE Trans Ind Electron*. 2011;58(4):1294-1306.
27. Gupta KK, kumar L, Jain S. A new seven-level hybrid inverter. IEEE Int Conf PEDES, 2012:1-6.
28. Solarex MSX-60 Photovoltaic Modules. Product Information Sheet http://www.Solarelectricsupply.com
29. Hohm DP, Ropp ME. Comparative study of maximum power point tracking algorithms. *Prog Photovoltaics: Res Appl*. 2003;11(1):47-62.
30. Kouro S, Fuentes C, Perez M, Rodriguez J. Single DC-link cascaded H-bridge multilevel multistring photovoltaic energy conversion system with inherent balanced operation. *38th Annual Conf. on IEEE Industrial Electronics Society,*2012:4998-5005.
31. Patidar K, Umarikar AC. High step-up pulse-width modulation DC-DC converter based on quasi-Z-source topology. *IET Power Electron*. 2015;8(4):477-488.
32. Ji B, Wang J. High-efficiency single-phase Transformerless PV H6 inverter with hybrid modulation method. *IEEE Trans Power Electron*. 2013;60:2104-2115.

33. Perantzakis GS, Christodoulou CA, Anagnostou KE, Manias SN. Comparison of power losses, current and voltage stresses of semiconductors in voltage source transformerless multilevel inverters. *IET Power Electron*. 2014;7(11):2743-2757.

34. Pal A, Basu K. A Unidirectional single-stage three-phase soft-switched isolated DC-AC converter. *IEEE Trans. on Power Electron*. 2018:1-17.

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