

Nonlinear controller for maximum power extraction in asymmetric multilevel DC link reduced switch count inverter-based grid connected PV system

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Summary

This paper presents the grid integration of reduced switch count (RSC)-based asymmetric Multilevel DC-Link (MLDCL) inverter for photovoltaic (PV) system. Among the recently reported reduced switch count multilevel inverter (RSC-MLI) topologies, MLDCL possess modularity, switching redundancies and fault tolerant capability. MLDCL can achieve multilevel output with significant reduction in switch count as compared to cascade H-bridge (CHB). Similar to CHB, the structure of MLDCL allows to develop a common control strategy to obtain maximum powers from equal rated PV sources so that control complexity can be reduced. In this connection, a robust nonlinear sliding mode control (SMC) is designed for MLDCL-based PV system to extract maximum power from each PV source. For this, a three-phase asymmetrical eleven-level MLDCL inverter with PV sources in 2:2:1 voltage ratio is considered. Therefore, two SMCs are developed to extract maximum power from each group of equal rating PV sources. The performance of SMC under variable irradiance conditions is verified against PI controller, and the results are analyzed in MATLAB and hardware-in-loop OPAL-RT test beds.

KEYWORDS

asymmetric topology, closed-loop control system, grid, multilevel inverter, nonlinear controller, photovoltaic (PV), reduced switch count, sliding mode control (SMC)

1 | INTRODUCTION

In recent years, the conventional multilevel inverters (MLIs)¹ such as cascaded H-bridge (CHB), flying capacitor (FC), and diode clamped (DC) MLI configurations have been used in various applications such as adjustable speed drives, flexible AC transmission systems (FACTS), and electric drives etc. Recently, the adoption of MLIs in renewable energy systems^{2 and 3} is one of the new trends. In particular, the CHB MLI² is more dominant than the DC MLI and FC MLIs in the domain of photovoltaic (PV) power feeding to grid. Because of its modularity in its structure and consisting of isolated input dc sources, it is used in previous studies^{3,4} with the objective of injection of PV power into grid. But, these conventional MLIs require a large number of semiconductor devices in order to generate the output voltage with more

List of symbols and abbreviations: C, Capacitor across PV; CHB, Cascaded H-bridge; f_s, Switching frequency; I_{PV}, PV current; L, Lyapunov function; L_f, Filter inductance; MLDCL, Multi-level DC-link; MLI, Multilevel inverter; MPPT, Maximum power point tracking; P_g, Grid power; PV, Photo-voltaic; SMC, Sliding mode control; S_{PV}, Sliding surface; T_s, Sample time; V_{PV}, PV voltage; Y_{PV}, PV output matrix; δ_{PV} , State vector matrix

Correction added on 10 December 2019, after first online publication: Figures 1-22 have been added accordingly.

levels. This leads to increase in complexity and cost of the MLI. In order to avoid these, the reduced switch count (RSC) MLIs have recently gained more prominence in the field of power electronics.

The main objective of RSC MLI topologies is to generate more number of voltages levels using less number of switching devices. Based on this objective, recently, many RSC MLIs have been proposed. An overview of the recently proposed RSC MLIs is presented in.⁵ Among them, the topology in which the switches connect the sources in series (SCSS),⁶ T-type RSC-based MLI reported in Ceglia et al⁷ the topology with cascaded bipolar switched cell (CBSE)-based MLI⁸ and multilevel module (MLM)-based MLI⁹ are modular in structure and contributed to significant reduction in the switch count. However, the topologies presented in previous studies⁶⁻⁹ have drawbacks of unequal load sharing among dc sources, switches having different voltage blocking capabilities. The topology with 'reversing voltage'(RV) MLI¹⁰ and the topology presented in Hota et al¹¹ are modular in structure with possible scope of having common dc-link for three-phase implementation, thereby offering savings in the number of input dc sources. However, these topologies require bidirectional switches and the highest rating switches operate at carrier frequency. The MLIs presented in previous studies^{12,13,14} have single dc voltage source only. Further, topology¹² provides the feature of peak inverse voltages appear across all the switches are less than or equal to dc source voltage. Another RSC-MLI introduced in Noroozi et al¹⁵ is a modified H-bridge to obtain five-level inverter with lesser number of switches to facilitate low cost. Even though the topologies presented in previous studies^{6-10,12-15} have lesser device count than conventional MLIs, but they cannot facilitate the asymmetric nature of the dc sources in their structures for obtaining more number of voltage levels with further reduction in device count.

In order to overcome the above drawbacks, multilevel dc-link (MLDCL) RSC MLI is presented in previous studies.²⁸ This topology is modular and simple in structure, easily scalable, fault tolerant,¹⁶ uses unidirectional switches and there can work with asymmetric input sources. Another popular RSC MLI is switched series parallel sources (SSPS) MLI,¹⁷ which has similar merits of MLDCL. However, in order to generate high number of voltage levels in the output, SSPS MLI requires more switches when compared to MLDCL RSC MLI. Further, MLDCL MLIs have adequate redundancies and require isolated dc sources; therefore, this topology is most suitable and an effective alternate to conventional CHB MLI in the field of integration of PV sources to the grid.

The maximum power injection of PV sources into the grid through conventional MLI topologies is carried out in^{3,4} with appreciable control objectives. For obtaining maximum powers from nonlinear PV sources, conventional PI controllers are adopted in³⁻⁴. In general, the PI controller is linear controller and its performance is sensitive to operating point changes and/or to other disturbances. This is because the gains of PI controller are designed for a specific operating point only. If any changes in operating points or any short time uncertainties occur in the system, then the PI controller detunes and may result overshoots/undershoots with delayed response. Especially in high power applications, these overshoots in the response causes damage to switches of MLI. So that, the use of fixed gain PI controller is a cumbersome process for extraction of maximum power from nonlinear PV sources during irradiance varying conditions. Further, the tuning process of multiple PI controllers becomes a challenging task in the case of individual maximum power extraction of each PV sources connected to each H-bridge of CHB MLI.^{3,4,18-22} To overcome the drawback of the PI controller, it is necessary to linearize the nonlinear PV source and a suitable controller needed to be implemented for extraction of maximum PV power. One of such controller is sliding mode controller (SMC), which is suitable for both linear and nonlinear systems. SMC offer better dynamic performance than PI controller and it results undershoots/overshoots free response of the PV based grid connected systems.

The other controllers such as fuzzy-logic control²³ and back stepping control²⁴ are used for maximum power extraction. However, these controllers are adopted for two-level inverter based dual stage systems and extending to higher level topologies is a tedious task. The power control of grid connected two-level converter under system parameter variations using SMC is reported in.^{25,26} However, the dynamic performance of both PI controller and SMC for maximum power generation from single-stage asymmetric PV sources under variable irradiance conditions has not yet reported.

Hence, this paper proposes a 11-level asymmetric MLDCL RSC MLI-based PV system for integration to a 11-kV grid. In MLDCL RSC MLI, asymmetric PV sources with 1:2:2 ratio is considered for generating more levels in the output voltage with minimum switch count. Furthermore, two SMCs are developed to extract maximum power from each group of equal rating PV sources. The superiority of SMC against the PI controller for generation of maximum power from asymmetric PV sources under varying irradiance conditions is established in both MATLAB and hardware-in-loop OPAL-RT²⁷-based environments.

This paper is organized as follows. Section 2 describes the overview of the proposed closed-loop system along with a description of MLDCL RSC MLI. The adoption of SMC for achieving maximum power from PV sources is explored in Section 3. Control of MLDCL MLI using two-loop PI controller is discussed in Section 4. Simulation results and their validation in real-time is carried out in Section 5.

2 | OVERVIEW OF THE SYSTEM CONFIGURATION

The proposed 11-kV grid connected system consists of three-phase eleven-level MLDCL RSC MLI with input as PV sources are shown in Figure 1. The maximum power of the PV source at different irradiance level can be obtained under the control of either conventional PI or SMC. In order to supply maximum power (P_{ref}) generated from the PV sources to the grid, a two-loop PI controller is involved and it generates reference voltages. The switching operation of MLDCL MLI allows the controller to carry out its control objectives.

2.1 | Proposed asymmetric eleven-level cascaded half-bridge MLDCL MLI

The per-phase structure of eleven-level asymmetric MLDCL topology with 1:2:2 dc voltage ratio is shown in Figure 2. The structure of this topology is divided into two parts, namely, level generator and polarity generator. The first one is responsible for generation of unipolar voltage levels, while the other one converts this unipolar voltage into bipolar. The level generation part can be formed by cascade connection of half bridge cells. Each half bridge cell consists of an isolated dc voltage source with complementary switch pair and produces an output voltage equal to dc source voltage or zero. On the other hand, the polarity generator consists of an H-bridge with switches that operate at fundamental frequency. The operation of MLDCL as an inverter is reported in Gui-Jia.²⁸ The switching table of MLDCL RSC MLI shown in Figure 2 to obtain eleven-levels in phase-voltage is given in Table 1. From this table, it can be observed that MLDCL have following features.

- Identical switching operation in level generator for obtaining positive and negative voltages levels.
- Voltage stress on the operating devices (level generator) remains same for any number of levels.
- The dc link voltage balance is possible with the presence of adequate switching redundancies.

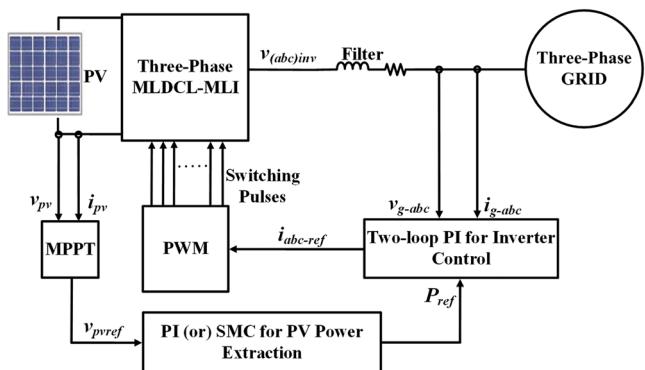


FIGURE 1 Schematic layout of proposed grid integration of PV based MLI system

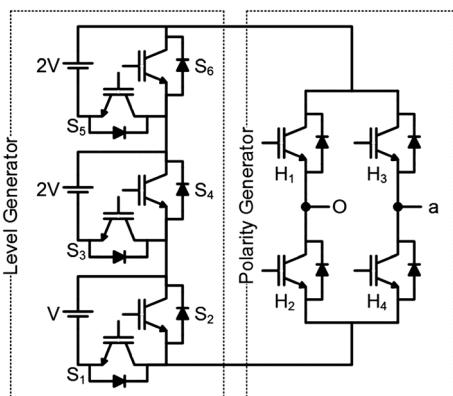


FIGURE 2 Single-phase eleven-level asymmetric MLDCL MLI

TABLE 1 Switching states and phase voltage of 11-level asymmetric MLDCL MLI.

Phase-Voltage Level	Switches Operate in Level Generator	Switches Operate in Polarity Generator
+5V	S ₁ -S ₃ -S ₅	H ₁ -H ₄
-5V		H ₂ -H ₃
+4V	S ₂ -S ₃ -S ₅	H ₁ -H ₄
-4V		H ₂ -H ₃
+3V	S ₁ -S ₃ -S ₆ (or) S ₁ -S ₄ -S ₅	H ₁ -H ₄
-3V		H ₂ -H ₃
+2V	S ₂ -S ₃ -S ₆ (or) S ₂ -S ₄ -S ₅	H ₁ -H ₄
-2V		H ₂ -H ₃
+V	S ₁ -S ₄ -S ₆	H ₁ -H ₄
-V		H ₂ -H ₃
0	---	H ₁ -H ₃ (or) H ₂ -H ₄

In order to obtain 11-levels with 1:2:2 dc voltage ratio, the number of switches required for three-phase asymmetric CHB is 36 as compared to 30 in MLDCL. Hence, Asymmetric configuration will reduce the switch count. Further, a common maximum power extraction control can be used for all equal voltage rated PV sources. This will reduce the cost and complexity of controller.

3 | CONTROL OF POWER FROM PV SOURCES OF ASYMMETRIC MLDCL MLI

In PV energy generation system, the primary element is PV module and its characteristics and design considerations are explained in.²⁹ The methodology of the proposed system (shown in Figure 1) to extract maximum power from PV sources and injection of extracted power to the grid are explained below.

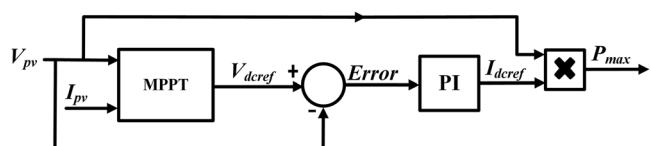
3.1 | Extraction of maximum power from PV source

For extracting maximum power (P_{max}) from PV source, in literature, conventional PI controller along with maximum power point tracking algorithm (MPPT) is reported in Mishra and Sekhar²⁶ and explained below.

3.1.1 | PV power extraction under the control of conventional PI control:

The process of deriving P_{max} from conventional PI control is given in Figure 3 in which input to the PI controller is the error between V_{dcref} and actual V_{pv} and the output is I_{dcref} . In this paper, the voltage (V_{dcref}) which is corresponding to maximum power of PV source is obtained by P & O MPPT algorithm.²⁶

Power extraction using PI based MPPT controller is a simple method. However, the three-phase proposed eleven-level asymmetric MLDCL MLI consists of multiple PV sources with two different voltage ratings, ie, V and 2V as shown in Figure 2. In order to extract maximum power from PV sources, two PI controllers are required, one for V (ie, PV_0) and other for 2V source (ie, PV_1 and PV_2). Tuning of two PI controllers for extracting the powers from two different ratings of nonlinear PV sources in the grid connected MLI system is a challenging task. Further, during

**FIGURE 3** Maximum power extraction from PV source using conventional PI controller

the insolation changes, the conventional PI control may generate overshoots/undershoots with delayed response of P_{\max} . In order to avoid these disadvantages, it is necessary to linearize the nonlinear PV sources using an effective linearization scheme and a robust nonlinear controller can be adopted instead of conventional linear PI controller for extracting maximum power from PV sources. Further, the proposed nonlinear controller should be able to give fast dynamic response without any overshoots/undershoots in response to irradiance changes. One of such linearization scheme is feedback linearization technique and one of such nonlinear controller is sliding mode controller and these are explained below.

3.1.2 | Linearization of nonlinear PV source:

This section describes the input-output linearization scheme to develop nonlinear controller to extract maximum power from PV source. Once the linearized system is developed for nonlinear PV system, a robust SMC can be developed to obtain nonlinear control quantities.

The nonlinear transformation of PV system involves the implementation of feedback linearization scheme. This technique can avoid degraded performance of controller because of irradiance changes. Further, this in turn allows the PV source to be controlled for wide range of irradiance levels.

The PV source as shown in Figure 4 with a parallel capacitor C can be represented as mathematical equations (1) and (2):

$$I_c + I_{pv} = I_{dc} \quad (1)$$

$$I_{pv} + C \frac{dV_{pv}}{dt} = I_{dc} \text{ (or)} \frac{dV_{pv}}{dt} = -\frac{1}{C} I_{pv} + \frac{1}{C} I_{dc} \quad (2)$$

where I_{pv} , I_c , and I_{dc} are PV current, capacitor current, and dc-link current, respectively.

The above nonlinear equation (2) can be converted to linear equation by converting it into state-space representation, which is shown below.

$$\frac{dh}{dt} = f_{pv}(h) + g_{pv}(h) \cdot u_{pv} \quad (3)$$

The state space equation of the PV source is obtained by converting equation (2) into (3) and the results as (4) with V_{pv} as state variable.

$$h = [V_{pv}] g_{pv}(h) = \left[\frac{1}{C} \right] f_{pv}(h) = \left[\frac{-1}{C} I_{pv} \right] u_{pv} = [I_{dc}] \quad (4)$$

After linearization, the new transferred PV system with linearization can be represented as

$$U_{pv} = \left(-g_{pv}^{-1}(h) \times f_{pv}(h) \right) + \left(g_{pv}^{-1}(h) \times \delta_{pv} \right) \quad (5)$$

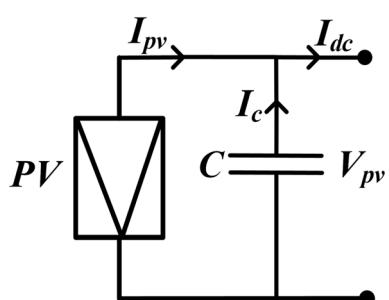


FIGURE 4 Photovoltaic source

Equation 5 can also be represented in the following form as

$$U_{pv} = \alpha_{pv}(h) + (\beta_{pv}(h) \times \delta_{pv}) \quad (6)$$

where $\alpha_{pv}(h) = -g_{pv}^{-1}(h) \times f_{pv}(h)$, $\beta_{pv}(h) = g_{pv}^{-1}(h)$ and δ_{pv} is the state vector matrix with dV_{pv}/dt as an element.

$$i.e., \delta_{pv} = [\delta_{11}]^T = \left[\frac{dV_{pv}}{dt} \right]^T \quad (7)$$

For the PV source, the output parameter is also V_{pv} and hence the output matrix is defined as equation (8):

$$Y_{pv} = [V_{pv}] \quad (8)$$

3.1.3 | Adoption of SMC for PV power extraction:

Sliding mode control^{25,26} is a robust control method and it is successfully tested for control of linear and nonlinear systems. Due to its infinite gain, it nullifies the errors associated with system parameter changes, operating point changes and uncertainties in the system. In this control technique, the state of the system is brought back toward the sliding surface and commutated up to the equilibrium point. The switching and sliding surface do not depend upon the operating point, circuit parameters and converter dynamics. In this paper, SMC is used to obtain new δ_{pv} and subsequently U_{pv} as in (5) for achieving controlled PV power.

3.1.4 | Development of sliding surface and its stability concept:

The obtained state matrix δ_{pv} in linearization of PV source is the input for SMC and it is going to change from old to new state vector until the actual value of a quantity reached reference value. The output of SMC is reference control $U_{pv}(t)$, ie, I_{dcref} which is responsible for obtaining maximum PV power. $U_{pv}(t)$ is a combination of equivalent control and switching control. Equivalent control can be obtained from the process of system linearization while switching function has accomplished the process of cancelling the error in output states V_{pv} .

$$U_{pv}(t) = U_{pr}(t) + U_{sw} = U_{pr}(t) + G \tanh(S_{pv}) \quad (9)$$

where G is a constant and S_{pv} is a sliding surface. For efficient operation of the controller, it is necessary to define sliding surface. There exists one sliding surface S_1 , since Equation (8) has only one output state, V_{pv} . The sliding surface which is a function of error is defined below.

$$S_{pv} = \text{error} = (V_{pv} - V_{dcref}) \quad (10)$$

Hence, in this paper, error in variable parameter V_{pv} is chosen as the sliding surface. The state of the PV system is directed by the SMC towards the equilibrium point at which the error becomes zero and it is achieved by considering Lyapunov approach as shown below.

$$L = \frac{1}{2} S_{pv}^2 \quad (11)$$

As stated in Lyapunov stability concept, the PV system is asymptotically stable if L is positive definite and its derivative ie, dL/dt is a negative one.

$$i.e., \frac{dL}{dt} = \left(S_{pv} \times \dot{S}_{pv}^T \right) < 0 \quad (12)$$

To satisfy the above condition $(S_{pv} \times \dot{S}_{pv})^T < 0$, \dot{S}_{pv} is represented as $\text{Gsign}(S_{pv})$.

$$ie, \dot{S}_{pv} = -G.\text{sign}(S_{pv}) \quad (13)$$

However, the controller performance is highly chattering because of the “sign” function which is a hard switching function. In order to improve the controller performance with chattering free and for continuous switching, a hyperbolic tangent function²⁵ is considered in this paper.

Hence, according to the new chosen soft switching function, Equation 13 is modified as

$$\dot{S}_{pv} = -G.\tanh(S_{pv}) \quad (14)$$

Substituting (10) in (14),

$$\dot{S}_{pv} = -G.\tanh(V_{pv} - V_{dcref}) \quad (15)$$

Using the new dynamics of SMC, the new state vector of PV source can be represented as:

$$\delta_{pv-new} = [\delta_{11}] = [-G.\tanh(V_{pv} - V_{dcref})] \quad (16)$$

where V_{dcref} can be obtained from P & O MPPT algorithm.²⁶ Figure 5 shows the schematic of achieving for maximum power of PV source, P_{max} using SMC. The same procedure is implemented for PV sources (PV0, PV1, and PV2) of the proposed asymmetric three-phase MLDCL MLI in order to get maximum power from all of them.

4 | CONTROL OF MLDCL MLI USING TWO-LOOP PI CONTROLLER

The main control objective of the proposed system is to supply all the maximum powers of asymmetric PV sources into the grid at various irradiance conditions. This objective can be attained by controlling MLDCL MLI using a single-loop based PI controller to which the input is error between the sum of the powers of PV sources as P_{ref} and grid power, P_g . The output of this controller is modulating or reference voltages required for PWM scheme. However, this single-loop direct power control scheme cannot process the errors in the currents. Due to the absence of current loop, it may results overshoots in the current and activates protection circuits in the converters which lead to discontinuity in the operation. In order to avoid the overshoots in the currents, a two-loop PI control scheme is considered and it is shown in Figure 6. In this control scheme, two sets of PI controllers are involved. The first set of PI controller processes the power error and generates reference currents in d - q frame of reference. These reference currents are compared with grid currents and generate current error. The derived current error is given to input of second set of PI controller which gives modulating voltages as output as shown in Figure 6.

Figure 6 shows the grid integration of asymmetric PV sources ($PV_1=PV_2=2V$ and $PV_0=V$) through three-phase MLDCL MLI. The extraction and injection of PV power into the grid is carried out using SMC and two-loop PI controllers respectively and the schematic procedure is shown in Figure 6. Since the proposed asymmetric MLDCL MLI facilitates the redundancies for obtaining the output voltage levels, there is a benefit of uniform or even power distribution between equal rated PV_1 and PV_2 sources. Thus, a common MPPT control mechanism can be used for both PV_1 and PV_2 sources thereby avoiding one extra controller and hence reducing the control complexity. The other PV source, PV_0 is controlled by another MPPT controller since it has half of the I - V ratings as compared to PV_2 or PV_1 . Therefore, two SMCs are developed to extract maximum power from each group of equal rating PV sources. In three-phase MLDCL

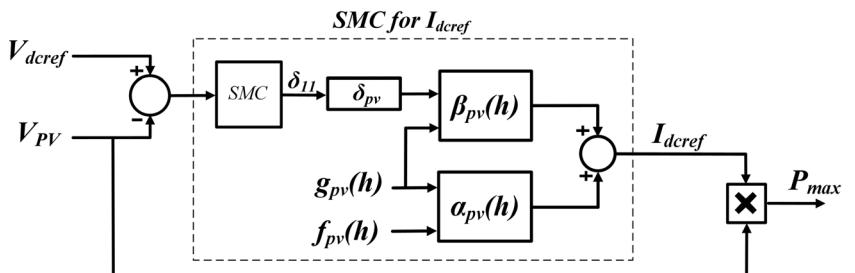


FIGURE 5 Realization of maximum power from PV source using SMC

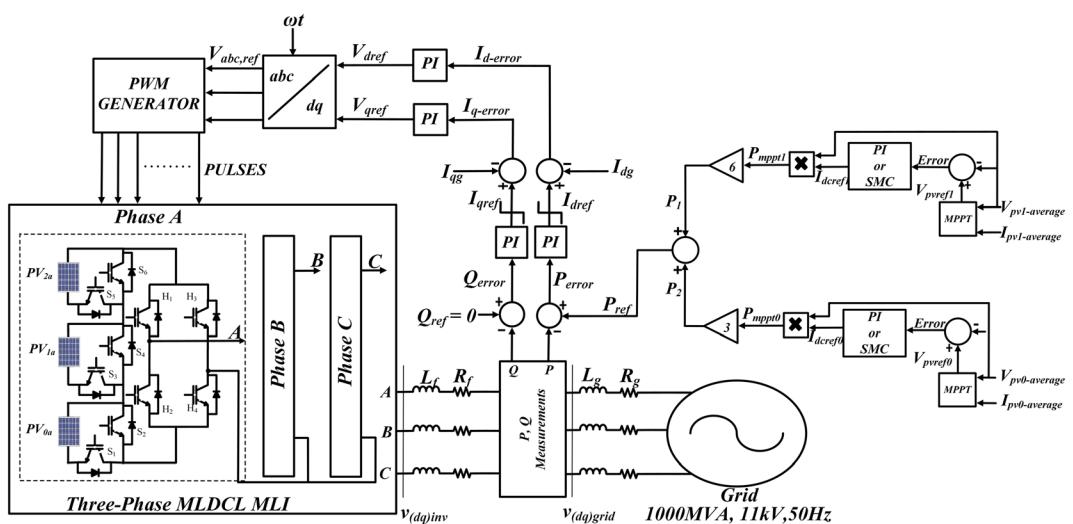


FIGURE 6 The schematic diagram of grid connected PV based MLDCL MLI system using SMC and PI controllers

MLI, there are six equal $I\text{-}V$ rated PV sources (ie, three PV_2 and three PV_1) and three PV_0 sources. Therefore, in order to extract maximum power from each group of equal rating PV sources, the power of single PV_1 source is multiplied with a gain of six. Similarly, a gain of three is used to the power of single PV_0 source as shown in Figure 6. The total PV power is sum of the powers of six PV_1 (or PV_2) sources and three PV_0 sources and it is considered as P_{ref} to two-loop PI control strategy.

5 | RESULTS ANALYSIS

In this section, the performance of PI and SMC controllers for maximum power generation from input PV sources of the proposed closed-loop MLI based grid connected system under various irradiance conditions is studied in MATLAB/Simulink and the results obtained are validated in real-time OPAL-RT platform.

5.1 | Simulation results

The maximum power generation from PV sources using PI controller and SMC is discussed in section 3. The injection of generated power to the grid using two-loop PI controller is developed as shown in Figure 6. The comparative analysis between PI and SMC was taken at 1200, 1000, 900, 800, and 600 W/m^2 irradiance levels and results were carried out through MATLAB/Simulink environment. In this paper, 1000 W/m^2 is considered as 100% irradiance. The input PV sources PV_0 , PV_1 and PV_2 of the asymmetric MLDCL MLI have MPPT voltages of 1600, 3200, and 3200 V at an irradiance of 1000 W/m^2 (100%), respectively. The maximum powers and corresponding voltages of PV sources at different irradiance levels is shown in PV characteristics in Figure 7. The parameters taken for the proposed system is listed in Table 2. The generated eleven-level output voltage from the proposed MLI is shown in Figure 8. The percentage of

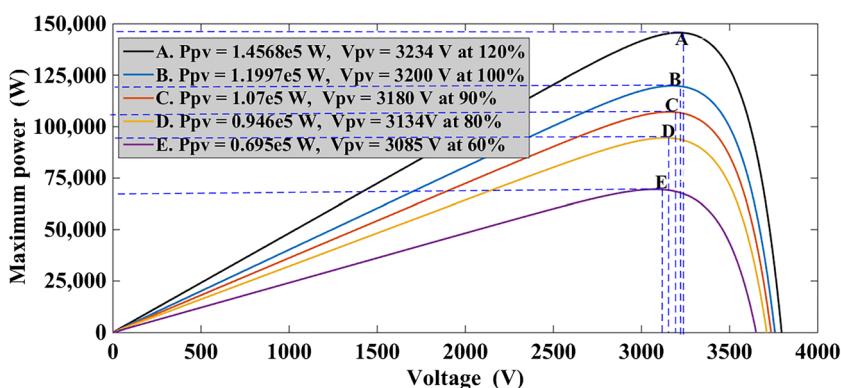
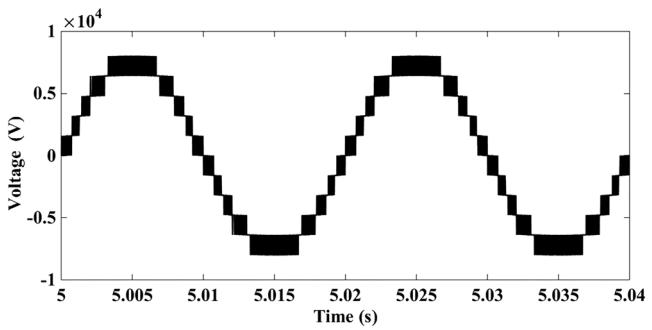


FIGURE 7 P-V characteristics of PV source under various irradiance levels

TABLE 2 Parameters considered for the proposed system

Parameter	Value
Grid Voltage, V_g (line-voltage)	11 kV
Grid frequency, f	50 Hz
Filter inductance, L_f	50 mH
Filter Resistance, R_f	0.2 Ω
Number of parallel and series cells (N_p and N_s) for generation MPPT voltage of 3200 V from PV_1 and PV_2 sources	5 and 4040
Number of parallel and series cells (N_p and N_s) for generation MPPT voltage of 1600 V from PV_0 source	5 and 2020
Capacitor across PV_1 (PV_2) panel, C	0.01 F
Switching frequency, f_s	5 kHz
Sample time, T_s	50 μ s
Base power	1 MVA
Short circuit MVA	1000 MVA

**FIGURE 8** Output voltage of Single-phase 11-level MLDCL MLI

THD in the generated output voltage is 12.1%. All the PV powers are represented in per unit (p.u) based system with a base power of 1 MVA.

The design of filter inductance, L_f mainly depends on the grid current ripples and switching frequency f_s . The filter inductance is given as in Kumar and Mishra³⁰

$$L_f = \frac{1.6V_m}{4hf_{smax}} \quad (17)$$

where V_m is peak of the phase-voltage and h is allowable ripple band in grid current of 1 MVA, 11 kV system. Normally, h is taken as 5% of the grid current. f_{smax} is the maximum switching frequency and it is considered as 20 kHz. The design value of capacitor (C) across the PV sources is given by Jain and Agarwal.³¹

$$C = \frac{2 \times P_{pv}}{4 \times (2 \times \pi \times f) \times V_{pv} \times \Delta V_{pv}} \quad (18)$$

where V_{pv} is the maximum value of the allowed ripple in the voltage (V_{pv}) of the PV source and f is the fundamental frequency of the grid voltage. The value of V_{pv} of the PV source is taken is 3200V, and its corresponding power (P_{pv}) is 0.12MW as shown in Figure 7

Figure 9 shows the maximum power of PV_1 or PV_2 source using PI controller and SMC. From Figure 9, it is observed that during irradiance changes, the maximum power extraction using PI results larger overshoot and undershoots when compared with SMC. Figure 10 represents the maximum power of PV_0 source using PI and SMC. Both Figures 9 and 10 confirm that the delayed performance of PI controller during irradiance changes. On the other hand SMC gives faster response.

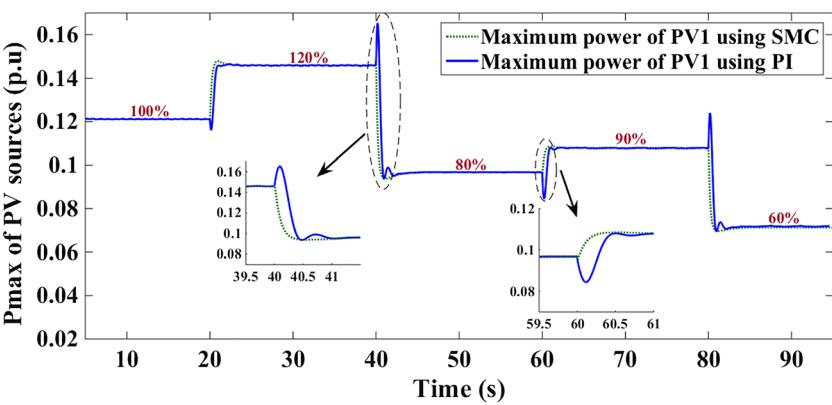


FIGURE 9 Comparative performance of PI and SMC for extraction of maximum power from PV₁ (or) PV₂ source of MLDCL MLI at various irradiance levels

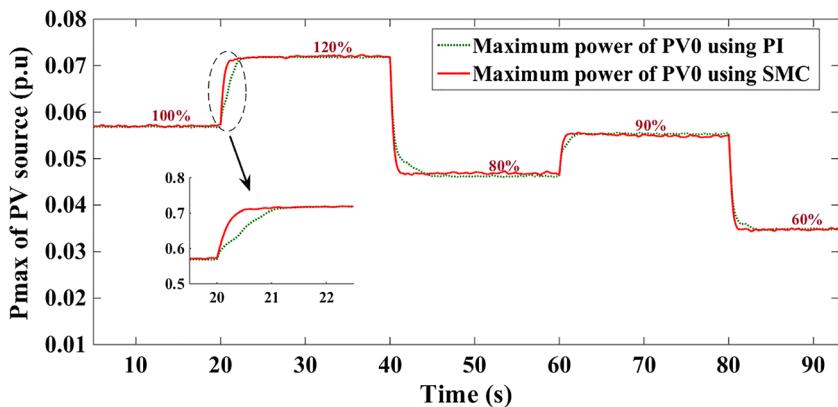


FIGURE 10 Comparative performance of PI and SMC for extraction of maximum power from PV₀ source at various irradiance levels

The performance of both PI and SMC controllers for achieving MPPT voltage across PV₁ or PV₂ is shown in Figure 11. Whenever the irradiance changing from 100% to 120%, a large overshoot in the voltage (V_{PV1}) is observed and this is because of degraded performance of PI controller. Similarly at 40 s, the PI controller performance causes undershoot in the output voltage as shown in Figure 11. Since the PI controller consists of fixed gains and is unable to adapt the gains according to irradiation changes and error, it delivers highly oscillating performance with large overshoots/undershoots in PV power and in corresponding voltages. Whereas SMC can adapt its gains according to error ($V_{dref} - V_{pv}$), quick irradiance changes and exhibits extraordinary performance while delivering the output with very less overshoots/undershoots and settles within very less time as shown in Figure 11. Similarly the superior performance of the SMC while achieving the desired voltage (V_{PV1}) corresponding to maximum power of PV₀ is shown in Figure 12.

Figures 13 and 14 represent the sum of the maximum powers of six PV sources (ie, 3PV₁ and 3PV₂) and maximum power of 3PV₀ sources of the proposed three-phase MLDCL MLI respectively. By observing the sum of individual PV powers at different irradiance levels as shown in Figures 13 and 14, it is confirmed that all the individual PV sources of three-phase MLDCL MLI are delivering their maximum powers according to their PV characteristics. Further Figures

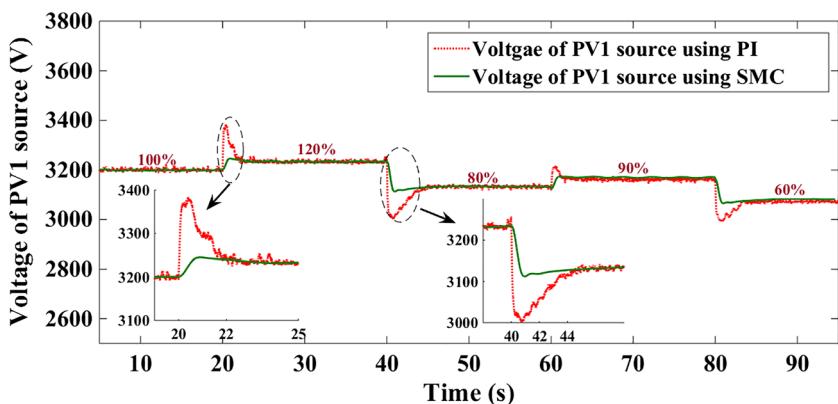


FIGURE 11 Comparative performance of PI and SMC for obtaining desired voltage across PV₁

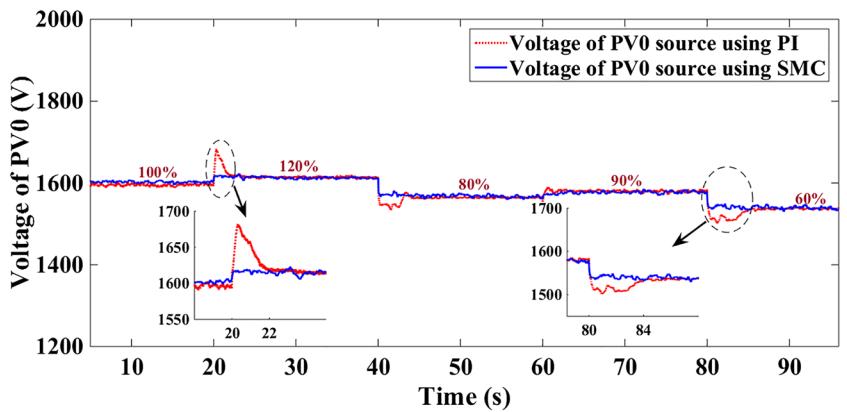


FIGURE 12 Comparative performance of PI and SMC for obtaining desired voltage across PV0

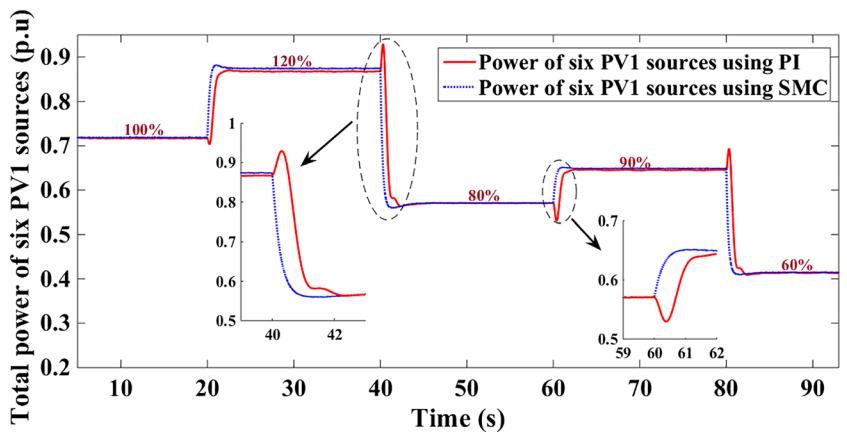


FIGURE 13 Total power extraction of six PV₁ (or PV₂) sources of three-phase MLDCL MLI using PI and SMC

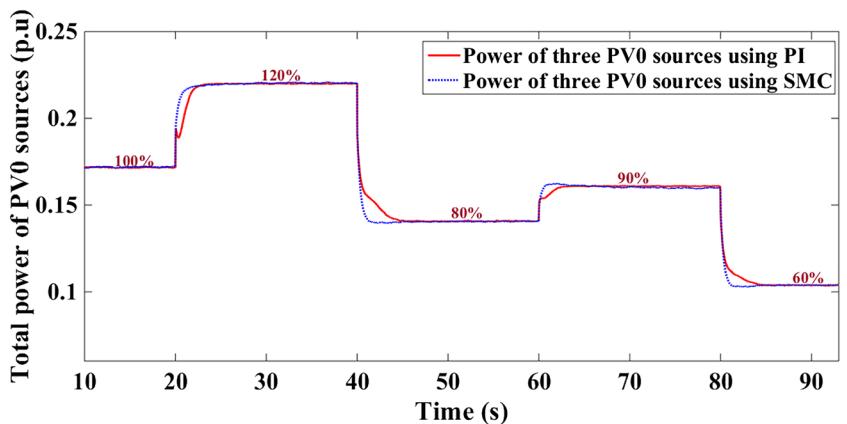


FIGURE 14 Total power extraction of three PV₀ sources of three-phase MLDCL MLI using PI and SMC

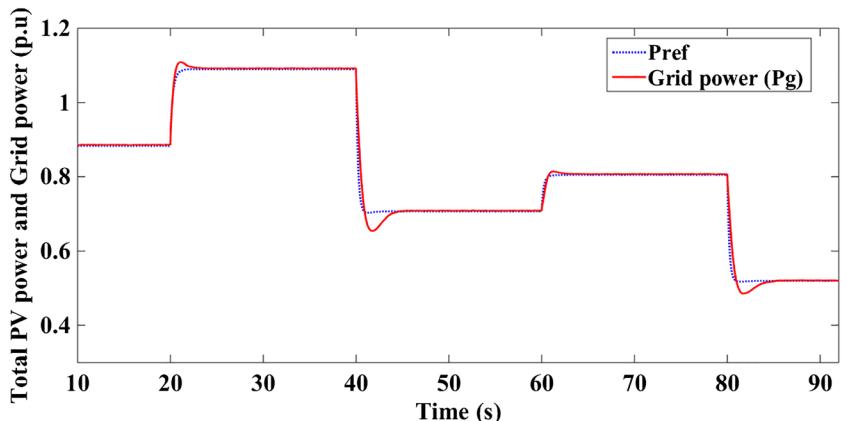


FIGURE 15 Total generated PV power as Pref and grid power (Pg)

13 and 14 again confirm superior performance of SMC over PI controller during the maximum power extraction from all PV sources of the three-phase system.

Figure 15 shows the injected PV power to grid and final grid power (P_g). The total injected PV power is considered as reference (P_{ref}) to the two-loop PI controller which controls the MLI in such a way that it can supply P_{ref} to the grid at all irradiance levels. From Figure 15 it is confirmed that the PV power generated is completely supplied to the grid under the control of two-loop PI control.

5.2 | Hardware-in-the-loop results

The proposed grid connected PV based MLI system under the control of SMC and PI controller is tested in real-time using OPAL-RT modules. The schematic view of hardware-in-the-loop testing of the proposed system using two OP-4500 modules is shown in Figure 16 and the corresponding photograph is shown in Figure 17. The control signals between two OPAL-RT modules are processed by considering three-phase MLDCL MLI connected to the grid is in one module works as plant and SMC or PI controller with PWM method is in another module as a controller. The communication between plant and controller systems is made through DB-37 connector by scaling down the real-time control parameters shown in Figure 16. The sample time and system parameters considered for execution of proposed system in real-time environmental setup is the same as simulation study. The generated eleven-level output voltage from the proposed MLI in real-time using OPAL-RT modules is shown in Figure 18.

Figures 19A and 19B represent the change of maximum power of PV_1 source under control of PI and SMC, respectively. From Figure 19A it is observed that while irradiance is changing from 60% to 100%, PI controller results a large undershoot in the power and it settles in nearly 20 cycles which is high settling time in real case. On the other hand, PV

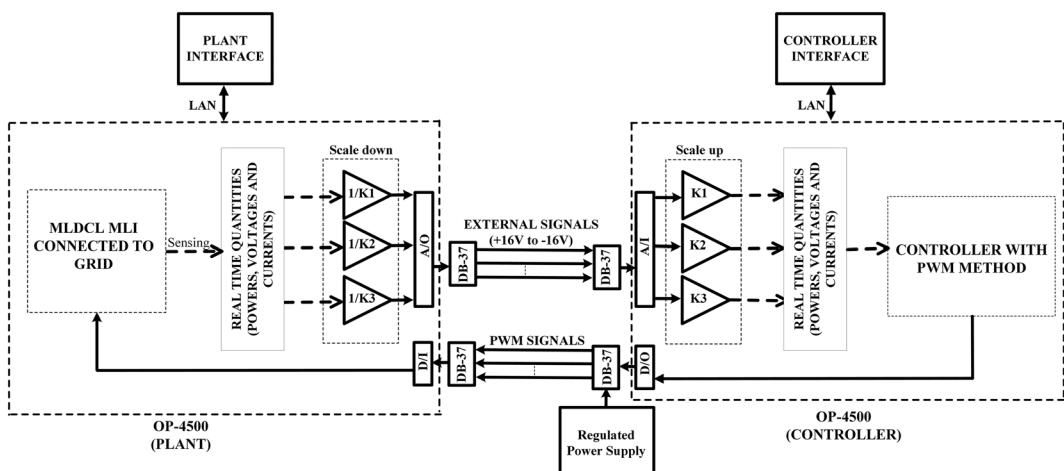


FIGURE 16 Schematic layout of the proposed closed-loop system in HIL environment³⁰

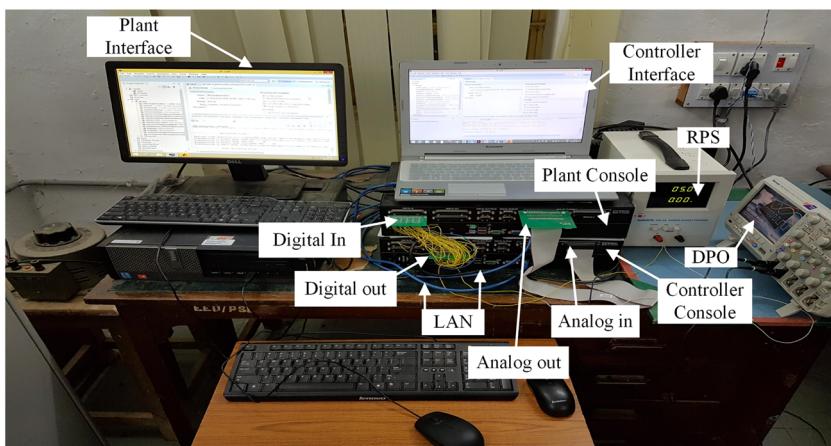


FIGURE 17 HIL setup for the proposed system in real time

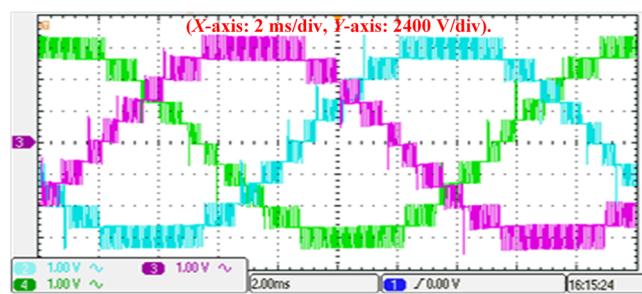


FIGURE 18 11-level output voltages of three-phase MLDCL MLI from OPAL-RT

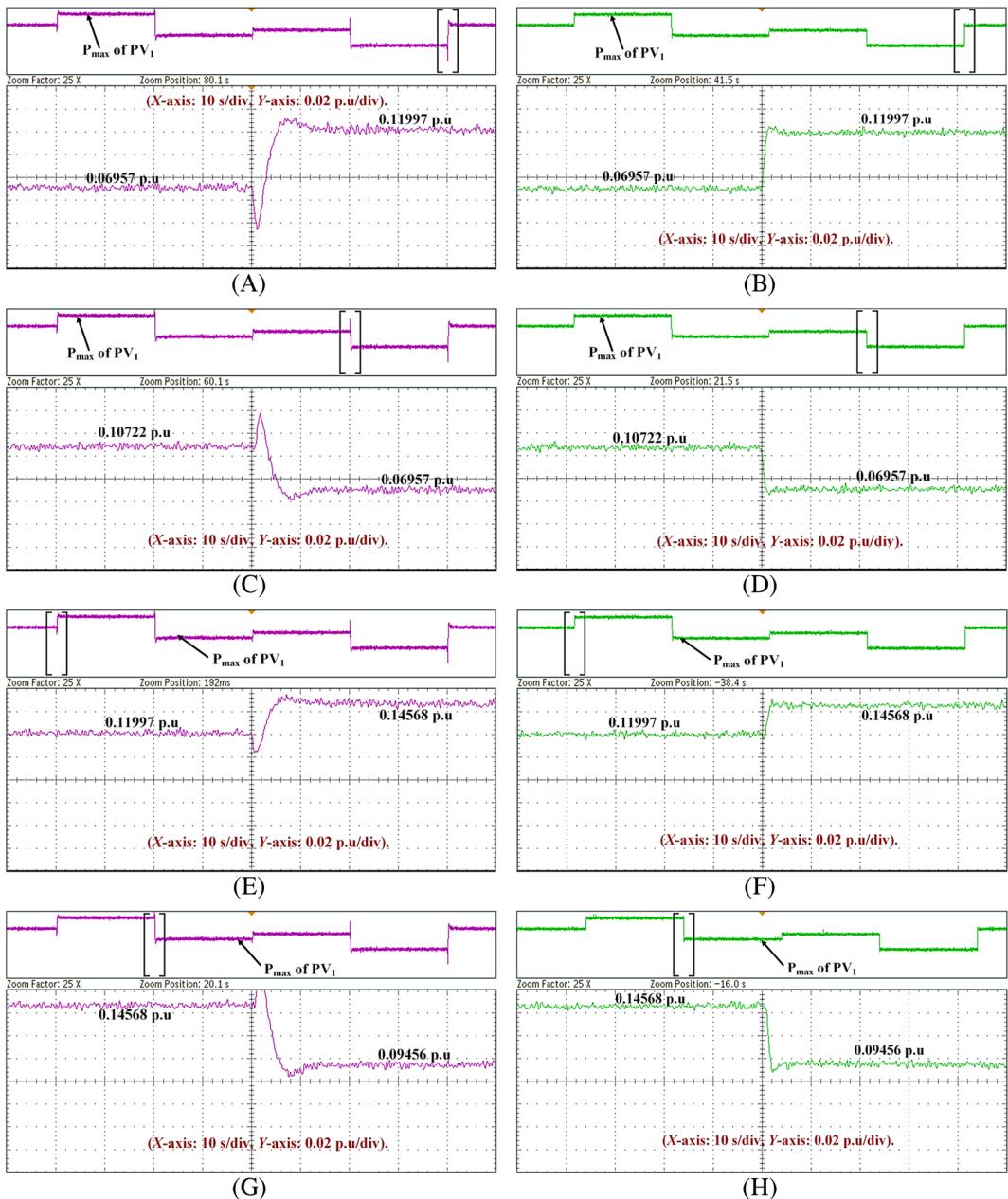


FIGURE 19 Performance of PI and SMC for generation of maximum Power of PV₁ (or PV₂) source under various irradiance conditions. (a) Change in irradiance level from 60% to 100% with PI. (b) Change in irradiance level from 60% to 100% with SMC. (c) Change in irradiance level from 90% to 60% with PI. (d) Change in irradiance level from 90% to 60% with SMC. (e) Change in irradiance level from 100% to 120% with PI. (f) Change in irradiance level from 100% to 120% with SMC. (g) Change in irradiance level from 120% to 80% with PI. (h) Change in irradiance level from 120% to 80% with SMC

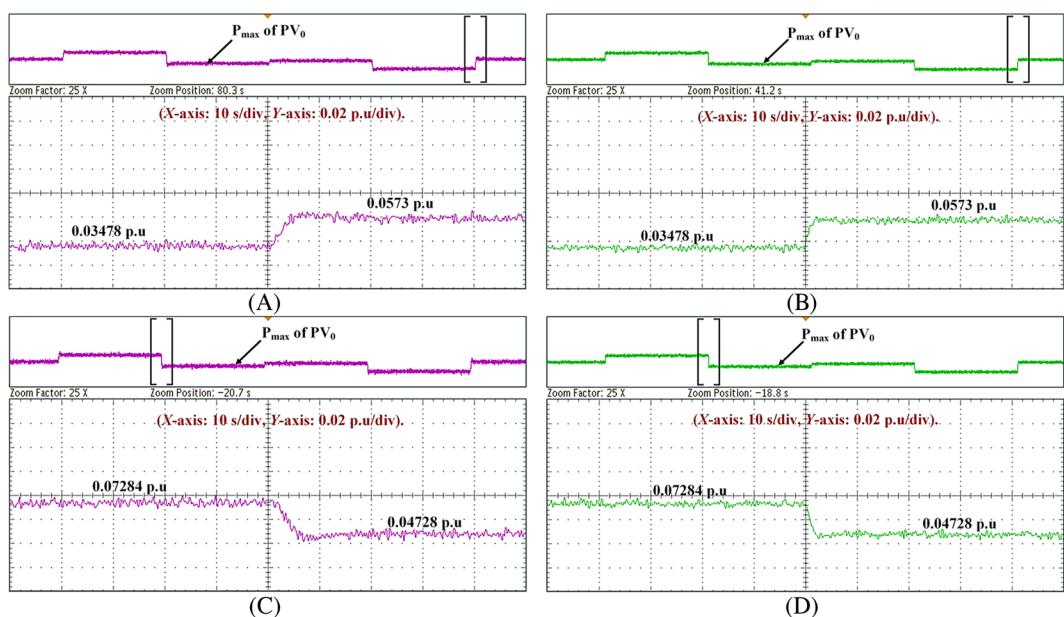


FIGURE 20 Performance of PI and SMC for generation of maximum Power of PV₀ source under various irradiance conditions. (a) Change in irradiance level from 60% to 100% with PI. (b) Change in irradiance level from 60% to 100% with SMC. (c) Change in irradiance level from 120% to 80% with PI. (d) Change in irradiance level from 120% to 80% with SMC

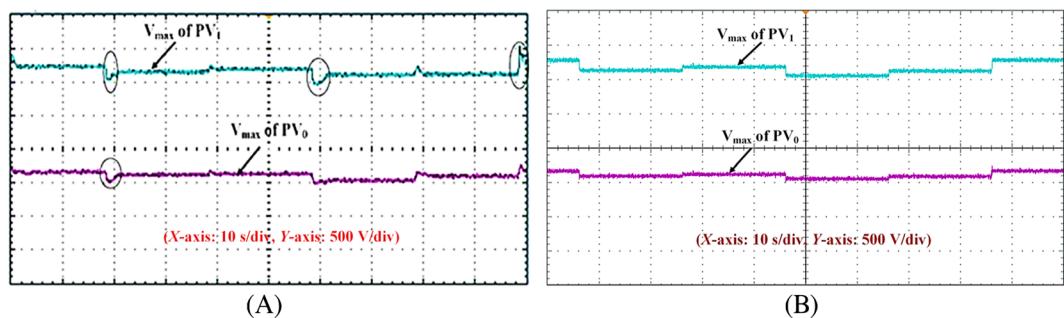


FIGURE 21 Voltages of PV₁ (or PV₂) and PV₀ sources at various irradiance conditions using PI and SMC controllers. (a) With PI. (b) With SMC

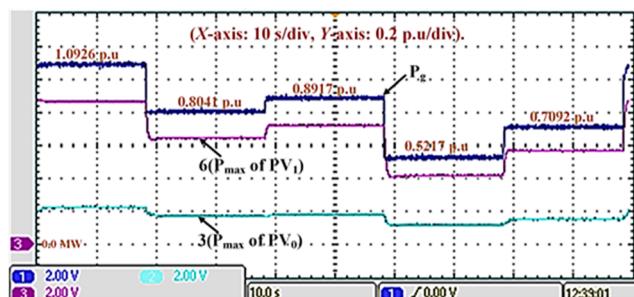


FIGURE 22 Powers of six PV₁ (or PV₂) sources and three PV₀ sources of three-phase MLDCL MLI and grid power (Pg)

power extraction using SMC results good response without under/overshoot and settles to new maximum power point within 3 to 4 cycles and this is confirmed by observing Figure 19B. Similarly, PI controller results a large overshoot in power response as shown in Figures 19C and 19G during irradiance transition from 90 to 60% and 120 to 80%, respectively. These large overshoots may damage the switches of MLI and cause discontinuity in system operation. In order to avoid this, an extra protection circuit is needed, which leads to increase in complexity and cost. Whereas the power

extraction with SMC shows better performance without overshoot and with faster dynamic response rather than PI controller and it is confirmed by observing the Figures 19D and 19H.

Figures 20A and 20B show the variation in power of the PV_0 source under control of PI and SMC respectively during irradiance is changing from 60% to 100% in hardware-in-the-loop environment. In this case, the performance of PI controller is similar to SMC except a delay in reaching new PV power. Similarly, both PI controller and SMC exhibit similar dynamic performance for extracting PV_0 power during other irradiance changing condition also. Further, both controllers show good performance in steady-state without error since maximum powers of PV_1 source and PV_0 sources are obtained and follow according to the PV characteristics as shown in Figure 7 at given irradiance levels.

Further, at the respective irradiance of 120%, 90%, 100%, 60%, and 80%, the change in voltages of the PV sources (ie, PV_1 or PV_2 and PV_0) corresponding to their maximum powers under the control of PI and SMC are shown in Figures 21A and 21B, respectively. The superior performance of SMC controller for obtaining desired voltages of PV sources of MLDCL MLI is shown in Figure 21B in which, transient free and fast dynamic response is observed.

5.2.1 | Grid power and total powers of all the PV sources of three-phase MLDCL MLI

Figure 22 shows the grid power and sum of the total power of all PV sources (ie, $3PV_1$, $3PV_2$, and $3PV_0$) of asymmetric three-phase MLDCL MLI. From Figure 22, it is confirmed that at various percentage of irradiance conditions, the objective of injection of PV power into the grid is satisfied under the effective control of SMC and two-loop PI controller. Therefore, the entire maximum PV power generated from all the PV sources is injected into the grid.

6 | CONCLUSION

In this paper, grid integration of PV sources through a three-phase asymmetric RSC-MLI is discussed. The proposed asymmetric MLDCL MLI facilitates less switch count, highly modular, and enables the operation of unequal rated PV sources, and hence it can be an alternate to conventional MLIs for closed-loop power control in grid integration of PV based applications. The superior performance of variable gain SMC results fast dynamic PV power response under irradiance varying conditions and it is verified against fixed gain PI controller which results large overshoots/undershoots with delayed response. Further, SMC enables the extraction of maximum power from multiple PV sources with ease. The maximum PV power generated under the efficient control of SMC are successfully supplied to 11 kV grid through MLDCL RSC MLI.

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APPENDIX A.

Parameters used for photo-voltaic cell

Parameter	Value
Cell's short circuit current (I_{sc})	8.03 A
Cell reverse saturation current, I_{rs}	$1.2e^{-7}$ A
Charge of an electron, q	1.602×10^{-19} C
Boltzmann's constant, k	1.38×10^{-23} J/K
Ideality factor, A , Cell's reference temp, T_{ref}	1.92, 300 K
Short circuit current temperature co-efficient of cell, K_I	0.0017