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RESEARCH ARTICLE

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Power quality enhancement by hybrid DSTATCOM with improved performance in distribution system

Hareesh Myneni | Siva Kumar Ganjikunta | Sreenivasarao Dharmavarapu

Electrical Engineering Department, National Institute of Technology Warangal, Warangal, Telangana, India

Correspondence
Siva Kumar Ganjikunta, NIT Warangal, Warangal, Telanga, India.
Email: gsivakumar@nitw.ac.in

Summary

The current quality of the utility in distribution system is improved by using distribution static compensator (DSTATCOM). The voltage source inverter (VSI) of DSTATCOM is connected to utility through an interfacing inductor for smoothing the current. But the required inductance value is high in conventional DSTATCOM. Due to this, the requirement of DC-link voltage of VSI is increased to improve the current quality. In this paper, a hybrid DSTATCOM topology is proposed to reduce the inductance value, which will reduce the requirement of the DC-link voltage. In conventional hybrid DSTATCOM, DC-link voltage is maintained to a fixed value; due to this, the switching losses is more under the reduced load conditions. In order to minimize the switching losses, a variable DC-link voltage control is proposed, which is based on the ac series capacitor voltage and the compensation performance. The effectiveness of the proposed method is validated by simulation and experimental studies.

KEYWORDS

DC-link voltage, harmonics, hybrid DSTATCOM, power quality, switching losses

1 | INTRODUCTION

The proliferation of power electronic devices and reactive loads in three-phase four-wire (3P4W) distribution system causes high reactive power burden as well as power quality issues such as current harmonics, poor voltage regulation, load unbalancing, and excessive neutral current. The distribution static compensator (DSTATCOM) is a commonly used

Nomenclature: C_{dc1},C_{dc2}, upper and lower dc-link capacitances; C_r, resonance capacitance; DSTATCOM, distribution static compensator; $f_{sw,max}$, maximum switching frequency; f_r, resonance frequency; h, hysteresis band; i_s, instantaneous source current; i_l, instantaneous load current; i_f, instantaneous filter current; $I_{f,min}$, minimum rms filter current; i_{la},i_{lb},i_{lc}, instantaneous load currents of phase a,b,c; i_{fa},i_{fb},i_{fc}, instantaneous filter currents of phase a,b,c; i_{sa},i_{sb},i_{sc}, instantaneous source currents of phase a,b,c; i_{sn}, instantaneous source side neutral current; i_d, DC side current of VSI; $I_{f,max}$, maximum rms filter current; I_f^*, reference rms filter current; ISCT, instantaneous symmetrical component theory; i_{dc}^m, mean current on dc side of VSI; k_P, proportional gain factor; k_I, integral gain factor; L_{f1}, inverter side interfacing inductance; L_{fg}, grid side interfacing inductance; m_a, amplitude modulation index; PCC, point of common coupling; Q_{rated}, rated reactive power demand by load; R_f, internal resistance of L_{fg}; R_{f1}, internal resistance of L_{f1}; R_d, damping resistance; THD, total harmonic distortion; $V_{inv,min}$, minimum inverter voltage; $\boldsymbol{V}_{dc,ref}$, calculated reference dc-link voltage; $\boldsymbol{V}_{dc}^*$, final reference dc-link voltage; $\boldsymbol{V}_{dc,m}$, maximum dc-link voltage; $\boldsymbol{V}_{dc1}$,$\boldsymbol{V}_{dc2}$, upper and lower dc-link capacitor voltages; V_{pcc}, RMS voltage at PCC; V_{inv}, RMS inverter voltage; $\boldsymbol{V}_{dc}$, total dc-link voltage; VSI, voltage source inverter; v_{sa},v_{sb},v_{sc}, instantaneous source voltages of phase a,b,c; V_{Cf}, voltage across series ac capacitor; X_{Cf}, reactance of series ac capacitor; X_{Lf}, Equivalent reactance of L_{f1} and L_{fg}; ΔI_f^*, change in reference filter current; ε_i, tolerance allowed in filter current; ω_n, natural frequency of system; ζ, damping factor

device to minimize the above stated power quality issues.[1-4] DSTATCOM is realized by voltage source inverter (VSI) supported by DC-link capacitor and coupling or interfacing inductor. The coupling inductor serves as a filter to attenuate the unwanted switching frequency harmonics in the output current of VSI. The purpose of the DC-link capacitor is to maintain average energy exchange between distribution system and DSTATCOM to zero. This is achieved by maintaining the DC-link capacitor voltage to the reference value by a dc-link voltage regulator. The reference dc-link voltage is selected as twice the peak of PCC voltage in inductive filter–based DSTATCOM (considered as *L*-DSTATCOM). The kVA rating of VSI depends on dc-link voltage and current. To reduce the kVA rating of VSI, hybrid topologies are exist in literature.

In Fujita and Akagi,[5] a hybrid topology with combination of passive filter and active filter is presented, in which the passive filter removes the harmonics and active filter compensates the load reactive power. In Valdez-Fernandez et al,[6] a hybrid power filter is discussed, which is capable of harmonic compensation under unbalanced operation. But this method requires high value of dc-link voltage for satisfactory compensation. A thyristor-controlled *LC* filter (TC*LC*)–based hybrid active filter[7] and static var compensator (SVC)–based hybrid active filter[8] are proposed for power quality improvement. In these topologies, generation of pulses for both active filter and TC*LC* or SVC switches makes the algorithm complex. Moreover, the losses due to switches in the TC*LC* or SVC reduces the efficiency of the system. An adaptive fuzzy hysteresis band current control for switching losses reduction in hybrid active power filter is discussed.[9] A hybrid DSTATCOM with reduced dc-link voltage is proposed for reactive power compensation and harmonic mitigation.[10] In this topology, the required volt-ampere rating of VSI is low when compared with VSI rating in *L*-DSTATCOM.[11] A split-capacitor active filter topology is proposed to improve the dc-link voltage utilization.[12] But in this method, the number of switching devices and passive elements are increased. A series hybrid active filter is discussed with small inverter capacity rating.[13] But it requires an extra diode bridge and single-phase source for dc-link capacitor charging. In the above discussed topologies, the dc-link voltage of VSI is maintained constant to reference dc-link voltage, which is calculated based on rated reactive load. Because of that, the voltage stress across switches of VSI is high under reduced load conditions. This drawback is minimized by proposing adaptive dc-link voltage regulation methods.

An adaptive dc-link regulation of *LC* hybrid active power filter (*LC*-HAPF) is presented for reactive power compensation.[14] In this case, the dc voltage is selected based on reactive power sharing between passive and active filters. Further, a new topology of active filter with TC*LC* is proposed with the variable dc-link voltage.[15] In which, the switching devices are more, and the gating pulses generation for both the active filter and TC*LC* makes the system control to be more complex. In these methods, the calculation of dc-link voltage involves many transformations, which increases the computational burden. A dynamic dc-link voltage regulation method is proposed to reduce the computation burden.[16] In existing methods, the dc-link voltage is regulated to reference voltage by a proportional integral (PI) controller with fixed gains. This leads to poor transient response during dc-link voltage variation. In case of non-stiff source, an additional ripple filter is required in the above discussed topologies to make the PCC voltages sinusoidal, which increases the overall cost of the system.[16,17] Also, the required interfacing inductance value is high.

In this paper, a hybrid DSTATCOM is proposed, in which the required inductance value is less when compared with conventional DSTATCOMs. This leads to reduction of voltage drop across the interfacing inductance. Therefore, the dc-link voltage requirement is reduced, which in turn reduces the rating of VSI. For the case of non-stiff source, an extra ripple filter is not required in the proposed method. The operation of ripple filter is achieved with low rating shunt resonant capacitor with proper design of hybrid DSTATCOM parameters. A variable dc-link voltage control method corresponding to load operating condition is proposed to improve the hybrid DSTATCOM performance by reducing switch voltage stress and switching losses. Therefore, the VSI reliability and efficiency are increased. Further, an adaptive PI controller is implemented, in which the gains are adjusted corresponding to load operating condition such that the transient response of dc-link voltage is also improved.

2 | PROPOSED VARIABLE DC-LINK VOLTAGE CONTROL FOR HYBRID DSTATCOM

The schematic diagram of the hybrid DSTATCOM is shown in Figure 1. i_{si} and i_{li} are the source current and the load current, respectively. i_{fi} is the filter current injected by DSTATCOM for reactive power compensation and harmonics mitigation (here, i=a,b,c). L_{f1} and L_{fg} are VSI side and grid side interfacing inductors used for smoothening filter currents. The resonant capacitor, C_r, is used for switching frequency harmonics elimination, and the combination of C_r with interfacing inductors forms an *LCL* filter. R_d is a damping resistor used for stability of the system. V_{pcc} (rms)

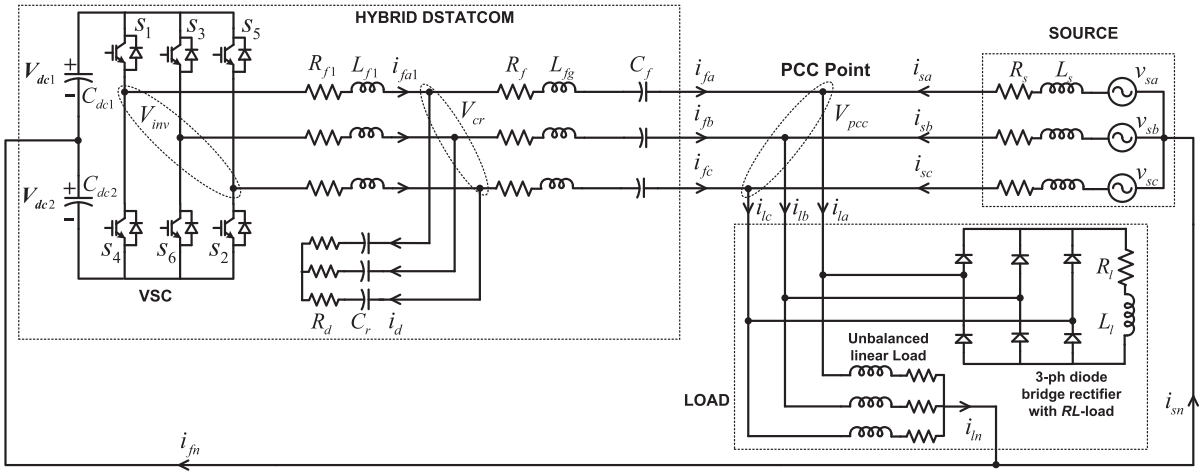


FIGURE 1 Hybrid DSTATCOM topology for power quality improvement in 3P4W distribution system

and V_{inv} (rms) are the voltages at PCC and VSI output, respectively. $\mathbf{V}_{dc1}$ and $\boldsymbol{V}_{dc2}$ are the dc-link voltages maintained with voltage controller across C_{dc1} and C_{dc2}, respectively.

The dc-link voltage magnitude of DSTATCOM plays a very important role in the compensation performance. In conventional *L*-DSTATCOM, the dc voltage is maintained constant and this constant value is selected as twice the peak of PCC voltage in[17], 1.6 times peak of PCC voltage in[18] based on the rated load condition. A DSTATCOM with reduced dc-link voltage is discussed by connecting an ac capacitor in series with interfacing inductor.[10] However, the choice of dc-link voltage magnitude is fixed for fixed ac capacitor value and is selected based on the rated load condition. The selection of dc-link voltage for variable load conditions is discussed in below.

2.1 | DC-link voltage reference selection in existing methods

In literature review, very few authors have discussed the variable dc voltage control, in which dc voltage is selected based on reactive powers.[14,15] The following disadvantages are noticed in these methods:

1. The calculation of reactive power involve *abc* to $\alpha\beta$ transformation and vice versa, which increases the computational burden.
2. The transient response of the dc-link voltage variation is not discussed, which will affect the performance of DSTATCOM, because the fixed PI controller gains not gives the desired response during dc-link voltage variation.

A dynamic dc-link voltage variation of DSTATCOM is discussed based on the filter currents,[16] in which the computational burden is reduced because of eliminating transformations. The dc-link voltage in this method is calculated as given below.

$$\boldsymbol{V}_{dc} = \frac{V_{pcc}}{m_a}\left(\frac{I_f^* + I_{f,m}}{I_{f,m}}\right), \tag{1}$$

where m_a is the amplitude modulation index, $I_{f,m}$ (rms) is the maximum filter current to be compensated by DSTATCOM, and I_f^* is the reference filter current obtained from instantaneous symmetrical component theory (ISCT).[19,20] The above equation (1) is not valid for dc-link voltage calculation in hybrid DSTATCOM topologies. Also, the following disadvantages are observed in the above method.[16]

1. The transient response of the dc-link voltage is still poor.
2. Performance index, THD of source current is not considered.
3. An extra ripple filter is required in case of non-stiff source, which increases cost of the system.

2.2 | Proposed method of dc-link voltage reference selection

In hybrid DSTATCOM topology, the voltage across series capacitor (C_f) supports the inverter voltage; due to this, the requirement of DC-link voltage is reduced. Here, the capacitor voltage (V_{Cf}) magnitude depends on the filter current (I_f) injected by the DSTATCOM. In conventional hybrid DSTATCOM, the DC-link voltage is maintained to fixed value and is designed based on the rated filter current injected by DSTATCOM.[10] Because of that, the switching losses and voltage stress across switches of VSI are high for the reduced load conditions. These drawbacks are minimized by the proposed variable DC-link voltage method.

In the proposed method, the reference DC-link voltage is expressed in terms of minimum filter current ($I_{f,min}$), maximum series capacitor voltage ($V_{Cf,max}$), and reference filter current (I_f^*). By expressing the reference DC-link voltage in terms of $I_{f,min}$ and $V_{Cf,max}$ avoids the extra sensing elements. From Figure 1, by applying Kirchhoff voltage law (KVL), the inverter voltage is given as (neglecting internal resistance of filter components)

$$V_{inv} = V_{pcc} + X_{Lf}I_f - X_{Cf}I_f, \tag{2}$$

where X_{Lf} is the equivalent reactance of the interfacing inductors (L_{f1} and L_{fg}) and X_{Cf} is the reactance offered by series capacitor (C_f). The inverter voltage at minimum filter current $I_{f,min}$ will be written from (2),

$$V_{inv,min} = V_{pcc} + X_{Lf}I_{f,min} - X_{Cf}I_{f,min}. \tag{3}$$

The above equation is rewritten as

$$V_{inv,min} - V_{pcc} = (X_{Lf} - X_{Cf})I_{f,min}. \tag{4}$$

Here, the value of X_{Cf} is always greater than X_{Lf} such that the series capacitor voltage support for VSI output voltage and thereby reduce the DC-link voltage requirement. During the operation of DSTATCOM, the reference inverter voltage will be written from (2),

$$V_{inv,ref} = V_{pcc} + X_{Lf}I_f^* - X_{Cf}I_f^*. \tag{5}$$

The above equation can be rearranged as follows:

$$V_{inv,ref} - V_{pcc} = (X_{Lf} - X_{Cf})I_f^*, \tag{6}$$

where I_f^* is the reference filter current. By dividing (6) with (4), the following relation is obtained.

$$\boldsymbol{V}_{inv,ref} = V_{pcc} + \left(V_{inv,min} - V_{pcc}\right)\frac{I_f^*}{I_{f,min}}. \tag{7}$$

The relation between inverter voltage ($V_{inv,ref}$) and DC-link voltage ($V_{dc,ref}$) is given by $V_{inv,ref}$=$m_aV_{dc,ref}$. Here, m_a is amplitude modulation index. Then (7) becomes

$$\boldsymbol{V}_{dc,ref} = \frac{1}{m_a}\left[V_{pcc} + \left(V_{inv,min} - V_{pcc}\right)\frac{I_f^*}{I_{f,min}}\right]. \tag{8}$$

During minimum filter current, the voltage drop across interfacing inductor can be negligible as the inductive reactance is also small. Thus, the voltage difference between inverter voltage and PCC voltage during minimum filter current can be written from (4) as

$$V_{inv,min} - V_{pcc} = -X_{Cf}I_{f,min}. \tag{9}$$

In the above equation, the product $X_{Cf}I_{f,min}$ is equal to the minimum series capacitor voltage ($V_{Cf,min}$). Then (8) becomes

$$\boldsymbol{V}_{dc,ref} = \frac{1}{m_a}\left[V_{pcc} - V_{Cf,min}\frac{I_f^*}{I_{f,min}}\right]. \tag{10}$$

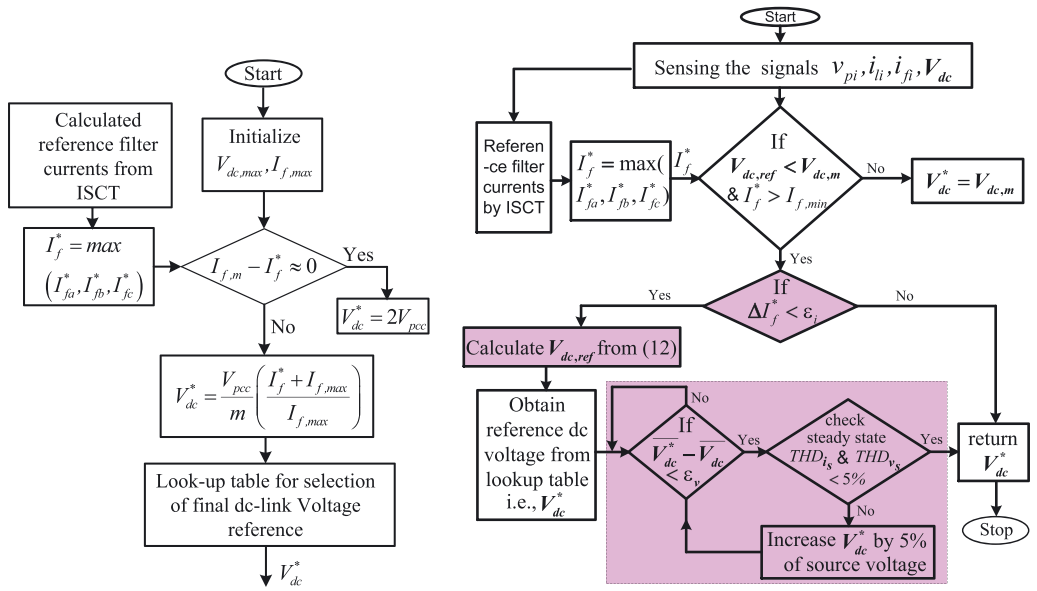
The above equation is to be expressed in terms of maximum capacitor voltage ($V_{Cf,max}$), because the maximum capacitor voltage ($V_{Cf,max}$) is defined value, which is nothing but the rated value of the series capacitor. If $V_{Cf,max}$=$X_{Cf}I_{f,max}$, then the relation between $V_{Cf,max}$ and $V_{Cf,min}$ is given as

$$V_{Cf,min} = \frac{V_{Cf,max}I_{f,min}}{I_{f,max}}. \tag{11}$$

In the proposed method, the DC link voltage is varied with respect to variation of the filter current due to load change in the distribution system. Because of this, the DC-link voltage has to change frequently, and it leads to affect the compensation performance. To avoid this, the DC-link voltage is varied in the step change variation of the filter current. Here, the step size is considered as 10% of the maximum filter current. The first step is from 0% to 10% of the maximum filter current, second step is 10% to 20%, and so on up to maximum value. So the minimum filter current is considered as 10% of the maximum filter current, which is the higher value of the first step. Therefore, by substituting $I_{f,min}$=0.1$I_{f,max}$ in (11), the obtained $V_{Cf,min}$ value is equal to 0.1$V_{Cf,max}$. Then, from (10), the reference DC-link voltage is given as

$$\boldsymbol{V}_{dc,ref} = \frac{1}{m_a}\left[V_{pcc} - 0.1V_{Cf,max}\left(\frac{I_f^*}{I_{f,min}}\right)\right]. \tag{12}$$

The flow-chart for selection of dc-link voltage in existing method is shown in Figure 2A. In the existing method,[16] the calculated dc-link voltage from (1) may not be sufficient to track the filter current for some of the cases, during which



% of maximum filter current $\left(I_f^*\right)$	0-0.1	0.1-0.2	0.2-0.3	0.3-0.4	0.4-0.5	0.5-0.6	0.6-0.7	0.7-0.8	0.8-0.9	0.9-1
Range of dc voltage	$V_{dcL} \leftrightarrow V_{dcH}$	$V_{dcL1} \leftrightarrow V_{dcH1}$	$V_{dcL2} \leftrightarrow V_{dcH2}$	$V_{dcL3} \leftrightarrow V_{dcH3}$	$V_{dcL4} \leftrightarrow V_{dcH4}$	$V_{dcL5} \leftrightarrow V_{dcH5}$	$V_{dcL6} \leftrightarrow V_{dcH6}$	$V_{dcL7} \leftrightarrow V_{dcH7}$	$V_{dcL8} \leftrightarrow V_{dcH8}$	$V_{dcL9} \leftrightarrow V_{dcH9}$
Final dc voltage $\left(V_{dc}^*\right)$	V_{dcH}	V_{dcH1}	V_{dcH2}	V_{dcH3}	V_{dcH4}	V_{dcH5}	V_{dcH6}	V_{dcH7}	V_{dcH8}	V_{dcH9}

(C)

FIGURE 2 Flowchart for reference dc-link voltage selection: (A) existing method[16] and (B) proposed method. (C) Lookup table for the proposed method (highlighted boxes are for better performance)

the source current THD is more than IEEE-standard limits. This problem is considered in the proposed method and is explained here.

The selection of final reference dc voltage ($\boldsymbol{V}_{dc}^{*}$) in the proposed method is shown in Figure 2B. It is observed from (12) that the dc voltage depends on I_f^*. Therefore, first calculate the reference filter currents from ISCT and then calculate maximum among three filter currents. Initially, check the reference filter current and calculated dc voltage from (12) are less than the maximum filter current, $I_{f,m}$ (rms), and maximum dc voltage ($\boldsymbol{V}_{dc,m}$), respectively. The checking of change in filter current (ΔI_f^*) less than error (ε_i) condition eliminates the calculation of dc-link voltage for the same filter current. In this case, the previous dc-link voltage is maintained as present value. After calculation of dc voltage from (12), to minimize frequent fluctuations in dc voltage, choose final reference dc-link voltage ($\boldsymbol{V}_{dc}^{*}$) from the look-up table. The lookup table is implemented based on the filter current with 10% step variation of each range as shown in Figure 2C. Further, an algorithm of performance index check is proposed and is shown in dotted box of Figure 2B. In this, first check the dc-link voltage is reached steady state or not. After reaching steady state, the THDs of source current and voltage are measured over one cycle. If THDs are not satisfied by the prescribed limits, then dc-link voltage increased by 5% of source voltage, and this process is repeated until THDs are with in prescribed limits.

The reference dc-link voltage calculated in the proposed method is less when compared with conventional method for reduced load conditions. Therefore, the switching losses are reduced, which are calculated from energy dissipation in the IGBT switches.[21] But for load variation, the compensation performance may not be satisfactory because of insufficient dc voltage during transient period. In such cases, sensitive equipment (which require fast response, for example, operation theater equipment) connected to the source may malfunction. It can be minimized by implementing an adaptive PI controller, which is presented below.

2.3 | Adaptive PI controller for dc-link voltage control

The dc-link voltage of DSTATCOM should be maintained at sufficient value for proper compensation. In conventional method, fixed PI controller has been used to maintain the dc-link voltage constant. The error between reference and measured dc voltages is given as input to PI controller. The output of PI controller is taken as power loss, P_{loss}, in the VSI, where fixed PI controller gives satisfactory performance because of the reference dc-link voltage is fixed.[10] As the dc-link voltage is varied in the proposed method, the fixed PI controller may not give satisfactory performance at different reference dc voltages.

An adaptive PI controller is proposed, in which the gains are adjusted during the change of reference dc-link voltage, such that the performance always matches desired response. The block diagram of the adaptive PI controller is shown in Figure 3, in which $\boldsymbol{V}_{dc}^{*}$ and $\boldsymbol{V}_{dc}$ are reference and measured dc voltages, respectively. i_d is the current flowing through VSI, i_{dc}^{m} is the average value of dc side current of VSI. The relation between i_d and i_{dc}^{m} is represented with gain (G), which is obtained by equating ac side and dc side powers of VSI. The product of average dc current and dc voltage is considered as power losses in the VSI. From Figure 3, the transfer function of $\boldsymbol{V}_{dc}/\boldsymbol{V}_{dc}^{*}$ is given as

$$\frac{\boldsymbol{V}_{dc}}{\boldsymbol{V}_{dc}^{*}} = \frac{\frac{G}{C_{dc}}k_P s + \frac{Gk_I}{C_{dc}}}{s^2 + \frac{G}{C_{dc}}k_P s + \frac{Gk_I}{C_{dc}}}, \tag{13}$$

where k_P and k_I are PI controller gains, C_{dc} is dc capacitor value, and $G = 3\mathbf{V}_m/2\boldsymbol{V}_{dc}^{*}$. By comparing the denominator of (13) with the general second-order system, the following relations are obtained.

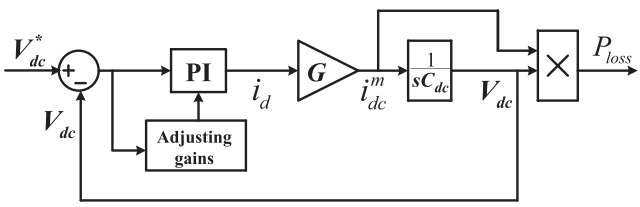


FIGURE 3 Block diagram of the adaptive PI controller

$$k_P = \frac{2\zeta\omega_n C_{dc}}{G}, \qquad k_I = \frac{\omega_n^2 C_{dc}}{G}, \qquad \text{where} \quad 0 < \zeta < 1. \tag{14}$$

In the proposed variable dc-link voltage control, corresponding to load operating point, $\boldsymbol{V}_{dc}^{*}$ changes so that PI controller gains (k_P and k_I) are updated. Therefore, the transient response during the variation of dc-link voltage is improved.

3 | SELECTION OF HYBRID DSTATCOM PARAMETERS

The design of parameters C_f, L_{f1}, C_r, and L_{fg} of the hybrid DSTATCOM shown in Figure 1 is discussed here. The design eliminates the extra ripple filter at PCC for smoothing PCC voltages. Also, the required effective interfacing inductance is reduced when compared with conventional methods.

3.1 | Design of series ac capacitor (C_f)

The series ac capacitor, C_f, is designed based on reactive power compensation. As a solution to avoid the occurrence of overcompensation, the capacitor value is designed corresponding to 25% of rated reactive power (Q_{rated}).[22,23] Therefore, the C_f value is

$$C_f = \frac{0.25Q_{rated}}{3\omega V_{pcc}^2}, \tag{15}$$

where $\omega = 2\pi f$ and V_{pcc} is the voltage at PCC. At higher frequencies, the impedance offered by the series ac capacitor (C_f) will be much lower. Therefore, C_f can be neglected during the design of remaining parameters (L_{f1}, C_r, and L_{fg}).

3.2 | VSI side interfacing inductor (L_{f1})

The VSI side interfacing inductor, L_{f1}, value is selected to provide sufficient rate of change of filter current in order to track reference filter current. The inductor dynamics is given as

$$L_{f1}\frac{di_{fa}}{dt} = -V_{C_f} - i_{fa}R_f + V_{dc}. \tag{16}$$

To simplify analysis, R_f is neglected. As the hysteresis current control is implemented for gate pulses generation, the switching frequency is not constant. However, to provide better tracking performance, the inductor value is designed at maximum switching frequency.[18] Therefore, from (16), the inductor value with this consideration is given as

$$L_{f1} = \frac{V_{dc}}{4hf_{sw,max}}, \tag{17}$$

where h is hysteresis band and its value is taken as $\pm$2% of rated filter current. $f_{sw,max}$ is the maximum switching frequency. In the proposed method, the reference dc-link voltage is varied as given in (12), however while designing inductor value the rated dc voltage is considered. The rated dc voltage in the hybrid DSTATCOM is considered as 600 V. Therefore, by substituting the values of rated dc voltage, h and $f_{sw,max}$=10 kHz in (17), the calculated inductor, L_{f1}, value is 7.5 mH. To restrict the maximum switching frequency less than 10 kHz, the L_{f1} value should be more than the calculated value. In the proposed hybrid DSTATCOM, grid side interfacing inductor (L_{fg}) supports to restrict the operating switching frequency less than 10 kHz, and its design is explained below.

3.3 | Grid side interfacing inductor (L_{fg})

In conventional methods, to eliminate switching frequency harmonics in PCC voltages, a ripple filter is connected at PCC.[17] But in the proposed hybrid DSTATCOM, the capacitor (C_r) in *LCL* circuit eliminates the switching frequency

harmonics and does not need of an additional ripple filter circuit. This can be possible only when the inductor (L_{fg}) value is low and less than (L_{f1}). For that, the L_{fg} value is obtained from the resonance frequency of the transfer function i_f/v_{inv}. From the dynamics of hybrid DSTATCOM shown in Figure 1,

$$\frac{i_f}{v_{inv}} = \frac{1 + sC_rR_d}{B_0s^3 + B_1s^2 + B_2s + B_3}, \tag{18}$$

where $B_0{=}L_{f1}L_{fg}C_r$,$B_1{=}R_{f1}C_rL_{fg}{+}L_{f1}C_rR_f{+}L_{f1}R_dC_r{+}R_dC_rL_{fg}$,$B_2{=}R_{f1}R_fC_r{+}R_fR_dC_r{+}R_dC_rR_{f1}C_f{+}L_{f1}{+}L_{fg}$,$B_3{=}R_{f1}{+}R_f$.

To simplify the analysis, the internal resistances R_{f1} and R_f are neglected. This is a valid assumption as resistance values are very small and their influence on stability of system is limited. If damping resistance, R_d, is not provided, the transfer function (18) becomes

$$\frac{i_f}{v_{inv}} = \frac{1}{L_{f1}L_{fg}C_rs^3 + (L_{f1} + L_{fg})s}. \tag{19}$$

Applying unity feedback control for (19) gives overall closed-loop system. In the closed-loop characteristic polynomial, s^2 term is missing, which infers the system is unstable according to Routh-Hurwitz stability criterion. Therefore, damping is compulsory to stabilize the system. The resonance frequency expression from (19) is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{L_{f1} + L_{fg}}{L_{f1}L_{fg}C_r}}. \tag{20}$$

In (20), the resonance frequency is selected based on higher order harmonic compensated by hybrid DSTATCOM. In this paper, the highest order harmonic to be compensated by DSTATCOM is selected as 41st order for 50 Hz supply system with consideration of 20% variation. As a trade-off between the above requirements, the value of C_r is chosen as 8 μF. The calculated L_{fg} value from (20), with above consideration, is 0.56 mH. The effect of different C_r values on frequency response plot is shown in Figure 4. It is observed that the resonance frequency increases with decreasing C_r value and results to allowing switching ripples to grid. Therefore, the selected C_r value (ie, 8 μF) is best suitable for compensation. The bode plot of *L*-filter and *LCL*-filter with different passive damping values is shown in Figure 5. The *LCL* filter introduces a resonant peak without damping resistor, which causes instability of the system. The resonant peak can be damped out by using passive damping resistor R_d in series with capacitor (C_r) as shown in Figure 1. It is observed that for increasing R_d value, the resonance peak reduced, and system becomes stable. For above the resonance frequency (ie, 41∗50=2050 Hz), the attenuation of switching frequency harmonics is high in *LCL*-filter when compared with *L*-filter. It is clear from Figure 5 that, for R_d=6Ω, no resonance peak occurs and attenuation of the signal is more after the resonance frequency. Therefore, damping resistance (R_d) value 6 Ω is chosen in this paper.

The hybrid DSTATCOM performance with above designed parameters and proposed algorithm is validated with the simulation and experimental studies in the next sections.

4 | SIMULATION STUDIES

The 3P4W split-capacitor hybrid DSTATCOM, shown in Figure 1, with the variable dc-link voltage scheme is simulated using MATLAB simulink. In simulation, two different loads are considered: one is three-phase diode bridge load, and another one is three-phase unbalanced linear load. The simulation parameters are given in Table 1.

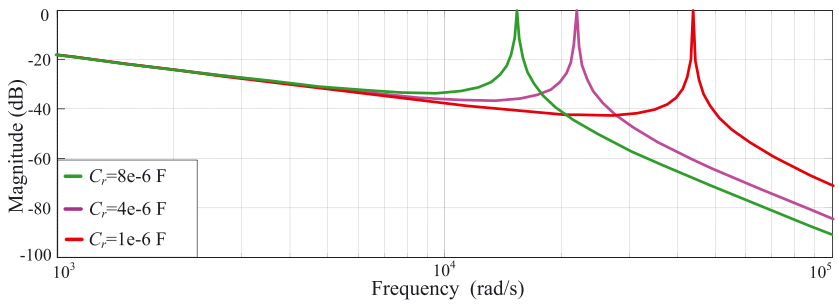


FIGURE 4 Bode plot for different C_r values when R_d=0Ω

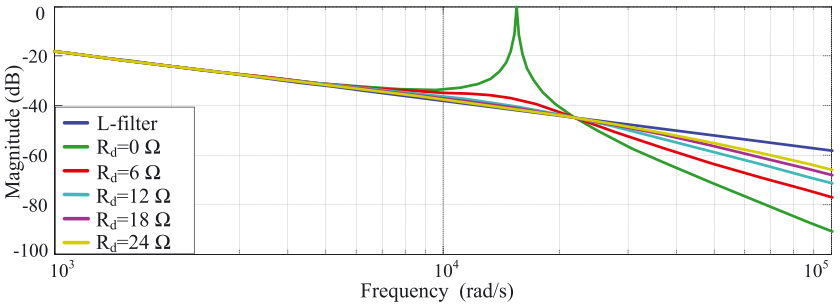


FIGURE 5 Bode plot for different R_d values when C_r=8μF

TABLE 1 Simulation parameters

Symbol	System Parameters	Values
V_s	Supply voltage	400 V, 50 Hz
L_{f1},L_{fg}	Interfacing inductances	7.5 mH, 0.5 mH
C_f	Series capacitor	60 μF
C_r	Resonance capacitor	8 μF
R_d	Damping resistor	6 Ω
C_{dc1},C_{dc2}	dc capacitance	2400 μF
Load-1	3-phase diode bridge and :	250 Ω, 300 mH
	unbalanced 3-ϕ linear load :	ph-*a*: 34 Ω, 150 mH, ph-*b*: 81 Ω,
		126 mH, ph-*c*: 31 Ω, 226 mH
Load-2	3-phase diode bridge and :	84 Ω, 52 mH
	unbalanced 3-ϕ linear load :	ph-*a*: 34 Ω, 150 mH, ph-*b*: 81 Ω,
		126 mH, ph-*c*: 31 Ω, 226 mH

The simulation results without and with compensation are shown in Figure 6. The PCC voltages are balanced and sinusoidal, which are shown in Figure 6A. Figure 6B shows three-phase source currents and neutral current. The DSTATCOM is not connected up to t=0.06 s; therefore, the source currents are non-sinusoidal and unbalanced, and neutral current flows. After DSTATCOM is connected at t=0.06 s, the compensation starts in one cycle, and source currents become balanced and sinusoidal, and neutral current reduced to zero. During this process, the filter currents injected by DSTATCOM are shown in Figure 6C. The dc-link voltages are shown in Figure 6D. It is observed that, initially, the dc-link capacitors are charged to 220 V. After DSTATCOM is connected at t=0.06 s, the dc-link capacitors are charged to 250 V. This voltage is sufficient for satisfactory compensation for a given load condition and is calculated from the proposed algorithm.

The simulation results of the proposed method during dynamic load variation are shown in Figure 7. The PCC voltages shown in Figure 7A are balanced and sinusoidal. The source currents and source side neutral current are shown in Figure 7B. It is observed that source currents are balanced and sinusoidal before and after load variation at t=0.22 s; therefore, the source side neutral current is also zero. The load currents for both load conditions are shown in Figure 7C. The filter currents injected by hybrid DSTATCOM during compensation for both load conditions are shown in Figure 7D. The required reference dc-link voltages for the operated loads are calculated from the proposed algorithm. The reference dc-link voltages for load-1 (ie, before t=0.22 s) and load-2 (ie, after t=0.22 s) are 250 and 300 V, respectively. The voltage across dc-link capacitors is maintained to these voltages with adaptive PI controller and are shown in Figure 7E.

The upper dc-link voltage, $\boldsymbol{V}_{dc1}$, with fixed PI controller and proposed adaptive PI controller are shown in Figure 8. The dc-link voltage magnitude is same in both methods up to t=0.22 s, because of same gains are considered for initial load. The load is changed at t=0.22 s, and then the dc-link voltages are changed to 300 V, which is the reference dc-link voltage calculated from the proposed algorithm. It is observed from Figure 8 that the dc-link voltage settles faster in the adaptive PI controller compared with fixed PI controller method, which indicates the improvisation in the transient response of dc-link voltage.

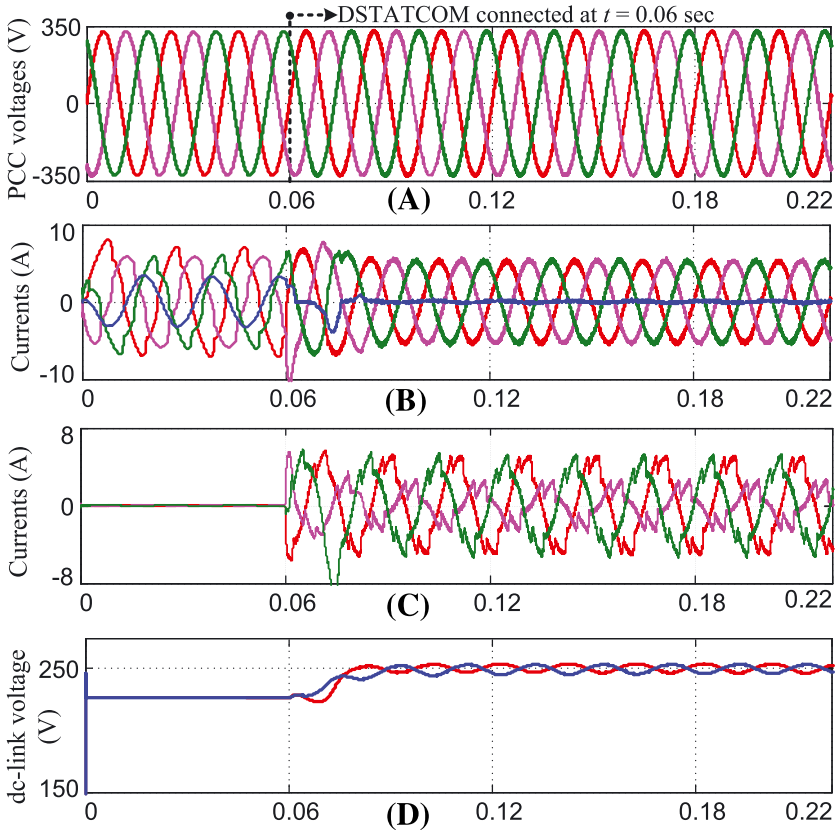


FIGURE 6 Simulation results of the proposed method for DSTATCOM connected at t=0.06 s

The simulation waveforms of PCC voltages for conventional[14] and proposed hybrid DSTATCOM with non-stiff voltage source are shown in Figure 9A,B, respectively. In both methods, the DSTATCOM is operated at t=0.06 s. It is observed from Figure 9A that up to t=0.06 s, the PCC voltages are distorted and non-sinusoidal. After t=0.06 s, the PCC voltages become sinusoidal but have switching frequency component. To minimize these switching frequency components, a ripple filter is used in conventional method, which increases the cost and makes the system bulky. But, in proposed hybrid DSTATCOM without ripple filter, the PCC voltages become sinusoidal and balanced as shown in Figure 9B.

The source current THDs comparison of the proposed variable dc-link voltage control hybrid DSTATCOM with other conventional methods for load-1 and load-2 is mentioned in Table 2. The source current THDs in proposed method is less when compared with other conventional methods because the optimum dc-link is maintained corresponding to load condition.

The comparison of the proposed hybrid DSTATCOM with other topologies in terms of voltage requirement, VSI rating, and cost is mentioned in Table 3. The proposed variable dc-link voltage of hybrid DSTATCOM costs less, because of lower rating IGBT switches are sufficient to achieve compensation. The C_r filter voltage rating, which has been used to eliminate switching frequency components, is less in the proposed method when compared with conventional filter (ie, called ripple filter). Because, in conventional topologies, filter is connected at PCC point, therefore, the voltage rating should be greater than PCC voltage. As the dc-link voltage is reduced in the proposed method, the switching loss is reduced when compared with conventional methods.

However, more filter components are present in the proposed method, but the loss component is only in passive damping resistor. In industrial applications, the method with the minimum number of sensors with least complex algorithm will be preferred. Therefore, the passive damping method is suitable while accepting the passive damping power loss.

The rms current (I_d) flowing through the damping resistor in the proposed method for given loads is shown in Figure 10. It is observed that the rms values of damping current for load-1 and load-2 are 0.58 A and 0.64 A, respectively. Then the calculated damping losses (P_d) are given as

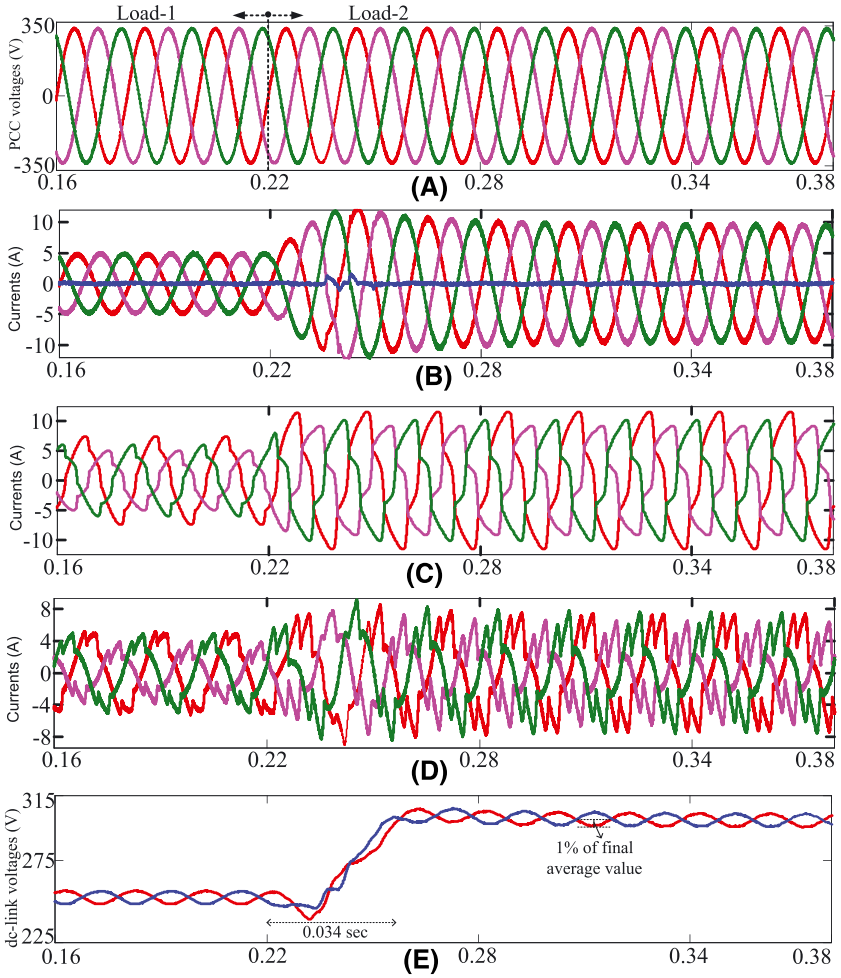


FIGURE 7 Simulation results of the proposed algorithm during dynamic load variation at t=0.22 s

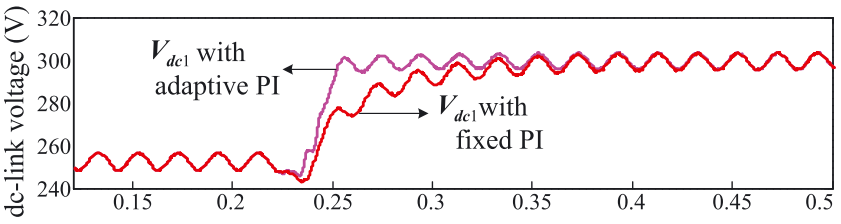


FIGURE 8 Dynamics of upper dc-link voltage waveforms with fixed PI and adaptive PI control methods

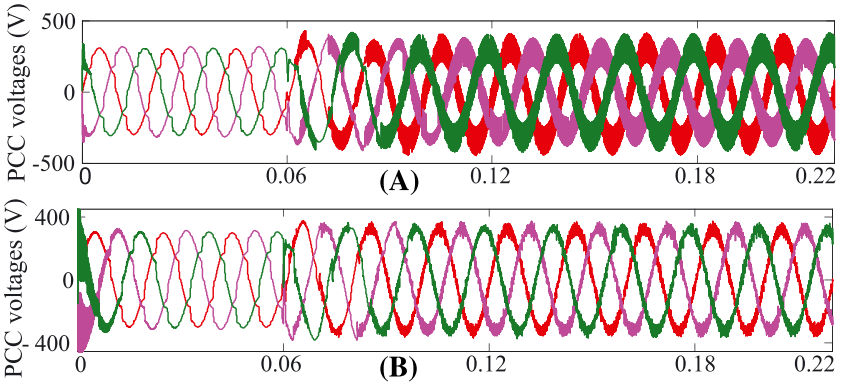


FIGURE 9 PCC voltages for non-stiff voltage source without ripple filter: (A) conventional method and (B) proposed method

TABLE 2 Comparison of %THD of source currents

Type of Filter	Load-1			Load-2		
	i_{sa}	i_{sb}	i_{sc}	i_{sa}	i_{sb}	i_{sc}
Without filter	8.54	10.4	11.1	14.2	15.4	16.9
L-filter DSTATCOM[11]	3.87	3.94	3.8	2.33	2.36	2.32
Hybrid DSTATCOM[10]	3.61	3.05	3.15	1.98	2.2	2.31
Proposed method	3.16	2.83	2.4	1.2	1.83	1.9

TABLE 3 Comparison of different DSTATCOM topologies

Parameter	*L*-filter DSTATCOM[11]	Hybrid DSTATCOM[10]	Proposed Method
DC-link voltage	1200 V	680 V	600 V
VSI rating[a]	15 kVA	8.5 kVA	7.5 kVA
Inductor values	26 mH	26 mH	7.5 mH, 0.5 mH
Ripple filter	Required	Required	Not required
Cost	High	Low	Very low

The rated filter current is 10 A.

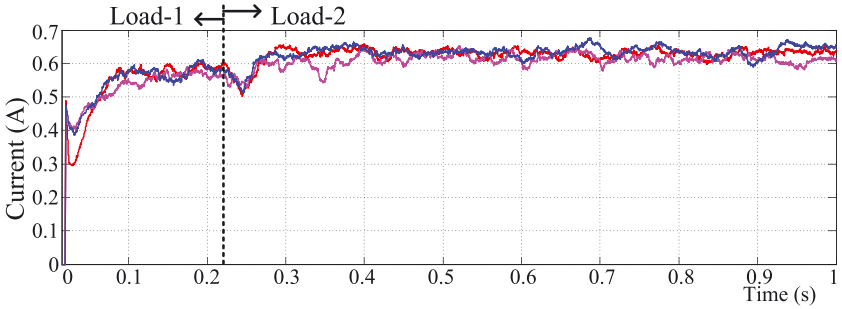


FIGURE 10 Damping rms current (I_d) flowing in damping resistor

$$\begin{aligned} P_d &= 3I_d^2 R_d \\ &= 3 \times 0.58^2 \times 6 = 6.05 \quad \text{W} \qquad \text{(for load -1)} \\ &= 3 \times 0.64^2 \times 6 = 7.37 \quad \text{W} \qquad \text{(for load -2).} \end{aligned} \tag{21}$$

The DC-link voltage, switching loss, and damping loss for different topologies under stiff and non-stiff source conditions are given in Table 4. In conventional topologies (L-filter and LC-filter), for the case of non-stiff source, an extra ripple filter is connected at PCC to minimize the PCC voltage ripple. Therefore, damping loss takes place in damping resistor of the ripple filter. The overall loss (switching loss plus damping loss) in the proposed method and conventional topologies are calculated and are given in Table 4. It is observed from Table 4 that the overall loss in the proposed method is less when compared with conventional methods.

5 | EXPERIMENTAL STUDIES

The performance of the proposed method is verified with experimental studies for reduced voltage of 100 V. dSPACE MicroLabBox DS-1202 has been used to implement the control algorithm of the proposed method. The main experimental components to implement the experiment setup and there specification are given in Table 5. The variable dc-link voltage control of hybrid DSTATCOM have been tested for reactive power compensation, source current balancing,

TABLE 4 Comparison of overall loss in conventional and proposed methods

Cases	Topology	DC-link Voltage, V		Switching Loss, W		Damping Loss, W		Overall Loss, W	
		Load-1	Load-2	Load-1	Load-2	Load-1	Load-2	Load-1	Load-2
	L-filter	1100	1100	74	95	-	-	74	95
Stiff source	LCL-filter	1040	1040	69.5	88.5	7	7.5	76.5	96
	LC-filter	340	340	42	55	-	-	42	55
	L-filter	1100	1100	74	95	11.6	10	85.6	105
Non-stiff source[a]	LCL-filter	1040	1040	69.5	88.5	7	7.5	76.5	96
	LC-filter	340	340	42	55	9.3	9	51.3	64
Both cases (stiff	Proposed	250	300	28	46	6	7.37	34	53.37
and non-stiff sources)									
% reduction w.r.t									
LC-filter (in case of	Proposed	26.4	11.7	33.3	16.3	35.5	18.1	33.7	16.6
non-stiff source)									

In case of non-stiff source, the L-filter and LC-filter based topologies are required an extra ripple filter at PCC to minimize voltage ripple, so damping losses are present.

TABLE 5 Experimental components and specifications

Circuit	Component	Specification Type
Sensing devices	Voltage transducer	LEM LV 25-P
	Current transducer	LEM LA 55-P
Controller	dSPACE MicroLabBox	DS 1202, FPGA
	Sampling time (T_s)	based controller 30 μs
VSI circuit	IGBT with anti-parallel diode	SKM 75GB123D
	DC-link capacitors	Electrolyte 1200 V, 4400 μF
±15 V dc power supply	Diode bridge, Capacitors	IN4007, Electrolyte 2000 μF
	Regulator (ICs)	7815,7915
Driver circuit	IC's	Opto-isolator 3120
Waveforms capturing	Mixed signal oscilloscopes	Tektronix-2014B,
device	(MSO)	100 MHz, 1GS/s
THD measurement	Power quality analyzer	FLUKE-435 II series

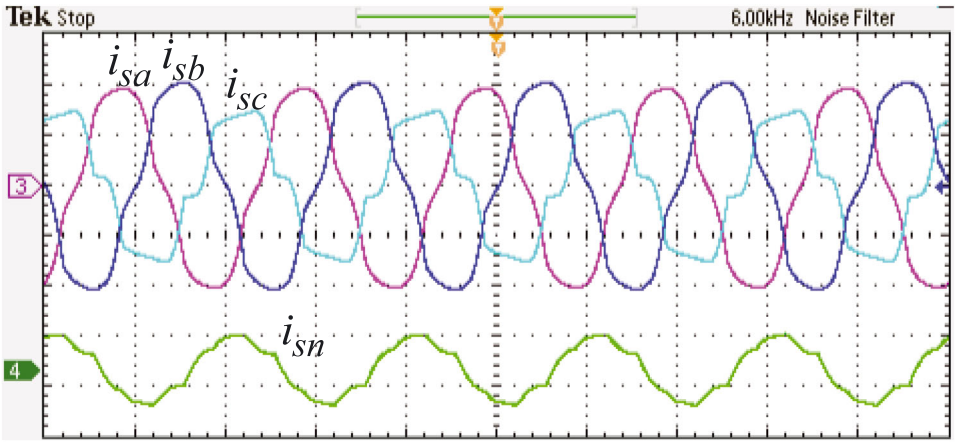


FIGURE 11 Three-phase source currents (i_{sa},i_{sb},i_{sc}) and source side neutral current (i_{sn}) before compensation (voltage, 100 V/div; currents, 4 A/div)

and harmonic mitigation in the presence of three-phase diode bridge load (load-1) and three-phase unbalanced load (load-2).

The three-phase source currents and source side neutral current before compensation are shown in Figure 11. It is observed that, before compensation, the source currents are unbalanced and non-sinusoidal, and therefore, the neutral

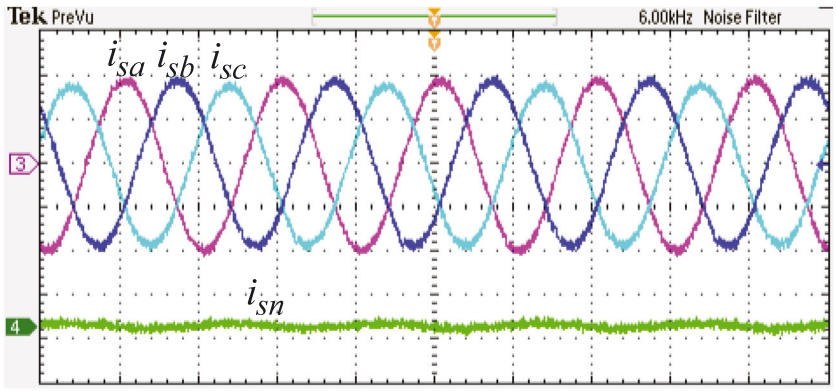


FIGURE 12 Three-phase source currents (i_{sa},i_{sb},i_{sc}) and source side neutral current (i_{sn}) after compensation (voltage, 100 V/div; currents, 4 A/div)

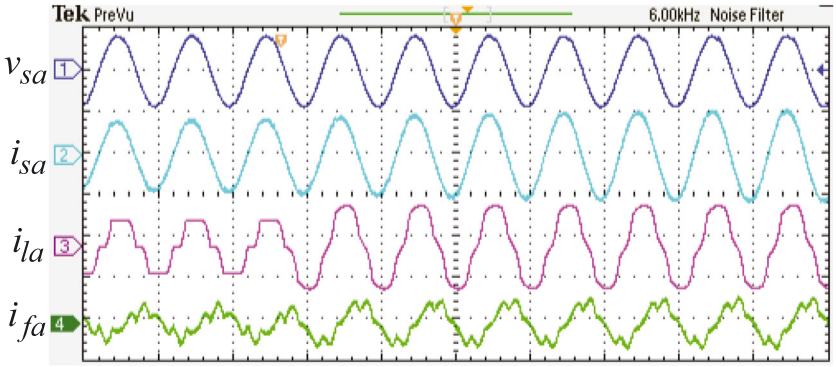


FIGURE 13 Source voltage (v_{sa}), source current (i_{sa}), load current (i_{la}), and filter current (i_{fa}) of phase-*a* for load variation (voltage, 100 V/div; currents, 4 A/div)

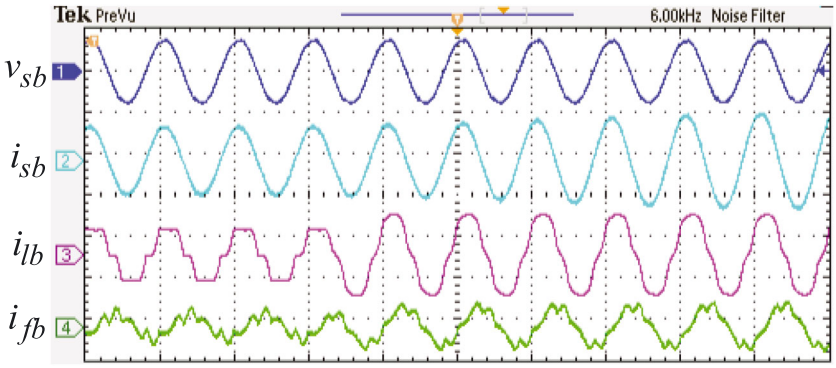


FIGURE 14 Source voltage (v_{sb}), source current (i_{sb}), load current (i_{lb}), and filter current (i_{fb}) of phase-*b* for load variation (voltage, 100 V/div; currents, 4 A/div)

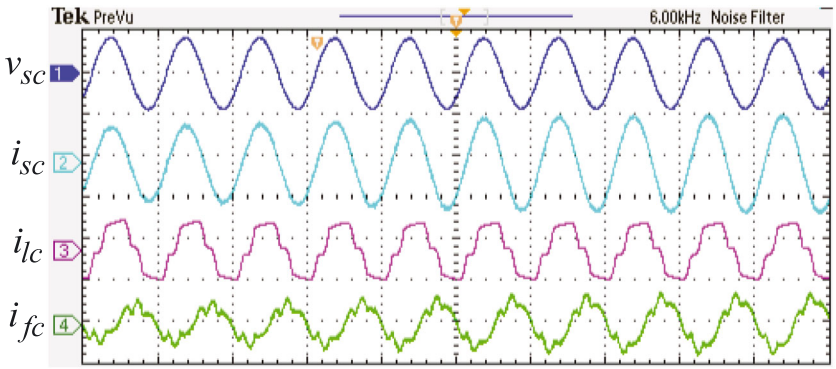
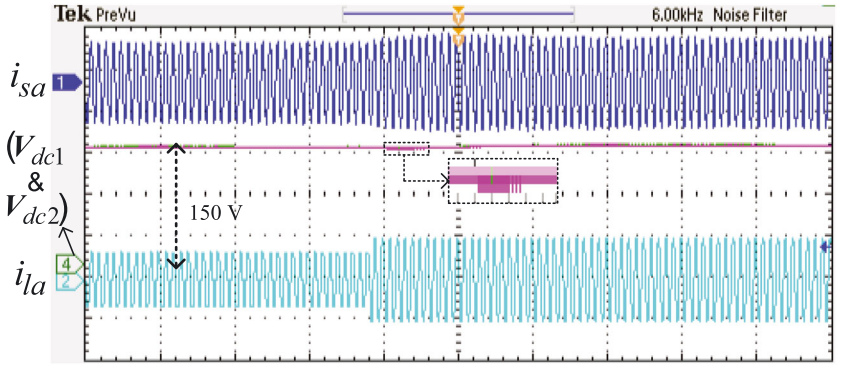
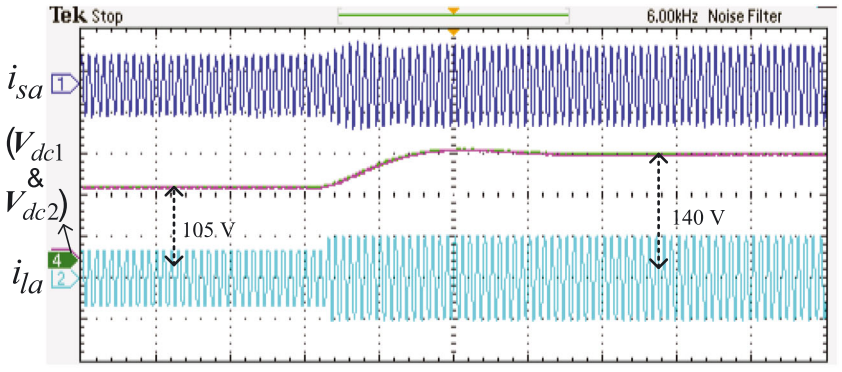


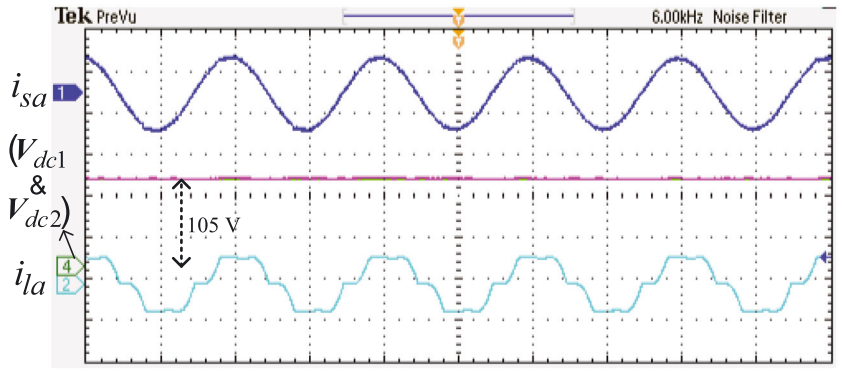
FIGURE 15 Source voltage (v_{sc}), source current (i_{sc}), load current (i_{lc}), and filter current (i_{fc}) of phase-*c* for load variation (voltage, 100 V/div; currents, 4 A/div)

current exists. Three-phase source currents and source side neutral current after compensation are shown in Figure 12. It is observed that the source currents become sinusoidal and balanced, and therefore, source side neutral current becomes zero.

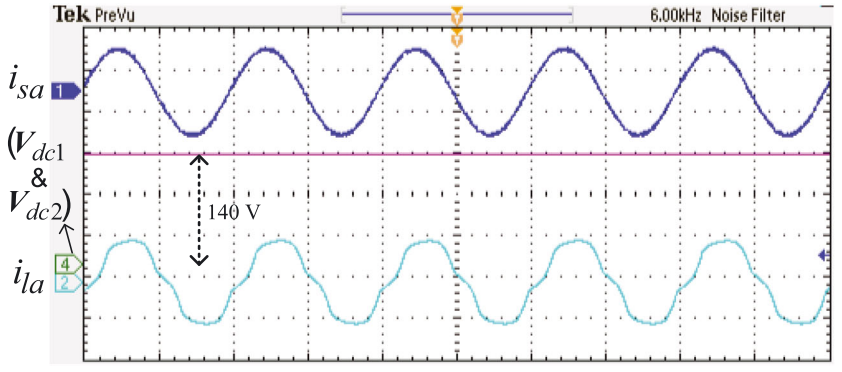




(A)



(B)



(C)

FIGURE 16 Experimental waveforms in conventional method for load variation (voltage, 50 V/div; currents, 4 A/div)

FIGURE 17 (A) Experimental waveforms in proposed method. (B, C) Zoomed waveforms during load-1 and load-2, respectively (voltage, 50 V/div; currents, 4 A/div)

The phase *a*, *b*, and *c* source voltage (v_{sa}, v_{sb}, v_{sc}), source current (i_{sa}, i_{sb}, i_{sc}), load current (i_{la}, i_{lb}, i_{lc}), and filter current (i_{fa}, i_{fb}, i_{fc}) are shown in Figures 13, 14, and 15, respectively. It is observed that the compensation will not affect even if load is varied. The source current is sinusoidal and in-phase with corresponding source voltage.

The source current (i_{sa}), load current (i_{la}), and dc-link voltages ($\boldsymbol{V}_{dc1}$ and $\boldsymbol{V}_{dc2}$) in conventional method are shown in Figure 16. It is observed that the dc-link voltages are maintained to 150 V (1.6 times of peak of PCC voltage with consideration of 5% voltage variation). A small dip in the dc-link voltage is observed, which is shown in zoomed part. The reason for that is the energy stored in dc-link capacitor is discharged at the instant of load increased; however, it is recovered to 150 V because of dc-link voltage regulation with PI controller. The voltage stress across switches and switching losses are more in fixed dc-link voltage regulation, because of constant dc-link voltage for any load condition.

The above disadvantage is minimized by implementing variable dc-link voltage regulation. The experimental results, source current (i_{sa}), load current (i_{la}), and dc-link voltages ($\boldsymbol{V}_{dc1}$ and $\boldsymbol{V}_{dc2}$) with variable dc-link voltage regulation are shown in Figure 17A. It is observed that the dc-link voltage for load-1 (105 V) and for load-2 (140 V) are maintained; these values are calculated from the proposed method as discussed in Section 2. The zoomed figures during load-1 and load-2 are shown in Figure 17B,C, respectively. It is observed that the compensation performance is satisfactory (ie, source current becomes sinusoidal) even though dc-link voltages 105 and 140 V for load-1 and load-2 are maintained, respectively. Therefore, the voltage stress and switching losses are minimized during these load conditions compared with conventional fixed dc-link voltage method (ie, with 150 V).

The experimental results with fixed PI control and adaptive PI control dc-link voltage regulation are shown in Figures 18 and 19, respectively. It is observed from Figure 18 that, in fixed PI control method, during load variation, the dc voltages settling time is 0.46 s. And also, the transient response is oscillating. In the proposed adaptive PI control as shown in Figure 19, the settle time during load variation is reduced to 0.28 s and also no oscillation during transient period. The reduction in settling time of dc-link voltages and no oscillations in dc-link voltages has improved the compensation performance of the source current.

The harmonic spectrum and phasor diagram of source currents before and after compensation for load-2 are shown in Figure 20. It is observed from Figure 20A that the THDs of three-phase source currents before compensation are 13.2%, 12.9%, and 19.6%. The source current phasors lag respective voltage phasors by −30°, −29° and −34°, which are shown in Figure 20B. After compensation, the three-phase source current THDs are reduced to 2.7%, 2.8%, and 3.0% as shown in Figure 20C. The three-phase source current phasors lag respective voltage phasors by −3°, −3°, and

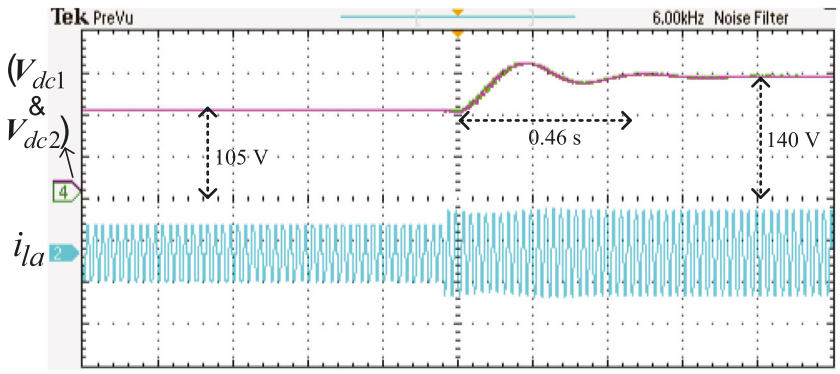


FIGURE 18 DC-link voltages ($\boldsymbol{V}_{dc1}$ and $\boldsymbol{V}_{dc2}$) and load current (i_{la}) with fixed PI controller method (voltage, 50 V/div; currents, 4 A/div; time, 200 ms/div)

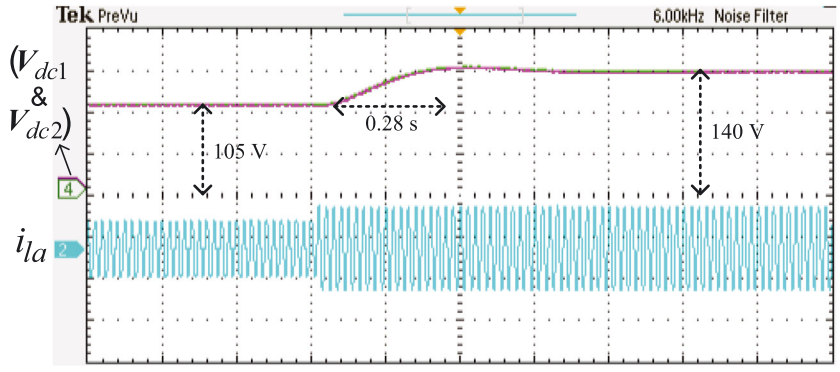


FIGURE 19 DC-link voltages ($\boldsymbol{V}_{dc1}$ and $\boldsymbol{V}_{dc2}$) and load current (i_{la}) with adaptive PI controller for proposed method (voltage, 50 V/div; currents, 4 A/div; time, 200 ms/div)

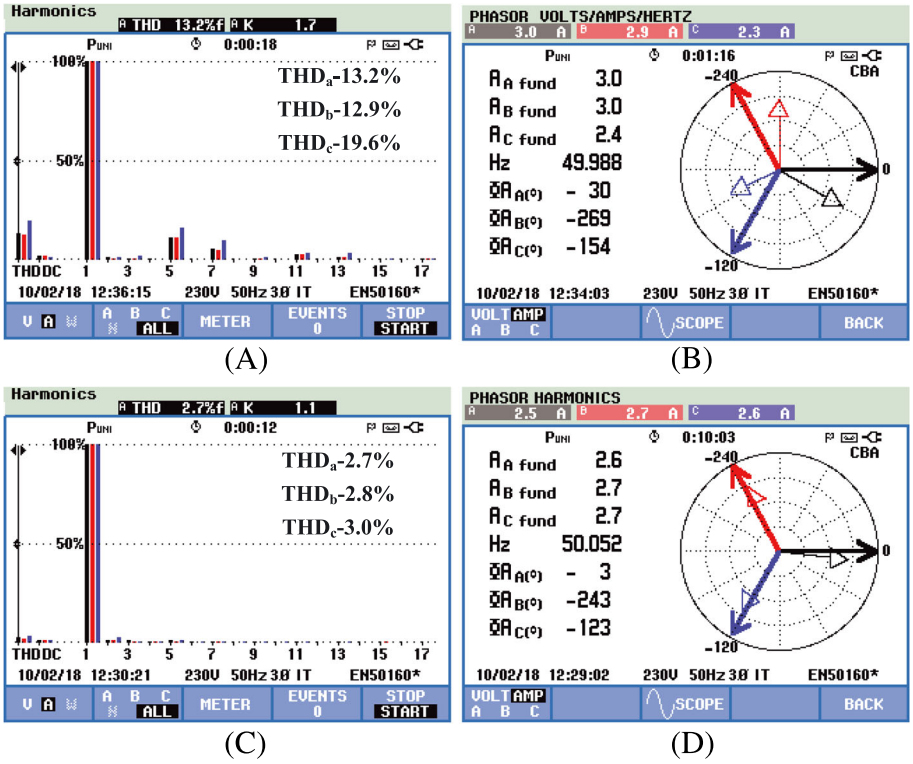


FIGURE 20 (A, B) Harmonic spectrum of source currents and phasor diagram before compensation; (C, D) harmonic spectrum of source currents and phasor diagram after compensation

−3° as shown in Figure 20D. This indicates that, after compensation, almost unity power factor is achieved on source side, and source currents THDs are within specified limit (below 5% according to IEEE-519 standards).

6 | CONCLUSION

In this paper, a hybrid DSTATCOM with adaptive dc-link voltage control is proposed to compensate unbalanced and nonlinear loads in 3P4W distribution system. The performance of the proposed method for reactive power compensation, load current balancing, harmonic mitigation, neutral current compensation, and dc-link voltage regulation is demonstrated through simulation and experimental studies. The advantages of the proposed method are as follows:

1. The overall coupling inductance value required is less when compared with conventional method, and therefore, voltage drop across coupling inductor is reduced. This leads to reduction of the dc-link voltage requirement.
2. Sufficient dc-link voltage is maintained corresponding to the operating load condition such that the voltage stress across switches is reduced. It leads to minimization of the switching losses.
3. The proper design of hybrid DSTATCOM parameters eliminates the ripple filter requirement.
4. Transient performance of the dc-link voltage is improved.

ORCID

Siva Kumar Ganjikunta https://orcid.org/0000-0001-5512-5669

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