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Model predictive control with constant switching frequency for four-leg DSTATCOM using three-dimensional space vector modulation

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Abstract: In this study, model predictive control (MPC) with constant switching frequency is proposed for four-leg distribution static compensator (FL-DSTATCOM) to compensate the current related power quality issues. MPC techniques having many advantages compared to conventional pulse width modulation and hysteresis control techniques. In MPC, the future behaviour of the controlled variable is predicted using the model of the system and a cost function is formed using reference and predicted variable. MPC for DSTATCOM applications consider the difference between the reference and actual DSTATCOM current as a cost function and selects the switching state which minimises the cost function. However, while using MPC, the switches of DSTATCOM operate in variable switching frequency and sometimes the values are also very high. Due to this reason higher switching losses, unequal stress appear across the inverter switches and it also reduces the lifetime of the switch. Therefore, in this study, the concept of three-dimensional space vector modulation is adopted to achieve a constant and user-defined switching frequency MPC for FL-DSTATCOM to conquer the limitations of conventional variable switching frequency MPC. The validation of the proposed work is achieved using simulation and experimental studies.

1 Introduction

In a distribution system, custom power devices (CPDs) are used to compensate the power quality issues [1, 2]. Distribution static compensator (DSTATCOM) is a shunt connected CPD, which is mainly dedicated to address current related power quality issues [3, 4]. Among the available DSTATCOM topologies, three H-bridge (HB), three-leg voltage source inverter (VSI), three-phase split-capacitor (TPSC), four-leg DSTATCOM (FL-DSTATCOM) and multi-level inverter (MLI) topologies are treated as traditional topologies [5–10]. Three single-phase HB inverters are used to implement a three HB DSTATCOM, which can be applicable to both three-phase three wire (3P3W) and three-phase four wire (3P4W) systems. However, the limitations of this topology are the requirement of a higher number of switching devices and coupling transformers, which will increase the size and cost of the DSTATCOM [7–9]. A three-leg VSI-based DSTATCOM has fewer switching devices and does not require any coupling transformers. However, this topology is not suitable for 3P4W systems due to the absence of a neutral conductor [10–12]. The structure of TPSC topology is the same as for three-leg topology except for the number of capacitors in its dc link. The dc link of three-leg DSTATCOM consists of only one capacitor whereas, the dc link of TPSC topology consists of two capacitors. The mid-point of the dc link is connected to the neutral conductor so that it is suitable for both 3P3W and 3P4W systems [13–15]. The limitation of TPSC topology is that there is unequal voltage sharing of dc link capacitors during the transient operation of non-linear and unbalanced loads and the system also require higher dc link voltage [7, 8]. MLI-based DSTATCOM topologies are an attractive solution for voltages greater than 2.3 kV. However, in the secondary distribution system (voltages less than 2.3 kV), usage of MLI for DSTATCOM applications is not a cost-effective option. This is because, it requires more number of switches and higher control complexity compared to the two-level inverter [16, 17]. Finally, FL-DSTATCOM is suitable for both 3P3W and 3P4W systems, however, it requires two additional switches compared to three-leg and TPSC DSTATCOM. The other advantages of this topology are better controllability, simple structure, easy control and the absence of capacitor voltage balancing problem unlike TPSC topology [7, 18, 19]. Therefore, FL-DSTATCOM is the best suited topology to compensate for the power quality issues in 3P4W distribution system.

Over the past few decades, pulse width modulation (PWM) and hysteresis control techniques are considered as conventional pulse generation techniques for the inverter switches of DSTATCOM [12, 14]. However, the limitation of the PWM controller include the design of controller parameters and frequency of reference current [20]. Because of the interaction between phases, the current error in hysteresis controllers is not restricted to the hysteresis band limits. At the same time, the dependency of switching frequency on load parameters and operating conditions are leading to higher switching frequencies which increases the switching losses [20]. The advantages of model predictive control (MPC) such as the convenience of adding additional control parameters and their treatment according to the importance, elimination of proportional and integral (PI) controllers, good transient and steady-state performance have attracted the attention of researchers to using MPC techniques over PWM and hysteresis controllers for DSTATCOM applications [11, 15, 21, 22]. The continuous progress of MPC techniques to the DSTATCOM applications and the reason to go for constant switching MPC for FL-DSTATCOM is explained as follows.

A single-phase shunt active filter is controlled using MPC to compensate for reactive and harmonic currents. However, most of the industries use three-phase supply which makes it a non-viable option for industrial applications [23]. Predictive control of a three-leg DSTATOM is proposed to compensate for reactive power [24]. This method is only compensating the reactive power so that it cannot compensate the harmonic currents. MPC is applied to a three-leg DSTATCOM to improve the power factor and to reduce the harmonic distortion [11]. Modelling and simulation of three-leg VSI-based DSTATCOM is proposed and is implemented in alpha–beta frame [25]. However, the proposed method is unable to tackle the problem of unbalanced currents because of which its applications are restricted for 3P3W systems. Predictive control of a TPSC DSTATCOM is proposed to compensate for current related power quality issues in 3P4W distribution system [15]. However, this method suffers from issues of with variable switching

frequency and it is also having the problem of capacitor voltage balancing during compensation of heavier unbalanced load current [13]. The same methodology is extended to an FL-DSTATCOM which is based on FPGA to compensate the reactive, harmonic and unbalanced load currents [20]. The absence of modulator in this control algorithm makes it as a variable switching frequency control technique and this topology also suffers from the higher neutral switching frequency. MPC of four-leg inverter is proposed in [26, 27] which will track the reference currents. However, the switches of the inverter operate with variable switching frequency. The other limitations of variable switching frequency are higher switching losses, the high value of interfacing inductor because they are designed by considering maximum switching frequency, filter design and also uneven stress on inverter switches [28], similarly, the limitation of FL-DSTATCOM is higher neutral leg switching frequency [28].

To achieve constant switching frequency MPC for DSTATCOM applications, a new technique is developed using conventional space vector modulation (SVM) to overcome the variable switching frequency limitation of three-leg VSI [29]. However, the adopted SVM technique cannot be extended to an FL-DSTATCOM and the three-leg DSTATCOM topology cannot compensate for the imbalance in load currents. This is because, the number of possible switching states is eight for a three-leg inverter [11] where the number of possible switching states is 16 for an FL-DSTATCOM [20, 26, 27]. The phase voltages of FL-DSTATCOM are not decoupled unlike TPSC topology, which provides an opportunity to incorporate the concept of three-dimensional space vector modulation (3DSVM) with MPC to achieve constant switching frequency. Therefore, in this paper, MPC is applied to FL-DSTATCOM based on the concept of 3DSVM [30–32], to compensate for power quality issues and to operate the inverter of DSTATCOM at a constant frequency.

This paper is organised as follows. The proposed 3DSVM-based control algorithm is presented in Section 2, followed by simulation and experimental results in Sections 3 and 4, respectively. Finally, Section 5 concludes the proposed work.

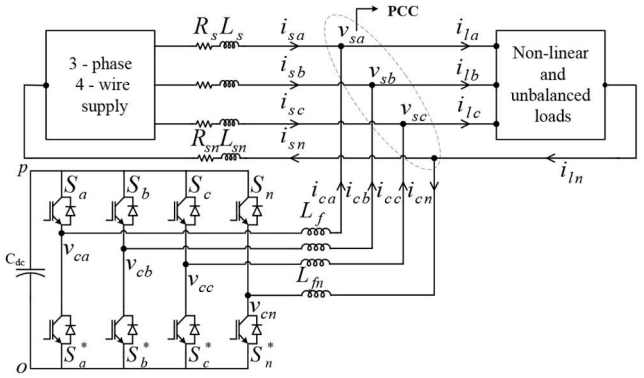


Fig. 1 *Schematic diagram of FL-DSTATCOM connected distribution system*

2 MPC algorithm with constant switching frequency

A four-leg inverter is used to implement the FL-DSTATCOM and the schematic diagram of the FL-DSTATCOM connected to a distribution system is shown in Fig. 1. The inverter topology of FL-DSTATCOM consists of eight switches and they are arranged as four legs. The mid-point of each leg is connected to the point of common coupling (PCC) through the interfacing inductor which reduces the switching harmonics in FL-DSTATCOM currents. A detailed explanation of the design of the proposed control algorithm is provided in Sections 2.1–2.3. Section 2.1, explains about the reference current generation using SRF theory [15, 33]. In Section 2.2 predictive model of FL-DSTATCOM is explained. Finally, constant switching frequency MPC with 3DSVM is explained in Section 2.3.

2.1 Reference current extraction using SRF theory

The implementation of SRF theory [15, 33] requires various parameters such as load currents (i_{labc}), DSTATCOM currents (i_{cabc}), voltages at PCC (v_{sabc}) and dc link voltage (V_{dc}). Fig. 2 shows the pictorial representation of SRF theory along with switching pulse generation using 3DSVM-based MPC.

The main objective of using SRF theory is the extraction of reference DSTATCOM currents from non-linear and unbalanced load currents. Initially, the detected load currents are converted from *abc* frame to *dq* frame using Parks transformation and it requires the information of ωt, which is obtained from a three-phase phase locked loop (PLL). The input for the PLL is sensed PCC voltages and the output is ωt

$$\begin{bmatrix} i_{ld} \\ i_{lq} \\ i_{l0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\omega t & -\sin\omega t & 0.5 \\ \cos\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & 0.5 \\ \cos\left(\omega t + \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) & 0.5 \end{bmatrix} \begin{bmatrix} i_{la} \\ i_{lb} \\ i_{lc} \end{bmatrix}. \quad (1)$$

The extracted *dq* current components are the combination of fundamental and ripple currents

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld}; i_{lq} = \bar{i}_{lq} + \tilde{i}_{lq}. \quad (2)$$

To achieve balanced and sinusoidal source currents, the supply has to send fundamental active component of load current. Therefore a low pass filter is used to eliminate the oscillating component ($\tilde{i}_{ld}$) from the active component of load current so that the remaining active component of current ($\bar{i}_{ld}$) will become part of the reference source current. In general, DSTATCOM requires an active component of load current (i_{dc}) to maintain a constant voltage across the dc link, failing which the dc bus voltage will collapse [15, 33]. As shown in Fig. 2, the variation between the reference and measured dc link voltage is passed through a PI controller and

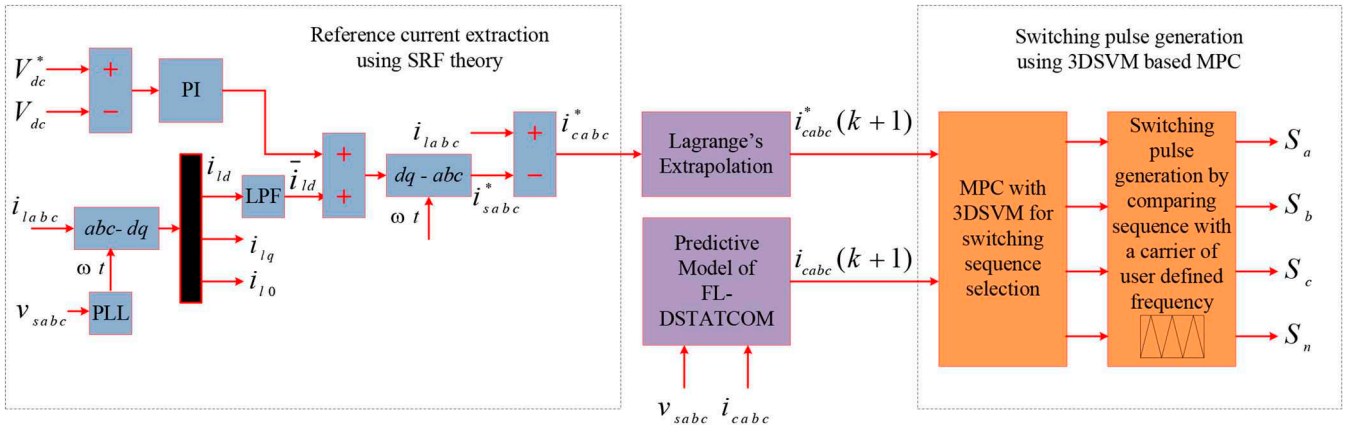


Fig. 2 *Reference current extraction and switching pulse generation*

the resulting output of it is added to the $\bar{i}_{ld}$ to get the amplitude of total reference source current

$$I^*_{sm} = \bar{i}_{ld} + i_{\mathrm{dc}}\,. \tag{3}$$

Further, inverse Parks transformation with I^*_{sm} as input is used to estimate the reference source currents (i^*_{sabc})

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t & 1 \\ \cos\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\omega t + \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} I^*_{sm} \\ 0 \\ 0 \end{bmatrix}. \tag{4}$$

Finally, the difference between the load currents (i_{labc}) and reference source currents (i^*_{sabc}) will be considered as the required reference DSTATCOM currents (i^*_{ca}, i^*_{cb} and i^*_{cc}) for the implementation of MPC

$$i^*_{ca} = i_{la} - i^*_{sa}; \quad i^*_{cb} = i_{lb} - i^*_{sb}; \quad i^*_{cc} = i_{lc} - i^*_{sc}\,. \tag{5}$$

2.2 Conventional predictive model of FL-DSTATCOM

In conventional MPC, a cost function is formed using reference and predicted variables. Then a switching state is selected from the available switching states, which minimise the considered cost function [11, 15, 21, 22]. The primary objective of the proposed work is to maintain source currents balanced, sinusoidal and in-phase with the voltage at PCC. Therefore, the cost function is considered as the difference between reference (i^*_{cabc}) and actual DSTATCOM currents (i_{cabc}). As mentioned in the previous section, SRF theory is used to extract the reference DSTATCOM currents ($i^*_{cabc}(k)$) while the reference currents at $(k+1)$th state are obtained by applying second-order Lagrange's extrapolation to the currents obtained from SRF theory [26, 27]

$$i^*_{cabc}(k+1) = 3i^*_{cabc}(k) - 3i^*_{cabc}(k-1) + i^*_{cabc}(k-2)\,. \tag{6}$$

Similarly, the model of the DSTATCOM is used to predict the actual currents at $(k+1)$th state (i.e. $i_{cabc}(k+1)$). The prediction of $i_{cabc}(k+1)$ starts by applying KVL between the nodes v_c and v_s in Fig. 1 [26, 27]

$$\begin{aligned} v_{can} &= L_f \frac{\mathrm{d}i_{ca}}{\mathrm{d}t} + v_{sa}; \\ v_{cbn} &= L_f \frac{\mathrm{d}i_{cb}}{\mathrm{d}t} + v_{sb}; \\ v_{ccn} &= L_f \frac{\mathrm{d}i_{cc}}{\mathrm{d}t} + v_{sc}\,. \end{aligned} \tag{7}$$

In the above equation, v_{can}, v_{cbn} and v_{ccn} represent the inverter output voltage which is measured with respect to the mid-point of the fourth leg and it is completely dependent on switching states of the inverter. Switching states and their respective normalised voltages are given in Table 1. Similarly, v_{sa}, v_{sb} and v_{sc} represent the voltage of each phase at PCC which is measured with respect to neutral line. Solving (7) for DSTATCOM current gives us:

$$\begin{aligned} \frac{\mathrm{d}i_{ca}}{\mathrm{d}t} &= \frac{v_{can} - v_{sa}}{L_f} \\ \frac{\mathrm{d}i_{cb}}{\mathrm{d}t} &= \frac{v_{cbn} - v_{sb}}{L_f}\,. \\ \frac{\mathrm{d}i_{cc}}{\mathrm{d}t} &= \frac{v_{ccn} - v_{sc}}{L_f}\,. \end{aligned} \tag{8}$$

According to forward Euler's approximation method [26, 27]

$$\frac{\mathrm{d}i_c}{\mathrm{d}t} = \frac{i_c(k+1) - i_c(k)}{T_s}\,. \tag{9}$$

where T_s is the sampling time. Substitute (9) in (8) to get the DSTATCOM currents at $(k+1)$th state. Therefore

$$\begin{aligned} i_{ca}(k+1) &= \frac{(v_{can} - v_{sa})T_s}{L_f} + i_{ca}(k); \\ i_{cb}(k+1) &= \frac{(v_{cbn} - v_{sb})T_s}{L_f} + i_{cb}(k); \\ i_{cc}(k+1) &= \frac{(v_{ccn} - v_{sc})T_s}{L_f} + i_{cc}(k)\,. \end{aligned} \tag{10}$$

As mentioned, in conventional MPC [20, 26, 27], the cost function is the variation between reference and actual DSTATCOM currents and it is expressed as (11)

$$\begin{aligned} C = {} & \left|i^*_{ca}(k+1) - i_{ca}(k+1)\right| + \\ & \left|i^*_{cb}(k+1) - i_{cb}(k+1)\right| + \\ & \left|i^*_{cc}(k+1) - i_{cc}(k+1)\right|. \end{aligned} \tag{11}$$

For each switching state, the values of $i_{ca}(k+1)$, $i_{cb}(k+1)$, and $i_{cb}(k+1)$ are determined using (10) and calculate the cost function value using (11). Among the available switching states, the state which gives the minimum value of C is applied for the next sampling to achieve proper control of FL-DSTATCOM. Using this method, the switches of the FL-DSTATCOM will operate at variable switching frequency [20]. To overcome this limitation a constant and user-defined switching frequency MPC is proposed in this paper and explained in the following section.

2.3 Proposed MPC with 3DSVM to generate constant switching frequency gate pulses

In the proposed work, the concept of 3DSVM [30–32] is adopted to implement the constant and user-defined switching frequency MPC for FL-DSTATCOM. In conventional SVM, all the 8 switching vectors form a hexagonal shape [29]. Similarly, in 3DSVM, available 16 switching states of a four-leg inverter form a dodecahedron as shown in Fig. 3. The dodecahedron is further divided into 24 tetrahedrons. Each tetrahedron is accompanied by three active vectors and two zero vectors [30, 31]. Tetrahedrons and their associated active voltage vectors are mentioned in Table 2. In this table, TH represents Tetrahedron and VV represents the voltage vectors. Depending on the type of reference frame used, the implementation of 3DSVM can be done in two different ways.

Table 1 Switching states and voltage vectors

State	S_a	S_b	S_c	S_n	v_{can}	v_{cbn}	v_{ccn}	Vector
1	0	0	0	0	**0**	**0**	**0**	V_1
2	0	0	0	1	**−1**	**−1**	**−1**	V_2
3	0	0	1	0	**0**	**0**	**1**	V_3
4	0	0	1	1	**−1**	**−1**	**0**	V_4
5	0	1	0	0	**0**	**1**	**0**	V_5
6	0	1	0	1	**−1**	**0**	**−1**	V_6
7	0	1	1	0	**0**	**1**	**1**	V_7
8	0	1	1	1	**−1**	**0**	**0**	V_8
9	1	0	0	0	**1**	**0**	**0**	V_9
10	1	0	0	1	**0**	**−1**	**−1**	V_{10}
11	1	0	1	0	**1**	**0**	**1**	V_{11}
12	1	0	1	1	**0**	**−1**	**0**	V_{12}
13	1	1	0	0	**1**	**1**	**0**	V_{13}
14	1	1	0	1	**0**	**0**	**−1**	V_{14}
15	1	1	1	0	**1**	**1**	**1**	V_{15}
16	1	1	1	1	**0**	**0**	**0**	V_{16}

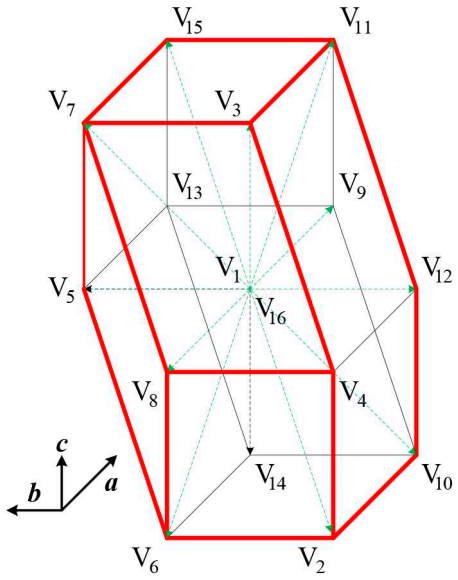


Fig. 3 *Dodecahedron with associated all the voltage vectors*

Table 2 Tetrahedrons and their associated voltage vectors of dodecahedron

TH	VV1	VV2	VV3	TH	VV1	VV2	VV3
1	V_9	V_{13}	V_{15}	13	V_9	V_{10}	V_{14}
2	V_5	V_{13}	V_{15}	14	V_2	V_{10}	V_{14}
3	V_5	V_7	V_{15}	15	V_2	V_6	V_{14}
4	V_5	V_7	V_8	16	V_2	V_6	V_8
5	V_9	V_{13}	V_{14}	17	V_9	V_{11}	V_{12}
6	V_5	V_{13}	V_{14}	18	V_3	V_{11}	V_{12}
7	V_5	V_6	V_{14}	19	V_3	V_4	V_{12}
8	V_5	V_6	V_8	20	V_3	V_4	V_8
9	V_9	V_{11}	V_{15}	21	V_9	V_{10}	V_{12}
10	V_3	V_{11}	V_{15}	22	V_2	V_{10}	V_{12}
11	V_3	V_7	V_{15}	23	V_2	V_4	V_{12}
12	V_3	V_7	V_8	24	V_2	V_4	V_8

Among them, one is using $\alpha\beta\gamma$ reference frame [30] while the other is in *abc* reference frame [31]. However, the method using $\alpha\beta\gamma$ requires complex calculations and also difficult to implement [31]. Therefore, in the proposed work, 3DSVM is implemented in *abc* coordinates, which simplifies the selection of tetrahedron and switching sequence. The step-by-step procedure for developing the proposed control algorithm is explained below.

(1) Initially, the value of cost function (C) is calculated using (11) for all the 16 switching states

$$C = [C_i]^{\mathrm{T}}(i = 1{:}16) \tag{12}$$

(2) Using the cost function value of each voltage vector, the duty cycles of associated voltage vectors for each tetrahedron are calculated. In each tetrahedron, the voltage vector with minimum C value has to be applied for a longer duration the one with maximum C value has to be applied for least duration. Therefore, the cost function value and the duty values are inversely proportional to each other. The equation used to calculate the duty values of zero vector (d_0) and active vectors (d_1, d_2 and d_3) are given as

$$\begin{aligned}
\frac{1}{d_0(i)} &= C_{VV0}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right),\\
\frac{1}{d_1(i)} &= C_{VV1}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right),\\
\frac{1}{d_2(i)} &= C_{VV2}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right),\\
\frac{1}{d_3(i)} &= C_{VV3}\left(\frac{1}{C_{VV0}} + \frac{1}{C_{VV1}} + \frac{1}{C_{VV2}} + \frac{1}{C_{VV3}}\right).
\end{aligned} \tag{13}$$

In (13), i value varies from 1 to 24 (total 24 tetrahedrons), C_{VV0}, C_{VV1}, C_{VV2} and C_{VV3} represent the cost function values of zero voltage vector and the three active vectors of a tetrahedron. To understand (13), tetrahedron 1 is taken as an example and duty cycle calculation of the associated voltage vectors V_1, V_9, V_{13} and V_{15} are given as follows:

$$\begin{aligned}
d_0 &= \frac{C_9C_{13}C_{15}}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9},\\
d_1 &= \frac{C_1C_{13}C_{15}}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9},\\
d_2 &= \frac{C_9C_1C_{15}}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9},\\
d_3 &= \frac{C_9C_{13}C_1}{C_1C_9C_{13} + C_9C_{13}C_{15} + C_{13}C_{15}C_1 + C_{15}C_1C_9},
\end{aligned} \tag{14}$$

where C_1, C_9, C_{13} and C_{15} represent the cost function values of voltage vectors V_1, V_9, V_{13} and V_{15}, respectively.

(3) The new cost function (G) value of each tetrahedron is calculated using duty cycle values and also the cost function values of associated voltage vectors

$$G_i = d_0(i)C_{VV0} + d_1(i)C_{VV1} + d_2(i)C_{VV2} + d_3(i)C_{VV3}\,. \tag{15}$$

After calculating the new cost function values for each tetrahedron, the tetrahedron which has minimum G value is selected. Then the switching sequence is chosen by using the associated voltage vectors of the selected tetrahedron. In general, the switching sequence selection for a selected tetrahedron is not unique. The basic condition to satisfy the selection of switching sequence is that the switching transition from one state to another state involves only two switches of a leg [34]. Therefore, to satisfy this condition, each sequence is always started by a zero vector followed by three active vectors [34]. For example, if the tetrahedron 1 is giving the minimum cost function value, according to Table 2, the switching sequence will be $V_1 - V_9 - V_{13} - V_{15} - V_{16} - V_{15} - V_{13} - V_9 - V_1$. The pictorial representation of the switching sequence is shown in Fig. 4. From this figure, it is observed that

$$\begin{aligned}
S_a &= d_1 + d_2 + d_3 + \frac{d_0}{2},\\
S_b &= d_2 + d_3 + \frac{d_0}{2},\\
S_c &= d_3 + \frac{d_0}{2},\\
S_n &= \frac{d_0}{2}\,.
\end{aligned} \tag{16}$$

(4) Finally, each switching sequence is compared with a triangular carrier signal of constant switching frequency as shown in Fig. 2, to generate the switching pulses for FL-DSTATCOM.

The flowchart of the switching sequence generation using 3DSVM is shown in Fig. 5. To understand the selection of tetrahedron, the duty values (d_0, d_1, d_2 and d_3) and cost function values (G) of each tetrahedron (TH) in one sampling time are shown in Table 3. From this table, it is observed that, tetrahedron 7 is giving the minimum G value and it is shown with bold letters. Therefore, the associated voltage vectors V_1, V_5, V_6 and V_{14} are used to generate the switching sequence.

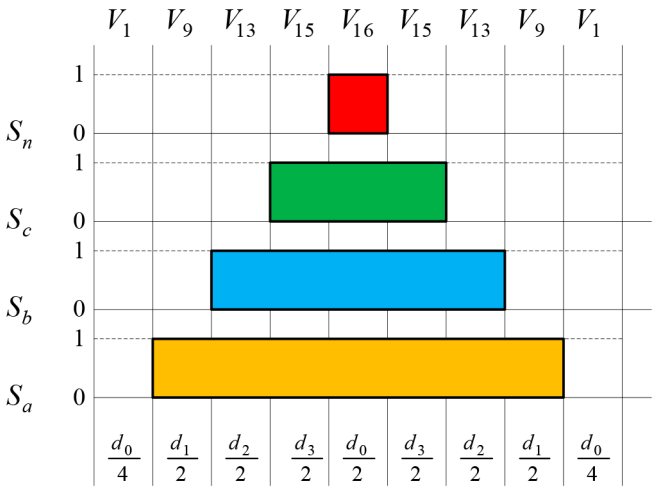


Fig. 4 *Switching sequence for tetrahedron 1*

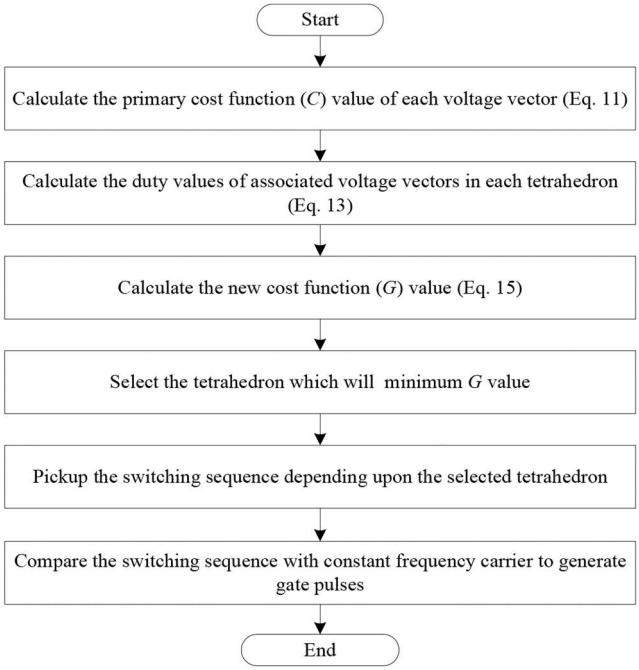


Fig. 5 *Flowchart of switching sequence selection using 3DSVM*

The implementation of the proposed 3DSVM-based constant switching frequency MPC is explained using a block diagram and it is shown in Fig. 6. Initially, non-linear and unbalanced loads are connected to the three-phase four-wire supply system through breakers. Sensors are connected at the PCC to measure the load currents, DSTATCOM currents, PCC voltages and dc link voltage. The detected voltages and currents are sent to the personal computer (PC) using MicroLabBox 1202, which acts as an interface between real-time environment and PC. The proposed control algorithm is implemented in the PC using sensed voltages and currents which generates the required gate pulses for the inverter switches. The generated gate pulses are given to the inverter switches using MicroLabBox 1202. Using these gate pulses, FL-DSTATCOM will generate the appropriate compensating currents which are connected at PCC through interfacing inductors.

3 Simulation studies

The simulation was done for two different load conditions to verify the efficacy of the proposed control algorithm. Parameters considered for the simulation are given in Table 4. The performance of the proposed control algorithm was compared with conventional variable switching frequency MPC (CMPC) and also MPC with switching frequency reduction constraint (MPCSFR).

Table 3 Example for tetrahedron selection

TH	d_0	d_1	d_2	d_3	*G*
1	0.5318	0.1034	0.1414	0.2234	2.5679
2	0.3954	0.3335	0.1051	0.1661	1.909
3	0.3675	0.3099	0.1682	0.1544	1.7744
4	0.3817	0.322	0.1748	0.1215	1.8433
5	0.5318	0.1034	0.1414	0.2234	2.5679
6	0.3954	0.3335	0.1051	0.1661	1.909
7	**0.3663**	**0.309**	**0.1709**	**0.1539**	**1.7687**
8	0.3805	0.3209	0.1775	0.1211	1.8372
9	0.5318	0.1034	0.1414	0.2234	2.5679
10	0.4574	0.2289	0.1216	0.1921	2.2086
11	0.4205	0.2104	0.1925	0.1766	2.0303
12	0.4393	0.2198	0.2011	0.1398	2.1211
13	0.5318	0.1034	0.1414	0.2234	2.5679
14	0.4552	0.2325	0.121	0.1912	2.1982
15	0.4171	0.2131	0.1946	0.1752	2.1041
16	0.4356	0.2225	0.2032	0.1386	2.1034
17	0.5318	0.1034	0.1414	0.2234	2.5679
18	0.4574	0.2289	0.1216	0.1921	2.2086
19	0.4427	0.2215	0.1498	0.186	2.1378
20	0.4636	0.232	0.1568	0.1476	2.2387
21	0.5318	0.1034	0.1414	0.2234	2.5679
22	0.4552	0.2325	0.121	0.1912	2.1982
23	0.4407	0.2251	0.1491	0.1851	2.128
24	0.4614	0.2357	0.1561	0.1469	2.228

Fig. 7 shows various parameters of the system for load-1, such as PCC voltages (v_{sabc}), load currents (i_{labc}), source currents (i_{sabc}), compensator currents (i_{cabc}), load and source neutral current (i_{ln} and i_{sn}). In this figure, from 0 to 0.1 s, performance of the system is shown without connecting the FL-DSTATCOM. At 0.1 s, FL-DSTATCOM is connected to the distribution system to improve the quality of source current. From this figure, it is observed that load currents are non-linear as well as unbalanced. During 0 to 0.1 s, source currents are the same as load currents and the entire load neutral current flows through the source neutral. After connecting FL-DSTATCOM, the source currents are balanced, distortionless and in-phase with their respective PCC voltages.

To compare the performance of the proposed control algorithm with conventional variable switching frequency MPC, the THD spectra of compensator currents is provided for both conventional [27] and proposed 3DSVM-based MPC. From Fig. 8*a*, it is observed that the harmonics are spread over the entire area which implies that the frequency is a variable quantity for conventional MPC. However, with the proposed 3DSVM-based MPC, the switching frequency is maintained as constant. Figs. 8*b* and *c* show the THD spectrum of compensator currents and source currents with the proposed method. From the two figures, it is observed that the harmonic components are spread around 10 kHz and in integral multiples of 10 kHz, which implies that the switching frequency is constant and its value is equal to 10 kHz. The rms values and THDs of source currents in Fig. 8*c* indicate that they are balanced and sinusoidal.

Three single-phase diode bridge rectifiers feeding a parallel combination of resistor and capacitor are connected to the supply as load-2, to evaluate the performance of the proposed control algorithm for highly distorted load currents. Fig. 9 shows the simulation results during load-2. Before connecting the FL-DSTATCOM to the distribution system, the rms values of source currents are 34.27 A with THD 42.25%, which indicates that the load currents are balanced, distorted and the load neutral current is very high. Even though the load is balanced, the main reason for the high neutral current is triplen harmonic components present in the load [8]. After connecting the FL-DSTATCOM to the system, the rms values of the source currents are 32.22, 32.24 and 32.22 A with THDs 3.11, 3.13 and 3.16%, for phase-*a*, phase-*b* and phase-

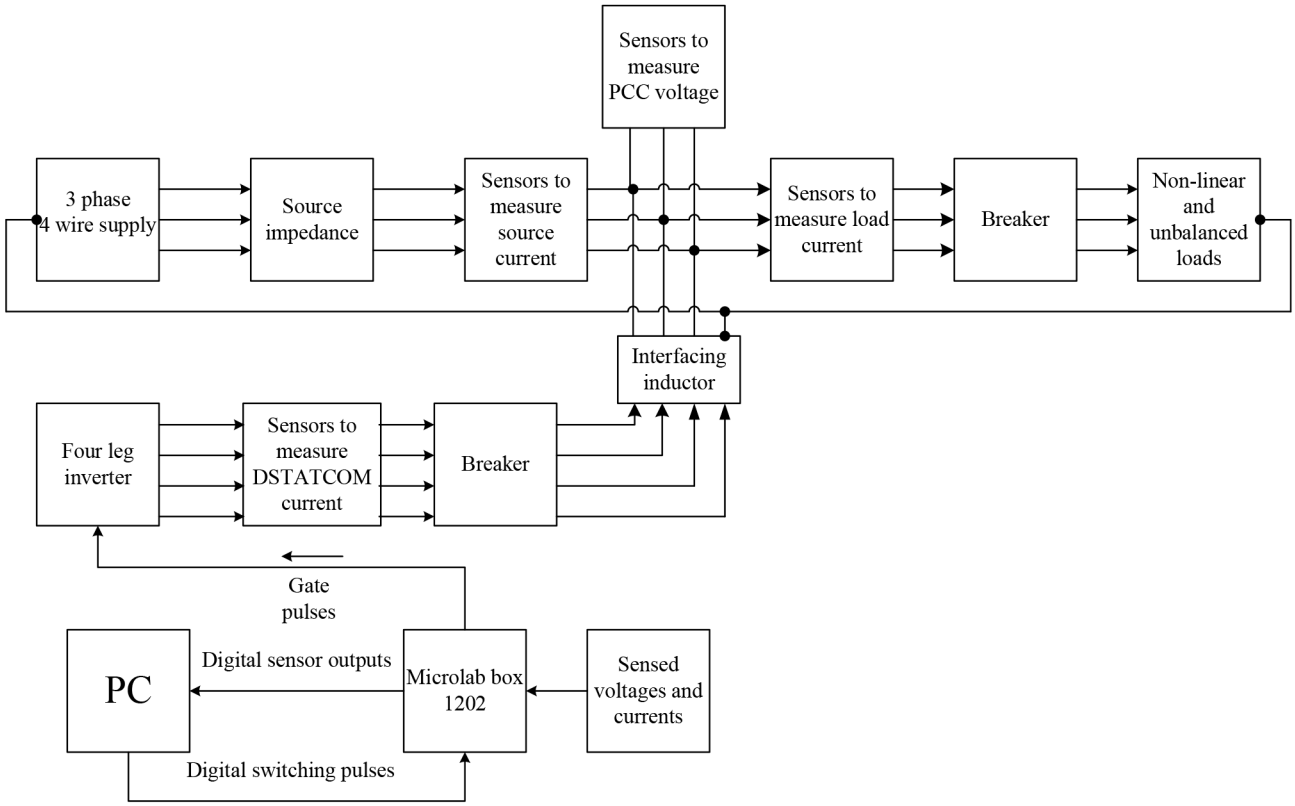


Fig. 6 *Implementation block diagram of proposed 3DSVM-based MPC for FL-DSTATCOM*

Table 4 Simulation parameters

Paramter	Value
Supply voltage (v_s)	415 V
Interfacing inductor (L_f)	4.5 mH
Dc link voltage (V_{dc})	700 V
Dc link capacitance (C_{dc})	5000 μF
load-1	unbalanced non-linear load: three single-phase diode bridge rectifiers feeding $R = 10\,\Omega$, $L = 150$ mH on phase-*a*, $R = 12.5\,\Omega$, $L = 150$ mH on phase-*b*, $R = 7.5\,\Omega$, $L = 150$ mH on phase-*c*. balanced linear load: 10 kVA with 0.7 power factor lagging. Balanced linear load to verify transient performance: 10 kVA with 0.95 power factor lagging.
load-2	non-linear load: three single phase diode bridge rectifiers feeding a parallel combination of $R = 10\,\Omega$, C=500 μF on each phase.
sampling time (T_s)	10 μs
switching frequency	10 kHz

c, respectively, which indicates that they are balanced, sinusoidal and the source neutral current is almost zero as evident from Fig. 9.

The performance of the proposed control algorithm is also validated for load variation. Fig. 10 shows the performance of the proposed control algorithm during a load change. From the figure, it is observed that the DSTATCOM is not taking more than one cycle to follow the currents during load variation. It is also observed that the source neutral current is nearly zero which indicates that the source currents are balanced. From Fig. 10, it is also observed that the dc link voltage is 700 V and it is maintained constant even under the load variation. The THDs of load currents and source currents for both load-1 and load-2 are mentioned in Table 5.

3.1 Comparison of proposed method with conventional MPC and MPC with reduced switching frequency

As discussed in Section 1, conventional MPC leads to variable switching frequency and sometimes the switching frequencies are also very high, which further leads to higher switching losses. To reduce these losses, it is required to add switching frequency reduction constraint in the cost function, which further reduces the switching losses [13]. Using conventional MPC, to reduce the switching frequency an additional control parameter is required to be included in the cost function, and it is given as

$$S = |S_a(k) - S_a(k-1)| + |S_b(k) - S_b(k-1)| + |S_c(k) - S_c(k-1)| + |S_n(k) - S_n(k-1)| \quad (17)$$

Therefore, the complete cost function to compensate power quality issues along with the switching frequency reduction can be written as

$$C_f = C + \lambda S \quad (18)$$

where C is given in (11), λ is weighting factor and the reduction in the value of switching frequency will completely depend on it. Table 6 shows the comparison between conventional MPC, reduced switching frequency MPC and proposed MPC in terms THDs of source currents and switching losses. As reported in the literature, conventional MPC is leading to higher switching frequencies which leads to higher switching losses. After adding the switching frequency reduction constraint using the weighting factor, the switching frequency is reduced, which further reduces the switching losses. From the table, it is observed that the switching losses (SL) are reduced by adding switching frequency reduction constraint in the cost function with $\lambda = 0.2$, and they are further reduced by making $\lambda = 0.5$. However, with the proposed control technique, the losses are further reduced and also it achieves constant switching frequency operation (10 kHz).

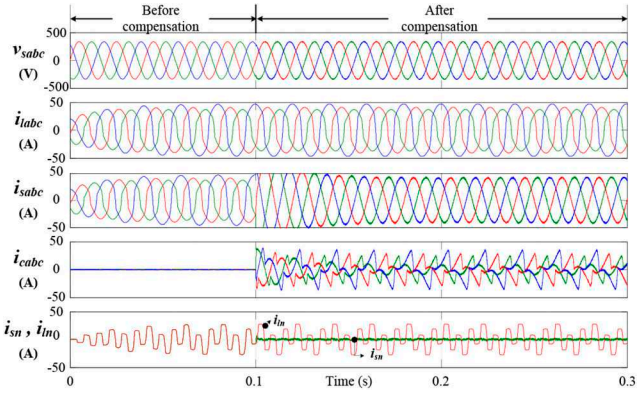


Fig. 7 *Voltages and currents of the system during load-1*

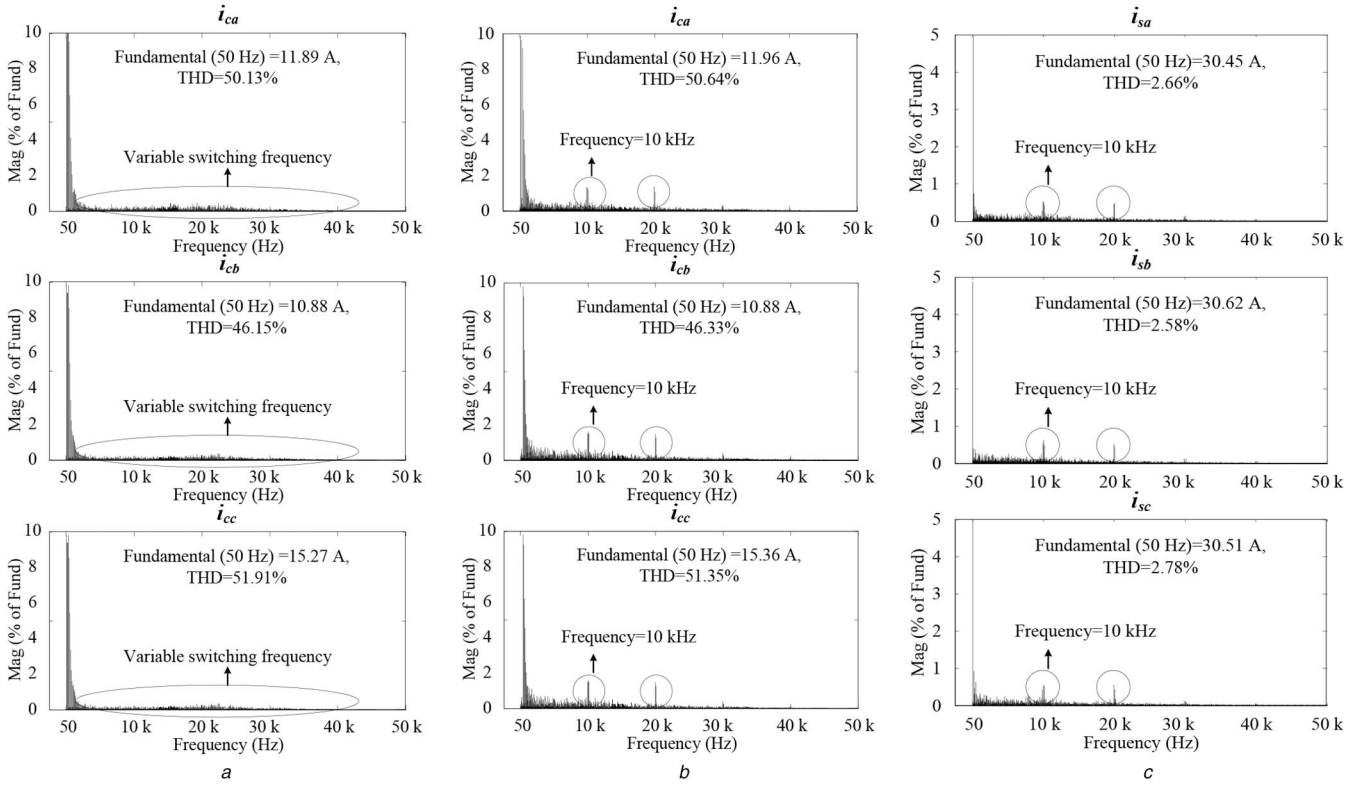


Fig. 8 *Harmonic spectra of*
(a) FL-DSTATCOM currents with conventional method, ***(b)*** FL-DSTATCOM currents with proposed method, ***(c)*** Source currents after compensation with the proposed method for load-1

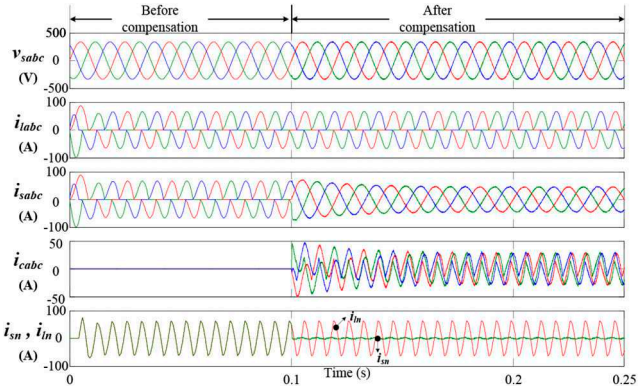


Fig. 9 *Voltages and currents of the system with highly distorted load currents (Load-2)*

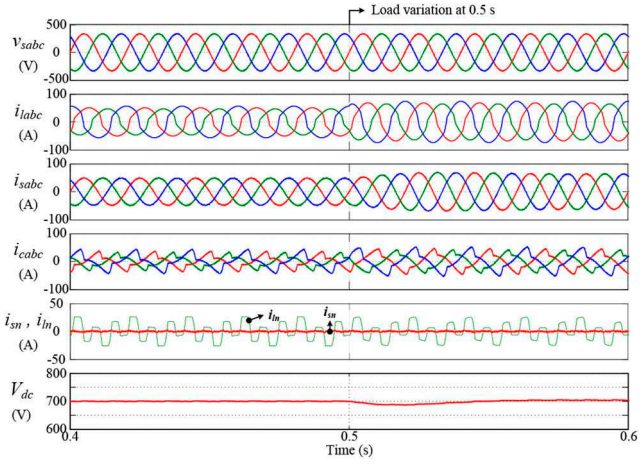


Fig. 10 *Transient performance of the proposed method*

4 Experimental studies

The performance of the proposed 3DSVM-based constant switching frequency MPC is tested for compensation of non-linear and unbalanced load currents. Parameters considered for the experimental studies are mentioned in Table 7. Due to the laboratory constraints, the experimental parameters are considered

Table 5 THDs load and source currents for load-1 and load-2

Load	i_{la}, A	i_{lb}, A	i_{lc}, A	i_{sa}, A	i_{sb}, A	i_{sc}, A
load-1	32.52	29.04	38.19	30.45	30.62	30.51
	19.86%	18.08%	21.86%	2.68%	2.48%	2.84%
load-2	34.27	34.27	34.27	32.22	32.24	32.22
	42.26%	42.26%	42.26%	3.11%	3.13%	3.16%

Table 6 Comparison of proposed method with conventional methods

Parameter	CMPC	MPCSFR ($\lambda = 0.2$)	MPCSFR ($\lambda = 0.5$)	Proposed
i_{la}, A	32.19 19.00%	32.19 19.00%	32.19 19.00%	32.19 19.00%
i_{lb}, A	28.8 17.33%	28.8 17.33%	28.8 17.33%	28.8 17.33%
i_{lc}, A	37.67 20.88%	37.67 20.88%	37.67 20.88%	37.67 20.88%
i_{sa}, A	30.29 1.95%	30.3 2.01%	30.3 2.08%	30.32 2.66%
i_{sb}, A	30.46 1.67%	30.45 1.76%	30.45 1.86%	30.45 2.58%
i_{sc}, A	30.31 1.94%	30.31 2.00%	30.31 2.02%	30.34 2.78%
SL_a, W	382.8	320	275.3	264.2
SL_b, W	355	286.5	259.3	250.4
SL_c, W	506.2	414.3	381.4	374.3
SL_n, W	679.8	452.4	363.9	282.2

Table 7 Experimental parameters

Paramter	Value
supply voltage (v_s)	50 V
Interfacing inductor (L_f)	9 mH
Dc link voltage (V_{dc})	100 V
Dc link capacitance (C_{dc})	4700 μF
non-linear load	Load-1: Three phase diode bridge rectifier feeding $R = 20\,\Omega$, $L = 150\,\text{mH}$ Unbalanced linear load: $R = 12.5\,\Omega$, $L = 60\,\text{mH}$ on phase-*a* $R = 12.5\,\Omega$, $L = 120\,\text{mH}$ on phase-*b* $R = 12.5\,\Omega$, $L = 80\,\text{mH}$ on phase-*c* Load-2: Three-phase diode bridge rectifier feeding a resistor with filter capacitor ($R = 200\,\Omega$, C=4700 μF)
sampling time (T_s)	50 μs
switching frequency	2 kHz

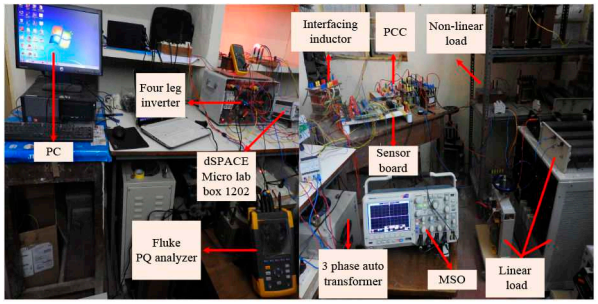


Fig. 11 *Photograph of the experimental setup*

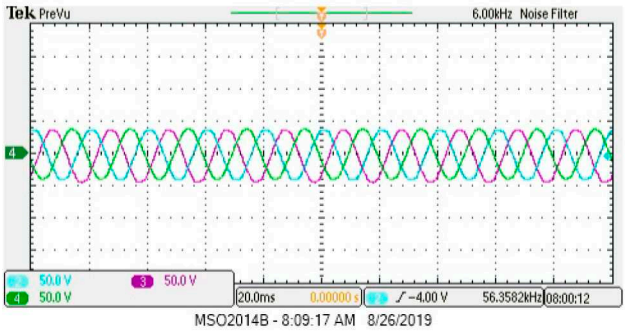
for reduced rating compared to simulation. The photograph of the complete experimental setup is shown in Fig. 11.

A combination of three unbalanced single phase *RL* loads and a three-phase diode bridge rectifier is connected to the three-phase supply to achieve non-linear and unbalanced load currents and it is considered as load-1. The transient performance of the proposed control algorithm is tested by adding an additional three-phase diode bridge rectifier as load-2. dSPACE MicroLabBox 1202 was used as an interfacing device between the real-time environment and PC. Fluke make power quality analyser was used to measure the THDs of various currents and voltages of the system. Hall effect voltage and current sensors are used to sense the required voltages and currents. Sensed voltages and currents are sent to the PC using MicroLabBox, which further used to implement the proposed control algorithm.

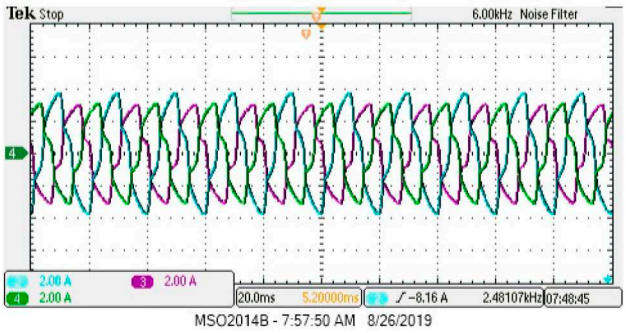
4.1 Performance during non-linear and unbalanced load currents (load-1)

Fig. 12 shows the PCC voltages, load currents, source currents and DSTATCOM currents with their scaling.

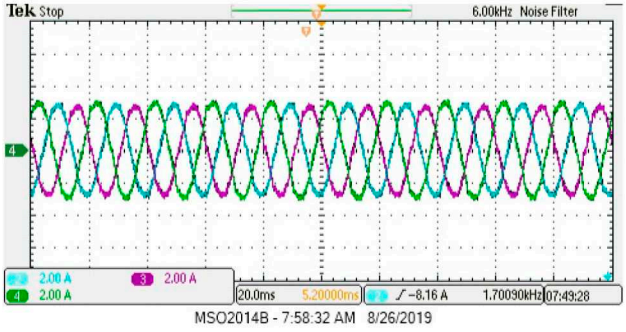
From this figure, it is observed that the currents required by the load-1 are non-linear as well as unbalanced. However, with the proposed control algorithm, FL-DSTATCOM is achieving balanced and sinusoidal source currents even though there is an unbalance and distortions in the load currents. From Fig. 13, it is observed that the phase difference between the voltage and current at PCC is almost zero which implies that DSTATCOM is maintaining the source power factor as unity. Figs. 14 and 15 show the THD spectra of DSTATCOM currents and source currents of three phases using the proposed control algorithm, respectively. From Fig. 14, it is observed that the harmonic components are present



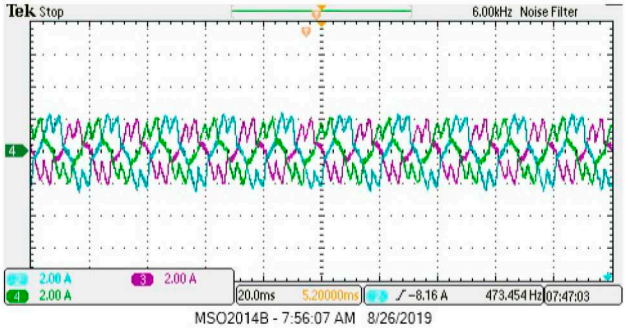
a



b



c



d

Fig. 12 *Various parameters of the distribution system*
(a) PCC voltages (v_{sabc}), ***(b)*** Load currents (i_{labc}), ***(c)*** Source currents (i_{sabc}), ***(d)*** FL-DSTATCOM currents (i_{cabc})

around 2 kHz and integral multiples of 2 kHz, which implies that the switching frequency is 2 kHz. It is also observed from Fig. 15 that, the THDs of source currents 3.54, 3.34 and 3.20% which are well under the limits of IEEE standards 516-1992 (< 5%).

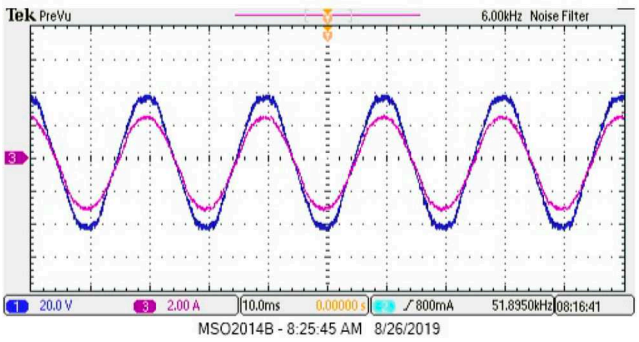
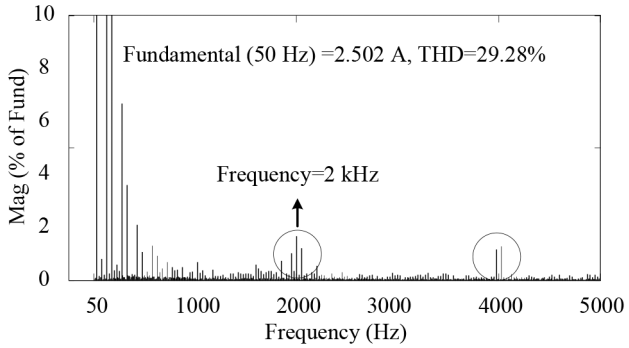
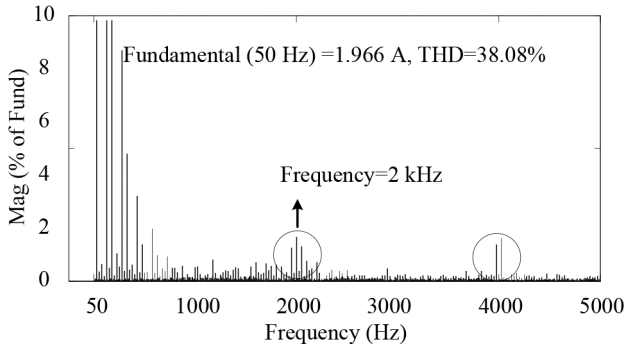


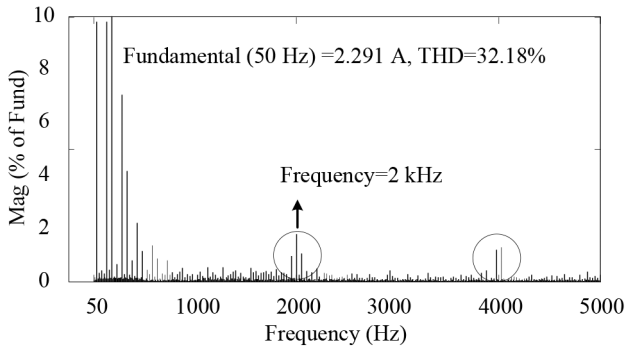
Fig. 13 *Phase angle between v_{sa} and i_{sa} after compensation*



a



b



c

Fig. 14 *Harmonic spectra of FL-DSTATCOM currents*
(a) i_{ca}, ***(b)*** i_{cb}, ***(c)*** i_{cc}

4.2 Transient performance of the proposed method

Fig. 16 shows the voltages and currents during load variation. In this figure, the voltage scaling 50 V/div and current scaling is 4 A/div. From this figure, it is observed that DSTATCOM currents are adjusted as per the load variation, which makes source currents balanced as well as sinusoidal.

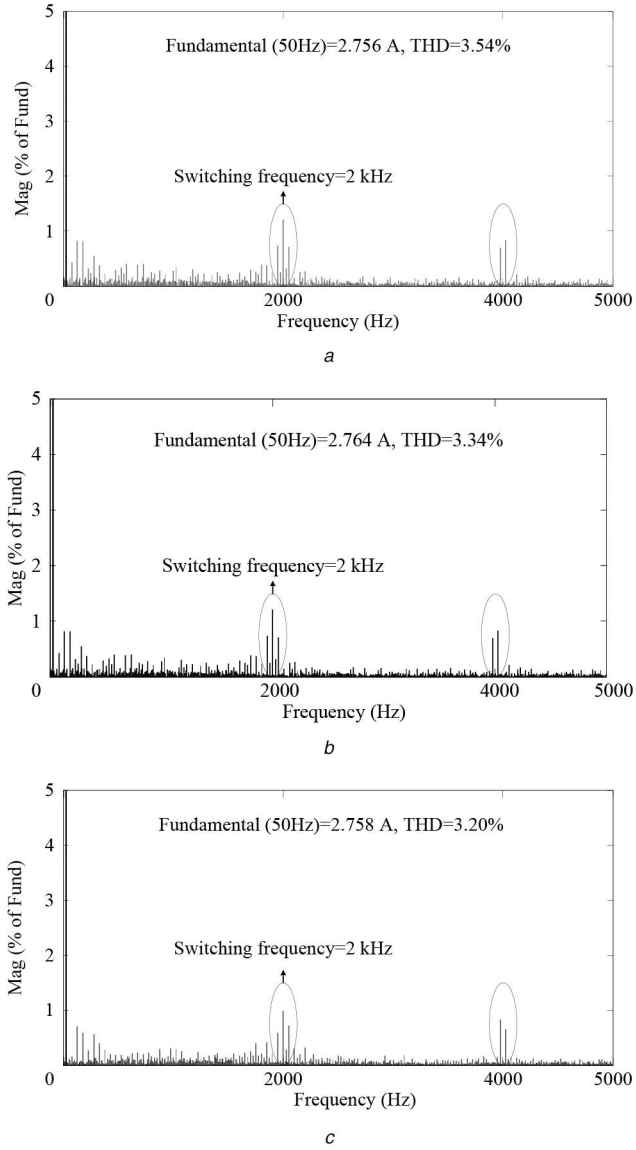


Fig. 15 *Harmonic spectra of source currents*
(a) i_{sa}, ***(b)*** i_{sb}, ***(c)*** i_{sc}

Table 8 Losses of IGBT module

Losses	S_a, W	S_b, W	S_c, W	S_n, W
conventional [20, 26]	8.082	6.286	7.395	3.15
proposed	6.057	4.88	5.731	1.389

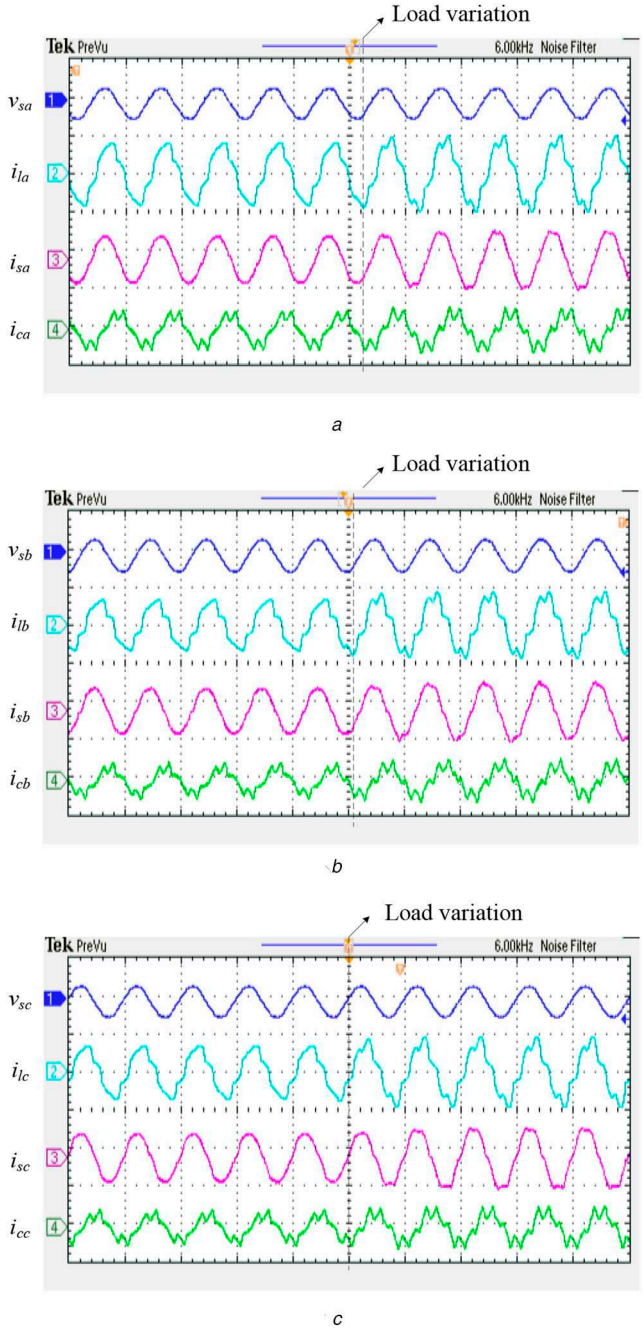


Fig. 16 *Voltages and currents during load variation for*
(a) Phase-*a*, ***(b)*** Phase-*b*, and, ***(c)*** Phase-*c*

As proved in simulation studies, it is also proved with experimental studies, the proposed control algorithm is reducing the switching losses compared to convention MPC. In the experimental studies, SKM75GB123D is used as an IGBT module, which consists of two IGBT switches with anti-parallel diodes. The losses of IGBT modules (SKM75GB123D) are calculated and they are mentioned in Table 8. From this table, it is observed that the percent reduction of losses are 22% for phase-*a*, phase-*b* and phase-*c*. Similarly, the losses are reduced by 55% in the neutral leg.

5 Conclusion

In this paper, 3DSVM-based constant switching frequency MPC for FL-DSTATCOM is presented. The proposed algorithm evaluated the cost function value for each tetrahedron then selects a tetrahedron which minimises the cost function. Depending on the selected tetrahedron, appropriate switching sequence is picked up and it is compared with a constant frequency carrier signal which further generates the switching pulses for the inverter. From the simulation studies, it is observed that source currents are balanced, sinusoidal and also in-phase with the voltages at PCC. The comparison of the proposed algorithm with the conventional algorithm proved that the switching frequency is variable for conventional MPC and constant for proposed 3DSVM-based MPC. Therefore, the variable switching frequency limitation of MPC is overwhelmed with proposed 3DSVM-based constant switching frequency MPC which further reduced the switching losses. Finally, experimental studies are also proved that the proposed control algorithm is compensated, the current related power quality issues as well as achieved constant switching frequency.

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