A Nine-Level Inverter for Open Ended Winding Induction Motor Drive with Fault-Tolerance

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***Abstract*— This paper presents a nine level inverter for an open ended winding induction motor (OEWIM) drive with fault-tolerance property for switch faults. The proposed topology consists of three three-phase inverters with an isolated DC source for each inverter, three bi-directional switches and three capacitors. The three inverters are configured such that they all have a common neutral connection between them. Such configuration provides the advantage of producing peak output voltage twice the source voltage magnitude and hence lower rating voltage sources can be employed. Conventional sinusoidal pulse width modulation techniques are employed for generating gate pulses for the switches in the proposed topology for normal and post-fault operation. A fault-tolerance strategy is proposed for the post-fault operation of the inverter to produce balanced three phase supply. Simulations are carried out in MATLAB/Simulink environment and results are presented.**

Keywords: multilevel inverter, open end winding, fault-tolerance, switch-faults.

I. INTRODUCTION

Advances in material science has changed the face of the power systems with increased involvement of power electronic components. The extended operating range of power semiconductor switches aids in designing of multilevel inverters (MLIs) for medium and high voltage applications [1]. However, owing to the advantages such as increased voltage levels, enhanced harmonic profile, reduced voltage stress on power semiconductor devices, flexibility of operation, reduced interference with the communication signals, lower slew rates in output voltages compared to conventional two level or three level VSIs make their application inevitable[2]. With these advantages, MLIs find vast applications in power system transmission and electric drive applications.

MLIs with increased number of voltage levels reduces harmonic distortions and elude the need for expensive and bulky filters, hence such MLIs are preferred in drive applications [3]. Nevertheless, the increase in voltage levels are attained with increased number of components, hence the industry is reluctant for such MLIs because of uncertainty of reliability and control complexity [4]. This provides the need for designing MLIs with high number of voltage levels but with fewer components. With increase in component count, the reliability of the system decreases. Failure of a single switch may lead to a complete shutdown of the system. Hence reduced switch-count MLIs with fault tolerance capability find better applications in industrial drives these days [5]. MLIs with increased output voltage levels and reduced control complexity were proposed to extract the best performance of the induction motors in the drive applications. The configuration involving an open end winding induction motor (OEWIM) fed by dual two-level inverters has become a competitive alternative [6]. The three phase windings of the motor are fed from both ends with two identical three-phase VSIs. Induction motor is known for its rugged construction and maintenance free operation and hence finds many applications in industrial drives. The dynamic performance of the drives with induction motor can be enriched by various flexible control schemes while being fed from VSIs [7]-[9].

In [10]-[11], the authors have proposed MLI topologies with single DC source and reduced number of capacitors compared to conventional topologies. Though the output voltage takes multiple levels, the peak voltage obtained across the load terminals is the same as DC link voltage, which triggers to have high rating voltage sources and complex control for capacitor voltage balancing. In [12] the authors have proposed a complex circuit with simple control scheme for drive applications.

Some authors proposed inverters with redundant legs such that the additional leg provides fault tolerance to switch open faults [13]. Fault-tolerant MLI topologies with constant output power capability even with the switch faults are also present but the control strategy is complex even for normal operating conditions and hence are preferred only when delivering constant power output and reliability are of utmost importance [14]-[15]. In [16], a modified hardware circuit is employed to deliver power during switch faults resulting in an increase in the cost of the circuit by 50% with reduced output power capacity of 58% only. In [17]-[19], fault-tolerable topologies without any additional hardware requirement and controlled by conventional sinusoidal pulse width modulation (SPWM) techniques are presented. MLI topology for obtaining increased number of levels in output voltage for OEWIMD is presented in [20].

Hence a new MLI topology is proposed for OEWIM drive with fault tolerance capability with simple control scheme for normal and post-fault operation. The proposed topology is designed with conventional three-phase inverters, capacitors and bi-directional switches. A capacitor in series with a bi-directional switch is connected across the lower switch of one leg in each three-phase inverter. Such legs of all the three inverters are combined together to form a neutral path for the inverters. The bi-directional switch is realized by connecting two IGBTs in anti-series with the common-emitter configuration such that both the switches are operated by same switching pulses and hence considered as a single switch for easy analysis of the topology. The proposed configuration yields a peak voltage magnitude of twice the source voltage with nine level across the phase windings of OEWIM with each voltage step-magnitude of half the source voltage.

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II. Proposed Topology

The proposed topology employs three three-phase voltage source inverters (VSIs) each with an isolated DC source connected in a star configuration. Additionally, a branch consisting of a capacitor with a bidirectional switch in series is connected across the lower switch of the first leg in in each VSI as illustrated in Fig. 1. The bi-directional switch is realized with two switches (here IGBTs) connected in anti-series with common emitter configuration. The switches S_{11} through S_{17} represent inverter-1. Similarly, the switches S_{21} through S_{27} and S_{31} through S_{37} represent inverter-2 and inverter-3 respectively.

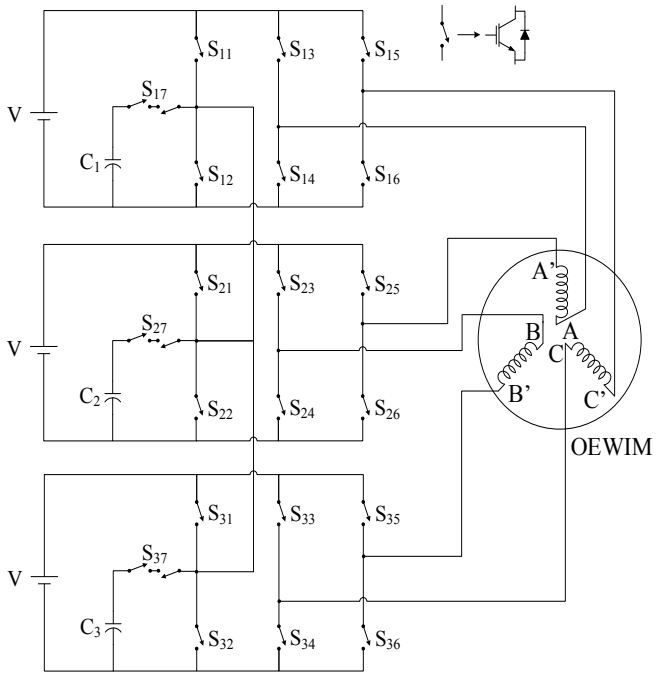

Fig. 1. Proposed topology

The proposed topology is configured such that each inverter will give out three output connecting terminals. First terminal is from the mid-point of switches S_{x1} and S_{x2} (where x ϵ 1, 2, 3), the same point where one end of bidirectional switch is connected. The second and third terminals are taken from mid-points of switches S_{x3}-S_{x4} and S_{x5}-S_{x6} respectively. The first terminals of all the three inverters are connected together and forms the neutral connection of the inverters. The second and the third terminals are connected to phase windings of the OEWIM and the connections are made such that each inverter feed two distinct phases at distinct ends.

For example, inverter-1 second terminal is connected to phase-A winding at end A whereas the third terminal is connected to phase-C winding at end C'. Other two inverters are also connected in the similar manner. The idea behind such configuration is that each phase winding is connected between two inverters that are fed from separate sources and switched with 120^0 phase shift. This will allow the phase winding to experience a resultant fundamental voltage magnitude of √3 times of the source voltage with a peak voltage magnitude of twice the source voltage.

Comparing with dual inverter configuration, the proposed topology requires an additional DC source but delivers increased peak output voltage, i.e., $2V_{dc}$ whereas $1.33V_{dc}$ in case of dual inverter. Owing to this property of the proposed topology, DC sources with lower voltage rating can be employed which would reduce the blocking voltage capacity of the switching devices. This offers further scope for employing lower power rating high frequency semiconductor switches (such as MOSFETs), which will be an additional advantage. The direct applicability of the conventional SPWM technique is another advantage because the computational burden on the digital processors reduces.

The possible switching states of the inverter-1 and inverter-2 feeding phase-A winding and corresponding voltage levels obtained are presented in Table I. The switches S_{11}, S_{12}, S_{13}, S_{14} and S_{17} of inverter-1 and S_{21}, S_{22}, S_{25}, S_{26} and S_{27} of inverter-2 determine the voltage magnitude across the phase-A winding. Since switches S_{13} and S_{14} operate in complementary with each other, only switching states of S_{13} are presented. Similarly, for switches S_{25} and S_{26}, only switching states of S_{25} are presented in Table-I.

TABLE I. Switching States of Inverters and Corresponding Voltage Levels across Winding A-A'($V_{AA'}$)

Voltage $V_{AA'}$	Inverter-1				Inverter-2				Capacitor state
	S_{11}	S_{12}	S_{13}	S_{17}	S_{21}	S_{22}	S_{25}	S_{27}	
2V	0	1	1	0	1	0	0	0	No change
3V/2	0	0	1	1	1	0	0	0	C_1-Charging
	0	1	1	0	0	0	0	1	C_2-Discharging
V	0	1	1	0	0/1	1/0	0/1	0/0	No change
	0/1	1/0	0/1	0/0	1	0	0	0	
V/2	0	0	1	1	1/0	0/1	1/0	0/0	C_1-Charging
	0/1	1/0	0/1	0/0	0	0	0	1	C_2-Discharging
0	1	0	1	0	1/0	0/1	1/0	0/0	No change
	0	1	0	0	1/0	0/1	1/0	0/0	
	1/0	0/1	1/0	0/0	1	0	1	0	
	1/0	0/1	1/0	0/0	0	1	0	0	
-V/2	0	0	0	1	1/0	0/1	1/0	0/0	C_1-Discharging
	1	0	0	0	0	0	0	1	C_2-Charging
-V	1/0	0/1	1/0	0/0	0	1	1	0	No change
	1	0	0	0	1/0	0/1	1/0	0/0	
-3V/2	0	0	0	1	0	1	1	0	C_1-Discharging
	1	0	0	0	0	0	1	1	C_2-Charging
-2V	1	0	0	0	0	1	1	0	No change

The voltages across the winding terminals are dependent on the switching states of the switching devices. Considering the switches are ideal, their blocking and conduction states are represented by binary variables as 0 and 1 respectively. Considering inverter-1, the following conditions can be depicted from the switching states as

If S_{13}= 1 then S_{14} = 0,
i.e., if switch S_{13} is ON then switch S_{14} is OFF

Similarly, if S_{14} = 1 then S_{13} = 0,
if S_{11} = 1, then S_{12} = S_{17} = 0,
if S_{12} = 1, then S_{11} = S_{17} = 0,
if S_{17} = 1, then S_{11} = S_{12} = 0.

These conditions are also applicable for the other two inverters as well and with this representation the equation for output voltage across the phase-A winding can be written in terms of the switching states as

$$V_{AA'} = [S_{13}(S_{12}+0.5S_{17}) - S_{14}(S_{11}+0.5S_{17})] - [S_{25}(S_{22}+0.5S_{27}) - S_{26}(S_{21}+0.5S_{27})]$$

III. MODULATION SCHEME

The proposed topology exploit the benefit of employing conventional SPWM techniques for generating switching pulses. The operation of the proposed topology can be categorized as normal and post-fault operation. Hence to deliver balanced three phase supply in both the pre- and post-fault conditions two types of SPWM techniques are employed for the proposed topology. In-phase disposition (IPD) level-shifted carriers technique is used in normal operating conditions and the phase-shifted SPWM technique (PS-SPWM) is employed for the post-fault operation.

A. In-phase Disposition SPWM technique

IPD SPWM technique is employed for normal operating conditions because this modulation technique has the advantage of producing better harmonic profile compared to its counter parts [21]. Triangular waves with in-phase disposition are employed as carriers and a modified sinusoidal wave is employed as reference wave. The triangular carrier waves with switching frequency are compared with a sinusoidal reference signal of power frequency to generate the switching pulses as illustrated in the Fig. 2(a). The boolean logic for switching pulses for the switches in the inverter-1 are presented in Fig. 2(b).

The scheme of generating switching pulses for inverter-2 and inverter-3 remains the same except that the reference signal is displaced by 120^0 and 240^0 respectively. Hence the switching pulses are generated by comparison and the logic circuits. Consider the inverter-1: the switches S_{13} and S_{15} operate simultaneously and will be in turned-on condition for complete first half cycle and will be turned-off for next half cycle of the reference wave. The same will be repeated throughout the operation. Similarly the switches S_{14} and S_{16} operate simultaneously and complementary with switches S_{13} or S_{15}. These switches are directly connected to phase windings of the OEWIM. The switches S_{11} and S_{12} operate in complementary with S_{17}. The corresponding switches in other inverters will operate in the similar manner.

B. Phase-shifted SPWM technique

This modulation technique is employed for post-fault operation of the proposed topology. PS-SPWM technique employs a single carrier and two reference signals that are 180^0 out of phase. The reference signal for inverter-1 can be labelled as Ref_1 and the out of phase reference signal as $-Ref_1$. Similarly, the reference signals for inverter-2 and inverter-3 can be labelled as Ref_2 and Ref_3 that are displaced by 120^0 and 240^0 from Ref_1 respectively. The reference signals are compared with carrier wave to generate the switching pulses. The comparison of carrier wave and Ref_1 will produce switching pulses for switches S_{11} and its complementary pulses are given to switch S_{12}. In the same manner, the comparison of carrier wave with $-Ref_1$ wave will produce switching pulses for switches S_{13} and its complementary pulses are given to switch S_{14} of inverter-1. Similarly for inverter-2, Ref_2 and $-Ref_2$ are used to produce switching pulses for S_{21} and S_{23} respectively. Ref_3 and $-Ref_3$ are utilized to produce switching pulses for the switches S_{31} and S_{33} respectively. In the post-fault operation for switch OC faults, to obtain symmetrical and balanced output voltage, the use of capacitor is restricted hence no pulses are fed for switch S_{17}. The scheme of PS-SPWM and the obtained pulses for switches S_{11} and S_{13} are illustrated in Fig. 3.

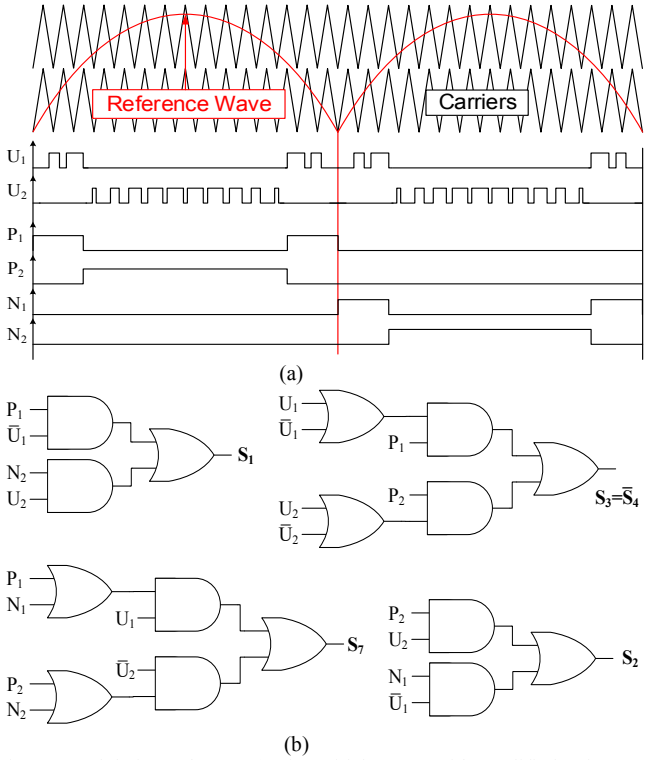

Fig. 2. Modulation scheme (a) Sinusoidal PWM with modified reference signal and corresponding switching pulses, (b) boolean logics employed to generate pulses for the switches.

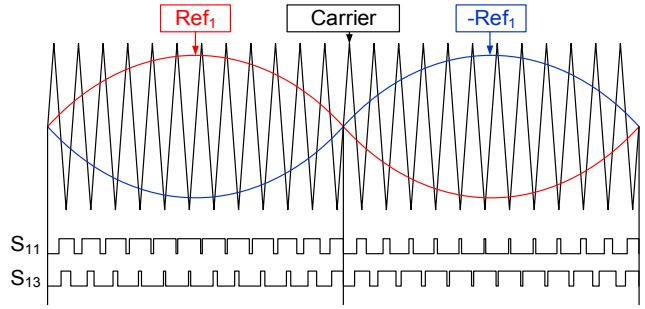

Fig. 3. Phase-shifted PWM technique and corresponding pulses

IV. PROPOSED FAULT-TOLERANCE STRATEGY

The proposed topology can still be operated with a switch fault, either an open-circuit (OC) or a short-circuit (SC) without requirement of any additional hardware, but by post-processing of the switching PWM signals. For post-fault operation with switch OC or SC in any of the inverter, the proposed topology continues to operate with change in modulation technique from IPD-SPWM to PS-SPWM delivering balanced three-phase supply with three-levels in the output voltage. PS-SPWM technique will yield lower harmonic distortion and near to sinusoidal average voltage compared to IPD technique in post fault operation. Hence the application of PS-SPWM technique is limited for post-fault operation of the proposed topology.

A. For switch open-circuit faults

The proposed topology employs minimum number of switching devices compared to other nine-level inverter feeding OEWIM drives and hence the redundant states for producing various voltage levels are very less. Hence fault in one of the switch will have a considerable impact on the

number of levels in the output voltage. The OC fault in switch S_{x7} (where x ϵ 1, 2, 3) will reduce the levels in the output voltage from nine to five keeping the peak output voltage magnitude unaffected. For example, if an OC fault occurs in S_{17}, then the modulation technique is shifted to PS-SPWM and the switching pulses produced (as illustrated in Fig. 3) are applied to switches S_{11} and S_{13}. The switches S_{12} and S_{14} are fed with complementary pulses of S_{11} and S_{13} respectively and the same is done for corresponding switches in the other inverters as well. But OC fault in the other switches in any inverter will result in reduction of voltage levels from nine to three and the peak output voltage is reduced to half. This will reduce the output power delivered but ensures the continuity in the supply for reliable operation of the OEWIM drive. The capacitors and bidirectional switches are not involved in post-fault operation i.e., the switching pulses for the switch S_{x7} are disengaged in the post-fault operation.

The fault-tolerance strategy (FTS) for the OC faults in the switches S_{11} or S_{12} is that the switching pulses of the faulty switch are to be fed to healthy switch in the same leg. For example, if the OC fault occurs in switch S_{11}, then the switching pulses of S_{11} and S_{12} are given to switch S_{12}. This will connect the switch S_{12} to negative rail of source throughout the operation. The same has to be done for the corresponding switches in the other inverters as well. If S_{11} is open-circuited, then the switching pulses to switch S_{21} are disengaged and added to the switching pulses of S_{22} and similarly, the switching pulses of S_{31} and S_{32} are given to S_{32}. This will create balanced switching of the inverters and hence produce balanced output voltages. For switches S_{13} and S_{15}, if OC faults occur in switch S_{13}, the switching pulses of the switches S_{13} and S_{14} are applied to S_{14} and also the switching pulses to switch S_{15} are disengaged and are added to the switching pulses of S_{16}. This has to be done for all the corresponding switches in all the inverters. The strategy remains same for the OC fault in any switch in the corresponding positions in other inverters as well.

B. For switch short-circuit faults

If a SC fault occurs in any of the switch, the source gets short-circuited when the other switch in the corresponding leg is turned-on. Hence, if a SC fault occurs in a switch, then immediately other switch in the corresponding leg has to be turned-off. The FTS for switch SC faults will be contradictory to the strategy for OC fault, i.e., instead of turning-off of the switches in similar positions of the other inverters, here switches are turned-on completely and the switches in similar positions of the healthy switches are turned-off completely.

For example, consider switches S_{13} and S_{14}, if S_{13} gets shorted, then S_{14} has to be turned-off and also the switches S_{24} and S_{34} are to be turned-off and switches S_{23} and S_{33} are to be turned-on completely. The same strategy is applicable for SC faults in switches S_{13}, S_{14}, S_{15}, S_{16} and switches in corresponding positions in other inverters. But if SC fault occurs in any of the switches (S_{x1}, S_{x2} and S_{x7}) that are in the neutral connection of the proposed topology, then the strategy is to turn-off the other two switches completely. If SC fault occurs in the bidirectional switch S_{17}, then the switches S_{11} and S_{12} are to be turned-off completely. Similarly the switches S_{21}, S_{22}, S_{31} and S_{32} are to be turned-off and the switches S_{27} and S_{37} are turn-on throughout the operation.

V. COMPARISON OF THE PROPOSED TOPOLOGY

An assessment of the proposed topology in terms of various parameters such as the levels in the output voltage (N_L), required number of switches (N_{sw}), DC sources (N_s), gate drivers (N_d), diodes (N_D), capacitors (N_{cap}), total component count and control complexity is done and is illustrated in Table II. As can be seen from Table II, it is clear that the component count for the proposed topology are minimum and control complexity is low in comparison with conventional topologies such as neutral-point clamped (NPC), flying capacitor (FC), cascaded H-bridge (CHB) inverters and with other existing nine-level topologies in literature feeding OEWIM drives.

TABLE II. COMPARISON OF THE PROPOSED TOPOLOGY WITH EXISTING TOPOLOGIES FEEDING OEWIM DRIVES

MLI Type	N_L	N_{sw}	N_d	N_D	N_s	N_{cap}	Component Count	Control complexity
NPC	9	48	48	168	1	9	274	Very high
FC	9	48	48	48	1	85	230	High
CHB	9	48	48	48	12	12	168	Low
[10]	9	36	36	36	1	8	126	High
[18]	9	24	24	24	3	6	81	Low
[19]	9	36	36	36	2	12	122	High
[20]	7	48	48	60	6	6	168	Very high
Prop. Top.	9	24	24	24	3	3	78	Low

VI. SIMULATION RESULTS

To demonstrate the feasibility of the proposed topology and the control scheme, the models are developed and simulated in MATLAB/Simulink environment. The parameters considered for the simulation are source voltage V=130 volts, capacitance, C_x=1000μF (where x ϵ 1, 2, 3) and frequency of carriers is taken as 1500Hz. The capacitance required is evaluated using fundamental relation $I_c=C(\Delta V*f_{sw})$, where I_c is the peak current, ΔV is the permissible peak to peak voltage ripple and f_{sw} is the switching frequency.

The simulations results of three-phase output voltage and currents are presented in Fig. 4(a) and (b) respectively. The capacitors are charged to half the source voltage and hence ensures equal magnitude of voltage levels in the output. The voltage across the capacitors in all the three inverters are presented in Fig. 4(c). The proposed topology can deliver output voltage with reduced modulation index as well. The output voltages with changes in modulation index (M_a) are presented in Fig. 4(d). The fast fourier transform (FFT) analysis for the total harmonic distortion (THD) in the phase voltage and current are presented in Fig. 4(e) and (f) respectively.

The performance of the proposed topology with switch faults are analyzed by disengaging switching pulses for the corresponding switch to realize the OC fault. The effect on the three phase output voltage and currents due switch S_{11} OC are presented in the Fig. 5(a). The windings of phase-A and phase-C that are connected to the inverter-1 will be effected due to OC in switch S_{11}. The positive peak of phase-C voltage and negative peak of Phase-A voltage are reduced and hence the currents in these two phases are decreased and distorted. The effect of OC in switch S_{13} on inverter performance is presented in Fig. 5(b). Since the switches S_{13}, S_{14}, S_{15} and S_{16} are connected to phase windings and hence OC in these switches will clamp the currents in respective phases to which they are connected. The positive wave of voltage is reduced and current is clamped in phase-A winding due to OC in

switch S_{13}. Similarly, an OC fault in switch S_{15} will reduce the voltage peak and clamp the current in negative cycle for phase-C. The peak magnitude of output voltage remains same but the number of levels decreases with OC fault in bidirectional switch S_{17} as illustrated in Fig. 5(c). The output voltages and currents with OC in switches S_{12} and S_{14} will be the vertical flip of the waveforms presented for switch S_{11} and S_{13} OC conditions. The proposed topology is tolerant for switch SC faults as well and the output results with FTS for switch SC faults will be same as the results presented for the complementary operating switches. For example, the outputs yielded with FTS for switch S_{11} OC will same as the results obtained with FTS for the switch S_{12} SC conditions. Hence the results with FTS for switch S_{17} SC fault condition are alone presented in Fig. 5(d).

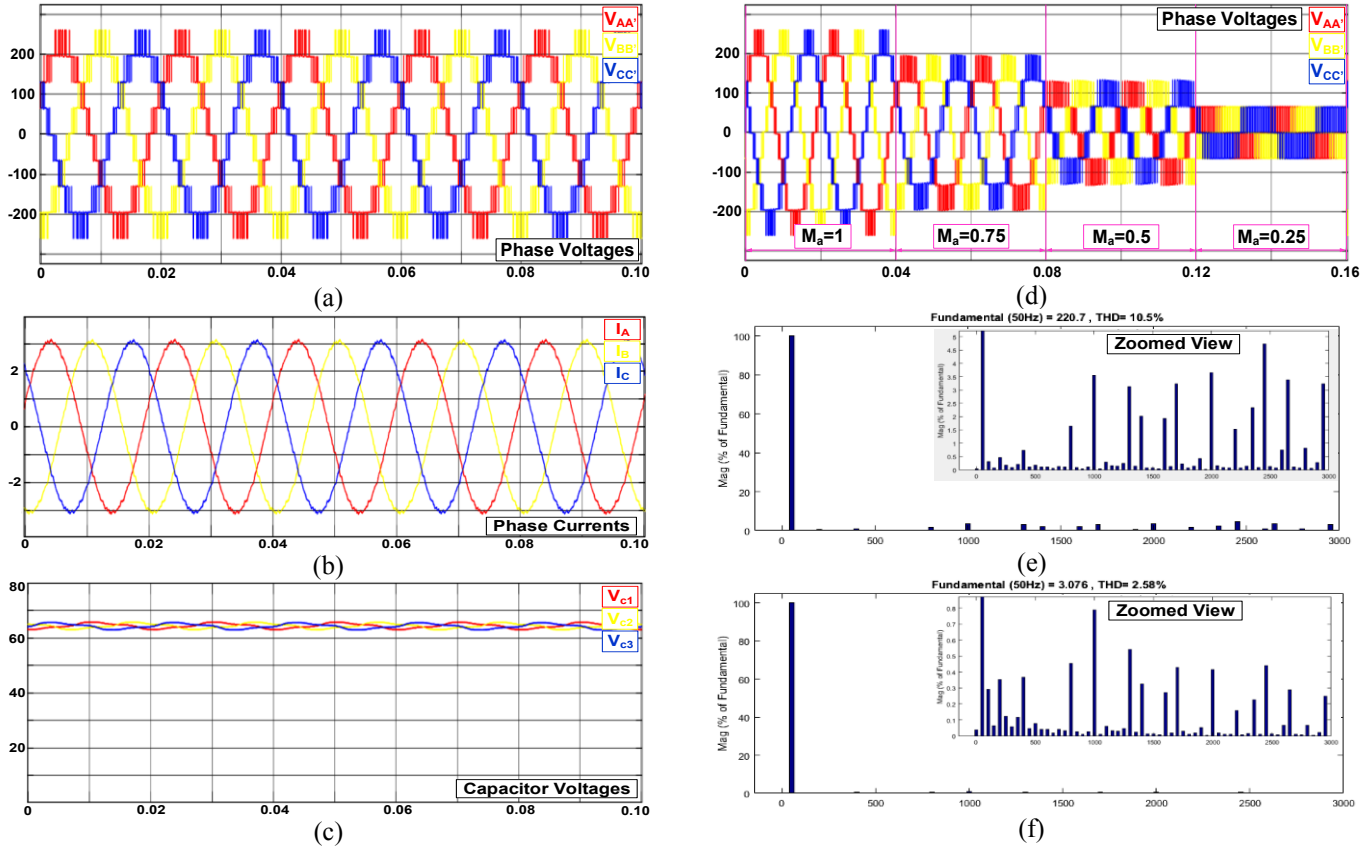

Fig. 4. Simulation results of (a) Three-phase output voltages, (b) three-phase currents at no-load (c) voltage across capacitors C_1, C_2 and C_3, (d) three-phase voltages with variation in modulation index, (e) FFT analysis for THD in output voltage (f) FFT analysis for THD in phase current.

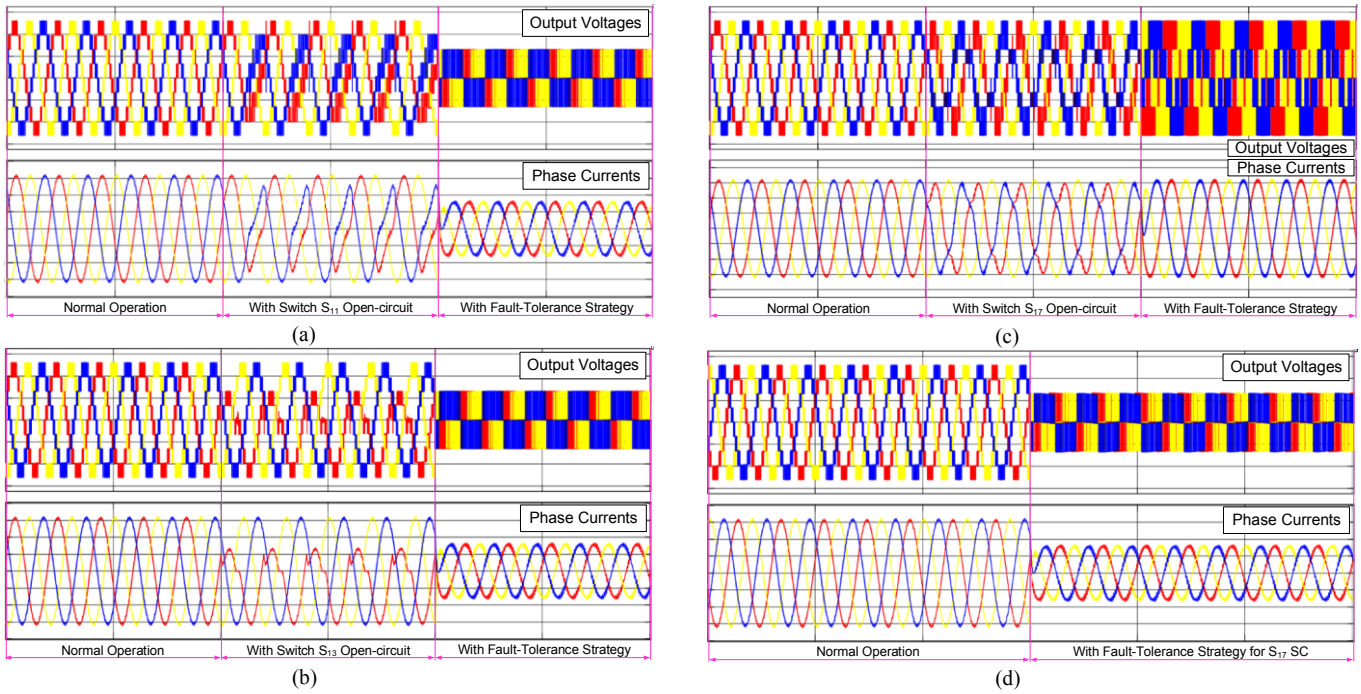

Fig. 5. Simulation results of three-phase output voltage and currents during normal, fault and with FTS (a) for OC in switch S_{11}, (b) for OC in switch S_{13}, (c) for OC in switch S_{17} OC, (d) for SC in switch S_{17}.

The performance of the induction motor with the change in load torque is presented in Fig. 6. The effect of load torque variation on the three-phase currents are presented in Fig. 6(a) and the variation of load torque is presented in Fig. 6(b). The changes in motor speed and voltage across the capacitors in all three inverters due to variation in load torque are presented in Fig. 6(c) and (d).

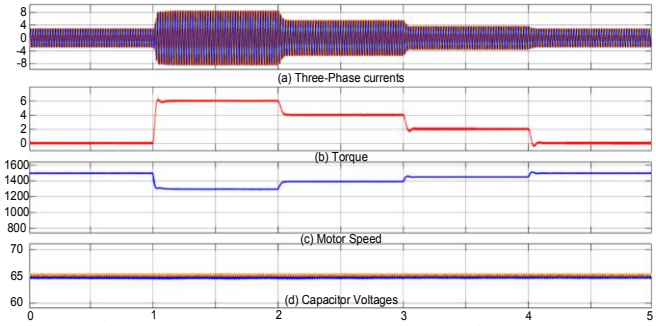

Fig. 6. Simulation results for change in load torque (a) Three-phase currents, (b) motor torque, (c) motor speed, (d) voltage across the capacitors.

The proposed topology exhibit advantages such as peak output voltage twice the source voltage and acceptance of conventional SPWM techniques for generating switching pulses but also suffers from shortcomings such as requirement of three isolated sources and non-modular construction. But the proposed topology can find application in battery electric vehicles (BEVs) designed with more number of batteries known as split battery technique for extending the drive range. However, the results presented prove that the proposed topology can be operated even with switch OC or SC fault conditions without need of any additional hardware and hence can be employed for drives applications for reliable operation.

VII. CONCLUSION

A nine-level inverter topology with fault-tolerance capability for switch faults designed with minimum number of switching devices is presented in this paper. The output voltage may be reduced during switch-fault conditions but safeguards continuousness in supply for reliable operation without the necessity of extra hardware. Sinusoidal modulation techniques which does not over burden digital processors for generating switching pulses are employed for the proposed topology. The performance of induction motor with possible faults in switches and variation in load torque are observed and the results are presented. The proposed topology finds applications in renewable energy generation systems such as solar cell or fuel cells fed electric drive applications where multiple sources with lower voltage ratings are employed.

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APPENDIX

Induction Motor specifications employed for simulation:

Specifications 3-phase, 4 Pole, 50 Hz, 415V, 1440 rpm, 2.2 kW.
Rated Torque 14.5 Nm
Stator & Rotor resistance 2.23 Ω & 1.17 Ω
Stator & Rotor leakage inductance 0.032 H & 0.032 H
Mutual inductance 0.198 H
Moment of inertia 0.051 kg.m^2