An Integrated Semi-Double Stage-Based Multilevel Inverter With Voltage Boosting Scheme for Photovoltaic Systems

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***Abstract*— This article proposes a single-phase, seven-level, transformerless inverter, employing a semi-double stage-based conversion technique, which is particularly suitable for photovoltaic (PV) applications. The proposed configuration achieves voltage boosting using a non-isolated interleaved buck-boost converter, which is fused with the inverter configuration through two switched capacitors (SCs). The interleaved front-end boost stage is capable of achieving a voltage gain of three while resulting in reduced peak current stress on the switching devices. In this topology, a part of the load power is transferred directly from the PV source, while the other part is transferred through the SCs. The proposed topology and the associated pulsewidth modulation (PWM) technique are capable of reducing the leakage current by isolating the terminals of the PV source in the freewheeling state. This article also presents a thorough analysis of the stray capacitor voltage and the common-mode voltage (CMV). These analyses reveal that the high-switching frequency transitions are eliminated in both of these waveforms. Furthermore, the proposed topology results in the reduction of low-frequency transitions in the stray capacitor voltage and the CMV, which in turn result in further reduction of the leakage current. The simulation and experimental results are in agreement with the mathematical analysis of the proposed inverter.**

***Index Terms*— Leakage current minimization, multilevel inverter (MLI), photovoltaic (PV) systems, pulsewidth modulation (PWM) inverters, semi-double stage system, voltage boosting.**

I. Introduction

THE ever increasing demand for electrical energy across the globe is the principal reason for severe power shortage. The detrimental effects on the global environment caused by power generation with fossil fuels motivate the need to promote renewable energy sources (RESs). These include solar, wind, and tidal power systems. Sustainability along with zero pollution are the most attractive features of the RES. Among all RESs, photovoltaic (PV)-based systems have become very popular, and are the center of focus for investment across the globe due to their features of low maintenance, noiseless operation, small size, reliability, and emission-free operation. In any PV inverter system, a major portion of the cost depends on any type of power conditioning unit (PCU). Based on the existence of isolation transformers in PCUs, PV inverters can be classified into isolated and non-isolated types. The non-isolated PV inverters received more attention over isolated inverters, as they avoid the use of expensive and bulky isolation transformers and also improve the overall power density and efficiency of the PV system. However, non-isolated PCUs do not have galvanic isolation between PV source terminals and load terminals. The capacitive nature of parasitic elements of the PV panel produces common mode leakage current (CMLC). The peak value of leakage current varies with the parasitic capacitance, which depends on the frame structure, humidity, weather conditions etc. The typical value of parasitic capacitance varies between 10 and 300 nF for mono-crystalline types of PV panel [1].

The common-ground based topologies completely eliminate the CMLC, as the stray capacitor voltage is constant irrespective of the voltage levels. This was demonstrated for the existing power circuit configurations such as: 1) NPC inverter [2]; 2) T-type inverter [3]; 3) ANPC inverter [4]; 4) flying capacitor (FC); 5) active virtual ground, etc. However, these topologies suffer from some drawbacks such as higher number of clamping diodes, FCs, semiconductor devices, voltage balancing of dc-link capacitors, and under-utilization of dc-bus. Besides that, several approaches [5] are also reported to mitigate the CMLC in various multilevel inverter (MLI) configurations such as: cascaded H-bridge (CHB)-based MLI structure by isolating the PV source and the grid in the freewheeling state. These modified configurations can be classified as dc side decoupling and ac side decoupling. But the existing MLI configurations do not provide any voltage boosting action beyond the input voltage. Therefore, for both grid-connected and standalone inverter applications, the dc-link is maintained by including a boosting stage [6]. This would address the issues of low-voltage problems caused by varying environmental conditions (including partial shading). This type of system is considered as a double-stage power-processing system [7]. However, these circuit configurations reduce the overall efficiency and also increases the switching device ratings in the boosting stage [8], [9].

The concept of switched capacitors (SCs) has been introduced in [10] and [11], in order to achieve multilevel operation along with the voltage boosting capability. However, the increased number of SCs in the configuration increases the size and reduces the overall power density of the inverter. Furthermore, SCs (which are generally bulky at those rating) also increase the peak current stress of the

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associated switches up to six to ten times of load current [12], depending on the loading condition of the inverter. This reduces the efficiency and the performance of the inverter configurations for high-power applications. It also reduces the durability and life-time of the semiconductor devices, which lead to an increased chance of failure of the system [13].

Some solutions have been proposed by J. Roy, Y. Xia, and R. Ayyanar [14] to alleviate the current stress on semiconductor devices. A technique of partial charging of the dc bus capacitor has been proposed by J. Wu and C. Chou [15]. In this manuscript, a seven-level (7-L) inverter topology, configured with an asymmetrical charged dc bus capacitor and a polarity generator configuration is proposed. A high-frequency transformer is used in this article to charge the dc bus capacitors with parallel processing of input PV power. Though the power circuit requires a single PV source, a boost converter is required on the input side of the converter. An improvised SC technique with a bi-directional buck-boost converter is proposed by Y. Xia, J. Roy, and R. Ayyanar [16]. In this article, a common ground transformerless inverter has been proposed to reduce the size requirement of the capacitor and the current stress over the switches. However, this topology achieves single-stage power conversion at the expense of multilevel operation. A new charge-pump concept is introduced by Ardashir et al. [17] to limit the current stress in semiconductor devices. However, the two-stage charge transfer operation increases the number of passive devices, which are involved in the process of power transfer [18].

A novel configuration for voltage boosting in a single stage by incorporating a buck-boost converter in the configuration is proposed by S. V. Araujo, P. Zacharias, and R. Mallwitz [19]. This article introduces a novel methodology for generating more voltage levels by charging the SC. The leakage current is minimized by employing a modified dc-decoupling technique. However, the analysis of common mode voltage (CMV) dv/dt transitions and leakage current is not reported in this article. The operation of the inverter and the converter in DCM and critical conduction mode (CCM)-DCM modes of operation is also not presented. Furthermore, the design and rating of the converter are also not analyzed in [30].

This manuscript presents a new integrated PV system, wherein a semi-double-staged voltage boosting network is fused into 7-L MLI. The proposed MLI configuration employs two half-bridges (HB) and one full H-bridge in its structure. Also, it contains an highly efficient and reliable inverter configuration (HERIC) leg to mitigate the issue of the leakage current due to the parasitic elements of the PV panel. The advantage of the proposed integrated PV system is that it needs only one PV source and two symmetrical SCs to synthesize a 7-L output voltage waveform with unipolar pulsewidth modulation (PWM) switching. Some unique features of the proposed inverter are mentioned below.

1) The configuration contains an interlinking high dc voltage, which is about three times that of the input PV voltage.
2) As the proposed PV system contains a single PV source, the implementation of MPPT algorithms is simplified.
3) The proposed configuration exhibits a structural symmetry, which increases the redundancy in the switching state. This feature facilitates devising PWM schemes, which have an inherent capability of balancing the voltage across the dc-link capacitors.
4) Owing to the structural symmetry of the proposed power circuit configuration, it is possible to devise symmetrical PWM schemes. Hence, the power losses are evenly distributed among the power semiconductor switching devices.
5) The proposed topology is capable of transferring nearly 36% of the total energy processed in single-stage conversion. The rest of the energy is equally shared between the two SCs, which is fed by an interleaved buck-boost converter.
6) Due to employment, single carrier-based implementation of the PWM scheme on a digital control platform is very much simplified. Furthermore, the PWM scheme described in this article achieves a seamless transition among various voltage levels present in the voltage source inverter (VSI). This PWM scheme can easily be extended for higher number of voltage levels.
7) The proposed inverter needs twelve switching devices to generate a 7-L waveform. Of these twelve devices, six devices are switched at a fundamental frequency (50 Hz), while other switches are driven at a high frequency in a given half-cycle. This ensures an overall reduction of switching power loss in the system.

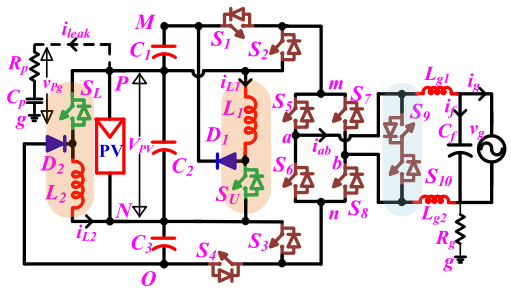

Fig. 1. Circuit schematic for the 7-L MLI with the PV source and parasitic elements.

Apart from achieving the aforementioned features of the proposed topology and the associated PWM technique, this article also presents a detailed analysis of the stray capacitor voltage, CMV, and leakage currents with the aid of switching theory. It is also shown that the PWM scheme employed in this article is capable of complying with the VDE-0126-1-1 [5] standards. The simulation results and experimental results obtained from the laboratory prototype validate the mathematical analysis of the proposed topology and the associated PWM scheme.

II. Operation Principle of the Proposed 7-L MLI

A. General Description

The schematic circuit of the proposed single-PV source-fed 7-L MLI is shown in Fig. 1. The proposed configuration employs two SCs (C_1, C_3), one dc-link capacitor (C_2), twelve semiconductor switches, two high-frequency inductors (L_1, L_2), two filter inductors (L_{g1}, L_{g2}), and one filter capacitor (C_f). The resistance in the ground path is indicated by R_g. The variable v_g refers to the instantaneous grid voltage.

TABLE I
SWITCHING STATES FOR THE RESPECTIVE OUTPUT VOLTAGE LEVELS

Output Voltage v_{ab}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$+3V_{PV}$	1	0	0	1	1	0	0	1	1	0
$+2V_{PV}$	1	0	1	0	1	0	0	1	1	0
$+2V_{PV}$	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**
$+V_{PV}$	0	1	1	0	1	0	0	1	1	0
0	0	1	1	0	0	0	0	0	1	0
0	0	1	1	0	0	0	0	0	0	1
$-V_{PV}$	0	1	1	0	0	1	1	0	0	1
$-2V_{PV}$	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**
$-2V_{PV}$	0	1	0	1	0	1	1	0	0	1
$-3V_{PV}$	1	0	0	1	0	1	1	0	0	1

The parasitic resistance and capacitance of the PV panels are denoted R_p and C_p, respectively, in Fig. 1. The currents through the high-frequency inductor is denoted i_{L1} and i_{L2}, respectively. The variables i_{ab}, i_f, i_g, and i_{leak}, respectively, represent the output current of the 7-L MLI, the current flowing through the filter capacitor, the current injected into the grid (load current), and the induced leakage current flowing between the PV array and the ground through the parasitic elements of the PV panel.

Each SC (C_1, C_3) of the proposed configuration is energized through an interleaved buck-boost converter, which is composed of two MOSFETs, two inductors, and two diodes. The SCC_1 is being charged through S_U, L_1, and D_1, whereas the capacitor C_3 is charged through S_L, L_2, and D_2. Both the SC C_1 and SCC_3 are being charged up to the same voltage level as that of the input PV voltage (V_{PV}). The proposed inverter configuration also contains four pairs of HB legs (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) and one bi-directional switch (S_9, S_{10}) which generates seven distinct levels in the output voltage waveform. The devices in the pair S_1 and S_2 are switched complimentarily. Similarly, the devices in the pair S_3 and S_4 are also switched complementarily. In order to avoid the high switching frequency operation of these switches (S_1, S_2, S_3, and S_4), switching states of these switches are not altered during the freewheeling state from the previous active switching state. These switch-pairs switch the voltages V_{C1} and V_{C3} (in Fig. 1) and determine the voltage across the points "m" and "n" (i.e., v_{mn}). However, the switches (S_5, S_6, S_7, and S_8), which constitute the H-bridge, are not switched in a complementary fashion in order to isolate the PV and the grid in the freewheeling state.

B. Switching State Description With Different Modes of Operation

The switching states of individual devices to obtain various voltage levels in the proposed circuit configuration are enumerated in Table I. The equivalent circuit of the proposed inverter for each level of operation is shown in Figs. 2–5. Corresponding to the output voltage levels $+/-3V_{PV}$, $+/-2V_{PV}$, $+/-V_{PV}$, and 0, four distinct modes of operation exist in the proposed power circuit. The operation of the power circuit in these four modes is described in the following.

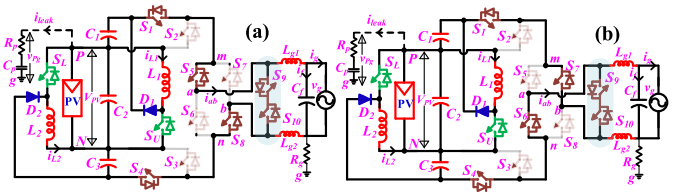

Fig. 2. Mode I operation for the proposed 7-L MLI for (a) positive and (b) negative half-cycle.

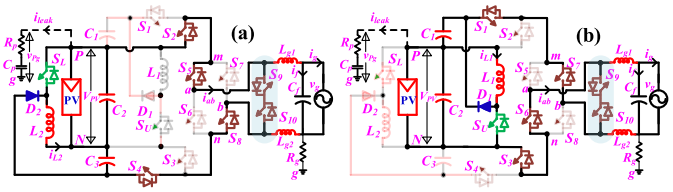

Fig. 3. Mode II operation for the proposed 7-L MLI for (a) positive and (b) negative half-cycle.

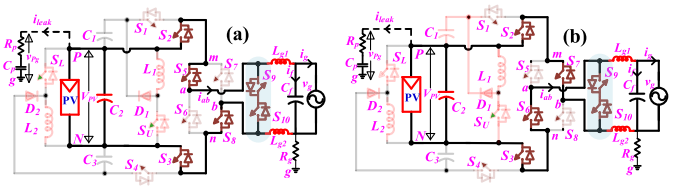

Fig. 4. Mode III operation for the proposed 7-L MLI for (a) positive and (b) negative half-cycle.

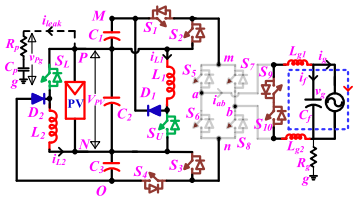

Fig. 5. Mode IV (freewheeling state) operation for the proposed 7-L.

Mode I: The proposed power circuit exhibits this mode of operation, when both the SC (C_1 and C_3) is charged up to V_{PV} and switches S_1 and S_4 are turned on. Due to this switching operation, $3V_{PV}$ appears across the terminals "m" and "n" (i.e., v_{mn} = 3 V_{PV}). Then, by turning on either the pair (S_5, S_8) or the pair (S_6, S_7) from the polarity generator circuit, it is possible to impress $+3V_{PV}$ or $-3V_{PV}$ across the load, respectively, as shown in Fig. 2(a) and (b).

Mode II: In this mode of operation, the voltage across the terminals "m" and "n" is $2V_{PV}$(i.e., $v_{mn} = 2V_{PV}$). This can be achieved by energizing any one of the SCs among C_1 and C_3 and turning ON the associated switch (S_1 or S_4). So, out of these redundancies, SC C_3 is energized during the positive half-cycle, whereas C_1 is energized during the negative half-cycle, in order to equalize the utilization over a fundamental period. Then, by turning on either the pair (S_5, S_8) or the pair (S_6, S_7) from the polarity generator circuit, it is possible to generate $+2V_{PV}$ or $-2V_{PV}$ across the load, respectively, as shown in Fig. 3(a) and (b).

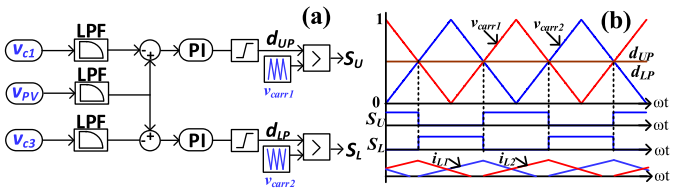

Fig. 6. (a) Closed-loop voltage control scheme. (b) Phase-shifted carrier employed for the front-end buck-boost converter.

Mode III: In this mode of operation, both the switches S_1 and S_4 are turned off, as neither of the SCs are utilized. Hence, V_{PV} appears across the terminals "m" and "n" (i.e., $v_{mn} = V_{PV}$). Thereafter, either the pair (S_5, S_8) or the pair (S_6, S_7) from the polarity generator circuit is turned on to generate $+V_{PV}$ or $-V_{PV}$ across the load, as shown in Fig. 4(a) and (b).

Mode IV: The most important feature of this mode of operation is the isolation or disconnection between the PV source and the grid. If the freewheeling state is obtained by turning on the devices S_5 and S_7, there exists a path of conduction between the positive terminal of PV and the freewheeling point through the body diode of S_2. A similar conduction path exists from the PV negative terminal due to the body diode of S_3 (when freewheeling is affected by turning on the devices S_6 and S_8). Lack of isolation between the PV source terminals and the grid leads to high-frequency voltage transitions in the stray capacitor voltage (i.e., across the PV positive terminal and the load ground terminal) [19]. Therefore, isolation is achieved by turning off all of the switches in the polarity generator circuit, as shown in Fig. 5. In order to provide the freewheeling path for the inductive current component during each ZERO state transition, either S_9 or S_{10} switch is turned on during the positive half-cycle and the negative half-cycle, respectively. Due to this switching action, the terminals of the PV panel are isolated from the grid terminals, which employ a high impedance path for the leakage current.

III. Modulation Strategy and Control Scheme of the Proposed 7-L MLI

As mentioned in Section II, the proposed system requires a single PV source and two SCs (C_1, C_3) to synthesize the 7-L output voltage waveform. The SCs are energized/charged through the front-end interleaved buck-boost converter, which consisted of two switches (S_U, S_L), two inductors (L_1, L_2), and two diodes (D_1, D_2), with the same voltage magnitude as that of the input PV voltage. The transitions in the output voltage always occur between zero voltage level and a specific level of level depending on the modes of operation, as discussed earlier. This switching action allows the configuration to eliminate the switching-frequency transitions in the stray capacitor voltage v_{Pg}.

This section describes the control scheme for charging the SCs, logical implementation of modulation strategy, and the analysis of the stray capacitor voltage v_{pg}.

A. Control Scheme for Charging SCs

An interleaved-based PWM technique is employed for the front-end buck-boost converter to extract power symmetrically from the PV source. The implementation of the control scheme and PWM generation are shown in Fig. 6(a). It can be observed that the carrier signals (v_{carr1}, v_{carr2}) are phase shifted by π radians to obtain interleaved PWM pulses. The capacitors (C_1 and C_3) are charged in alternative switching half cycles, which reduce the peak current stress on the PV source irrespective of the loading conditions. The duty factors for the lower and upper sections of boosting stages are, respectively, denoted d_{LP} and d_{UP}. To implement effective voltage control over the SCs, the boundary condition of CCM-DCM has been chosen to design the inductors and capacitors for the converter [20]. Assuming the converter is operating in the DCM-CCM, the voltage across the capacitor can be expressed as follows:

$$V_{C1} = \frac{d_{UP}}{1 - d_{UP}} V_{PV} \tag{1}$$

$$V_{C3} = \frac{d_{LP}}{1 - d_{LP}} V_{PV}. \tag{2}$$

A simple voltage mode-based closed loop control scheme is implemented with a linear PI regulator to maintain the same voltage at the SCs C_1 and C_3. The output of the PI regulator is limited to such a value that the maximum value for both the duty ratios (i.e., d_{LP} and d_{UP}) is 0.5 [see Fig. 6(b)]. This scheme improves the dynamic response of the capacitor voltages under various loading conditions of the inverter.

B. Generation of Voltage Levels

To generate the switching pulses for the inverter, a fundamental modulation wave with a modulating factor of m_a is considered as per the following equation:

$$v_m = m_a sin\omega t. \tag{3}$$

As a single carrier-based PWM scheme is adopted, it is required to modify the modulation signal to synthesize a 7-L output. Depending on the modulating factor (m_a), the modulating signal is modified in order to achieve the generation of a 7-L PWM signal. The modified reference signals are chosen, based on the mode of operation described in the previous section, as follows:

$$\text{Mode III}: v_{ref1} = v_m, \quad \text{when } 0 \le |v_m| < 0.33 \text{ switching actions from } V_{PV} \text{ to } 0 \tag{4}$$

$$\text{Mode II}: v_{ref2} = \frac{v_m}{2}, \quad \text{when } 0.33 \le |v_m| < 0.67 \text{switching actions from } 2V_{PV} \text{ to } 0. \tag{5}$$

$$\text{Mode I}: v_{ref3} = \frac{v_m}{3}, \quad \text{when } 0.67 \le |v_m| < 1 \text{ switching actions from } 3V_{PV} \text{ to } 0. \tag{6}$$

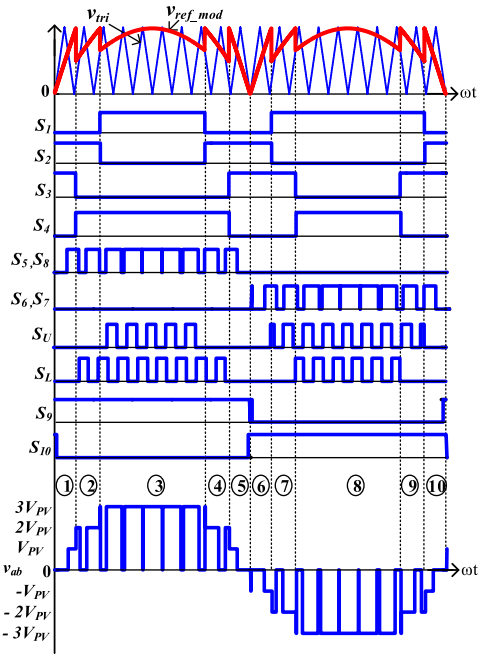

Fig. 7. Modified reference signal and PWM generation for the switches.

TABLE II
FACTORS OF DIFFERENT MODULATION INDEXES

Operation	Modulation limits	rv_1	rv_2	g_1	g_2
Seven-level	$1 < m_a \leq 0.67$	0.33	0.67	0.33	0.5
Five-level	$0.67 < m_a \leq 0.33$	0.5	1	0.5	0
Three-level	$0.33 < m_a \leq 0$	1	1	0	0

The modified reference signal (v_{ref_mod}) is obtained by concatenating individual reference signals, as given in (4)–(6) and shown in Fig. 7. The modified reference signal is compared with the symmetrical triangular carrier wave (v_{tri}) to achieve the 7-L output of the proposed inverter. In order to generate the switching pulses for the switches S_9 and S_{10}, the fundamental modulation wave (v_m) is compared with zero to identify the duration of the positive and negative half cycles. In other words, S_9 is turned on throughout the positive half cycle, while S_{10} is turned on throughout the negative half-cycle. Table II shows the relationship between the modulation index (m_a) and the voltage levels in the output of the proposed inverter. The implementation of the modulation technique for the proposed inverter is shown in Fig. 8. The reference variables rv_1, rv_2 and the gains g_1, g_2, which are used for the implementation of control scheme, are also defined in Table II. Whenever the magnitude of the modified reference signal is greater than that of the carrier, the switching pattern corresponding to the voltage level, as determined by the mode of operation [see (4)–(6)], is generated (see Table I). It can be observed that the switching pattern is chosen in such a way that only two devices toggle their switching state in any given half-cycle, leading to the reduction of switching power losses in semiconductor devices.

To achieve full utilization of the PV source, an MPPT algorithm is employed. In order to validate the proposed configuration with MPPT, the well-known Perturb and Observe

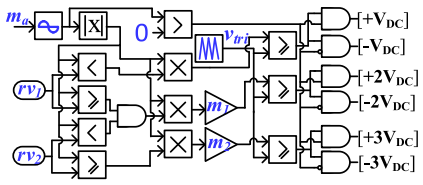

Fig. 8. Logical implementation for the modified-modulation signal from the modulation index m_a.

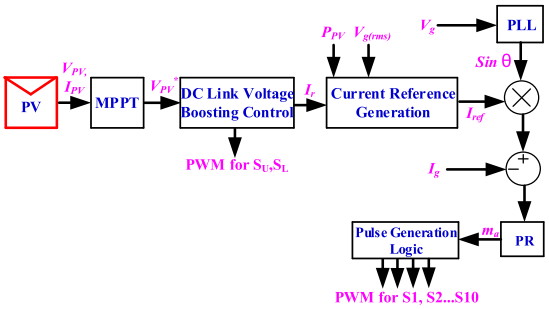

Fig. 9. Block diagram of the control scheme.

(P&O) algorithm can be implemented. Both the PV voltage (V_{PV}) and PV current (I_{PV}) are to be sensed to implement the MPPT algorithm [21]. The MPPT algorithm outputs the value of the modulation factor (m_a), which generates the modified reference signal for the inverter to synthesize the output.

The block diagram of the control scheme to inject power into a grid is shown in Fig. 9 In this scheme, an MPPT controller provides the reference voltage (V_{PV}*) to the dc-link boosting controller. Thereafter, a reference current (I_{ref}) is generated via the current controller, considering the available PV power (P_{PV}) and the rms voltage of the grid ($V_{g(rms)}$). A proportional resonant (PR) control is used to control the grid current [22], [25] with respect to the reference current. The output of the PR controller is the modulation index m_a, which acts as an input to the logical implementation of the proposed PWM technique, as presented in Fig. 8.

C. Analysis of Power Transmission Ratio

The proposed configuration processes the PV power either with only single-stage or with double-stage conversion. In the double-stage conversion mode, a second converter is augmented to the PV source. The second converter is an interleaved buck-boost converter. In order to design the second converter, instantaneous power utilization ratios (IPURs) are derived for the PV source and each SC. The extracted power from the PV source and the SCs is derived by the following equations:

$$P_{C1} = S_1 v_{ref\_\mathrm{mod}} V_{C1} i_g \tag{7}$$

$$P_{C3} = S_4 v_{ref\_\mathrm{mod}} V_{C3} i_g \tag{8}$$

$$P_S = v_{ref\_\mathrm{mod}} V_{PV} i_g. \tag{9}$$

Now, the IPUR is the ratio of power extracted from a given particular SC or the PV source to the total power processed through the inverter. The IPUR for the PV source and the SCs (C_1 and C_3) is represented by P_{S_ratio}, P_{C1_ratio},

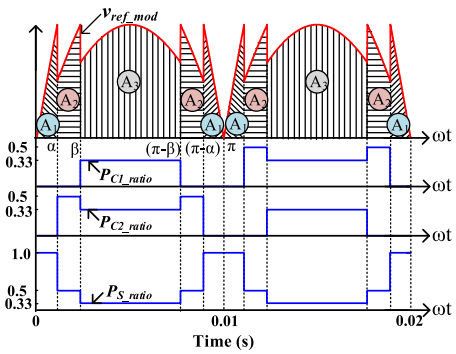

Fig. 10. IPURs for the PV source and SCs (C_1 & C_3).

and P_{C2_ratio}, respectively. The relationship between these variables is as follows:

$$P_{C1\_ratio} = \frac{P_{C1}}{P_{C1} + P_{C3} + P_s} \tag{10}$$

$$P_{C3\_ratio} = \frac{P_{C3}}{P_{C1} + P_{C3} + P_s} \tag{11}$$

$$P_{S\_ratio} = \frac{P_S}{P_{C1} + P_{C3} + P_s}. \tag{12}$$

The IPUR for the PV source (P_{S_ratio}) and the SCs C_1 and C_3 (P_{C1_ratio}, P_{C3_ratio}) is plotted with respect to time in Fig. 10. It can be observed that the peak power utilization ratio of the SCs is only 50% of the total power demand. Thus, it is evident that the upper and lower sections of the interleaved buck-boost converter are required to be designed for only 50% of the full load rating of the inverter.

In order to establish the energy utilization factor mathematically among the PV source and the SC, the total energy for a given fundamental cycle is calculated as follows:

$$E = 2 * \int_0^{\pi} (V_{C1} + V_{C2} + V_{C3}) * i_g * d(\omega t) \tag{13}$$

$$i_g = I_m \sin(\omega t - \phi) \tag{14}$$

where V_{C1} and V_{C3} are voltages across the SCs (C_1 and C_3), V_{C2} is the voltage across the PV source, and i_g is the load current.

As mentioned earlier, the extracted PV energy is either directly delivered to the load (single-stage operation) or via the energized SCs C_1 and C_3 (double-stage operation). The symbol E_S denotes the energy delivered to the load in a single-stage operation. Similarly, $E_{C1}$and E_{C3}, respectively, denote the energies transferred to the load from the SCs C_1 and C_3. The total energy extracted from the PV source is transferred to the load either through a single-stage operation (E_s) or through SCs (E_{C1} & E_{C3}). The expression for the total energy can be as follows:

$$E = \int (V_{C1}) * i_g * d(\omega t) + \int (V_{C2}) * i_g * d(\omega t) + \int (V_{C3}) * i_g * d(\omega t) \tag{15}$$

$$E = E_{C1} + E_{C3} + E_s. \tag{16}$$

It is assumed that the SCs (C_1, C_2) are charged to the same voltage as that of the input PV voltage. That is

$$V_{C1} = V_{C2} = V_{C3} = V_{PV}. \tag{17}$$

From Fig. 10, it can be observed that in order to calculate E_{C1}, E_{C3}, and E_S, the area under the modified modulation curve is to be determined. The relation between the area (E_{A1}, E_{A2}, E_{A3}) and the capacitors (E_{C1}, E_{C3}, E_S) is given as follows:

$$E_S = 2^*(2E_{A1} + 2E_{A2} + E_{A3}) \tag{18}$$

$$E_{C1} = (E_{A3}) + (2E_{A2} + E_{A3}) \tag{19}$$

$$E_{C3} = (2E_{A2} + E_{A3}) + (E_{A3}). \tag{20}$$

The energy under the section of areas A_1, A_2, and A_3 can be calculated as per the following equation:

$$E_{A1} = \int_0^{\alpha} V_{PV}{}^*(m_a \sin(\omega t))^*(I_m \sin(\omega t))d(\omega t) \tag{21}$$

$$E_{A2} = \int_{\alpha}^{\beta} V_{PV}{}^* \left(\frac{m_a}{2} \sin(\omega t)\right)^*(I_m \sin(\omega t))d(\omega t) \tag{22}$$

$$E_{A3} = \int_{\beta}^{(\pi-\beta)} V_{PV}{}^* \left(\frac{m_a}{3} \sin(\omega t)\right)^*(I_m \sin(\omega t))d(\omega t). \tag{23}$$

The average energy utilization factor for the PV source (E_{s_fund}) and each SC (E_{C1_fund} & E_{C3_fund}) can be derived using (13)–(23) as follows:

$$E_{C1\_fund} = \frac{E_{C1}}{E} \times 100\% = 31.5\% \tag{24}$$

$$E_{C3\_fund} = \frac{E_{C3}}{E} \times 100\% = 31.5\% \tag{25}$$

$$E_{S\_fund} = \frac{E_S}{E} \times 100\% = 37\%. \tag{26}$$

From these numerical values, it is evident that 37% of energy is transferred directly to the load through single-stage conversion. The rest of 63% is transferred through the double-stage conversion. The 63% double-stage power transfer is shared equally between the two SCs. Though the peak power handled by each of the SC is 50% (see Fig. 10), the average energy transferred to the load is 31.50% of the total energy. In contrast, in the case of the conventional dc–dc converter-based boosting method, the total PV power has to be processed through the dc–dc conversion stage. This shows that the structure of the proposed power circuit configuration inherently displays the capability to process energy efficiently while boosting the input PV voltage. Moreover, it can be observed that the values of both E_{C1_fund} and E_{C3_fund} are the same. It implies that the average energy transferred in a given fundamental period through the SCs (C_1 and C_3) is the same. This helps in self-balancing the SCs, and it enables the structure to be operated in the open loop condition in a fixed load condition. This feature achieves the voltage balancing of the SCs, alleviating the burden on the closed loop system, which is described earlier.

D. Analytical Expression of Stray Capacitor Voltage (v_{Pg}) and CMV

Now, the generation of leakage current in parasitic elements of PV panel, due to the high-frequency transitions in the stray capacitor voltage (v_{Pg}), is one of the significant issues of PV inverter configurations. To address the issue of leakage current in the proposed inverter, a modified modulation technique,

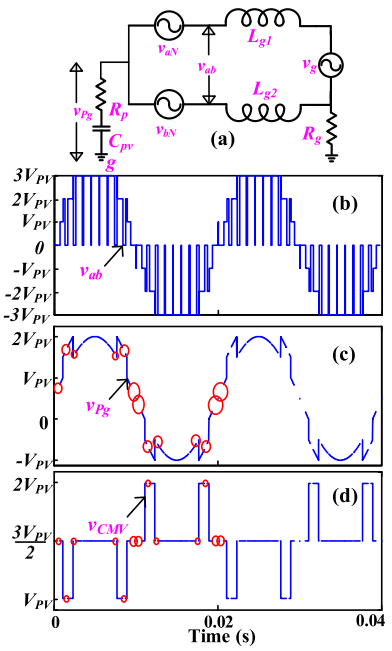

Fig. 11. (a) Equivalent common mode circuit of the inverter. Analytical waveforms of (b) output voltage, (c) stray capacitor voltage, and (d) CMV.

described in the previous section, is employed. The nature of leakage current can be analyzed mathematically by deriving an expression for the stray capacitor voltage with respect to the terminal points M, P, N, and O, as shown in Fig. 1. It may be noted that the PV source is connected across the points P and N (see Fig. 1). Therefore, to analyze the leakage current through the PV panel, the stray capacitor voltage υ_{Pg} is derived mathematically. The SS_x represents the switching function for the switch S_x with (S_1, $S_2, S_{3.....}S_{10}$). The value of SS_X is "1" or "0" with respect to the switching state of S_X (turned on or off), respectively. Applying the superposition theorem and using switching functions, the voltage υ_{Pg} (see Fig.1) can be expressed as follows:

$$\upsilon_{Pg} = SS_1\upsilon_{Pg1} + SS_2\upsilon_{Pg2} \tag{27}$$

where υ_{Pg1} and υ_{Pg2} are the voltages at the P terminal of the PV source with respect to the ground "g" when S_1 and S_2 are turned on, respectively. The following paragraph presents the analysis pertaining to the switching modes of switch S_1.

Case 1 (When S_1 is Turned ON): In this case, from the following equation, it is noted that it is required to evaluate $\upsilon_{Mg1}$to derive an expression of υ_{Pg1}:

$$\upsilon_{Pg1} = \upsilon_{Mg1} - V_{PV}. \tag{28}$$

Similarly, other terminal point equations (υ_{Og1}, υ_{Ng1}) can also be expressed in terms of υ_{Mg1} as follows:

$$\upsilon_{Og} = \upsilon_{Mg1} - 3V_{PV} \tag{29}$$

$$\upsilon_{Ng} = \upsilon_{Mg1} - 2V_{PV}. \tag{30}$$

The inverter output terminal voltages υ_{ag} and υ_{bg} are also derived using the switching function analysis. From Fig. 1, υ_{ag} and υ_{bg} are expressed in terms of υ_{Mg1}, υ_{Ng1}, and υ_{Og1} as follows:

$$\upsilon_{ag} = SS_1SS_5\upsilon_{Mg1} + (1 - SS_3)SS_6\upsilon_{Og} + SS_3SS_6\upsilon_{Ng} \tag{31}$$

$$\upsilon_{bg} = SS_1SS_7\upsilon_{Mg1} + (1 - SS_3)SS_8\upsilon_{Og} + SS_3SS_8\upsilon_{Ng}. \tag{32}$$

Using KCL to the circuit shown in Fig. 11(a), the relation between υ_{ag}, υ_{bg}, and grid voltage υ_g can be expressed as follows:

$$\upsilon_{ag} + \upsilon_{bg} = \upsilon_g. \tag{33}$$

Now, substituting the υ_{ag}, υ_{bg} expression [see (31) and (32)] into the above expression [see (33)] and simplifying, we get

$$\upsilon_{Mg1} = \frac{\upsilon_g + 3V_{PV}(SS_6 + SS_8) - V_{PV}SS_3(SS_6 + SS_8)}{SS_1SS_5 + SS_1SS_7 + (SS_6 + SS_8)}. \tag{34}$$

The voltage υ_{Pg1} is obtained by substituting υ_{Mg1} [see (34)] into (28)

$$\upsilon_{Pg1} = \frac{\upsilon_g + 3V_{PV}(SS_6 + SS_8) - V_{PV}SS_3(SS_6 + SS_8)}{SS_1SS_5 + SS_1SS_7 + (SS_6 + SS_8)} - V_{PV}. \tag{35}$$

Case 2 (When S_1 is Turned OFF): In this case, the expressions for the voltages in terminal points (N, O) υ_{Ng1} and υ_{Og1} are as follows:

$$\upsilon_{Og} = \upsilon_{Pg2} - 2V_{PV} \tag{36}$$

$$\upsilon_{Ng} = \upsilon_{Pg2} - V_{PV}. \tag{37}$$

Similarly, the inverter output terminal voltages can be expressed as

$$\upsilon_{ag} = (1 - SS_1)SS_5\upsilon_{Pg2} + (1 - SS_3)SS_6\upsilon_{Og} + (1 - SS_3)SS_6\upsilon_{Ng} \tag{38}$$

$$\upsilon_{bg} = (1 - SS_1)SS_7\upsilon_{Pg2} + (1 - SS_3)SS_8\upsilon_{Og} + (1 - SS_3)SS_8\upsilon_{Ng}. \tag{39}$$

Similarly, from (33), (36)–(40), one obtains

$$\upsilon_{Pg2} = \frac{\upsilon_g + 2V_{PV}(SS_6 + SS_8) - V_{PV}SS_3(SS_6 + SS_8)}{(1 - SS_1)(SS_5 + SS_7) + (SS_6 + SS_8)}. \tag{40}$$

Substituting υ_{Pg1} and υ_{Pg2} [see (35) and (40)] in (27) , the total stray capacitor voltage can be obtained.

Besides that, the CMV can be calculated from the following equation:

$$\upsilon_{CMV} = (\upsilon_{ag} + \upsilon_{bg})/2. \tag{41}$$

The CMV and the stray capacitor voltage are simulated using MATLAB. The following parameters are used for simulating the equations: 1) frequency of carrier = 1 kHz and 2) grid frequency = 50 Hz. In simulation studies, the frequency of the carrier wave was restricted to 1 kHz, to facilitate easy visualization of the discontinuities associated with undefined states in the stray capacitor voltage and the CMV. The stray capacitor voltage (υ_{Pg}) and the CMV (υ_{CMV}) are, respectively, shown in Fig. 11(c) and (d) for two grid cycles and the undefined states are encircled with red color. The voltage transitions in the stray capacitor voltage and the CMV for different switching combinations are also tabulated in Table III. It can be observed from Fig. 11(c) and (d) that the isolation between the grid and the PV module during the freewheeling state results in a discontinuity in the stray capacitor voltage and the CMV waveform. The discontinuities observed in the stray capacitor voltage and the CMV are due to the undefined values, arising out of the division by zero, within the simulation process. However, in practical circuits, the stray capacitor voltage and

TABLE III
STRAY CAPACITOR VOLTAGE AND CMVS OBTAINED FOR ALL SWITCHING STATES

Region	Output Voltage v_{ab}	S_1	S_3	S_5, S_8	S_6, S_7	S_9	Stray capacitor voltage v_{Pg}	CMV v_{CMV}
1	0	0	0	0	0	1	undefined	undefined
	V_{PV}	1	1	0	1	1	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$
2	0	0	0	0	0	1	undefined	Undefined
	$2V_{PV}$	1	1	0	0	1	$V_{PV}+\frac{e_g}{2}$	V_{PV}
3	0	0	0	1	0	1	undefined	Undefined
	$3V_{PV}$	1	1	1	0	1	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$
4	0	1	1	1	0	0	undefined	undefined
	$-V_{PV}$	1	0	1	0	0	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$
5	0	1	1	0	1	0	undefined	undefined
	$-2V_{PV}$	1	0	0	1	0	$\frac{e_g}{2}$	$2V_{PV}$
6	0	1	1	1	1	0	undefined	undefined
	$-3V_{PV}$	1	0	1	1	0	$\frac{V_{PV}}{2}+\frac{e_g}{2}$	$\frac{3V_{PV}}{2}$

the CMV are continuous, and these undefined values would be the same as obtained in the previous active state. Since there is no direct connection between the PV source terminals and the grid terminals, the PV terminal points (nodes P and N) float. Hence, they are not affected by any high-frequency voltage transitions. From Fig. 11(c), it is evident that the sinusoidal stray capacitor voltage is overridden by four spikes (two spikes during each half-cycle). As the spikes display identical geometrical properties and symmetry, the moving average of the stray capacitor voltage remains sinusoidal. This leads to the effective reduction of leakage current, as the PV-array capacitance offers high impedance to low-frequency transitions. It can also be observed from Table III that the low-frequency transitions among any two different voltage levels (in both the terminal and the CMV) is $V_{PV}/2$. However, the total dc-link voltage is $3V_{PV}$. Therefore, it can be inferred that the voltage transitions in both the CMV and the stray capacitor voltage are 1/6th of the total boosted dc-link voltage. This leads to the complete elimination of switching frequency transitions as well as the reduction in the low-frequency transitions (compared to most of the conventional modulation technique). As a consequence, an effective suppression of leakage current occurs, which is well below than the standard mentioned by VDE-126-1-1, due to the high impedance offered by the capacitive parasitic elements to the low-frequency stray capacitor voltage. Moreover, as the proposed system does not require any extra components such as the common mode filter, choke, etc., the size and efficiency of the proposed inverter are also optimized.

Now, the equivalent impedance for the common mode circuit of the proposed inverter configuration can be written [20] as per the following equation:

$$Z_{CM} = 0.5s(L_{g1} + L_{g2}) + R_g + R_P + \frac{1}{sC_P}. \quad (42)$$

In the present design and for the reference design, the following parameters are considered: 1) power rating (P_{rated}) = 1 kW; 2) switching frequency (f_{sw}) = 20 kHz; 3) modulation frequency (f_m) = 50 Hz; 4) input PV voltage (V_{PV}) = 133 V; 5) total boosted dc link voltage ($V_{dc-link}$) = 400 V; and 6) ground resistance R_g = 10 Ω. For the effective elimination of the switching harmonics, the LC filter is designed based on the procedure described in [22], which deduces C_f = 1.15 μF and ($L_{g1} = L_{g2}$ =)2.5 mH. The following transfer function expresses the relationship between the excitation voltage (stray capacitor voltage) and the leakage current:

$$i_{leak}(s) = \frac{v_{Pg}(s)}{Z_{CM}(s)} \quad (43)$$

where Z_{CM} is the equivalent impedance for the common-mode circuit of the proposed inverter configuration [20]

$$Z_{CM} = 0.5s(L_{g1} + L_{g2}) + R_g + R_P + \frac{1}{sC_P}. \quad (44)$$

In order to minimize the effect of resonance on the leakage current, the first measure is to decrease the high-frequency transitions in the excitation voltage (i.e., v_{Pg}) of the resonant circuit. In our manuscript, the high-frequency component across the parasitic capacitor is reduced by employing the proposed modulation strategy, as shown in Fig. 11. The magnitude Bode plot of Z_{CM} is shown in Fig. 12 for different combinations of parasitic capacitance and grid filter inductor $L_g (= L_{g1} + L_{g2})$. It is observed that the magnitude of Z_{CM} increases consistently at higher frequency points beyond the resonance frequency of the common mode network (f_{ZCM}). This indicates that when the proposed 7-L inverter is switched at a frequency more than f_{ZCM}, the leakage current is well suppressed. Hence, the optimal switching frequency for the inverter can be chosen from the following inequality:

$$f_m \ll f_{ZCM} \ll f_{sw}. \quad (45)$$

Thus, in order to avoid the resonance phenomenon, the resonant frequency (f_{ZCM}) must be much higher than the fundamental frequency (f_m) and at the same time much lower than the first switching sideband to avoid excessive i_{leak} [20], [23].

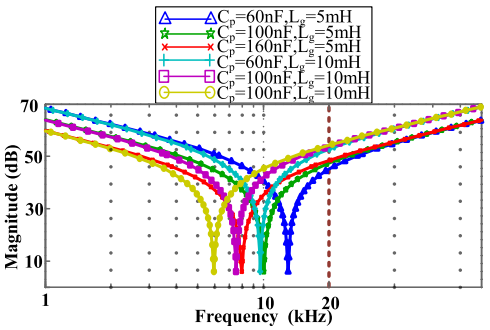

Fig. 12. Magnitude Bode plot of common mode equivalent circuit with various PV parasitic capacitances.

IV. SIMULATION RESULTS

In order to validate the working principle of the proposed inverter, it is simulated in a MATLAB-Simulink environment. The parameters for the numerical simulation of the inverter are presented in Table IV. An LCL filter is employed on the load side based on the above-mentioned design values for filtering

TABLE IV
SPECIFICATIONS CONSIDERED FOR SIMULATION OF THE PROPOSED INVERTER

Parameter	Values	Parameter	Values
V_{PV}	133 V	C_2	1.5 mF
$V_{DC\text{-}link}$	400 V	L_1 ,L_2	0.5 mH
P_{rated}	1 kW	L_{g1},L_{g2}	2.5 mH
f_m	50 Hz	C_f	0.1 uF
f_{sw}	20 kHz	R_p,C_p	10ohm,100nF
C_1,C_3	300 uF	R_g	0.1ohm

out the high-frequency components of output voltage (v_{ab}). In order to analyze the effect of the parasitic capacitance of the PV source in the proposed system, a parasitic path consisting of a resistance (R_p) series with a capacitance (C_p) is connected across the PV positive terminal and the load neutral. The parasitic capacitance varies between 60 and 160 nF/kW for different standards of PV panels and atmospheric conditions [24]. To evaluate the effectiveness of the proposed configuration in the worst conditions, a higher value of capacitance (about 150 nF/kW) and a lower value of ground resistance (about 10 Ω) are taken. The selection of the dc-link capacitor for the proposed system is based on the procedure described in [25]. A resistive load (R_L) of 100 Ω is considered to emulate the behavior of the proposed inverter, which injects only active power into the grid. This simplification allows emphasizing the structural benefits obtained with the proposed inverter and facilitates the analysis of the modulation strategy.

A PV array with a maximum power point (mpp) voltage of 133 V is considered as the input voltage for the inverter. The input voltage is boosted using an interleaved front-end buck-boost converter with a gain factor of three. Thus, the total dc-link voltage of 400 V is achieved. The simulated waveforms of output voltage, current, and SC voltage for the proposed 7-L inverter configuration are shown in Fig. 13. It can be observed that the inverter output voltage has seven distinct voltage levels at +/−400, +/−266, +/−133, and 0 V, which is in agreement with the 7-L unipolar operation of the inverter, as shown in Fig. 13(a). The total harmonic distortion (THD) of the load current shown in Fig. 13(b) is around 1.26%, which meets the IEEE519 standard. The input voltage (V_{PV}) and two SC voltages (V_{C1}, V_{C3}) maintain the voltage level of 133 V each, as shown in Fig. 13(c), whereas the total dc-link voltage goes up to 400 V, as presented in Fig. 13(a). The performance of the front-end buck-boost converter in the open loop condition as well as in the closed loop condition is analyzed and the voltage ripples in the SC (C_1 and C_3) are presented in Fig. 13(c) and (d), respectively. The simulation results demonstrate the effectiveness of the closed-loop operation, as the voltage ripple with the closed loop is lesser compared to the open loop condition.

Fig. 14 presents the simulation results of the performance of the front-end interleaved buck-boost converter for two different loading conditions. In light-laden condition (column I of Fig. 14), the front-end interleaved converter operates in the DCM mode, as it can be observed from Fig. 14I(c) and (d). However, when the load is increased, the converter operates in both DCM and CCM, as shown in Fig. 14II(c) and (d). For both the loading conditions, the voltage levels in the SCs (C_1 and C_3), as well as the total boosted voltage, remain unaltered, as shown in Fig. 14I(a) and II(a). Therefore, it can

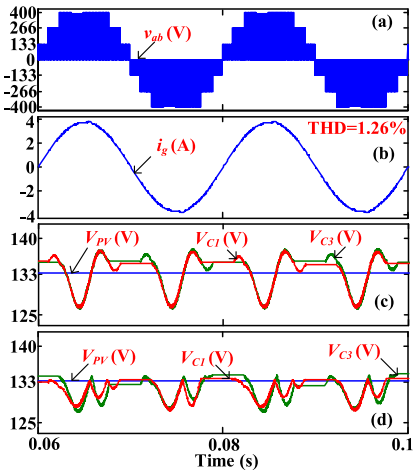

Fig. 13. Simulation waveforms. (a) Inverter output voltage. (b) Load current. (c) SC (C_1 and C_3) voltages in open-loop control. (d) SC (C_1 and C_3) voltages in closed-loop control.

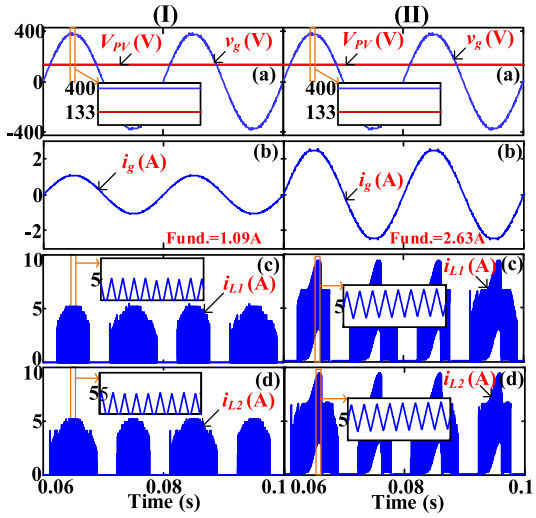

Fig. 14. Simulation waveforms of (a) input PV voltage and load voltage, (b) load current, (c) current through inductor L_1, and (d) current through inductor L_2 for (I) light loading (R_L = 200 Ω) and (II) full loading (R_L = 100 Ω) conditions.

be concluded that the performance of the proposed inverter is similar, irrespective of the DCM and CCM operation of the interleaved buck-boost converter.

Furthermore, to analyze the performance of the proposed inverter configuration, simulation results are presented in left and right columns (i.e., column I and II) of Fig. 15 for two different modulation indices of 0.9 and 0.6, respectively. The reduction in voltage levels can be observed by comparing Fig. 15I(a) and II(a). The fundamental peak of the load current is also reduced linearly with the modulation index. However, there is no significant variation in the harmonic spectrum as well as THD with respect to the variation in the modulation index variation, as shown in Fig. 15(I) and (II)(b). Fig. 15I(c) and II(c), respectively, shows the nature of the voltage across the positive terminal of the PV source and the load neutral. It can be observed that the stray capacitor voltage displays only eight voltage transitions, each with a magnitude of 1/6th of the total dc link voltage (i.e., 400 V), in any given fundamental cycle. These transitions limit the maximum; the peak value of the leakage current is limited

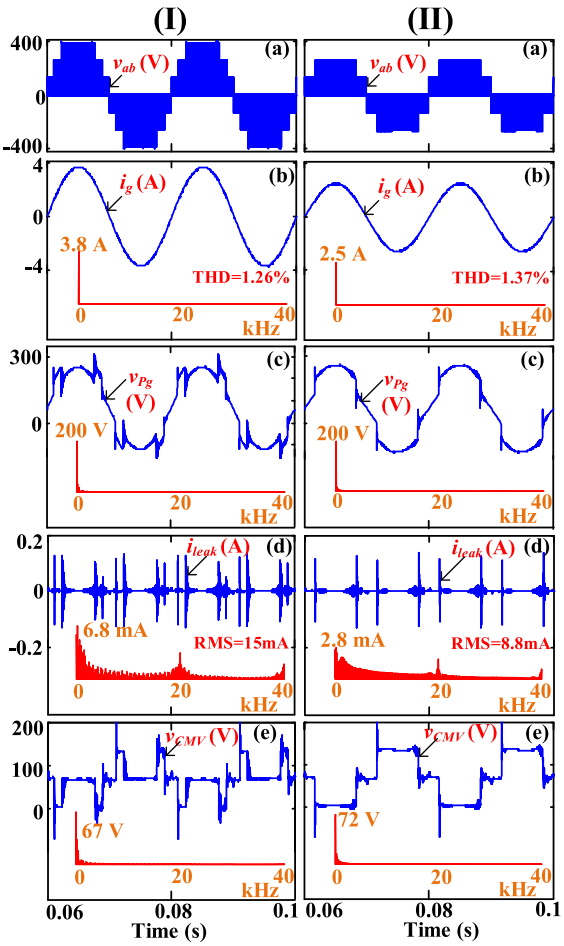

Fig. 15. Simulation waveform of (a) inverter output voltage (v_{ab}), (b) load current (i_g), (c) stray capacitor voltage (v_{Pg}), (d) leakage current (i_{leak}), and (e) CMV(v_{CMV}) for the modulation indices (I) $m_a = 0.9$ and (II) $m_a = 0.6$.

to 150 mA and the maximum rms value is 15 mA, which are well below than the standard DIN VDE 0126-1-1, as shown in Fig.15I(d) and II(d). In contrast, any conventional PWM technique would result in much higher number of transitions causing higher leakage current [26]. Thus, the proposed PWM scheme would lower the leakage current, significantly enhancing the level of safety to the operating personnel. Furthermore, the proposed modulation strategy also reduces the switching-frequency voltage transition in the CMV (v_{CMV}), which can be observed from Fig. 15I and II(e). This reduces the requirement of the size, weight, and cost of the common mode EMI filter/choke to be employed with the proposed PV inverter system.

V. Experimental Results

In order to assess the performance of the proposed power circuit configuration, an experimental prototype of 200 VA has been fabricated. Table V summarizes the operation and circuit parameters of the system. MOSFET (IRF 840) is used as a semiconductor switch for the inverter configuration and HCPL 3120 ICs are used as gate drivers for these MOSFETs. A programmable dc source is used in order to emulate a PV source for the inverter configuration. For the generation of PWM pulses for the inverter switches, the modulation technique is implemented using the Xilinx Blockset and deployed onto the

TABLE V
Specifications Considered for the Experimental Prototype

Parameter	Values
Input Voltage (V_{PV})	50 V
Total Boosted Voltage ($V_{DC\text{-}link}$)	150 V
Rated Power, S	200 VA
Modulation frequency (f_m)	50 Hz
Switching frequency (f_{sw})	20 kHz
Switched Capacitor(C_1,C_3) (metalized polyester)	24*6.8 uF,300V
DC link Capacitor C_2 (Electrolytic)	1 mF, 400V
DC inductors (L_1 , L_2)	0.5 mH
Grid inductors (L_{g1},L_{g2})	2 mH
Filter Capacitor (C_f)	1.25 uF
Parasitic elements (R_p,C_p)	10 ohm,100nF
Load Resistance (R_L)	300 ohm

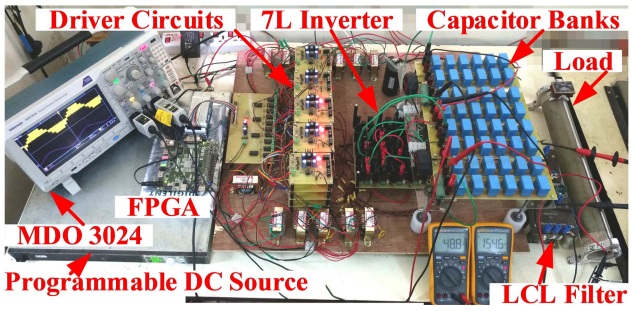

Fig. 16. Experimental prototype for the proposed 7-L inverter.

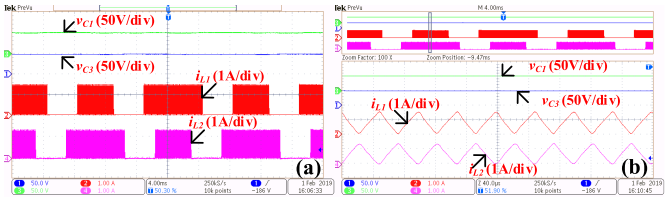

Fig. 17. Experimental results. (a) SC voltage at $m_a = 0.9$. (b) Zoomed waveform of (a).

FPGA SPARTAN 6. The Tektronix MDO 3024 is used for the acquisition of experimental results. A picture showing the fabricated inverter configuration with an experimental testing bench is depicted in Fig. 16. A capacitor bank of 24 capacitors (Metalized polyester type, each 6.8 μF, 300 V) is connected in parallel for each SC. The parasitic element of the PV source is added by connecting a resistance and a capacitance in series between the source positive terminal and the load neutral.

From Fig. 17(a), it can be observed that both the SCs are charged to the same voltage as the input PV voltage i.e., 50 V. It can also be observed that the charging duration of both the SCs is of cyclic nature, in order to equalize the utilization of the SCs. From the inductor current shown in Fig. 17(b), it can be observed that the switching logic employed creates a phase difference of π radians between them. This is in clear agreement with the phase shifted modulation technique presented in Section III-A (see Fig. 6).

The left and right columns (i.e., column I and column II) of Fig. 18 present the experimental results for the modulation indices of 0.9 and 0.6, respectively. The voltages of SCs (v_{c1}, v_{c3}) and the respective charging currents (i_{L1} and i_{L2}) for the modulation index are shown in Fig. 18I(a) and II(a). Fig. 18I(b) and II(b) shows the output voltage and load current.

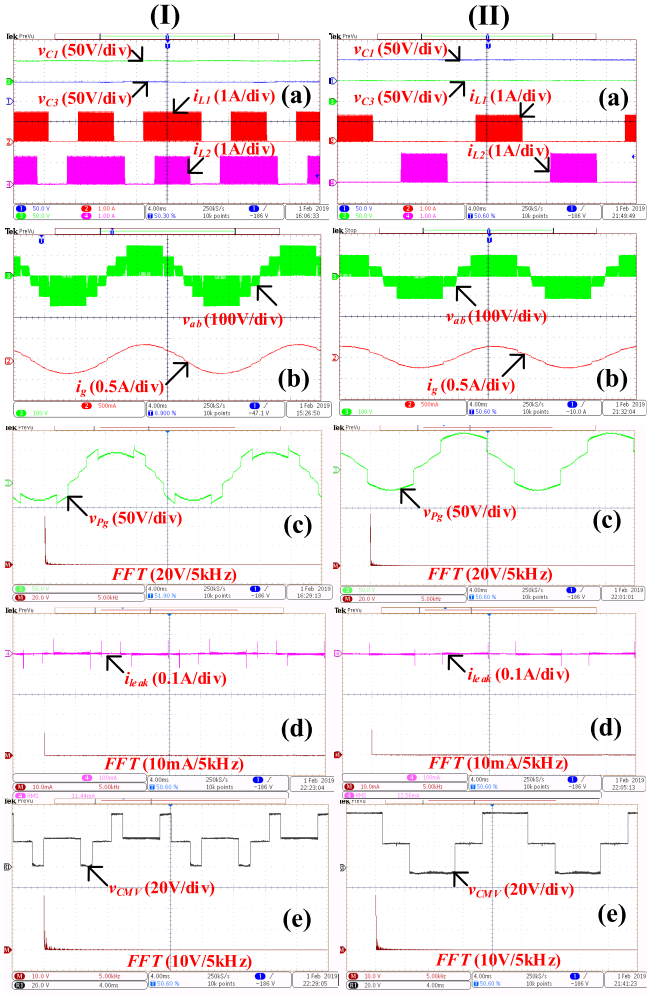

Fig. 18. Experimental results of (a) SC voltages (V_{C1}, V_{C3}), charging current (i_{L1}, i_{L2}), (b) inverter output voltage (v_{ab}) and load current (i_g), (c) stray capacitor voltage (v_{Pg}), (d) leakage current (i_{leak}), and (e) CMV (v_{CMV}) for the modulation indices (I) $m_a = 0.9$ and (II) $m_a = 0.6$.

It can be observed that the output voltage contains seven distinct levels at: +/−150, +/−100, +/−50, and 0 V, demonstrating the 7-L operation. As the modulation index reduces, the voltage level containing +/−150 V is eliminated and it continues to work as a five-level inverter [see Fig. 18(II)(b)]. This fact is in good agreement with the simulation results presented in Fig. 15(II). To analyze the performance of the inverter in terms of the leakage current, the stray capacitor voltage (v_{Pg}) across the PV positive terminal and the load neutral is recorded. This voltage appears across the parasitic path of the PV source. Therefore, the presence of switching voltage transitions in the stray capacitor voltage contributes to the transitions in the leakage current due to the fact that $i_{leak} = C_{PV}(dv_{Pg}/dt)$. From Fig. 18I(c) and II(c), it can be observed that the stray capacitor voltage (v_{Pg}) oscillates at the fundamental frequency, which effectively reduces the leakage current. The experimentally obtained leakage current for both the modulation indices is shown in Fig. 18(d). It is evident that the maximum rms value of i_{leak} reaches only 13 mA, which is significantly lesser than the maximum limit of 300 mA, as stipulated by VDE 0126-1-1. Moreover, the CMV, shown in Fig. 18(e), is recorded using the following mathematical operation on 0.5 ($v_{aN} + v_{bN}$). It can also be implied that the CMV also oscillates at the fundamental frequency. The fast Fourier transform (FFT) spectrum confirms the absence of high-frequency components in the CMV waveform. This further reduces the size and the order of the common mode choke and the EMI filter of the proposed configuration. Thus, the experimental results (presented in Fig. 18) are in good agreement with the simulation results (presented in Fig. 15), validating the operating principle of the proposed power circuit topology and the associated PWM technique.

VI. Comparison of Proposed 7-L MLI

A. Semiconductor Voltage and Current Stress Comparison

To demonstrate the merits of the proposed topology, a comparative evaluation is presented in Table V with the prevailing SC-based MLI (SCMLI) configurations. For a fair comparison, only those configurations, which are equipped with a single PV source, are taken into consideration. As the literature available on 7-L inverters with the features of voltage boosting and mitigation of leakage current is scanty, a comparison with five-level and three-level topologies is also carried out.

In order to comprehensively present the features of the proposed topology, it has been compared with various classical configurations as well as with the recently proposed topologies available in the literature. The comparison is performed in terms of the number of components and the performance indices enumerated in Table VI. Although the topologies proposed in [27] and [28] display higher efficiencies and better reduction of leakage current, they lack the inherent voltage gain and result in only 3-L output voltage. A modified T-type topology is proposed in [29], which results in the 5-L output voltage waveform as well as the low leakage current. However, significant CMV still exists and higher-order EMI filters are required to be employed in this topology for its suppression. A novel integrated dc–dc converter-based topology is proposed in [30], which results in multilevel operation with a single dc source as well as significant reduction in the leakage current. Compared to the topology proposed in [30], the proposed configuration achieves about three times at 7-L operation with a single dc source. The topologies proposed in [11] and [31] employ bulky SCs to achieve a gain of three and operate with a single dc source, thereby reducing the energy density of the inverter. Furthermore, due to the SC technique, these configurations are prone to high switch current stress and high ESR loss in the capacitor. Thus, the principal advantage of the proposed power circuit configuration and the associated PWM scheme is that, together, they render the dual advantage of 7-L operation and good voltage boosting (of about three times) with lower switch count and lower SC size (see Table VI).

B. Semiconductor Power-Loss Calculation and Comparison

In order to assess the performance of the proposed topologies, a thermal model has been employed and simulations are carried out in the PLECS environment for a power rating of 1.5 kW with an input voltage of 133 V. All the specifications of the semiconductor devices are obtained from the datasheet of the IGBT device (with the body diode) IKW30N60T. In the comparative analysis, the following parameters have been considered: 1) semiconductor losses [both

TABLE VI
COMPARISON TABLE WITH THE EXISTING CONFIGURATIONS

Parameter	[27]-3L	[28]-3L	[29]-5L	[30]-5L	[11]-7L	[31]-7L	Proposed-7L
N_{Sw}	6	5	6	9	16	14	12
N_{diode}	0	0	2	1	0	2	2
N_{Cap}	1 bulky	2 bulky	2 bulky	2 small	2 bulky	2 bulky	2 small, 1 bulky
N_{Ind}	0	0	0	1	0	0	2
TSV_{pu}	6	5	6	8.5	5.33	4.67	8.67
Gain	Unity	Unity	Unity	2	3	3	3
i_{leak}	Min.	NIL	Min.	NIL	High	High	Min.
Peak i_{sw}	I_L	$6I_L$	I_L	$2\text{-}3I_L$	$6I_L$	$5\text{-}6I_L$	$2.5I_L$
ESR loss	Low	High	High	Low	High	High	Low

switching loss (P_{sw}) and conduction loss (P_{cond})]; 2) inductor conduction loss (P_{ind}); and 3) capacitor ESR loss (P_{cap}). The losses in the passive devices are theoretically calculated from the equations given in [32]. The proposed configuration is compared with the four existing configurations proposed in [21], [11], [27]–[31], [33], and [34] for the same power output. In order to facilitate a fair comparison of the proposed boosting technique, a boost converter is employed with the existing power circuit configurations reported in [21], [27]–[29], [33], and [34] to maintain a total dc-link voltage of 400 V from the 133-V input voltage. Fig. 19(a) illustrates various power losses incurred in power circuit configuration as well as those incurred in the proposed 7-L MLI along with the respective front-end boosting circuits. The configuration proposed in [30] is more efficient. However, it results in lower number of voltage levels (five levels) and lower voltage boosting (by a factor of two) compared to the work presented in this manuscript. The conduction losses in the switches for the configuration [11], [31] are more, as the SC-based boosting technique is incorporated for the boosting of voltage. Moreover, from Fig. 19(a), it is evident that the power loss in the parasitic elements of the passive devices is higher with most of the existing configurations compared to the proposed configuration. The principle reason for this phenomenon is that all these topologies employs the conventional boost converter as a boosting stage between the PV source and the respective inverter configuration. This means that all the power obtained by the PV source must necessarily be processed through the conventional boost converter. In contrast, in the proposed power circuit topology, only 63% is processed through the boosting stage. Thus, it may be expected that the power loss in the boosting stage is significantly lower, which is supported by Fig. 19(a). Furthermore, it may be observed that the power loss incurred in the capacitor in the proposed circuit is much lesser as the ESR associated with a metalized polyester capacitor is significantly lower than the bulky electrolytic capacitor.

Furthermore, a theoretical analysis is carried out to assess the efficiency of the proposed power circuit at different power levels considering the above-mentioned factors. The efficiency plot, presented in Fig. 19(b), is determined by considering the power loss in the inverter as well as in the boosting stage while varying the power-output from 500 W to 2.5 kW at two different input voltage levels (133, 270 V). It can be observed that, as the input voltage increases, the requirement

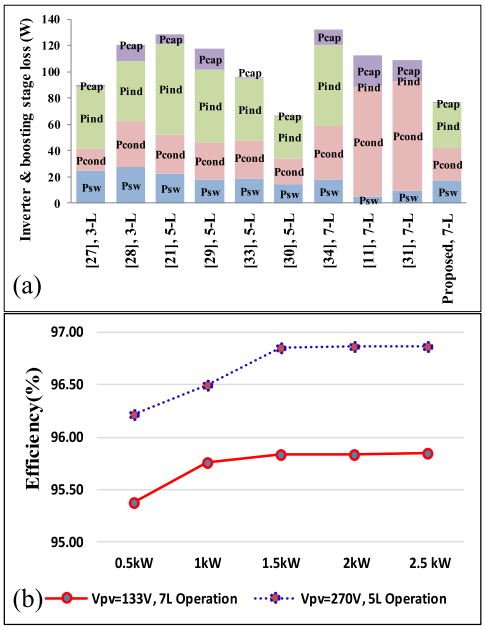

Fig. 19. (a) Comparison of total loss incurred in the existing and proposed configurations at a power rating of 1.5 kW. (b) Efficiency of the proposed configuration at two different voltage levels (i.e., 133 and 270 V).

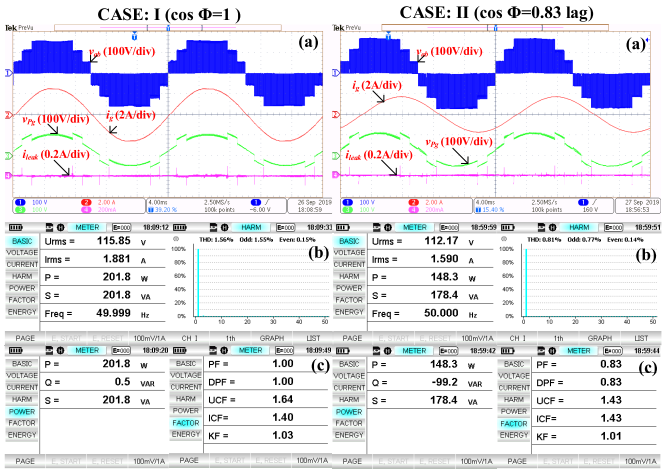

Fig. 20. (a) Inverter output voltage (v_{ab}), current (i_{ab}), stray capacitor voltage (v_{Pg}), and leakage current (i_{Leak}). (b) RMS output voltage (U_{rms}) and harmonic spectrum of the load current. (c) Active power (P), reactive power (Q), apparent power (S), and power factor (PF) for (I) 7-L operation at P_{out} = 200 W, UPF and (II) 7-L operation at P_{out} = 180 VA, with 0.83 lag.

of voltage boosting reduces, thereby reducing the power loss in the boosting section. Thus, higher input voltage with 5-L operation displays a higher efficiency compared to the 7-L operation of the proposed configuration.

The THD and the power factor are measured using a UNI-T UT283A single-phase power analyzer. Fig. 20(I)(b) and (II)(b) give the THD plot for the load current for the 7-L and 5-L operations at unity power factor condition, respectively. The THD of the load current is found to be 1.56% for the 7-L operation and 2.22% for the 5-L operation, which are within the limits specified in the IEEE-519-2014 standards. Moreover, according to EN 50438, the PV inverter should be able to operate at least up to PF = 0.95 [35]. Therefore, active and reactive power capability of the proposed inverter are examined experimentally by connecting a resistive load

($R_L = 60\ \Omega$) and a reactive load ($R = 100\ \Omega$, $L = 200$ mH ($\cos\phi = 0.83$)) at the output terminals of the inverter. For both of these cases, 110 V_{rms} is maintained with 7-L operation. It can be observed that, for both of these cases, the nature of the stray capacitor voltage is unaltered. Thus, the same leakage current results in both of these cases. The efficiency of the proposed converter at a PV voltage of 50 V and a total dc-link voltage of 150 V is found to be 90.10% (for $P_{out} = 150$ W) and 91.04% (for $P_{out} = 200$ W) for the 7-L operation. In the case of 5-L operation, the efficiency is observed to be 91.43% (for $P_{out} = 100$ W) and 93.50% (for $P_{out} = 150$ W). These results are similar to the ones reported in [30].

VII. Conclusion

In this manuscript, a transformerless, 7-L inverter configuration and its modulation technique are proposed. This semi-double-stage topology, wherein the boosting stage is integrated with 7-L VSI, achieves an overall boost factor of three. The proposed topology eliminates the problems associated with conventional SCMLI configurations, such as the requirement of bulky capacitors and peak current stress on the switches. The most important advantage of the proposed boost stage (integrated with the inverter) is that only 63% of the power from the PV source is processed through it, while the rest of 37% power is transferred directly from the PV source to the load. It is shown from the power loss analysis that the proposed boosting scheme reduces the losses in the passive devices compared to the conventional boosting schemes. Through detailed mathematical analysis, numerical simulation, and experimental validation, it is shown that both the rms value and the peak values of the leakage current are well below the German standard DIN VDE 0126-1-1. Thus, it is envisaged that the proposed topology, along with the PWM scheme, is suitable for both standalone as well as grid-connected applications.

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