2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)

A Zone-Based Modulation Strategy to Reduce the Leakage Current in Transformerless PV Inverters

Sumon Dhara
Department of Electrical Engineering
NIT Warangal
dsumon@student.nitw.ac.in
Warangal, India

V. T. Somasekhar
Department of Electrical Engineering
NIT Warangal
sekhar@nitw.ac.in
Warangal, India

***Abstract*— The reduction of the leakage current in transformerless grid-interfaced inverter topologies is essential to meet the requirements of the safety standards as well as to mitigate electromagnetic interference. The conventional PWM schemes for multilevel-inverters (MLIs) either generate a high-frequency leakage current or underutilize the resources of the multilevel inverters. In this paper, an asymmetrical 1-ϕ MLI inverter topology and its modulation scheme are presented for the PV system. Without any additional switching resources, the proposed modulation strategy achieves the avoidance of high-frequency components in the voltage impressed across the PV parasitic capacitor. Furthermore, a dual-mode boosting stage is integrated into the proposed multilevel inverter configuration in such a way that, it is capable of synthesizing thirteen distinct voltage levels while achieving a voltage boosting factor of three. Simulation results verifying the operating principle of the proposed power converter are presented, which employs the proposed modulation technique.**

Keywords—Photovoltaic inverter, Multilevel inverter, leakage current, common-mode voltage, Switched capacitor.

I. Introduction

Small-capacity transformerless solar inverter systems are increasingly being used in distributed power generation systems. The dc-link voltage boosting and minimization of the common-mode leakage current (CMLC) are the two major concerns in transformerless inverter configurations. Apart from being hazardous to the inverter, human operators, and the livestock, the CMLC adversely affects the life span of the PV panels. The CMLC also reduces the reliability of the inverter and causes electromagnetic interference (EMI). To safeguard against the ill-effects of CMLC, a maximum limit of 300mA is specified by the German standard VDE 0126-1-1 [1].

A good number of inverter configurations have been described in the literature for the reduction of leakage current and addressing the voltage boosting requirements in PV fed multilevel inverters. It has been shown that the leakage current and its ill-effects can be minimized by eliminating the switching frequency components from the TCMV (i.e. voltage between PV positive terminal and ground terminal) [2]. It can be inferred from the literature [3] that the symmetrical inverter topologies effectively manage to mitigate the CMV by compromising on the number of output voltage levels. To avoid this trade-off, several asymmetrical inverter configurations have been introduced in the literature [4-7]. A 9-level topology has been presented by Phanikumar *et. al.* [4], which can output voltage levels that commensurate with the number of switching devices while lowering stress on the switching devices. Despite its advantage of eliminating the leakage current, this topology suffers from the underutilization of the dc-link. A similar half-bridge ANPC based 7-level inverter configuration is proposed in [5]. This topology is capable of achieving a boosting factor of 1.5 times the input voltage. However, this configuration suffers from the problem of high-inrush current due to the switched capacitor (SC) network and the presence of sharp transitions in the total common-mode voltage (TCMV). The configuration proposed by Sun *et. al.* [6] is capable of achieving a 9-level output voltage with a voltage boosting factor of three. However, the proposed modulation technique in [6] is not capable of eliminating the high-frequency transitions in TCMV.

II. Working Principle and Description of the Proposed 13-Level Topology

The proposed 13-level inverter configuration is presented in Fig. 1. The power circuit configuration comprises twelve power switches, four capacitors (C_1 – C_4), two diodes (D_1, D_2), and two inductors (L_1, L_2). The switches (S_{U1}, S_{U2}, S_{L1}, S_{L2}) are used for the selection of switched-capacitor (C_1, C_3) and PV source. The dual-mode boosting stage of the configuration is highlighted in Fig. 1. Further, the H-bridge-structure in the inverter topology is implemented by four power switches (S_{P1}, S_{P2}, S_{P3}, S_{P4}), which functions as a polarity generator. The asymmetrical part of the proposed configuration is constituted with two switches (S_{P5}, S_{P6}) and a capacitor (C_4). The proposed configuration is connected to the grid with an LCL filter as shown in Fig. 1. The equivalent lumped model of the parasitic elements of the PV panel is represented by a series connection of a resistance (R_p) and capacitance (C_p). The voltage across PV positive terminal and ground (i.e. TCMV), the grid current, and leakage current for the proposed configuration are denoted by v_{Pg}, i_g, and i_{leak} respectively.

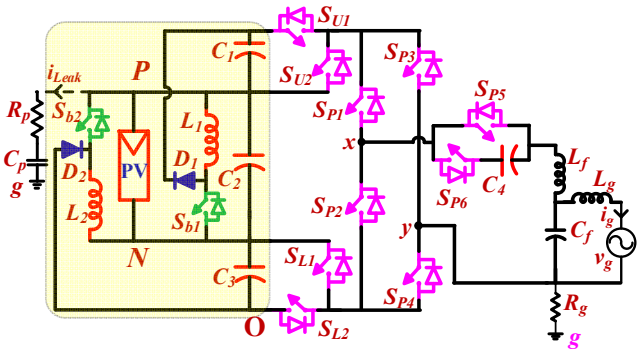

Fig. 1. Circuit diagram of the proposed asymmetrical 13-level inverter configuration.

The working principle of the proposed converter is described with the aid of the following modes of operation:

a. Direct Power Mode: To generate the voltage levels $\pm V_{PV}$ and $\pm 0.5V_{PV}$, the direct PV source is utilized and neither of the SCs (C_1 and C_3) is energized. In this mode S_{U2} and S_{L1} are

2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES) | 978-1-7281-5672-9/20/$31.00 ©2020 IEEE | DOI: 10.1109/PEDES49360.2020.9379479

978-1-7281-5672-9/20/$31.00 ©2020 IEEE

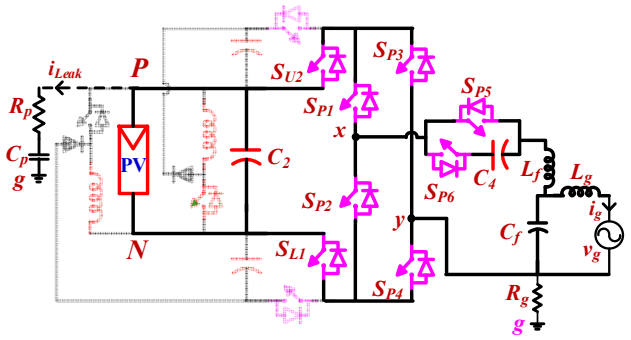

Fig. 2. Circuit operations for direct power mode.

turned on for all switching combinations. In order to generate positive and negative output voltages, the switches in the polarity generator part are utilized as shown in Fig. 2.

b. Single boosting mode: In this mode either the upper or lower section of the voltage boosting circuit is energized to charge respective SCs. Thus, redundant switching states are obtained to generate effective voltage level $2V_{PV}$ in the dc-link. To utilize the voltage of the SCs (i.e. C_1 and C_3), the respective switches from the basic unit (S_{U1} or S_{L2}) are turned on as shown in Fig. 3 (a) and (b) respectively.

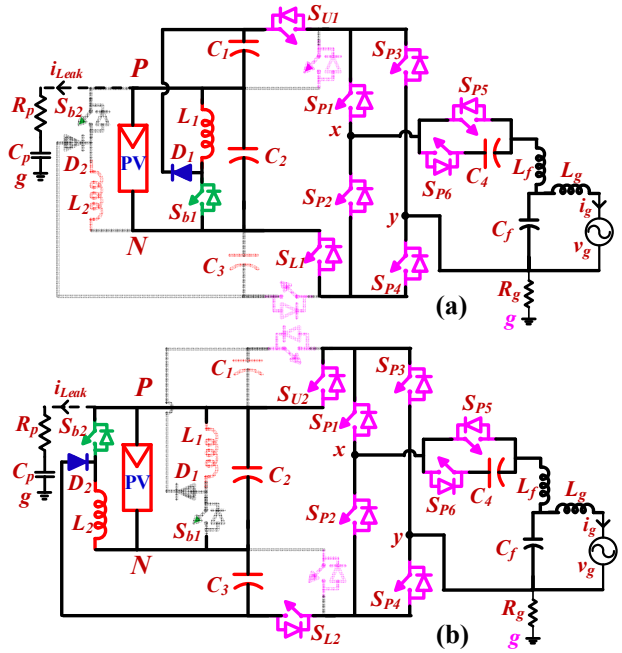

Fig. 3. Circuit operations for single boosting mode.

c. Double boosting Mode: In this mode, both of the boosting sections are energized to develop a voltage level of $3V_{PV}$ in the dc-link. It can be observed from Fig. 4 that, the

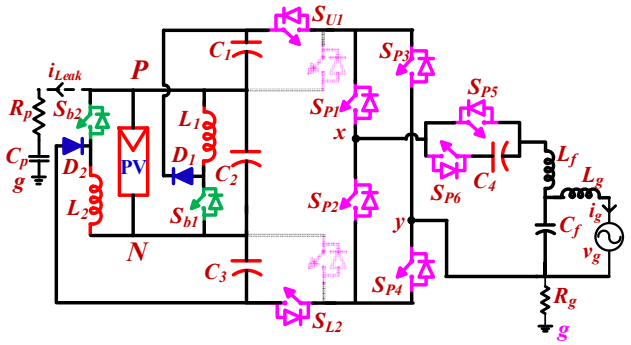

Fig. 4. Circuit operations for double boosting mode.

switches S_{U1} and S_{L2} are always turned on in this mode to utilize the total boosted dc-link voltage.

III. Modulation Strategy For Proposed Inverter Configuration

The conventional SPWM modulation technique induces time-varying common-mode voltage (CMV), which leads to generate high leakage current for the multilevel inverters. Thus, a CMV elimination modulation technique is generally used to achieve reduced CMV. This technique utilizes selective switching states, which results in the same magnitude of the CMV. This modulation technique underutilizes the switching resources of the multilevel inverter and increases THD of the load current as shown in Fig. 5. It can be observed from Fig. 5 (a) that, a basic symmetrical multilevel inverter configuration has 7 possible switching states. However, with the conventional CMV elimination technique, only 4 switching states can be utilized. Thus, there is a requirement of a PWM strategy, which is capable of utilizing all possible switching states of the MLI while eliminating the switching transitions from the CMV.

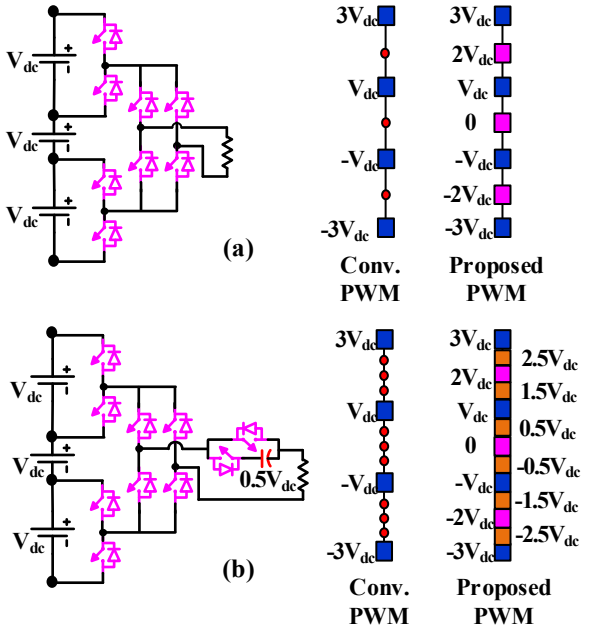

Fig. 5. (a) Symmetrical inverter configuration, (b) proposed asymmetrical inverter configuration, with conventional and proposed PWM strategy.

With this motivation, two PWM schemes, which are implemented with a modified level shifted-sinusoidal pulse width modulation (LS-SPWM), are proposed in this paper. Moreover, the peak-magnitude and RMS of the leakage current mainly depends on the rate of change (*dv/dt*) of TCMV as the parasitic capacitances in the system offer minimum impedance to the high-frequency components. So, both of the PWM strategies are capable of reducing the leakage current effectively, which generally, flows through the parasitic capacitance between the ground and PV panel [2]. It can also be observed from Fig. 5 (b) that, the proposed PWM can switch all 13 switching states of the proposed MLI structure. However, the conventional CMV elimination technique only switches between 4 switching states. All possible switching states of the proposed inverter structure are listed in Table I. In the proposed converter, the switch-

978-1-7281-5672-9/20/$31.00 ©2020 IEEE

TABLE I . SWITCHING STATES OF DIFFERENT VOLTAGE LEVELS

Sw. Seq.	S_{U1}	S_{L2}	S_{P1}	S_{P3}	S_{P5}	v_{ab}
Sq_{+3}	1	1	1	0	1	$+3V_{PV}$
$Sq_{+2.5}$	1	1	1	0	0	$+2.5V_{PV}$
Sq_{+2A}	0	1	1	0	1	$+2V_{PV}$
Sq_{+2B}	1	0	1	0	1	$+2V_{PV}$
$Sq_{+1.5A}$	0	1	1	0	0	$+1.5V_{PV}$
$Sq_{+1.5B}$	1	0	1	0	0	$+1.5V_{PV}$
Sq_{+1}	0	0	1	0	1	$+V_{PV}$
$Sq_{+0.5}$	0	0	1	0	0	$+0.5V_{PV}$
Sq_{0+}	0	0	0	0	1	0
Sq_{0-}	0	0	0	0	1	0
$Sq_{-0.5A}$	0	0	0	0	0	$-0.5V_{PV}$
$Sq_{-0.5B}$	0	0	1	1	0	$-0.5V_{PV}$
Sq_{-1}	0	0	0	1	1	$-V_{PV}$
$Sq_{-1.5}$	0	0	0	1	0	$-1.5V_{PV}$
Sq_{-2A}	0	1	0	1	1	$-2V_{PV}$
Sq_{+2B}	1	0	0	1	1	$-2V_{PV}$
$Sq_{-2.5A}$	0	1	0	1	0	$-2.5V_{PV}$
$Sq_{-2.5B}$	1	0	0	1	0	$-2.5V_{PV}$
Sq_{-3}	1	1	0	1	1	$-3V_{PV}$

pairs (S_{U1}, S_{U2}), (S_{U1}, S_{U2}), (S_{P1}, S_{P2}), (S_{P3}, S_{P4}), and (S_{P5}, S_{P6}) operate complementary to each other.

A. PWM Strategy I: Reduction of transitions in TCMV

To minimize the transitions in the TCMV, a zone-based PWM strategy is developed, which is capable of selecting switching states for each voltage level, based on the zone of operation (Fig. 6). Thus, the flexibility of redundant switching states with different TCMV can be effectively utilized. Only those switching states, which have the same magnitude of TCMV in a particular zone, are considered from the switching states listed in Table I. In any particular zone, the TCMV is clamped to a particular value; it changes only during the transition from one zone to another. The clamped waveform of TCMV, in turn, eliminates all the high-frequency transitions in each zone. The peak leakage current during the transition of zones can be further minimized with the aid of common-mode filters. This PWM strategy effectively utilizes all voltage levels and achieves a lower total-harmonic distortion (THD) in the output.

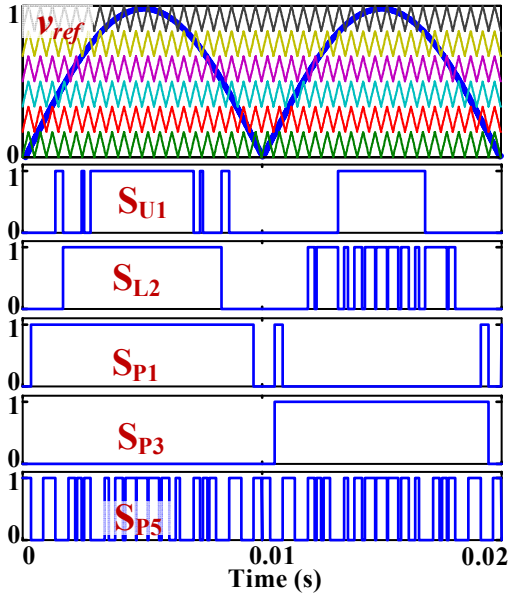

Fig. 6. Modulation signal and generation of PWM pulse for PWM strategy-I.

B. PWM Strategy II: Reduction of transitions in CMV

The proposed PWM strategy-II (Fig. 7) is implemented to reduce the transitions in the common-mode voltage (CMV). This PWM is also implemented using a zone-based selection of alternating levels with the redundant switching states. The switching states of alternating levels in a particular zone are selected from Table I such that, both switching states employ the same CMV. As the configuration employs constant CMV irrespective of the zone of operation, the TCMV also oscillates with a sinusoidal pattern with dc offsets. Thus, the transitions in the leakage current, as well as in the CMV both, are effectively reduced without the application of additional circuitry. This PWM strategy is capable of effective minimization of the leakage current as well as the requirement of common-mode filters. However, this PWM strategy increases the THD of the output current as of the alternating voltage levels in a particular-zone have a difference of $2V_{DC}$.

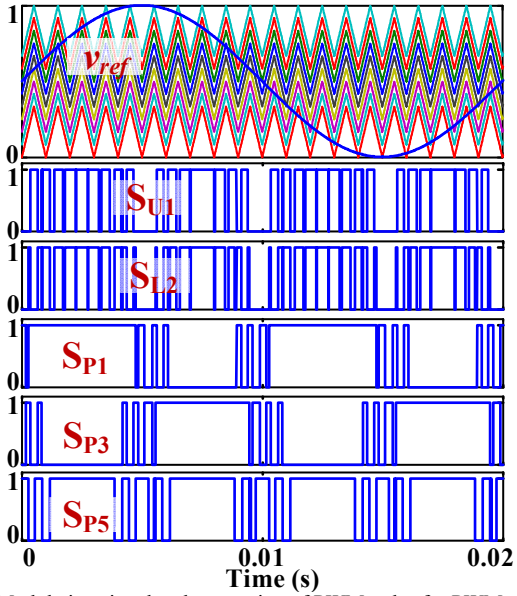

Fig. 7. Modulation signal and generation of PWM pulse for PWM strategy-II.

C. Analysis of the proposed MLI:

The pole voltages of the proposed configuration are derived mathematically using switching variables. The switching variables for the power switches S_{U1}, S_{L2}, S_{P1}, S_{P3}, and S_{P5} are represented as SV_{SU1}, SV_{SL2}, SV_{SP1}, SV_{SP3}, and SV_{SP5} respectively. The value of these switching variables is "1" when the corresponding switch is turned ON and "0" when the corresponding switch is turned OFF. Assuming that the switched capacitors C_1 and C_3 are charged equally to the input voltage (i.e. V_{PV}), the pole voltage v_{ao} can be derived as per the following equation:

$$\begin{aligned} v_{ao} &= 3SV_{SU1}SV_{SP1}V_{PV} + 2(1-SV_{SU1})SV_{SP1}V_{PV} \\ &\quad + (1-SV_{SL2})(1-SV_{SP1})V_{PV} - 0.5(1-SV_{SP5})V_{PV} \end{aligned} \quad (1)$$

Similarly, the pole voltage v_{bo} can also be derived from the following equation,

978-1-7281-5672-9/20/$31.00 ©2020 IEEE

$$v_{bo} = 3SV_{SU1}SV_{SP3}V_{PV} + 2(1-SV_{SU1})SV_{SP3}V_{PV} + (1-SV_{SL2})SV_{SP5}V_{PV} \quad (2)$$

Further, the inverter output voltage (v_{ab}) and common-mode voltage (v_{cmv}) are derived from the following equations:

$$v_{ab} = v_{ao} - v_{bo} \quad (3)$$

$$v_{cmv} = 0.5(v_{ao} + v_{bo}) \quad (4)$$

Now, the common-mode voltages for all possible switching sequences are derived using eqns. (1-4). The switching sequence for a particular zone is selected in such a way that, both of the switching sequences result in the same magnitude of TCMV (PWM strategy-I) or common-mode voltage (PWM strategy-II). The selected switching combinations for both PWM strategies are listed in Table II.

TABLE II . SELECTION SWITCHING SEQUENCES FOR PWM STRATEGY - I AND PWM STRATEGY- II

Zone	PWM Strategy-I	Zone	PWM Strategy-II
$+3V_{PV}$ ⬍ $+2.5V_{PV}$	Sq_{+3} / $Sq_{+2.5}$	$+3V_{PV}$ ⬍ $+1V_{PV}$	Sq_{+3} / Sq_{+1}
$+2.5V_{PV}$ ⬍ $+2V_{PV}$	$Sq_{+2.5}$ / Sq_{+2A}	$+2.5V_{PV}$ ⬍ $+0.5V_{PV}$	$Sq_{+2.5}$ / $Sq_{+0.5}$
$+2V_{PV}$ ⬍ $+1.5V_{PV}$	Sq_{+2A} / $Sq_{+1.5A}$	$+2V_{PV}$ ⬍ $+0V_{PV}$	Sq_{+2B} / Sq_{0+}
$+1.5V_{PV}$ ⬍ $+1V_{PV}$	$Sq_{+1.5B}$ / Sq_{+1}	$+1.5V_{PV}$ ⬍ $-0.5V_{PV}$	$Sq_{+1.5B}$ / $Sq_{-0.5B}$
$+1V_{PV}$ ⬍ $+0.5V_{PV}$	Sq_{+1} / $Sq_{+0.5}$	$+1V_{PV}$ ⬍ $-1V_{PV}$	Sq_{+1} / Sq_{-1}
$+0.5V_{PV}$ ⬍ 0	$Sq_{+0.5}$ / Sq_{0+}	$+0.5V_{PV}$ ⬍ $-1.5V_{PV}$	$Sq_{+0.5}$ / $Sq_{-1.5}$
0 ⬍ $-0.5V_{PV}$	Sq_{0-} / $Sq_{-0.5A}$	$0V_{PV}$ ⬍ $-2V_{PV}$	Sq_{0-} / Sq_{+2B}
$-0.5V_{PV}$ ⬍ $-1V_{PV}$	$Sq_{-0.5B}$ / Sq_{-1}	$-0.5V_{PV}$ ⬍ $-2.5V_{PV}$	$Sq_{-0.5B}$ / $Sq_{-2.5B}$
$-1V_{PV}$ ⬍ $-1.5V_{PV}$	Sq_{-1} / $Sq_{-1.5}$	$-1V_{PV}$ ⬍ $-3V_{PV}$	Sq_{-1} / Sq_{-3}
$-1.5V_{PV}$ ⬍ $-2V_{PV}$	$Sq_{-1.5}$ / Sq_{+2A}		
$-2V_{PV}$ ⬍ $-2.5V_{PV}$	Sq_{+2A} / $Sq_{-2.5A}$		
$-2.5V_{PV}$ ⬍ $-3V_{PV}$	$Sq_{-2.5B}$ / Sq_{-3}		

IV. SIMULATION RESULTS

The proposed single-phase asymmetrical 13-level inverter topology is simulated using the MATLAB-SIMULINK software to validate its operation. The parameters, which are used in the simulation study, are listed in Table III.

The simulation results are acquired at a modulation index m_a = 0.95 for the proposed inverter with PWM strategy-I as shown in Fig. 8. The 13 voltage levels can be distinctly observed from Fig. 8 (b), which resembles the conventional (staircase type) MLI waveform.

TABLE III . SIMULATION PARAMETERS

Sr. No.	Parameters	Values
1	Input PV voltage (open circuit)	165V
2	Capacitor (C1, C2, C3, C4)	1mF
3	switching frequency (f_{sw})	5kHz
4	Boosting stage inductors (L_1,L_2)	0.5mH
4	Filter inductor (L_f)	5mH
5	Grid interfacing inductor (L_g)	2mH
6	Parasitic Resistance (R_P) of the PV panel	10ohm
7	Parasitic Capacitance (C_P) of PV panel	10nF

An equivalent impedance of PF=0.85 lag is connected across the output terminals of the inverter; it is evident from the lagging inverter current as shown in Fig. 8 (c). It can be observed from Fig. 8 (e) that, the TCMV (v_{Pg}) varies at low frequency (i.e. modulation frequency), which leads to the reduction of the leakage current for the configuration. The RMS value of the leakage current is obtained as 15mA as shown in Fig. 8 (f). However, the common-mode voltage of the inverter configuration varies at the switching frequency of the inverter with PWM strategy-I.

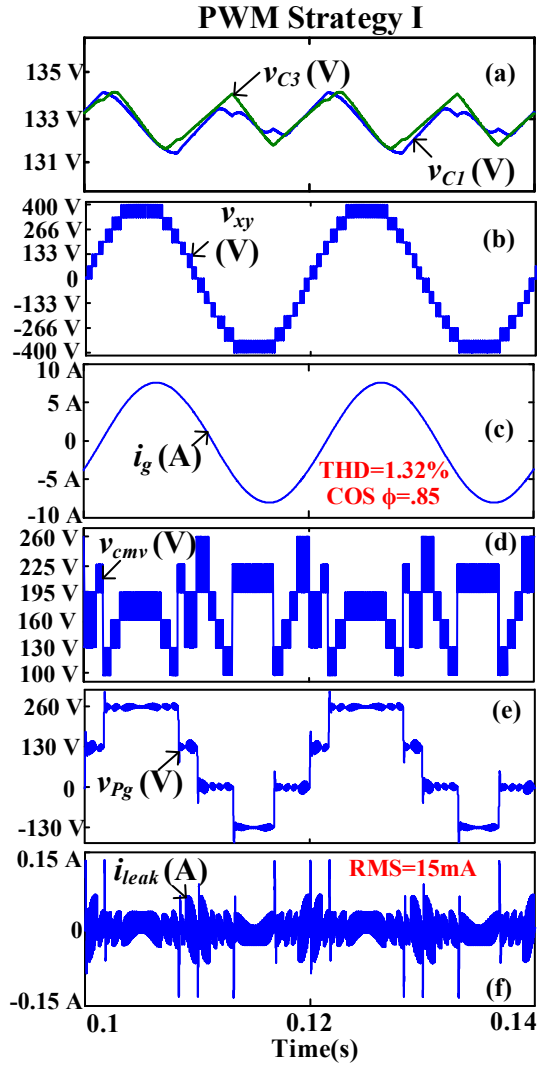

Fig. 8. SC voltage (v_{c1}, v_{c3}), output voltage (v_{xy}), grid current (i_g), CMV (v_{CMV}), TCMV (v_{Pg}), leakage current (i_{leak}) for PWM Strategy I.

978-1-7281-5672-9/20/$31.00 ©2020 IEEE

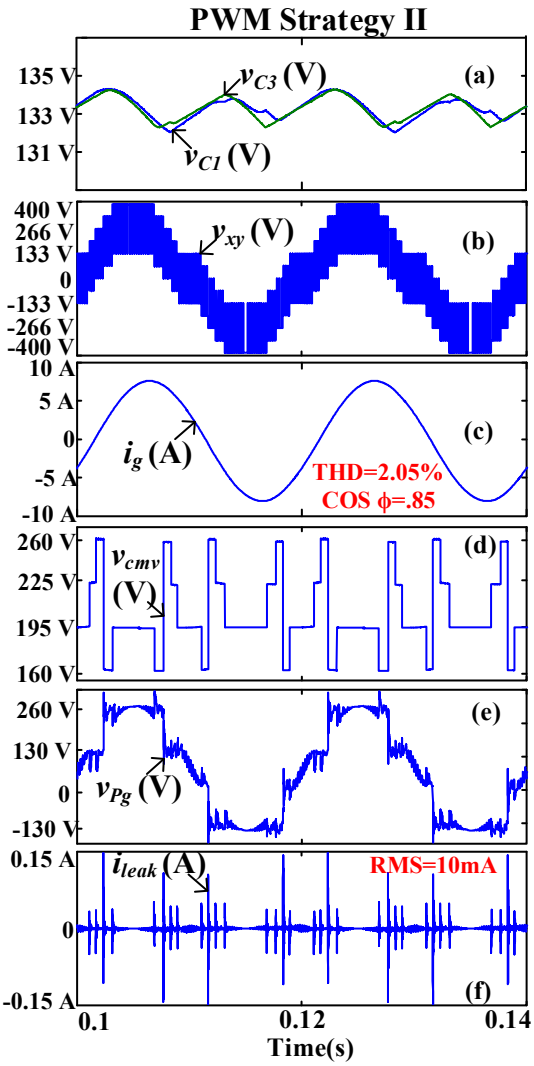

Fig. 9. SC voltage (v_{c1}, v_{c3}), output voltage (v_{xy}), grid current (i_g), CMV (v_{CMV}), TCMV (v_{Pg}), leakage current (i_{leak}) for PWM Strategy-II .

Another set of the simulation results are presented at m_a= 0.95 for the proposed inverter with PWM strategy-II. The simulation results for the PWM strategy-II are shown in Fig. 9. From Fig. 9 (b), it can be observed that, though the difference between consecutive voltage levels is $2V_{PV}$, all voltage levels are switched. It can be observed from Fig. 9 (c) that, this PWM strategy results in an increased THD value of the current compared to the one obtained with PWM strategy-I. However, this PWM strategy is capable of eliminating all switching frequency variations from both the CMV (v_{CM}) and TCMV (v_{Pg}) as evident from Fig. 9 (d) and (e). Thus, the leakage current for this configuration is also reduced. The obtained RMS value of the leakage current is obtained as 10mA. Besides that, with the employment of this PWM strategy, the required size of the EMI filter is reduced.

V. Comparison Of The Proposed Topology With Existing

Various inverter configurations have been compared based on the number of switches and diodes (N_{swd}), no of capacitors (N_{cap}), no of sources (N_{PV}), voltage gain factor (G), total standing voltage per no of levels (in p.u., TSV_{pu}). For a fair comparison, single-source based SCMLI and other boosting topologies, which are capable of minimizing the leakage current, are considered for comparison. To evaluate these power circuit configurations, a proportion of performance factor (CF) to the number of voltage levels is determined based on the component count and the TSV_{pu} as per the equation given in [7].

TABLE IV . Switching States of Voltage Levels

1- ϕ configurations	N_{swd}	N_{PV}	N_{cap}	N_{ind}	G	TSV_{pu}	CF
[5]-7L	10	1	4	0	1.5	7.3	3.2
[4]-9L	10	1	3	1	0.5	4	2.1
[6]-9L	16	1	3	0	3	8	3.1
[7]-9L	8	1	3	3	4	5.75	2.3
Proposed Topology-13L	12	1	4	2	3	7	2.0

VI. Conclusion

This paper proposes an asymmetrical transformerless 13-level inverter topology with the features of voltage boosting and the reduction of CMLC. A series capacitor network with two switches has been used as an asymmetrical leg to increase the number of levels. The configurations can feed high-quality power into the grid with a current THD of below 5%. The proposed topology achieves self-balancing of the switched capacitor voltage using the redundant switching states of the inverter. The proposed PWM strategies are devised from the redundant states to eliminate all high-frequency transitions from the TCMV. PWM strategy-I is capable of achieving complete multilevel performance with minimum *dv/dt* while minimizing the CMLC. PWM strategy-II is also capable of eliminating the high-frequency transitions from both TCMV and CMV. The PWM strategy-II results in a better performance in the elimination of CMLC, while reducing the requirement of the common-mode filter. Thus, both of the PWM strategies are capable of meeting the CMLC standard VDE 0126-1-1 with the proposed asymmetrical power circuit configuration without any additional circuit elements.

References

[1] Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems", *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2100-2111, March 2018.

[2] T. Kerekes, R. Teodorescu and M. Liserre, "Common mode voltage in case of transformerless PV inverters connected to the grid," 2008 *IEEE International Symposium on Industrial Electronics*, Cambridge, 2008, pp. 2390-2395.

[3] W. Li, Y. Gu, H. Luo, W. Cui, X. He and C. Xia, "Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4537-4551, July 2015.

[4] C. Phanikumar, J. Roy and V. Agarwal, "A Hybrid Nine-Level, 1-φ Grid Connected Multilevel Inverter With Low Switch Count and Innovative Voltage Regulation Techniques Across Auxiliary Capacitor," in *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2159-2170, March 2019.

[5] S. S. Lee and K. Lee, "Dual-T-Type Seven-Level Boost Active-Neutral-Point-Clamped Inverter," in *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6031-6035, July 2019.

[6] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du and Z. Lu, "A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7184-7194, Nov. 2016.

[7] J. Liu, W. Lin, J. Wu and J. Zeng, "A Novel Nine-Level Quadruple Boost Inverter With Inductive-Load Ability," in *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4014-4018, May 2019.

978-1-7281-5672-9/20/$31.00 ©2020 IEEE