An Open-End Winding BLDC Motor Drive With Fault Diagnosis and Autoreconfiguration

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***Abstract*— This article proposes a dynamically reconfigurable open-end winding brush-less dc motor drive (OEWBLDCMD). In this drive configuration, open-ended motor phase windings are fed with two voltage source inverters from each end, which are powered with separate battery banks. Power semiconductor switching devices, which constitute the dual-inverter system, are susceptible for the development of open-circuit (OC) fault and short-circuit faults (SCFs) on the fly, seriously hampering the reliability of the drive. This article proposes simple algorithms to diagnose both of these faults. In particular, the SCF detection is essentially preemptive in nature, as the acts of detection and the subsequent circuit-reconfiguration are carried out before the SCF can cause overcurrents in healthy switching devices and damage them. The fault diagnosis algorithms employ simple analog circuits and Hall current sensors, making them inexpensive and reliable. This article also presents the strategies for the dynamic reconfiguration of the power circuit, which ensures that the charge residing in the healthy battery bank is utilized even if the associated inverter develops a fault. The effectiveness of the proposed power circuit, fault diagnosis algorithms, and reconfiguration strategies is assessed with simulation studies and is validated experimentally.**

***Index Terms*— Brush-less direct current (BLDC) motor, fault tolerant, open-circuit fault (OCF), open-end winding, short-circuit fault (SCF).**

I. Introduction

ENVIRONMENTAL pollution and the need to conserve energy are the prime motivating factors for the promotion of electric vehicles (EVs). Apart from low emission of greenhouse gases, EVs also offer higher efficiencies and noiseless operation. To be effective and to be on par to internal combustion engines, EVs are expected to possess the following qualities: 1) greater torque to weight ratio for size reduction; 2) greater torque during starting and low-speed operation; 3) good reliability; and 4) robustness. Although the torque-speed behavior of the dc series motor satisfies some of these requirements, it is found wanting in terms of: 1) low power density; 2) maintenance issues due to mechanical commutation; and 3) low efficiency. Induction motors (IMs) and permanent magnet motors (PMMs) avoid these shortcomings and are being aided by the advent of semiconductor technology and the development of permanent magnets. Due to the lower torque density of IMs, EVs operated with them are larger in size in comparison with those operated with PMMs, which exhibit higher torque density.

In the category of PMMs, two principal variants exist, namely, permanent-magnet brush-less ac (PM-BLAC) machines and permanent-magnet brush-less direct current (PM-BLDC) motors. PM-BLDC motors offer advantages, such as higher power density (by about 15%), lower switching and conduction losses, enhanced thermal reliability, reduced complexity of control implantation, and the requirement of inexpensive sensors compared with the PM-BLAC motors [1].

PM-BLDC are well suited for low-power EV applications due to their better speed–torque characteristics, greater torque-to-weight ratio, good dynamic response, operating with low noise, electronic commutation, and little maintenance [2]–[6].

Reliability of power supply to the propulsion motor is a crucial factor in EVs. IGBT power switches are most widely employed in voltage source inverters (VSIs) because of their high switching frequency, high efficiency, and ability of handling short-circuit (SC) capabilities greater than 10-μS period [7]. Statistical studies show that semiconductor power switches, gate driver circuits, and capacitors display a propensity to fail. Around 31% of faults are due to power switch failures followed by capacitors and gate driver circuits [8]–[10].

Power semiconductor switching devices may fail either due to the open-circuit faults (OCFs) or short-circuit faults (SCFs). In general, OCFs do not require immediate shutdown. However, if they persist for a long time, secondary faults may occur at load and/or actuator system. In contrast, SCFs need immediate attention and shutdown as they cause large fault currents [11]–[13].

A fault-detection scheme for IGBTs, which can detect an OC/SC fault within 3 μS, is proposed in [14]. This method is based on the detection of the behavior of the gate-to-emitter voltage. This method, however, needs auxiliary inductors and IGBT-based converters.

The research work reported in [15]–[17] describes various methods for the diagnosis of OCF in conventional IM drives. The work reported in [18] proposes a multilevel inverter topology for a four-pole open-end winding IM drive, which is capable of handling OC/SC failures of the inverter switch as well as the dc source failure. A multilevel inverter configuration with dual three-level inverters (constituted by four two-level inverters) for a four-pole open-end winding IM drive, which is capable of handling OC&SC switch failure of any two switches, is proposed in [19]. However, the scope of the work reported in [18] and [19] is confined only to the

Manuscript received May 7, 2019; revised July 23, 2019 and September 11, 2019; accepted October 6, 2019. Date of publication October 22, 2019; date of current version November 5, 2020. Recommended for publication by Associate Editor Dian Guo Xu. *(Corresponding author: Patnana Hema Kumar.)*

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Digital Object Identifier 10.1109/JESTPE.2019.2948968

prefault and the postfault circuit operation. Also, the method of diagnosing the OC & SC faults are not presented in both of these works. This shortcoming is addressed to some extent in the work presented in [20], in which only the OCF diagnosis is carried out for the dual-inverter fed open-end winding IM drive configuration. However, these diagnosis methods are not suitable for BLDCs, as one of the motor phases is kept in a floating condition in them.

A fault-tolerant BLDC drive is reported in [21], in which the faulted phase is connected to the midpoint of the dc-link using a bidirectional switch. However, fault detection is only limited to the OCF and the topology cannot be extended for SCF in the actuator switch.

The work reported in [22] investigates the performance of the dual-inverter fed open-end winding brush-less dc motor drive (OEWBLDCMD) with three, four, and five phases under the normal and open-circuited fault condition. This article emphasizes the advantage of employing the open-end winding topology of the motor from the standpoint of fault tolerance. In this article, it is shown that the motor would be able to operate with a reduced torque and increased torque ripple despite the OCF either in the switching devices of the converter or the motor phase windings.

A single-sided matrix converter (SSMC) fed five-phase, four-pole, OEWBLDCMD for aerospace applications (electro-hydrostatic actuation system) is presented in [23]. It is shown that this power circuit configuration is also capable of handling OCF in one of the motor phase windings. However, both the works presented in [22] and [23] do not discuss about the diagnosis of the OCFs.

Fault-tolerant control moment gyros (CMGs), which are used in attitude control of space stations, are described in [24]–[26]. Buck converter fed inverter drive control is used for magnetically suspended CMG (MSCMG). OCF and SCF diagnosis for MSCMG was discussed in [24]. The scope of this article [24], however, is limited to the diagnosis of the fault.

The work reported in [25] achieves fault tolerance against both the OCF and the SCF occurring in the buck converter as well as the inverter switches. However, this approach cannot diagnose the fault occurring in the auxiliary bidirectional switches (TRIACs) that are placed in series and parallel to the inverter leg.

A dual-inverter fed OEWBLDCMD is proposed in [26], which is aimed for the MSCMG applications. In this topology, a front-end dc–dc buck converter provides a ripple-free dc input to the dual-inverter fed OEWBLDCMD. As in [26], the output voltage of the dc–dc converter is varied to control torque of the BLDC motor. In other words, the dual-inverter configuration reported in [26] is not modulated and is operated in the conventional six-step commutation mode. However, the motor in this scheme is constrained to handle twice its rated current in four modes of operation (out of six modes) after diagnosing the fault. This calls for the oversizing of the motor.

Furthermore, the fault diagnosis schemes in [24]–[26] are applicable only for the MSCMG drive operated by a buck converter fed inverter, as the fault diagnosis is based on the sensing of the output voltage and the dc-link current of the buck converter. Hence, this method cannot be applied to the conventional inverter fed BLDC motor drives.

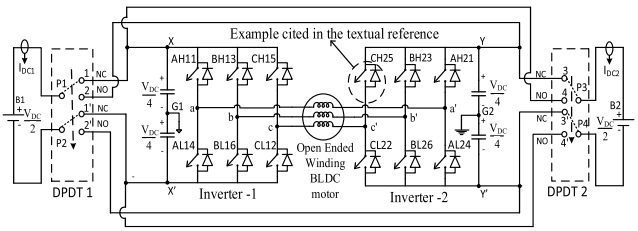


Fig. 1. Circuit configuration of OEWBLDC motor drive.

In this article, a fault-tolerant OEWBLDCM is presented. This OEWBLDCM drive is powered by two battery banks of equal voltage and power rating from both sides of the open-ended stator windings, which is capable of exhibiting tolerance against both OCF and SCF in any of the switching devices of the dual-inverter system.

The main contribution of this article is the proposal of new algorithms for OCF and SCF diagnosis for all the switching devices of the OEWBLDCM drive. In particular, the SCF is identified by sensing the line voltages before a short-circuited semiconductor device causes overcurrent through the device. To make the fault diagnosis cost effective and practicable without compromising on bandwidth, inexpensive and readily available current sensors and analog isolators are employed.

Upon the identification of fault, the power circuit is automatically reconfigured to supply reduced power to the motor, enhancing the reliability of the drive. With the help of appropriate switchgear, one can reconnect the battery of the faulted inverter side in parallel to the battery of the operating inverter.

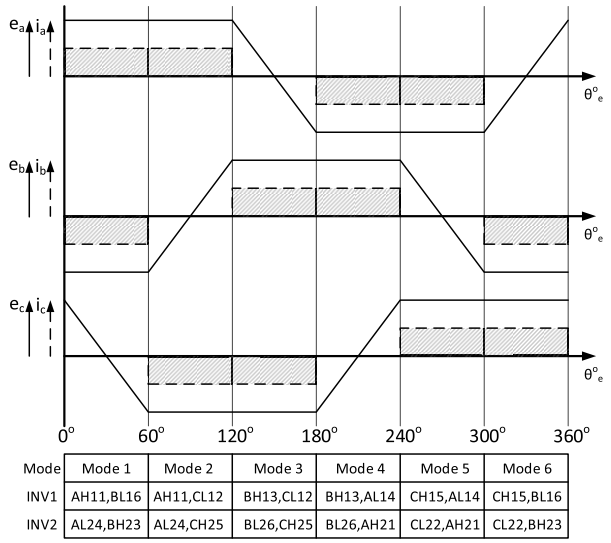
To assess the effectiveness of the proposed algorithms for OCF and SCF diagnosis, the OEWBLDCM drive is operated in both open loop and closed loop. It is shown that the drive is capable of delivering full-load torque, even when OCF and SCF occur, making it suitable for EV applications.

Furthermore, the topology presented also results in lesser (dv/dt) stress across the switching devices, enhancing the longevity of the drive compared with the conventional BLDC drive.

II. Open-End Winding Brush-Less DC Motor Drives

Fig. 1 shows the circuit diagram of the OEWBLDCMD. A dual-inverter system consists of Inverter-1(INV1 for short) and Inverter-2 (INV2). These inverters derive their dc inputs from two electrically isolated battery banks ("B1" and "B2") through two DPDT relays. The nomenclature of the power switching devices is based on the sequence: Phase (A or B or C), Position [Upper-bank (H) or Lower-bank (L)], inverter number (1 or 2), and switch number (1–6). For example, the switch CH25 pertains to the switching device present in the C-Phase of the upper bank of the Inverter-2, which bears the number 5 (see Fig. 1).

The discussion on the role of the DPDT relays is deferred to Section III. The batteries, by default, are connected to the normally closed (NC) terminals (11' for INV1 and 33' for



Mode	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
INV1	AH11,BL16	AH11,CL12	BH13,CL12	BH13,AL14	CH15,AL14	CH15,BL16
INV2	AL24,BH23	AL24,CH25	BL26,CH25	BL26,AH21	CL22,AH21	CL22,BH23

Fig. 2. Back EMF and motor phase current waveforms with switching logic.

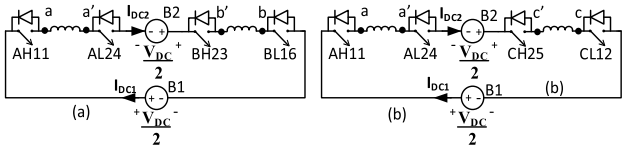


Fig. 3. Electrical equivalent of the OEWBLDCM drive. (a) Mode-1 operation. (b) Mode-2 operation.

INV2). Fig. 2 shows the back EMF waveforms across the phase windings of the OEWBLDCMD, the operating modes, and the switching regimes of the power switching devices of the dual-inverter system. As in the case of the conventional BLDC motor, each mode lasts for 60 electrical degrees. Also, the devices to be switched are identified by the Hall effect position sensors.

The equivalent circuit diagram for mode-1 and mode-2 are given in Fig. 3(a) and (b), respectively. From Fig. 3(a), it may be noted that the conducting phase windings are **aa'** and **bb',** while the phase **cc'** is left floating. The winding bb' provides the return path for the current flowing through aa' (and vice versa). Furthermore, if the top switch of INV1 for a given phase winding is turned on (AH11 in this case), the bottom switch of INV2 is also turned on (AL24 in this case).

III. Necessity of Additional Switchgear

After the diagnosis of either an OCF or an SCF, the following strategies should be followed to render the capability of fault tolerance to the drive. It is also important to redeploy the healthy battery connected to the faulty inverter to enhance the utilization of the battery and the reliability of the drive.

A. Reconfiguration of the Circuit for OC/SC Fault

The reconfiguration of the circuit is achieved by creating a switched neutral point by gating all the switching devices connected to either the positive or negative dc rail, depending up on the type of the fault developed in the faulty inverter.

For example, if an OCF is developed in any one of the three switches connected to the positive dc rail of INV1, say AH11, then all the switching devices of INV1, which are connected to the negative dc rail (AL14, BL16, and CL12), are simultaneously gated in order to create a switched neutral point on the negative dc rail of that inverter. The other two healthy switches, namely, BH13 and CH15, are never gated in order to avoid shoot-through faults in the "B" and "C" phase legs of INV1. A similar reconfiguration strategy is adopted for the other switching devices as well.

On the other hand, if an SCF occurs in AH11, then the other two healthy devices connected to the positive dc rail of INV1 (BH13 and CH15) are continuously gated so that the switched neutral point is created, this time on the positive dc rail of INV1. In this case, the switching devices, AL14, BL16, and CL12, are never gated to avoid the occurrence of the shoot-through fault.

B. Reconnection of the Healthy Battery Bank Using DPDT Relays

It is obvious that with the abovementioned maneuvers, the faulty inverter is isolated and the open-end winding BLDC motor is operated as a conventional BLDC motor with only one battery bank with half of the rated voltage. However, this move deprives the service of the healthy battery bank (connected to the faulty inverter) to the resulting system.

Thus, in order to salvage this situation, there is a necessity to connect the healthy battery bank in parallel to the existing battery bank associated with the healthy inverter. The employment of the two DPDT relays, shown in Fig. 1, would accomplish this task. Under normal conditions, the battery is connected to "NC" terminals (11' for INV1 and 33' for INV2), and thereby, INV1 and INV2 derive their dc inputs from batteries "B1" and "B2." When a fault (either OCF or SCF) is detected and the faulty inverter is identified and reconfigured, the battery bank of the faulted inverter is connected in parallel to its counterpart through the "normally open" (NO) terminals (22' of INV1 and 44' of INV2).

A detailed strategy of triggering these relays after diagnosing OCF and SCF is described in Sections IV and V, respectively. The method of energizing the relay coils is described in Section VI.

IV. Fault Diagnosis and Control for Open-Circuit Fault

This article proposes a method to extend the strategy described in [21] for the identification of the OCF for OEWBLDCMD. The procedure is described in the following paragraphs.

The OCF diagnosis algorithm always (i.e., by default) assumes that the OCF occurs in INV1 (see Fig. 1) and then proceeds to test whether it is true or not. If this test asserts that this assumption is false, then it is identified that the OCF has occurred in INV2. To optimize the number of current sensors, Hall CTs are placed in the dc links of respective inverters. The symbols I_{DC1} and I_{DC2}, respectively, denote the dc-link current of INV1 and INV2. Hence, when an OCF occurs due to the failure of any one switching device in mode-1

[see Fig. 3(a)], both dc-link currents drop down to zero. Thus, as far as INV1 is concerned (as by default, it is assumed that INV1 is faulty), either an OCF has occurred for AH11 or BL16. The exact identification of the OCF consists of the following stages.

A. Diagnosis of the Open-Circuit Fault

1) Fault Indication: In this stage, it is monitored, whether or not the dc-link current of INV1 drops below a certain critical threshold value of current "I_{th}." This threshold value is an appropriate fraction (R_f) of the reference current ("Iref"), which is output by the speed controller when the BLDC motor is operated in the closed loop. In this article, a value of 0.1 is employed for "R_f." However, if the motor is operated in open loop, a small current value, such as 50 mA, is used as the critical threshold. It is evident that a lower value of "R_f" ensures a more reliable identification of the fault. Thus

$$I\text{th} = Rf * I\text{ref} \tag{1}$$

$$\begin{cases} I_{\text{DC1}} < I\text{th}, & \text{fault condition is indicated} \\ I_{\text{DC1}} \geq I\text{th}, & \text{normal condition.} \end{cases} \tag{2}$$

2) Fault Assertion: Parts 1 and 2 are defined in the following.

Part 1: A mere indication of OCF is not adequate to assert that it has really occurred, as the dc-link current of INV1 can momentarily drop below the value of critical threshold due to disturbances. To conclusively assert that an OCF has occurred, it should last longer than a predetermined critical time period, denoted as "Tfault". Whenever $I_{\text{DC1}} < I_{\text{th}}$, a timer is triggered and the time period for which the abovementioned condition prevails is monitored. This time period is named the "error time period" and is denoted as "Te." The error time period "Te" is accumulated in terms of the current sampling time period "Ts" as

$$\text{Te(n)} = \text{Te(n} - 1) + \text{Ts} \tag{3}$$

where "T_s" denotes the sampling time period of I_{DC1} with $\text{Te}(-1) = 0$. In this article, the sampling time period is 70 μS.

In the process of the fault detection, the error time period "Te(n)" is compared with the critical time period "Tfault," which depends on the actual speed of the motor. Thus, the calculation of the critical time period "Tfault" requires the knowledge of the time period of one mode of operation "Tmode." The relationship between the electrical angular velocity "ω_{el}" and the mechanical angular velocity "ω_{me}" is given by

$$\omega_{\text{me}} = (2/P)\omega_{\text{el}} \tag{4}$$

$$f_{\text{el}} = \frac{\omega_{\text{el}}}{2 * \pi}; \quad t_{\text{el}} = \frac{1}{f_{\text{el}}} \tag{5}$$

where P denotes the number poles, (f_{el}) denotes the electrical frequency, and t_{el} denotes the time for one electrical cycle (t_{el}).

As there exist six operational modes (see Fig. 2) in one electrical cycle of operation, "Tmode" is (1/6) of the time for one electrical cycle (t_{el})

$$\text{Tmode} = \frac{1}{6 * f_{\text{el}}}. \tag{6}$$

From (5), (6) can be rewritten as

$$\text{Tmode} = \frac{4 * \pi}{P * \omega_{\text{me}} * 6}. \tag{7}$$

The critical time period "Tfault" is given by

$$\text{Tfault} = Sf * \text{Tmode} \tag{8}$$

where "Sf" is a fraction called sensitivity factor (i.e., $0 < \text{Sf} < 1$). It is obvious that a low value of "Sf" leads to a fast detection of OCF at the expense of accuracy and vice versa. A digital signal named "Fault Detection Flag-1" (FDF1) is set to a value "1" when an OCF is detected

$$\begin{cases} \text{FDF1} = 1, \text{OCFMOD} = m; \ \text{if Te}(n) > \text{Tfault} \\ \text{FDF1} = 0, \text{OCFMOD} = 0; \ \text{if Te}(n) < \text{Tfault} \end{cases}$$
$$(\text{For mode} - (m), \ \text{where } (1 \leq m \leq 6)). \tag{9}$$

The mode number in which the OCF detected is stored in the flag "OCFMOD" (i.e. , $1 \leq \text{OCFMOD} \leq 6$).

Part 2: Once an OCF is detected in mode-n, the dc-link current of INV1 (i.e., I_{DC1}), sampled in the next mode [i.e., mode-2; Fig. 3(b)] would facilitate the identification of the switching device that causes OCF. By adopting a similar procedure as described in Part-1 (fault Assertion) in mode-2 (or mode-($n+$ 1) in general), another digital signal called "Fault-Detction-Flag-2" (FDF2) is set to a value of "1," that is

$$\begin{cases} \text{FDF2} = 1 \ \text{if Te(n)} > \text{Tfault} \\ \text{FDF2} = 0 \ \text{if Te(n)} < \text{Tfault} \end{cases} \left(\frac{\text{for mode} - (\text{m}+1)}{\text{where}(1 \leq \text{m} \leq 6)} \right). \tag{10}$$

At the end of this stage, the switch, which causes the OCF (assuming that the fault occurs in INV1), is determined. The flag "OCFSW" stores the device number, i.e., OCFSW ϵ (AH11, AL14, BH13, BL16.CH15, CL12) depending on the status flags "FDF1," "FDF2," and "OCFMOD."

3) Fault Localization: Till this stage, it is assumed that the OCF always occurs in INV1. As the top switch of INV1 [AH11 in the present example; see Fig. 3(a)] is connected in series to the bottom switch of INV2 [AL24 in the present example; see Fig. 3(a)], for a given phase winding (phase **aa'** in the present example), a detection of OCF could be due to the failure of either AH11 or AL24. To identify if AL24 has failed instead of AH11, the following procedure is adopted.

Step 1: The gating signals of all the top devices of INV1 (i.e., AH11, BH13, and CH15) are disabled and the gating signals of all the bottom devices of INV1 (AL14, BL16, and CL12) are continuously fired. This would create an isolated switched neutral as the points "a," "b," and "c" are connected to the negative terminal of the dc link of INV1 (see Fig. 1). The resulting would system, therefore, be identical to the conventional BLDC drive with a single dc power supply (with voltage $V_{\text{dc}}/2$).

Step 2: The gating signals are then applied exclusively to INV2. Based on the dc-link current of INV2 (i.e., I_{DC2}) the procedure described in the fault indication and assertion (Part-1) of the OCF diagnosis is repeated for INV2. If the fault still persists, then it is obvious that the OCF has occurred in INV2 (meaning that AL24 has failed instead of AH11, contrary to the initial assumption). To rule out false detection

TABLE I
OCF DIAGNOSIS INFORMATION

(FDF1,FDF2,OCFMOD)	FINV	OCFSW	Clamped switches
(1,1,1) or (1,0,2)	0	AH11	AL14,BL16,CL12
	1	AL24	AH21,BH23,CH25
(1,1,3) or (1,0,4)	0	BH13	AL14,BL16,CL12
	1	BL26	AH21,BH23,CH25
(1,1,5) or (1,0,6)	0	CH15	AL14,BL16,CL12
	1	CL22	AH21,BH23,CH25
(1,1,4) or (1,0,5)	0	AL14	AH11,BH13,CH15
	1	AH21	AL24,BL26,CL22
(1,1,6) or (1,0,1)	0	BL16	AH11,BH13,CH15
	1	BH23	AL24,BL26,CL22
(1,1,2) or (1,0,3)	0	CL12	AH11,BH13,CH15
	1	CH25	AL24,BL26,CL22

of OCF in INV2, the abovementioned procedure is initiated after a safe time period of "Tinvchk" from the time instant at which the OCF was first asserted. An additional flag "FINV" is used to denote the faulted inverter. If the OCF occurs in INV1, then "FINV" is set to "0." On the other hand, if the OCF occurs in INV2, then "FINV" is set to "1."

B. Control for the Open-Circuit Fault

1) Reconfiguration of the Faulted Inverter: As mentioned in Section III, based on the information obtained with reference to the OC fault, the inverter that develops the OC fault switch is clamped to a neutral state by applying an appropriate null vector (i.e., - - - or + + +). The type of the null vector is determined by the position of the faulted switch. For example, if any switch connected to the positive dc-rail fails, then all the three bottom switches are gated continuously, clamping that inverter to the state (- - -) and vice versa.

It is evident that the topology presented for OEWBLDCMD is capable of handling multiple OCFs, so long as they occur at one side (i.e., one or more among AH11, BH13, and CH15) and the switches of the other side are healthy (AL14, BL16, and CL12).

Table I summarizes the details regarding the reconfiguration of the system based on the status flags "FDF1," "FDF2," "OCDMOD," and "FINV."

2) Reconnection of the Healthy Battery Bank: After the reconfiguration of the inverter, the healthy battery connected to the faulty inverter is redeployed to enhance the reliability of the drive. This task is accomplished with the aid of the DPDT relays using the procedure described in the following paragraphs.

If FINV = 0, then INV1 has developed the OCF and its battery bank is connected in parallel to its counterpart by energizing the relay coil of the DPDT1 (see Fig. 1). Similarly, if FINV = 1, then INV2 has developed the OCF and its battery bank is connected in parallel to its counterpart by energizing the relay coil of the DPDT1 (see Fig. 1).

A simple transistor-based relay coil circuit, triggered by the "FINV" signal under OCF conditions, is employed to facilitate the reconnection of the battery bank. It is also possible to affect this changeover manually, if needed. To facilitate a safe reconnection, the battery of the faulted inverter is connected to its counterpart (in parallel) after a delay of "Tdrelay."

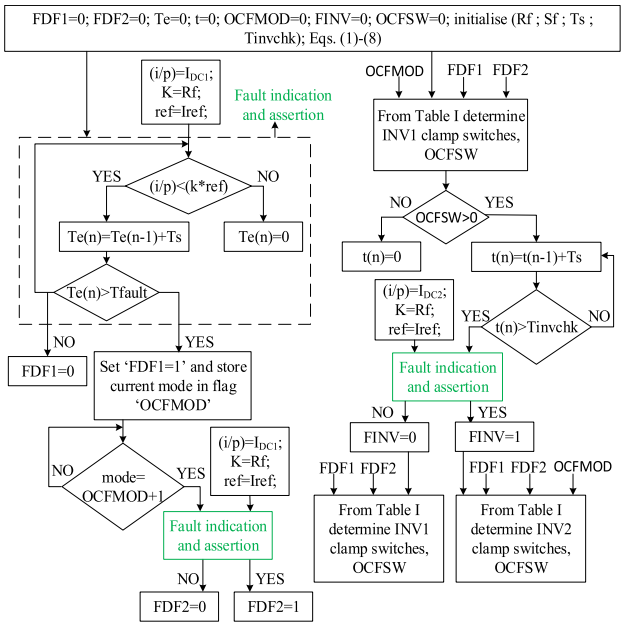


Fig. 4. Flowchart representing the fault diagnosis and reconfiguration for OCF.

Fig. 4 shows the flowchart of fault diagnosis and reconfiguration for OCF.

V. FAULT DIAGNOSIS AND CONTROL FOR SHORT-CIRCUIT FAULT

The proposed SCF detection method is based on the measurement of the instantaneous line–line voltages (v_{ab}, v_{bc}, v_{ca}, $v_{a'b'}$, $v_{b'c'}$, and $v_{c'a'}$). The matrix "v_L" represents the line voltages, that is

$$v_L = [v_{ab}\ v_{bc}\ v_{ca}\ v_{a'b'}\ v_{b'c'}\ v_{c'a'}]^{\mathrm{T}}. \tag{11}$$

The method of diagnosing and controlling the SCF is explained in the following paragraphs.

A. Diagnosis of the Short-Circuit Fault

If the SCF takes place in switch AL14 during its conduction in mode-4, then it will not affect its normal operation of mode-4 and mode-5. However, it must be detected during mode-6 (i.e., before entering mode-1, in order to avoid the shoot-through of dc supply as AH11 is scheduled to turn on in mode-1). It may be noted that in mode-6, the switches CH15 and BL16 are in conduction. Development of SCF due to the failure of AL14 would cause the line–line voltage v_{ab} to drop to zero in mode-6, which can easily be detected by monitoring all the six line–line voltages mentioned in (7). Thus, there exists a respectable time period corresponding to 60°(electrical) to detect if $v_{ab} = 0$ (where it should not be equal to zero if AL14 is healthy).

In practice, a threshold "$v_{th,sc}$" is used to detect the SCF, which is typically 5% (say "k") of the peak of rated line–line voltage ("v_{ref}")

$$v_{th,sc} = k * v_{ref}. \tag{12}$$

If any one of the absolute values of the measured line–line voltages (say $|v_{xy}|$) is lesser than "$v_{\text{th,sc}}$," then the error time period "Te(n)" starts accumulating according to the following difference equation:

$$\begin{cases} \text{Te(n)} = \text{Te(n} - 1) + \text{Ts}, & \left|v_{\text{xy}}\right| < v_{\text{th,sc}} \\ \text{Te}\,(n) = 0, & |v_{\text{xy}}| > v_{\text{th,sc}} \end{cases} \tag{13}$$

where $(x)\epsilon$ (a, b, c, a′, b′, c′) and (y) ϵ (b, c, a, b′, c′, a′)

When the count accumulated is more than critical time period "Tfault," then the corresponding flag "SCF_{ab}" is set to "1." Another flag named "SCFMOD" is used to identify the mode number in which the fault is detected. For example, the flag "SCF_{ab}" can be set to "1" either in mode-3 (due to the failure of AH11) or mode-6 (due to failure AL14). Consequently, the flag "SCFMOD" can have a value of either "3" (if AH11 fails) or "6" (if AL14 fails). The generalized procedure of setting the flags SCF_{xy} and SCFMOD is represented by the following equations:

$$\begin{cases} \text{SCF}_{\text{xy}} = 1;\ \text{SCFMOD} = \text{m if Te(n)} > \text{Tfault} \\ \text{SCF}_{\text{xy}} = 0;\ \text{SCFMOD} = 0 \text{ if Te(n)} < \text{Tfault} \end{cases} \\ (\text{For mode} - (m),\ \text{where } (1 \le m \le 6)) \tag{14}$$

where (x) ϵ (a, b, c, a′, b′, c′) and (y) ϵ (b, c, a, b′, c′, a′)

The matrix "SCF_L" contains all the six SC flags, that is

$$\text{SCF}_L = [\text{SCF}_{\text{ab}}\ \text{SCF}_{\text{bc}}\ \text{SCF}_{\text{ca}}\ \text{SCF}_{\text{a'b'}}\ \text{SCF}_{\text{b'c'}}\text{SCF}_{\text{c'a'}}]^T. \tag{15}$$

Table II summarizes all possibilities of SCF and the status of the corresponding flags, i.e., SCF_{xy}, where {(x, y) ϵ (a, b, c, a', b', c')} and the corresponding values of "SCFMOD." The device, which is identified to be the source of SCF, is also stored in an additional flag named "SCFSW."

TABLE II
SHORT-CIRCUIT FAULT DIAGNOSIS INFORMATION

Fault indication	Fault assertion (Te > Tfault)	SCF_{L}	SCFMOD	SCFSW	Clamped switches
$\lvert v_{\text{ab}}\rvert < v_{\text{th,sc}}$	Yes	$\text{SCF}_{\text{ab}} = 1$	3	AH11	AH11, BH13, CH15
			6	AL14	AL14, BL16, CL12
	No	$\text{SCF}_{\text{ab}} = 0$	-	-	-
$\lvert v_{\text{bc}}\rvert < v_{\text{th,sc}}$	Yes	$\text{SCF}_{\text{bc}} = 1$	5	BH13	AH11, BH13, CH15
			2	BL16	AL14, BL16, CL12
	No	$\text{SCF}_{\text{bc}} = 0$	-	-	-
$\lvert v_{\text{ca}}\rvert < v_{\text{th,sc}}$	Yes	$\text{SCF}_{\text{ca}} = 1$	1	CH15	AH11, BH13, CH15
			4	CL12	AL14, BL16, CL12
	No	$\text{SCF}_{\text{ca}} = 0$	-	-	-
$\lvert v_{\text{a'b'}}\rvert < v_{\text{th,sc}}$	Yes	$\text{SCF}_{\text{a'b'}} = 1$	6	AH21	AH21, BH23, CH25
			3	AL24	AL24, BL26, CL22
	No	$\text{SCF}_{\text{a'b'}} = 0$	-	-	-
$\lvert v_{\text{b'c'}}\rvert < v_{\text{th,sc}}$	Yes	$\text{SCF}_{\text{b'c'}} = 1$	2	BH23	AH21, BH23, CH25
			5	BL26	AL24, BL26, CL22
	No	$\text{SCF}_{\text{b'c'}} = 0$	-	-	-
$\lvert v_{\text{c'a'}}\rvert < v_{\text{th,sc}}$	Yes	$\text{SCF}_{\text{c'a'}} = 1$	4	CH25	AH21, BH23, CH25
			1	CL22	AL24, BL26, CL22
	No	$\text{SCF}_{\text{c'a'}} = 0$	-	-	-

B. Control for the Short-Circuit Fault

1) Reconfiguration of the Faulted Inverter: As in the case of OCF, an appropriate null vector (i.e., - - - or + + +) is also employed in this case to provide a switched neutral point by the faulty inverter. Here, also, the type of the null vector is determined by the position of the faulted switch. In this case, if any switch connected to the positive dc rail develops an SCF, then the remaining switches connected to the positive dc rail are gated continuously, clamping that inverter to the state (+ + +) and vice versa.

Upon the identification of the faulted switch (say AH11), all the switches connected to the positive dc terminal of INV1 (BH13 and CH15) in this case are continuously gated, creating a switched neutral at point "X" (see Fig. 1). In other words, the gating signals corresponding to the lower switches (AL14, BL16, and CL12) are withdrawn, reconfiguring the power circuit. A similar action is adopted if the SCF is identified in INV2. Table II (last column) also summarizes as to which switches are turned on for all the possible SCFs.

2) Reconnection of the Healthy Battery Bank: The process of triggering the DPDT relays after the reconfiguration of the faulty inverter is described in the following.

If the SCF is developed in INV1, then one of the flags SCF_{ab}, SCF_{bc}, and SCF_{ca} is set to a logic level of "1." These flags are input to an OR operation to derive the trigger signal to the relay coil of DPDT-1 (see Fig.1). A similar procedure is adopted for the reconnection of the battery bank connected to INV2, in which the flags ($\text{SCF}_{\text{a'b'}}$, $\text{SCF}_{\text{b'c'}}$, and $\text{SCF}_{\text{c'a'}}$) are used to derive the trigger signal for DPDT-2.

Fig. 5 shows the flowchart of fault diagnosis and reconfiguration for SCF. The principal advantages of the proposed fault-detection schemes are given in the following.

1) The SCF detection is essentially preemptive in nature as the acts of detection and the subsequent circuit reconfiguration are carried out before the SCF can cause overcurrents in healthy switching devices and damage them.

2) It uses simple, cheap, and easily available analog devices to achieve electrical isolation between the power circuit and the control platform, avoiding the high-cost Hall voltage sensors, without compromising on the bandwidth.

VI. SENSING AND INTERFACING CIRCUITRY

A. Description of Hardware Circuit Used for Fault Diagnosis

From the description of OCF presented in Section IV, it is obvious that the detection of OCF requires the sensing of the two dc-link currents. Similarly, the diagnosis of SCF requires

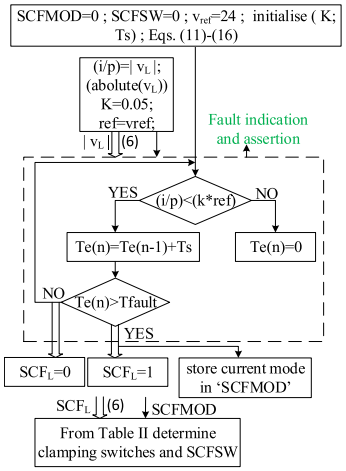


Fig. 5. Flowchart representing the fault diagnosis and reconfiguration for SCF.

TABLE III
MACHINE PARAMETERS

Rated voltage	48 V	B1=24 V B2=24 V
Rated Torque	0.6 N-m	
Rated Speed	3200 Rpm	
Resistance per Phase	0.295 Ω	
Back-EMF constant	11.8 V/Krpm	
Rated Power	250 W	
Number of Poles	8	

the measurement of all six line voltages (v_{ab}, v_{bc}, v_{ca}, $v_{a'b'}$, $v_{b'c'}$, and $v_{c'a'}$) present on either side of the motor, with open-ended stator windings. All these line–line voltages need to be electrically isolated with respect to the ground point of the control platform (i.e., dSPACE in the present case).

B. Design of Low-Cost Analog Voltage Sensor With Electrical Isolation

As mentioned in Section V, the sensing of SCF involves the measurement of six line voltages. The line–line voltages are measured using differential amplifiers (shown at extreme left and at extreme right of Block-1 and Block-2 in Fig. 6). Though Fig. 6 shows the sensing of the line voltages "v_{ab}" (Block-1) and "$v_{a'b'}$"(Block-2) only, such circuits are replicated for the sensing of the other line–line voltages as well (Blocks 4-6; see Fig. 6). The dc-link voltages of and INV2 are each equal to 24 V (see Table III). These dc-link voltages are split equally using capacitors (see Fig. 6), and two isolated ground points "G1" and "G2" are derived.

The operational amplifiers derive their power supplies from the X and X' points, Y and Y' points, to sense the line voltages on INV1 and INV2 sides, respectively ($v_{XG1} = v_{YG2} = 12$ V and $v_{X'G1} = V_{Y'G2} = -12$ V). In other words, the voltage sensing circuitry derives their power supplies directly from the vehicle battery. In order to achieve electrical isolation, precision isolation amplifiers (ISO124), which are of unity gain, are employed. However, this device needs another isolated power supply to obtain electrical isolation between the grounds "G1" and "G2" and the ground of the control platform (G3).

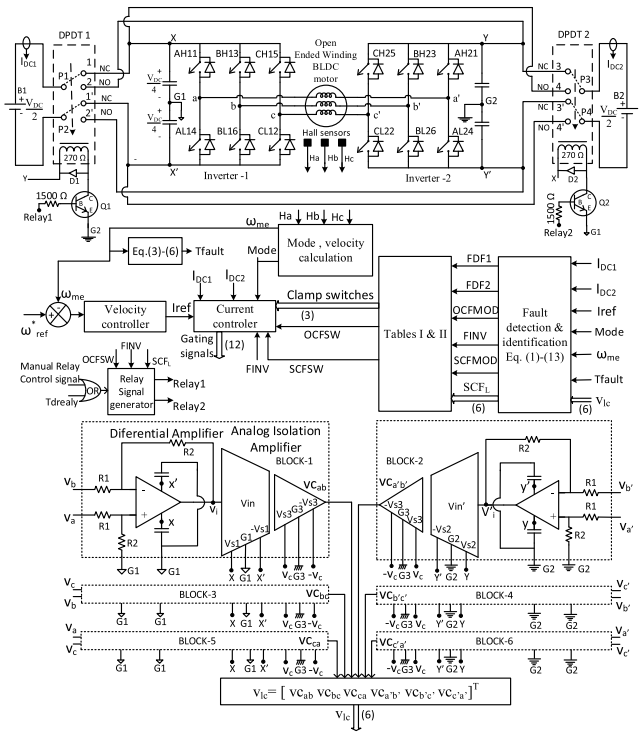


Fig. 6. Overall configuration of fault-tolerant drive.

The outputs of all the measured line–line voltages obtained at the outputs of the isolation amplifiers that are electrically isolated are represented by a matrix "v_{lc}," that is

$$v_{lc} = [vc_{ab}\ vc_{bc}\ vc_{ca}\ vc_{a'b'}\ vc_{b'c'}\ vc_{c'a'}]^{T} \tag{16}$$

These control voltages are restored back to the original value by multiplying with appropriate scale factor (i.e., depending on differential amplifier gain) in the control platform. Alternatively, all isolated power supplies can be derived directly from the vehicle battery using an appropriate switch mode power supply.

As stated in Section III, two DPDT switches are used in this system to connect the battery bank of the faulted inverter in parallel to its counterpart. The operating voltage of the DPDT relay coil is 12 V. After the diagnosis of the fault (i.e., OCF or SCF) and the subsequent reconfiguration of the power circuit, one of the relay coils is energized through a transistor, which derives its base signal from the control platform (i.e., dSPACE 1104 in this article). The transistors "Q1" and "Q2" control the relay coils of DPDT1 and DPDT2 relay, respectively (see Fig. 6). It can easily be verified that the power supplies for these transistors must be cross-connected for an appropriate reconnection of the healthy reconnection of the healthy battery corresponding to the faulted inverter. For example, when INV2 fails, the battery bank "B2" must be reconnected in parallel to its counterpart (i.e., "B1"). It can be easily verified that this objective is achieved only when the relay transistor that reconnects the battery "B2" derives its power supply from "B1" (and vice versa).

VII. RESULTS AND DISCUSSION

The behavior of the OEWBLDCM drive under OCF and SCF is first assessed with simulation studies using MATLAB/

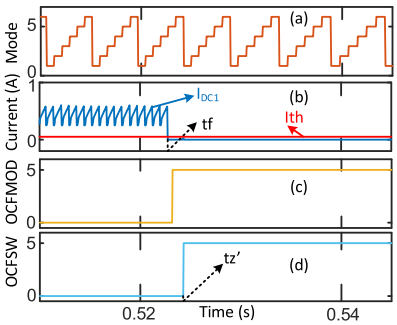


Fig. 7. Simulation results for OCF in INV1 (i.e., switch CH15). (a) Mode of operation. (b) I_{DC1} and I_{th}. (c) OCFMOD. (d) OCFSW.

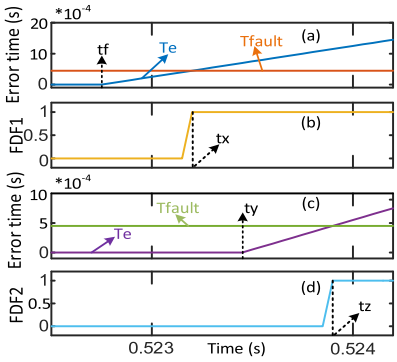


Fig. 8. Simulation results representing statuses of flags for OCF in INV1 (i.e., switch CH15). (a) Te, Tfault (mode-5). (b) FDF1. (c) Te, Tfault (mode-6). (d) FDF2.

Simulink and then is experimentally validated using the dSPACE 1104 control platform. The proposed fault-tolerant OEWBLDCM drive is simulated using MATLAB and is experimentally validated using the dSPACE control platform. Table III presents the motor parameters used for simulation as well as experimentation.

The drive is operated in open loop as well as closed loop to demonstrate the effectiveness of the proposed fault diagnosis and reconfiguration algorithms. Simulation and experimental results for OCF are studied by opening the switching devices CH15 and CL22 for INV1 and INV2, respectively.

During experimentation, the OCF condition is enforced on the inverters by withdrawing the gating pulses to them. Similarly, to enforce the SCF conditions, the gating pulses for AL14 and AL24 are applied continuously. As mentioned in Sections IV and V, two flags, namely, OCFSW and SCFSW, are employed to identify and indicate the faulted switching device. As stated in Section IV, it is assumed that OCF takes place in INV1 by default. OCF is identified in INV2 only when it is identified that it did not take place in INV1.

A. Simulation Results

Figs. 7 and 8 show the simulation results to detect the OCF in INV1. The mode number (1–6) of conduction is identified by monitoring the pattern of the Hall Position sensors placed on the shaft of the motor. Thus, the signal that identifies the mode of conduction starts at "1" and is incremented by "1," whenever a change in the mode of conduction is identified by monitoring the Hall sensor signals. It rolls back to "1" again

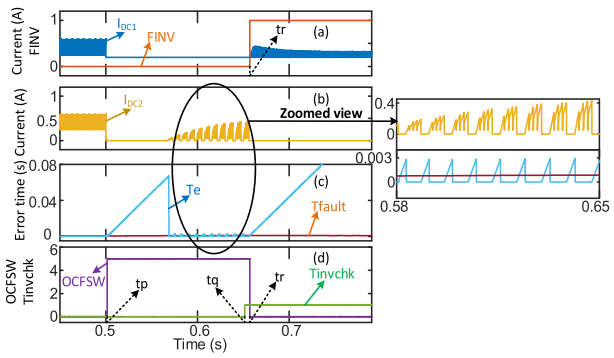


Fig. 9. Simulation results representing fault diagnosis of OC fault in INV2 (i.e., switch CL22). (a) I_{DC1}, FINV. (b) I_{DC2}. (c)Te, Tfault. (d) OCFSW, Tinvchk. Left: normal view. Right: zoomed-in view of encircled portion.

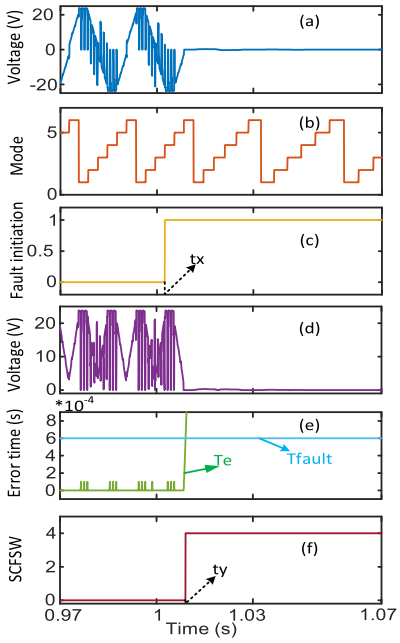


Fig. 10. Simulation results showing SC fault diagnosis for INV1 (i.e., switch AL14). (a) v_{ab}. (b) Mode. (c) Fault initiation. (d) $|v_{ab}|$. (e) Te, Tfault. (f) SCFSW.

from mode "6," as each mode of operation lasts for 60 electrical degrees [see Fig. 7(a)]. Thus, when the dc-link current falls to zero following the development of an OCF [see Fig. 7(b)], the mode of conduction in which the OCF occurs is identified and is registered in the flag "OCFMOD" [see Fig. 7(c)]. Based on the statuses of the internal flags "FDF1," "FDF2," and "OCFMOD" (see Figs. 7 and 8), the faulted switch is identified as CH15 in the present case (from Table I) and is stored in the flag "OCFSW" [at "tz"; see Fig. 7 (d)] with its device number.

Fig. 8 shows the internal process of setting the flags "FDF1" and "FDF2". When the dc-link current of INV1 drops to a value, which is lesser than the threshold current [at the instant "tf"; see Figs. 7(b) and 8(a)], an accumulator is initiated [see (3)]. When the count accumulated is more than the critical time period ("Tfault"), the flag "FDF1" is set [at the instant "tx"; see Fig. 8 (b)]. This means that at the instant "tx," it is identified that so far as INV1 is concerned, the faulted switch could be either CH15 or AL14. To further identify which of

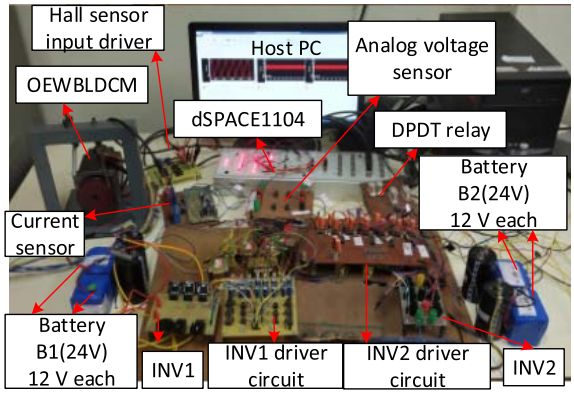


Fig. 11. Fault-tolerant OEWBLDCM drive experimental set-up.

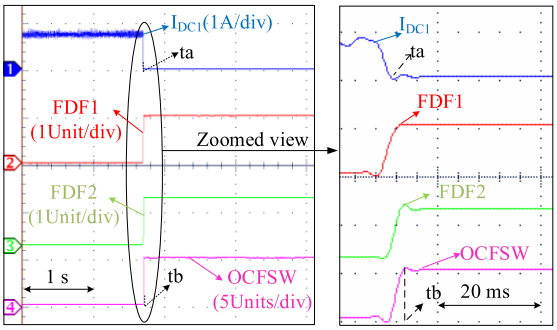


Fig. 12. Experimental results representing statuses of flags during OCF in INV1 (i.e., switch CH15). Left: normal view. Right: zoomed-in view of encircled portion.

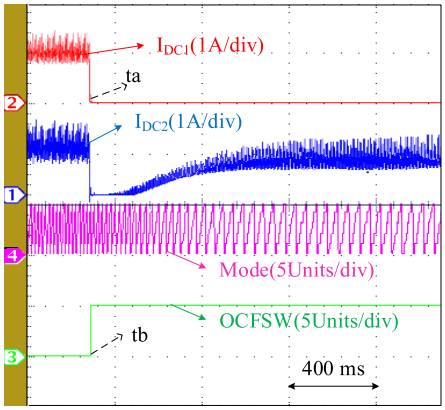


Fig. 13. Experimental results for OCF in INV1 (i.e., switch CH15).

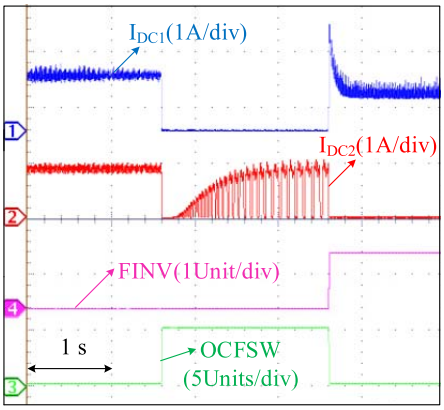


Fig. 14. Experimental results for OCF in INV2 (i.e., switch CL22).

these two switches has failed, another accumulator is initiated at the beginning of the next mode [instant "ty"; see Fig. 8(c)]. When the count accumulated is greater than the "Tfault," the flag FDF2 is set to "1" [at "tz"; Fig. 8(d)]. Based on the statuses of flags FDF1, FDF2, and OCFMOD, the faulted device is identified using Table I.

Fig. 9 shows the simulation results for the identification of OCF in INV2. The device CL22 is in series with CH15 under normal operation, and it is initially assumed that the OCF occurs in INV1. Thus, the OCF is initially attributed to CH15 at time "tp" [see Fig. 9(d)] and only INV2 is operated by clamping INV1 (i.e., a switched neutral point is created by turning on the switching devices connected to the negative dc rail of INV1). However, if the OCF exists in INV2, then it is observed that the dc current I_{DC2} is discontinuous in nature. This situation is presented in Fig. 9(b), where a pulsating current waveform [zoomed-in version of Fig. 9(b)] is observed as I_{DC2} can exist in only four modes out of the six possible modes of conduction, confirming that the OCF has occurred in INV2. To rule out false positive identification (i.e., a spurious detection), the process of fault detection is initiated at the time instant "tq" [see Fig. 9(d)] and is diagnosed at time "tr" and thereby "FINV" flag is set to high [at instant "tr"; in Fig. 9(a)]. When it is identified that the OCF has occurred in INV2, the switched neutral is created by INV2, and INV1 is operated normally.

The simulation result that demonstrates the SCF diagnosis process is presented in Fig. 10. The SCF was induced in AL14 by gating it continuously. However, as AL14 is expected to conduct normally during mode-4 and mode-5 (see Fig. 2), the effect of SCF is not visible immediately during these two modes of operation. It would be visible only in mode-6 and the circuit reconfiguration must take place within this mode of operation; otherwise, as described in Section V, a shoot-through fault would occur. Fig. 10(a) and (b) shows the line voltage "v_{ab}" and the signal corresponding to the mode of operation. The SCF induced into the system at the instant "tx" [see Fig. 10(c)]. Fig. 10(d) shows $|v_{ab}|$, which is actually compared with "v_{th}"(see Table II), which is selected to be 5% of the peak value of the line voltage (i.e., $0.05 \times 24 = 1.2$ V). As mentioned in Section V, if $|v_{ab}| < v_{th}$ for a time period of "Tfault" [see Fig. 10(e)], then the occurrence of SCF is confirmed in INV1. Fig. 10(f) shows the switching device in which SCF is identified (switch "4" in INV1 in this case, which is AL14).

B. Experimental Results

To validate the proposed diagnosis and reconfiguration of the dual-inverter fed OEWBLDCM drive, the dSPACE-1104 hardware control platform is used and the corresponding experimental setup is shown in Fig. 11.

Figs. 12 and 13 show the process of fault diagnosis and circuit reconfiguration with zoomed version when the drive is operated in open loop and an OCF is deliberately induced for CH15 (which is present in INV1; see Fig. 1). The top

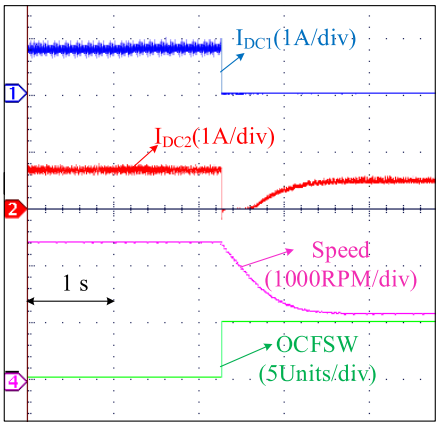


Fig. 15. Experimental results for the OCF in INV1 under open-loop operation of the drive.

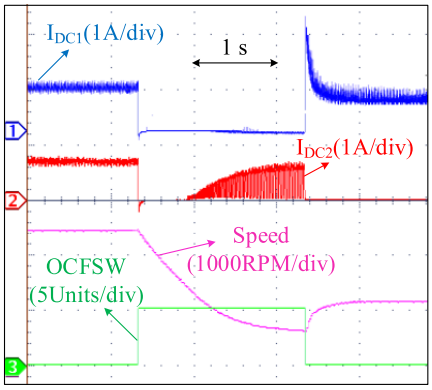


Fig. 16. Experimental results for the OCF in INV2 under open-loop operation of the drive.

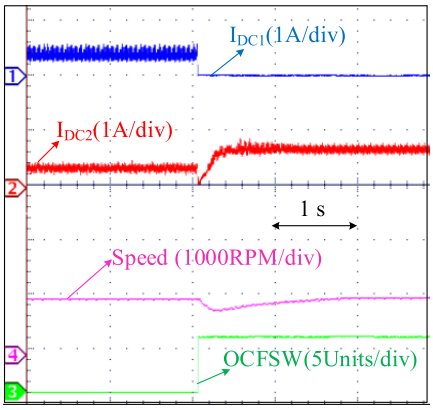


Fig. 17. Experimental results for the OCF in INV1 under closed-loop operation of the drive.

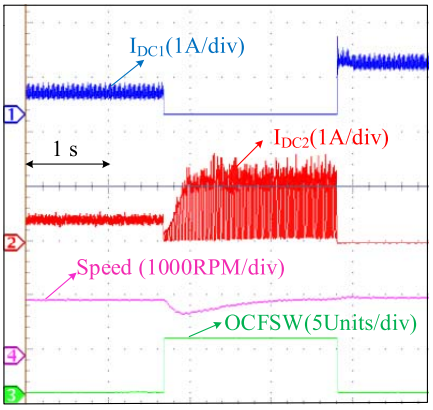


Fig. 18. Experimental results for the OCF in INV2 under closed-loop operation of the drive.

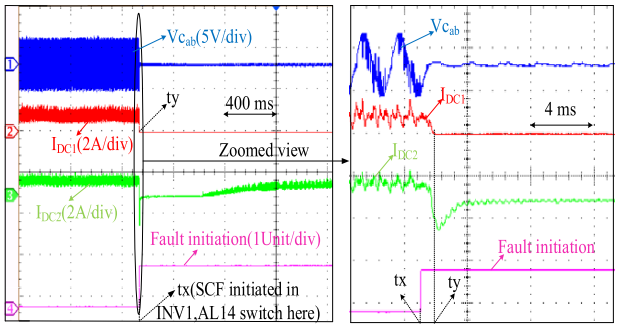


Fig. 19. Experimental results for the detection of SCF in INV1 (i.e., switch AL14). Left: normal view. Right: zoomed-in view of encircled portion.

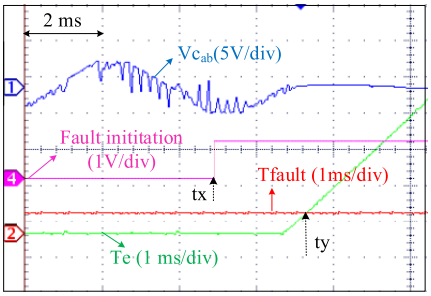


Fig. 20. Experimental results for the detection of SCF in INV1 (i.e., switch AL14).

trace of Fig.12 shows the dc-link current of INV1. When an OCF is induced for the switching device CH15, it drops down to zero. The second and third traces of Fig. 12, respectively, show the setting of the fault diagnosis flags (FDF1 and FDF2), which are set to "1" in response to the detection of OCF. The fourth trace shows the flag "OCFSW," which displays a value of "5," indicating that the OCF is detected in CH15.

The process of reconfiguration is shown experimentally in Fig. 13. It may be noted that after the identification of the OCF in CH15, a switched neutral is created on INV1 and INV2 is operated normally. Thus, one may notice a momentary interruption for both of the dc-link currents (I_{DC1} and I_{DC2}) of the respective inverters (at the instant "ta"). During the time period (tb-ta), the process of identification and the reconfiguration of the power circuit are carried out, as shown in Figs. 12 and 13. As the drive is operated in open loop, due to the reduced voltage applied to the phase windings of the motor, the motor speed is reduced, as it is evident from the third trace of Fig. 13.

Fig. 14 shows the experimental results when the OCF occurs in CL22 belonging to INV2. In this case, also, following the OCF, both dc-link currents (I_{DC1} and I_{DC2}) drop to zero momentarily. As explained in Section IV, it is assumed that the OCF takes place in INV1 and INV2 is operated normally, to ascertain whether or not this assumption is true. The presence of the current-zero instants in I_{DC2} clearly reveals that this assumption is false (as only four out of the six modes of conduction is possible in INV2). Due to the realization that the fault occurs in INV1, it is reconfigured to a switched

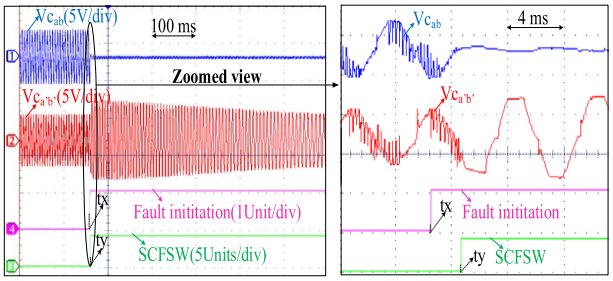


Fig. 21. Experimental results for the detection of SCF in INV1 (i.e., switch AL14). Left: normal view. Right: zoomed-in view of encircled portion.

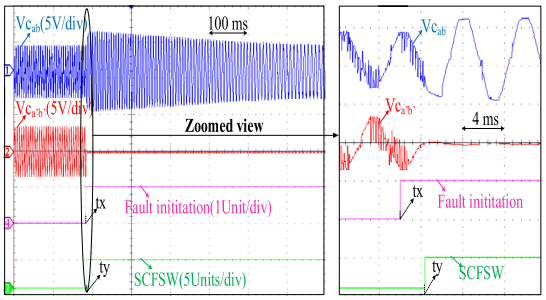


Fig. 22. Experimental results for the detection of SCF in INV2 (i.e., switch AL24). Left: normal view. Right: zoomed-in view of encircled portion.

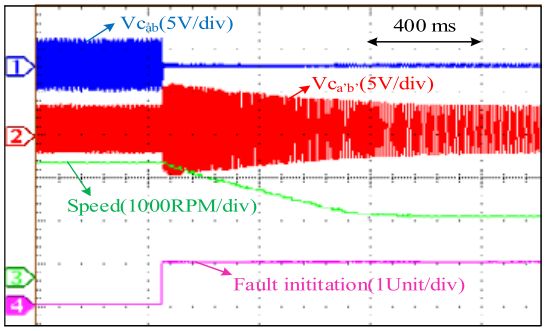


Fig. 23. Experimental results for SC Fault in INV1 under open-loop operation.

neutral and INV2 is operated normally. The third trace of Fig. 14 shows the status of the flag "FINV," which is set to "1," when the assumption of INV1 being faulty is wrong. Consequent to this, the flag "OCFSW," which identifies the faulted switch in INV1, is reset to "0."

The experimental results, which demonstrate the performance of the drive under faulted condition, are shown in Figs. 15 and 16 (open loop) and Figs. 17 and 18 (closed loop). From Figs. 15 and 16, it may be observed that the speed (shown in third trace) is reduced when only one inverter is in operation instead of two. In contrast, when the drive is operated in closed loop (see Figs. 17 and 18), the speed is restored to the reference value, despite one inverter being out of action. However, it should be realized that the restoration of speed is possible only up to the half of the rated speed of the motor.

The experimental results, which demonstrate the transition of SC and its diagnosis process, are shown in (see Figs. 19–21 and 23). The six line–line voltages are monitored corresponding to the sampling frequency of the

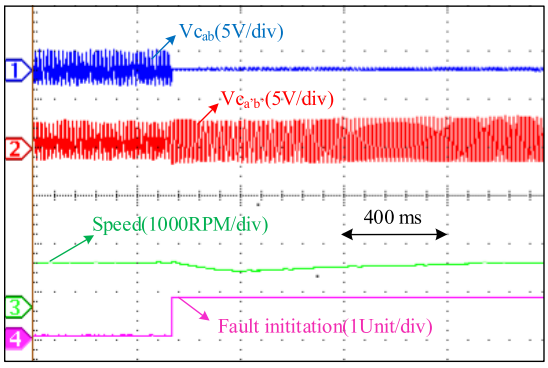


Fig. 24. Experimental results for SC Fault in INV1 under closed-loop operation.

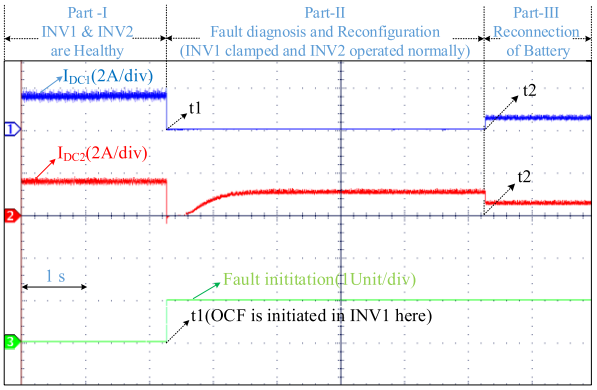


Fig. 25. Experimental results showing combination of fault diagnosis and fault control for OCF in INV1.

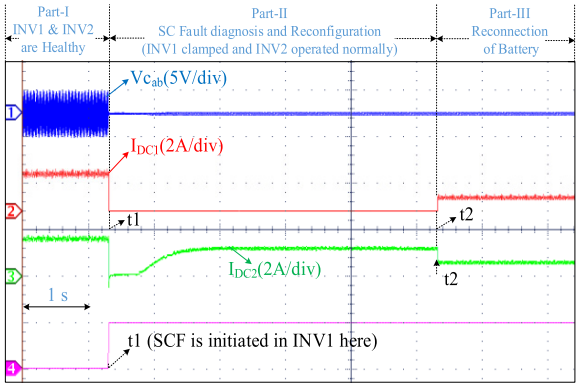


Fig. 26. Experimental results showing combination of fault diagnosis and fault control for SCF in INV1.

digital control platform (70 μS). To verify the effectiveness of the proposed fault diagnosis algorithm, the gating signal to the switching device AL14 is continuously turned on from the instant "tx" (see Figs. 19–21). Under normal operating conditions, it is apparent from Fig. 19 that the line voltage "v_{ab}" is not equal to zero. However, when an SCF occurs in INV1 at the instant "tx" (see Figs. 19–21), the line voltage (v_{ab}) drops to zero in mode-6 (which was not supposed to be during normal conditions), triggering an accumulator. When the output of this accumulator [which is denoted as Te; see (13)] is greater than a prespecified count "Tfault" (at the instant "ty" in Fig. 20), the flag "SCFSW" is loaded with the number corresponding to the faulted switch ("4," for the

TABLE IV
COMPARISON OF DIFFERENT TOPOLOGIES WITH THE PROPOSED TOPOLOGY

S. No	Topological features	Topology [21]	Topology [25]	Topology [26]	Proposed Topology
1	No. of switches in the inverter	6 switches (Conventional) + 3 TRIACs	6 switches (Conventional) + 6 TRIACs + 1 additional leg (2 switches)	12 switches	12 switches
2	Switch ratings	Rated motor voltage and current	Rated motor voltage and current	Rated motor voltage and twice the rated motor current	Half the rated motor voltage and rated motor current
3	Fault diagnosis in inverter extra switches	No	No	Yes	Yes
4	Fault diagnosis	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
5	Fault tolerance	Only OCF	OCF, SCF	OCF, SCF	OCF, SCF
6	Motor rating	Designed for rated voltage and current	Designed for rated voltage and current	Designed for double the rated current	Designed for rated voltage and current
7	Auxiliary components	No	Buck converter + 3switches + 1 fault protective leg	Buck converter + 1 SPDT switch + 1 fault protective leg	2 DPDT relays

TABLE V
COST INCURRED FOR PRODUCTS (IN INDIAN RUPEES)

Name of the equipment		Each unit cost (Rs./-)	No. of quantities	Total Cost (Rs./-)
(a) Motor (96 V, 3 KW BLDC motor)		30,082	1	30,082
(b) Cost of li-ion battery (12V, 60AH,720WH)		12,892	8	1,03,138
(c) Cost of Inverter with driver (with switch voltage and current safety factor taken as 2)	(c_1) Cost of OEWBLDCM Inverter topology	(60 + 285)	12	4,140
	(c_2) Cost of conventional Inverter topology	(148 + 285)	6	2,598
(d) Sensors	(d_1) Current sensor	1,366	2	2,732
	(d_2) Voltage sensor components in the present manuscript (ISO124, TL084CN)	(868 + 13)	ISO124→6 TL084CN→2	5,234
(e) Auxiliary components (DPDT Relay)		738	2	1,476

Percentage of additional cost incurred with respect to the conventional BLDC motor drive :

$$=\left(\frac{d_2+e+(c_1-c_2)}{a+b+c_2+d_1}\right)*100\%$$

$$=\left(\frac{5234+1476+(720+3420)-(888+1710)}{30082+103138+(888+1710)+2732}\right)*100$$

$$=5.96\%$$

switch AL14; see Fig. 21) by using Table II. It may be noted that after the identification of the fault and the reconfiguration of the power circuit, the entire drive current is sourced by INV2 alone (see Figs. 19 and 21). Fig. 21 clearly shows the time elapsed between the initiation of the fault (at "tx") and the identification of the fault (at "ty"). A similar experimental result for the SCF developed in INV2 for the device "AL24" is shown in Fig. 22. Figs. 23 and 24 show the speed transient when the drive is operated in the open-loop and closed-loop conditions, respectively, when the SCF occurs in INV1.

The experimental result, which demonstrates the combination of OC fault diagnosis and fault control, is presented in Fig. 25. As mentioned in Section III, whenever a fault is detected (OCF or SCF) and the faulty inverter is reconfigured to a switched neutral, the healthy battery bank feeding it is reconnected to its counterpart feeding the healthy inverter (in parallel). It may be noted that both I_{DC1} and I_{DC2} are nonzero prior to the fault (see Part-I; see Fig. 25). When an OCF is induced in INV1 (i.e., switch CH15) at instant "t1" (see Fig. 25), both I_{DC1} and I_{DC2} fall to zero. After the successful diagnosis of the OC fault and the reconfiguration of the faulty inverter, INV2 alone supplies power to the BLDC motor (see Part-II; see Fig. 25). Under these conditions, it is desirable to connect the battery ("B1") of INV1 in parallel to its counterpart ("B2"). This task is accomplished by turning on the transistor "Q1" (see Fig. 6) connected to the relay coil of DPDT1 (at instant "t2"; see Fig. 25). It may be observed from Fig. 25 that the load current is then shared by the battery "B1" and "B2" following the reconnection (see Part-III; see Fig. 25).

Fig. 26 shows the experimental results pertaining to the combination of the SC fault diagnosis and fault control. It may be noted that the line voltage (v_{ab}) and the dc-link currents of the respective inverters (I_{DC1} and I_{DC2}) are nonzero prior to the fault (see Part-I; see Fig. 26). From Fig. 10(a) and (b), it is evident that line voltage v_{ab} is not equal to zero in mode-6 under healthy conditions. However, when an SCF occurs in INV1 (induced forcefully during the experimentation by triggering AL14 permanently) at instant "t1" (see Fig. 26), the line voltage (v_{ab}) drops to zero in mode-6 [see Fig. 10(a) and (b)]. After the diagnosis of the SCF based on the analog signals corresponding to the line voltage and the subsequent reconfiguration of the faulty inverter, the motor is constrained to be fed exclusively by INV2 (see Part-II; see Fig. 26). As in the case of the OCF, in order to utilize the battery connected to the faulty inverter, the DPDT1 relay is energized (at instant "t2"; see Fig. 26) by turning on the transistor "Q1" (see Fig. 6). Thus, the battery bank "B1"of INV1 is connected in parallel to its counterpart. It may be observed from Fig. 26 that following the reconnection, the load current is shared by both the batteries "B1" and "B2" (see Part-III; see Fig. 26).

VIII. FEASIBILITY ANALYSIS OF THE PROPOSED POWER CIRCUIT CONFIGURATION

A comparative study is carried out to assess the feasibility of the proposed power circuit configuration vis-à-vis the other fault-tolerant topologies reported in the earlier literature.

Table IV summarizes the features of the proposed power circuit with other fault tolerant topologies reported in the earlier literature.

A cost analysis is also performed to assess the economic viability of the proposed power circuit configuration (shown in Table V). In this analysis, the costs of additional accessories, which impart the feature of fault tolerance to the drive configuration, are considered.

It should be noted that in the abovementioned analysis, only the raw material cost of the electrical items is considered and costs of vehicle chassis, vehicle body, control platform, and other accessories (which will be common for conventional and other topologies) are not included.

Thus, with an increment of reasonable additional raw material cost to the conventional electric drive configuration, the drive is capable of achieving fault tolerance to both OCF and SCF in the semiconductor switching devices, enhancing the reliability of the drive.

IX. Conclusion

Exploiting the structural symmetry of the power circuit configuration, this article shows that fault-tolerant capabilities can be imparted to the OEWBLDCM drive against both open-circuited as well as the short-circuited faults. This articlei proposes simple algorithms to diagnose these two faults for the OEWBLDCM drives. The scheme to diagnose the SCF is based on the fact that there exists a natural gap of 60 electrical degrees in a BLDC motor drive between the turn-off and turn-on times of the switching devices of any given phase leg. This observation paves way to devise a diagnostic scheme, which is based on the sensing of the line voltages of the open-end winding BLDC motor. This scheme ensures that the fault is diagnosed before it can cause overcurrents through the switching devices. The SCF is sensed with simple and easily available components, without compromising on the issues of electrical isolation and bandwidth. The OEWBLDCM drive can be operated at reduced power following either of these two faults. This feature enhances the reliability of the drive. It is shown that the speed of the drive is controlled at a constant value following either OCF or SCF, if it is intended to run the drive below half of its rated speed. A simple method of reconfiguring the power circuit is described in this article, in which the faulted inverter is reconnected to provide a switched neutral point. The charge available in the healthy battery bank connected to the faulted inverter is also utilized in the proposed drive.

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