2020 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)

An Integrated Four-leg Three-phase Transformerless PV Inverter with Voltage Boosting Capability

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***Abstract*— The leakage current minimization and voltage-boosting are the two essential features for transformerless PV inverter configurations. In this paper, a conventional four-leg three-phase inverter is retrofitted with an inverting buck-boost converter to achieve the voltage boosting capability. The proposed power circuit configuration facilitates power transfer either directly from the PV source or through the buck-boost converter. Further, a new group of PWM schemes is introduced for the proposed power circuit configuration. These modulation strategies are capable of eliminating the switching frequency transitions from the common-mode voltage while maintaining the dc-link utilization for the inverter. The proposed modulation strategy results in a higher effective frequency for the fourth leg to optimize the design of the boosting inductor. The working principle of the proposed power converter is validated with simulation results.**

Keywords—Photovoltaic inverter, Four-leg inverter, leakage current, common-mode voltage, Voltage boosting.

I. Introduction

The transformerless solar inverters are gaining popularity in both residential as well as industrial applications. Transformerless inverters suffer from the disadvantage of leakage current as these inverter configurations lack the galvanic isolation in their structures. The leakage current adversely affects the safety and the life span of the PV panels. In view of this, the German standard VDE 0126-1-1 stipulates the restriction on the leakage current below the maximum limit of 30mA [1].

Several techniques have been described in the literature to eliminate the common-mode voltage from the three-phase multilevel inverter. It has been shown in [2] that, the transitions in the CMV can be reduced with additional switching devices, which are switched in the zero states of the inverter. However, the modulation strategy and the modification of the configuration are not adequate to eliminate all of the transitions from the common-mode voltage (CMV). Also, these modified configurations result in higher power losses. To optimize the loss and obtain a constant CMV, various PWM techniques are analyzed for three-phase inverters in [3]. But, these PWM techniques suffer from various disadvantages such as the underutilization of the dc-link, increased THD in the current. Though these PWM schemes effectively reduce the CMV, they won't result in the complete elimination of the CMV and the leakage current. Thus, these solutions are ineffective when the complete elimination of the CMV and leakage current are desired. In this context, a good solution is suggested in [4], which introduces a four-leg inverter configuration along with its modulation technique. Some modulation techniques are also introduced for a four-leg three-phase inverter in [5] to address the issue of CMV. However, these solutions lack voltage boosting capability. To address these issues, an improvised z-source based three-phase inverter with four-leg is proposed in [6]. This configuration is capable of attaining voltage boosting along with a constant CMV response. However, this inverter configuration suffers from an increased number of components causing a significantly higher power loss.

This paper proposes an integrated three-phase four-leg inverter, which is capable of boosting the input PV voltage as well as eliminating the switching transitions from the common-mode voltage. A modified PWM strategy is also proposed for the inverter to select appropriate switching vectors in a particular sector to achieve these objectives. As the CMV of the proposed power circuit configuration is free from all high-frequency transitions, the leakage current (which flows through the parasitic elements of the PV panel) is also reduced with the employment of the proposed PWM technique.

II. Working Principle And Description Of The Proposed Four-Leg Boost Inverter

The proposed power circuit configuration for the integrated transformerless four-leg inverter is shown in Fig. 1. The inverter configuration comprises eight power switches (S_{1A}, S_{2A}..S_{1D}, S_{2D}), one diode (D_1), inductor (L_1), and one capacitor (C_1). Three legs (a, b, c) of the proposed inverter configuration is connected to a balanced three-phase load through a symmetrical LC filter. The fourth leg of the inverter is fused with an inverting buck-boost converter to boost the total dc-link voltage of the inverter. The equivalent parasitic resistance and capacitance between the PV panel and the ground are indicated as R_P and C_P respectively. The voltage across the PV terminal and the ground, the load current, and the leakage current are represented as v_{PVg}, i_a, i_b, i_c, and i_{leak} respectively.

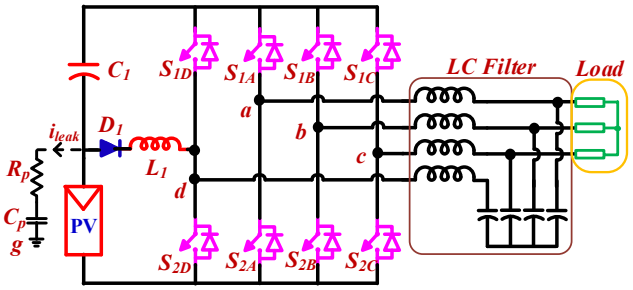

Fig. 1. Circuit diagram of the proposed integrated four-leg three-phase inverter.

The equivalent common-mode model of the proposed four-leg inverter is shown in Fig. 2. Here, the voltage across the parasitic branch of the PV panel is v_{Pg}. The current flowing through the parasitic elements is shown as i_{leak}. The pole voltages of each switching legs of the inverter are

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represented as v_{aO}, v_{bO}, v_{cO} and v_{dO}. The common-mode voltage of the proposed configuration can be determined from the following equation,

$$v_{CMV} = \frac{v_{aO} + v_{bO} + v_{cO} + v_{dO}}{4} \quad (1)$$

Based on the above equation, the magnitudes of the common-mode voltage for each switching state is determined. The switching states of the four-leg inverter are further categorized based on the common-mode voltages as shown in Table-I (a total of seven categories comprising of the zero and the active vector groups).

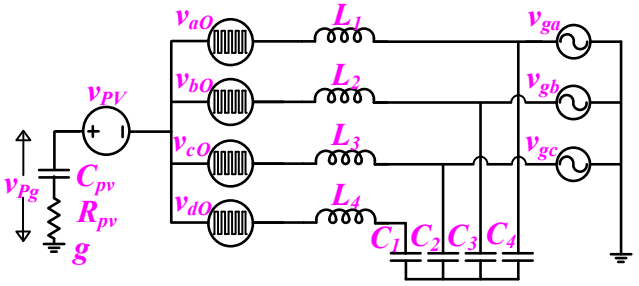

Fig. 2 Common mode equivalent model for the proposed four-leg inverter.

III. Modulation Strategy For Proposed Four-Leg Three Phase Inverter Configuration

The modulation technique for the four-leg inverter is mainly based on 3D space vector modulation to accommodate sixteen possible vectors in the space vector diagram. The switching vectors for the four-leg inverter can be broadly categorized as zero vector group (V_0-V_3) and active vector group (V_4-V_{15}) as shown in Table I. In the conventional SVPWM [7] technique of the four-leg inverter, the switching pattern of each sector consists of three active vectors, and two zero vectors. These adjacent switching vectors are utilized to synthesize the reference vector. The switching pattern of the sector-I for the conventional SVPWM is given in Fig. 3. It can be observed that, with the application of each switching vector, the magnitude of the CMV is altered. The CMV waveform consists of eight voltage transitions during a single switching cycle. Thus, the effective transitions in the CMV voltage will be eight times that of the switching frequency. Consequently, the leakage current also increases for this modulation technique. Besides that, the discontinuous PWM technique [8] for the four-leg inverter utilizes one zero vector and three active vectors

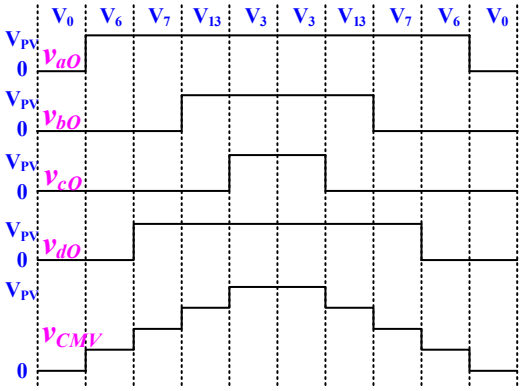

Fig. 3. Switching pattern of the conventional SVPWM technique for the conventional four-leg inverter.

to synthesize the reference vector. However, this PWM technique also has six voltage transitions in the CMV waveform in each switching period as shown in Fig. 4. The PWM techniques such as modified SVPWM [9], NSPWM [10] are capable of reducing the magnitude of CMV to ¼ of the total dc-bus voltage. Thus, the peak-to-peak value of the CMV can be reduced with the application of such PWM schemes. However, transitions in the CMV cannot be eliminated completely. Thus, the conventional PWM schemes [11] are not effective in terms of the leakage current elimination for the transformerless PV inverter applications.

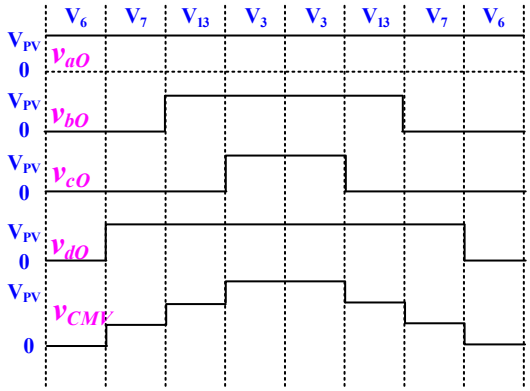

Fig. 4. Switching pattern of the DPWM technique for the conventional four-leg inverter.

To achieve the complete elimination of CMV, a new modulation strategy is proposed. All the switching vectors are grouped and categorized in Table I based on the magnitude of the CMV.

TABLE I . Switching Vector Groups

Type	No	Switching Vectors	Switching Sequence	CMV (v_{CMV})
Zero Vector Group	I	V_0	0000	0
	II	V_1	0001	$0.5V_{PV}$
	III	V_2	1110	$1.5V_{PV}$
	IV	V_3	1111	$2V_{PV}$
Active Vector Group	I	V_4	0010	$0.5V_{PV}$
		V_5	0100	
		V_6	1000	
	II	**V_7**	**1001**	V_{PV}
		V_8	**1100**	
		V_9	**0101**	
		V_{10}	**0110**	
		V_{11}	**0011**	
		V_{12}	**1010**	
	III	V_{13}	1101	$1.5V_{PV}$
		V_{14}	1011	
		V_{15}	0111	

All the switching vectors are primarily grouped as active vector group and zero vector group. To make the CMV constant, the switching vectors from these group are selected in such a way that, all vectors employs the same magnitude of CMV. It is also observed that all of the active vectors of a three-phase inverter are belonging to the active vector group-II (shown in boldface). However, no vectors from the zero-group display the same magnitude of CMV as the active vector group-II. Thus, zero vectors cannot be utilized for switching. However, two equal and opposite active vectors, situated at the same vector location, can be switched for half of the duration of the required zero-vector time period to emulate the behavior of the zero-vector time period. In the

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space vector diagram shown in Fig. 5 (a), there exist three possible pairs of vectors, which can be switched to emulate the behavior of the zero-vector (ex: the vectors **V8**(1100) and **V11** (0011) shown in red color). Further, to generate the timing signal for the active and zero vectors, three modulation

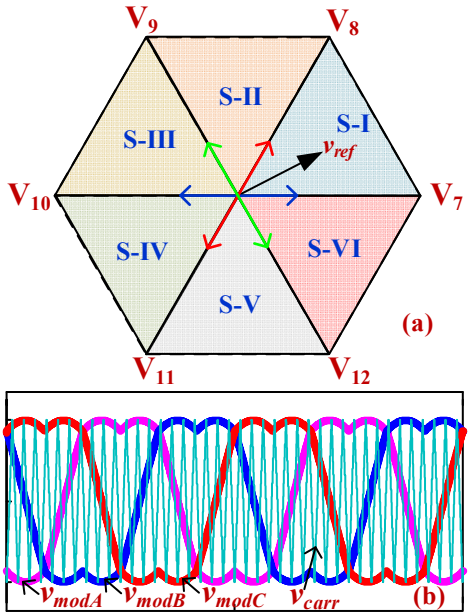

Fig. 5. (a) Space vector diagram of the proposed four-leg inverter, (b) generation of three phase modulation signals (v_{modA}, v_{modB}, v_{modC}).

signals (v_{modA}, v_{modB}, v_{modC}) and a carrier signal (v_{carr}) is considered as shown in Fig. 5(b). A center-spaced algorithm, which is based on the concept of imaginary switching time periods [12] is employed to implement the SVPWM for the proposed configuration. The opposite active vectors are so chosen that, they belong to the same sub-group of the CMV (i.e. active vector group-II). Thus, with the application of the proposed modulation strategy in each switching cycle, there will be no transitions in the CMV. Further, as all vectors are considered from active vector group-II, there will be no voltage transition during the sector to sector transit. These lead to the complete elimination of the common-mode voltage in a complete cycle. The possible active vector pairs to affect the zero-vector are (V_7, V_{10}), (V_8, V_{11}) and (V_9, V_{12}) as shown in Fig. 5 (a). These three possibilities are utilized to generate three different combinations of the switching sequence for each sector. The possible switching combinations for each sector are listed in Table II. The switching sequence in sector-I with the active vector pair (V_7 and V_{10}), to implement the effective zero-vector, is presented in Fig. 6.

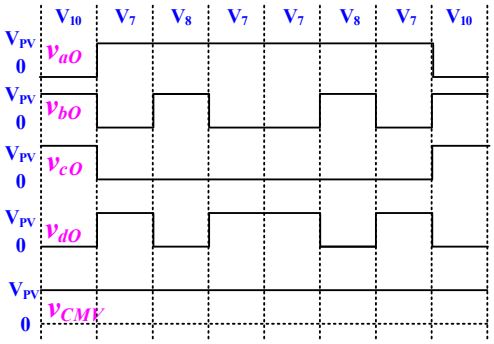

Fig. 6. Switching pattern of the PWM strategy-I for the proposed four-leg inverter.

Further, the switching sequence with the active voltage vector pairs (V_8, V_{11}) and (V_9, V_{12}) are shown in Fig. 7 and Fig. 8 respectively. It can be observed that the active vectors in each period are placed in such a way that the fourth-leg toggles its states for each active vector switching. This increases the effective switching frequency of the fourth leg, which constitutes a part of the boosting circuit.

TABLE II . SWITCHING SEQUENCES FOR SECTOR-I

	Type	Switching Sequence	v_{cmv}
Timing Seq.		$\frac{T_0}{4}-\frac{T_1}{2}-\frac{T_2}{2}-\frac{T_0}{2}-\frac{T_2}{2}-\frac{T_1}{2}-\frac{T_0}{4}$	-
Sector I	I	V_{10}-V_7-V_8-V_7-V_8-V_7-V_{10}	V_{PV}
	II	V_8-V_7-V_8-V_{11}-V_8-V_7-V_8	V_{PV}
	III	V_{12}-V_7-V_8-V_9-V_8-V_7-V_{12}	V_{PV}
Sector II	I	V_{10}-V_9-V_8-V_7-V_8-V_9-V_{10}	V_{PV}
	II	V_8- V_9-V_8-V_{11}- V_8-V_9-V_8	V_{PV}
	III	V_{12}- V_9-V_8-V_9- V_8-V_9-V_{12}	V_{PV}
Sector III	I	V_{10}-V_9-V_{10}-V_7-V_{10}-V_9-V_{10}	V_{PV}
	II	V_8-V_9-V_{10}-V_{11}-V_{10}-V_9-V_8	V_{PV}
	III	V_{12}-V_9-V_{10}-V_9-V_{10}-V_9-V_{12}	V_{PV}
Sector IV	I	V_{10}-V_{11}-V_{10}-V_7-V_{10}-V_{11}-V_{10}	V_{PV}
	II	V_8-V_{11}-V_{10}-V_{11}-V_{10}-V_{11}-V_8	V_{PV}
	III	V_{12}-V_{11}-V_{10}-V_9-V_{10}-V_{11}-V_{12}	V_{PV}
Sector V	I	V_{10}-V_{11}-V_{12}-V_7-V_{12}-V_{11}-V_{10}	V_{PV}
	II	V_8-V_{11}-V_{12}-V_{11}-V_{12}-V_{11}-V_8	V_{PV}
	III	V_{12}-V_{11}-V_{12}-V_9-V_{12}-V_{11}-V12	V_{PV}
Sector VI	I	V_{10}-V_7-V_{12}-V_7-V_{12}-V_7-V_{10}	V_{PV}
	II	V_8-V_7-V_{12}-V_{11}-V_{12}-V_7-V_8	V_{PV}
	III	V_{12}-V_7-V_{12}-V_9-V_{12}-V_7-V_{12}	V_{PV}

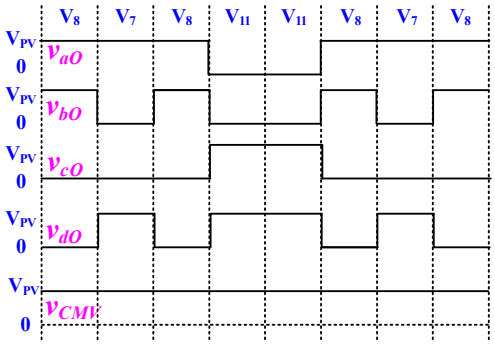

Fig. 7. Switching pattern of the PWM strategy-II for the proposed four-leg inverter.

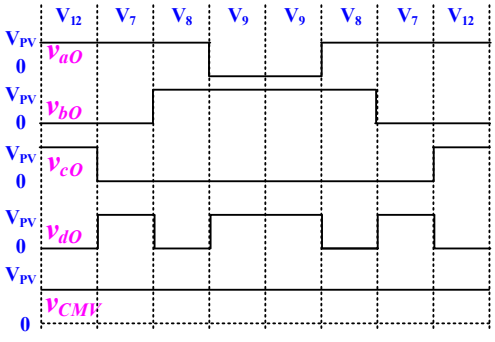

Fig. 8. Switching pattern of the PWM strategy-III for the proposed four-leg inverter.

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IV. Simulation Results

The proposed integrated four-leg three-phase inverter configuration is simulated in MATLAB-SIMULINK environment to verify its operation. The system parameters, which are used in the simulation study, are listed in Table III.

Table III. PARAMETERS USED FOR SIMULATION

1.	Input Voltage (V_{PV})	400V (Conv.) 200V (Prop.)
2.	C_1 Capacitance	1mF
3.	Switching frequency (f_{sw})	10kHz
4.	Energy storage Inductor (L_1)	2.5mH
5.	Load Resistance per phase (R_{load})	50Ω
6.	Parasitic Resistance (R_P)	10 Ω
7.	Parasitic Capacitance (C_P)	10nF

The simulation results for the four-leg inverter with the conventional SVPWM scheme is shown in Fig. 9 (a). The three-phase load current can be observed in Fig. (b). As stated in section-II, the common-mode voltage with this PWM technique results in eight voltage transitions in each switching cycle. The CMV can also be observed from the time-varying parasitic voltage (v_{Pg}). It can also be observed that the effective leakage current is very high and the magnitudes of both the peak-peak and the RMS currents do not comply with the limits given in VDE 0126-1-1.

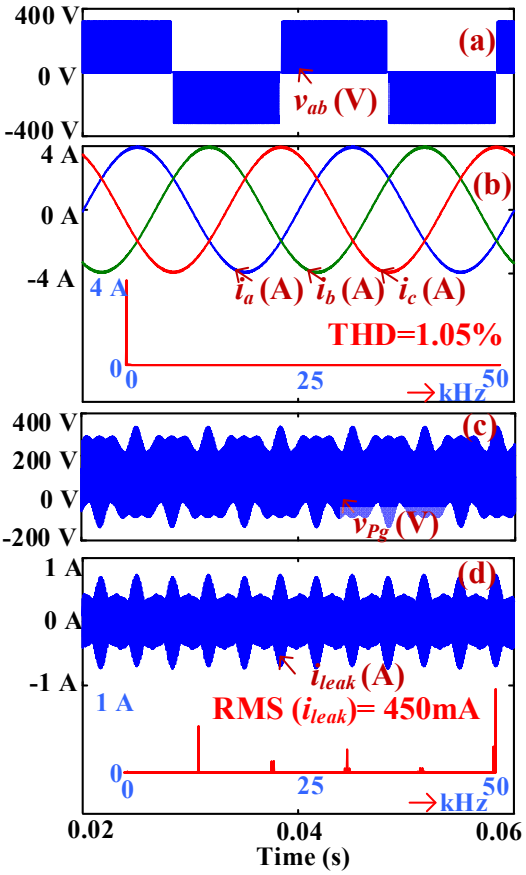

Fig. 9. Simulation results for the proposed four-leg inverter with conventional PWM technique : (a) inverter line to line voltage (v_{ab}), (b) three phase load currents (i_a, i_b,i_c), (c) common mode voltage (v_{CMV}), (d) leakage current (i_{leak}).

The simulation results of the proposed four-leg inverter with the modulation index (m_a) = 0.9 are shown in Fig. 10. The total dc-link voltage is boosted by a factor of two as it can be observed from Fig. 10 (a) that, the line-to-line voltage (v_{ab}) is switched between +400 to -400 whereas the input PV voltage is 200V. It is evident from Fig. 10 (b) that the behavior of the three output legs of the proposed four-leg inverter is identical to that of the conventional three-phase VSI. The proposed inverter does not contain any switching frequency transitions in the voltage across the parasitic branch (v_{Pg}) as it is shown in Fig. 10 (c). The PV common-mode leakage current and its corresponding spectrum are shown in Fig. 10 (d). It can be observed that both peak-to-peak and the RMS values of the leakage current are below 30mA. Thus, these simulation results assert that the proposed transformerless PV based inverter is suitable for PV applications.

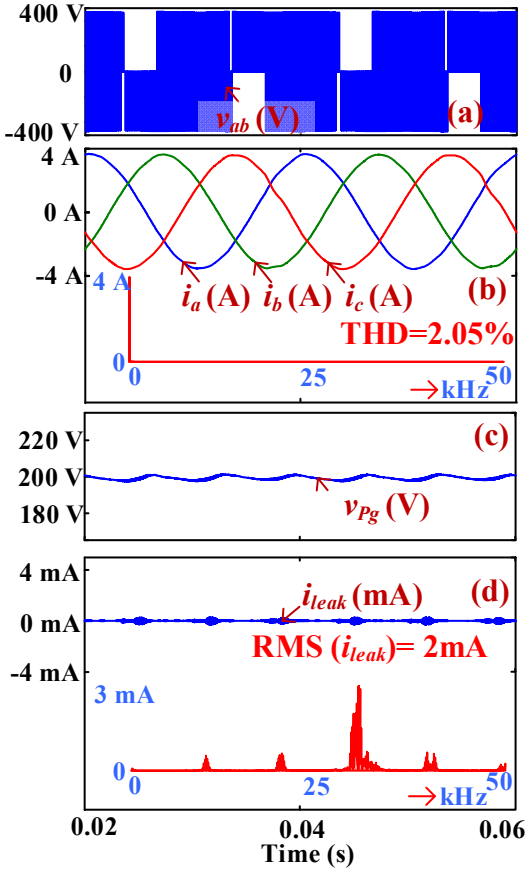

Fig. 10. Simulation results for the proposed four-leg inverter with proposed PWM technique : (a) inverter line to line voltage (v_{ab}), (b) three phase load currents (i_a, i_b,i_c), (c) common mode voltage (v_{CMV}), (d) leakage current (i_{leak}).

A separate simulation study is performed to validate the performance of the proposed integrated four-leg inverter at an unbalanced loading condition. It can be observed from Fig. 11 that the magnitude of the load current is unbalanced. Despite the unbalanced loading condition, the aspect of leakage current reduction is unaltered. Further, to assess the power loss incurred in the proposed converter, an equivalent simulation model is implemented in the PLECS environment. A thermal model based on the IGBT devices along with their anti-parallel diodes is used in the simulation study to analyze the switching and conduction power loss of each switching device. In order to compare the performance of the proposed system with the conventional boosting strategy, a similar

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model with the conventional boosting strategy and a separate three-phase inverter is also simulated. It is observed that the efficiency of the proposed system is about 2.5% more than the efficiency obtained with the conventional boosting strategy for the same dc-link voltage (i.e. 400V) and the power output (i.e. 1kW).

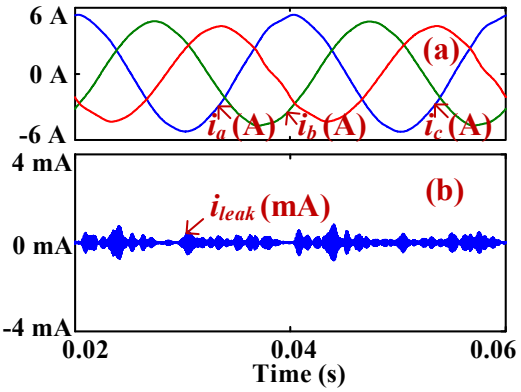

Fig. 11. Simulation results for the proposed four-leg inverter with proposed PWM technique at unbalanced loading condition : (a) three-phase load currents (i_a, i_b,i_c), (b) leakage current (i_{leak}).

V. Conclusion

This paper presents an integrated four-leg inverter configuration, which is capable of achieving both voltage boosting and the reduction of the leakage current. The proposed modulation technique also increases the effective switching frequency of the fourth leg to optimize the size of the boosting inductor. The proposed modulation technique selects the switching vectors in such a way that the common-mode voltage is constant in every switching cycle irrespective of the operating sector. Thus, it eliminates all the switching transitions from the common-mode voltage. Therefore, the modulation technique is capable of reducing the leakage current and the requirement of the common-mode filter. The proposed power converter, therefore, meets the standard specified by VDE 0126-1-1 for leakage current and the IEEE 1547 standard for the THD. With these advantages, it is envisaged that the proposed transformerless three-phase four-leg PV inverter could be useful in standalone and grid-tied applications.

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