Improved H5 Circuit Based Five-Level Quasi Z-Source Inverter With Reduced Leakage Current

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***Abstract*—This paper presents an improved H5 circuit based five-level quasi Z-source inverter for photovoltaic applications. The inverter circuit is formed by utilizing an improvised H5 circuit with a dual quasi Z-source that can produce a five-level stepped voltage waveform rather than a three-level voltage waveform. The developed modulation technique results in a trapezoidal common-mode voltage. An active filter was used to eliminate the leakage current and filter out the harmonics in order to feed the grid voltage. The converter also possesses the reactive power sourcing capability, which helps in supporting changing load conditions. The leakage current resulting from this converter is well within the stipulated IEEE standards.**

Keywords—quasi Z source, leakage current, neutral point clamped.

I. INTRODUCTION

Since the last decade, there is a huge surge in the use of renewable energy sources (RES) as a clean source to produce power. The wide spread employment of photovoltaic (PV) systems is attributed to several contributory factors such as the reduction in the costs of PV panels and inverters. PV systems also offer advantages such as easy grid-integration and simpler control, due to development of recent power electronic interfaces [1]. The RES constitute the backbone of distributed generation (DG) that reduces the dependence on the grid. In DG power systems, the dc power produced by RES needs additional inverters to convert it into the ac power. The principal disadvantage of the two-level inverters, used previously is that, they are essentially buck converters; meaning that they require twice the grid peak voltage. Other disadvantages include high filter requirement and higher leakage current.

Tranformerless inverters are extensively being researched owing to the ever-increasing penetration of RES for DG systems. The main reason behind these inverters is to reduce the leakage current that flows from the PV terminals to the ground point of the load. The leakage current flows through the parasitic leakage-capacitor, which is present between the PV terminals and the ground point. The variation in voltage across this capacitor causes the leakage current into the grid. Various methods have been proposed to reduce the leakage current in literature [2]-[5]. One of the methods listed out in [2] is separating the AC and DC sides during the freewheeling period.

Another important method to decrease the leakage current is to prevent alternation in the common mode voltage (CMV) using either modulation methods or additional switches. The method reported in [6] obtains a constant CMV (i.e. avoids high frequency oscillations in it). Though this method has been effectively utilized in two-stage based system, its applicability has not been adequately explored in the area of singles-stage systems. Quasi Z-source (qZS) [7] based multilevel inverters (MLI), which belong to the category of single stage boosting inverters (SSBI), integrate the quality of qZS and MLI. The qZS-MLI comes under the family of the Z-source inverters, which were introduced in 2002 by F.Z. Peng [8]. Some of its advantages are: (i) continuous input current and (ii) lower component rating. These advantages make quasi Z-source inverters attractive for applications related to PV based systems.

Many qZS based MLI topologies have been proposed in the past [10]-[18]. Their classification is based on the structure, modulation technique, number of levels and the boost factor. However, only a few of them have addressed the issue of leakage current in this class of inverters. The integration of classical single phase ZSI and HERIC based structure was proposed [9] to reduce the leakage current. This adds 2 more switches that operates at line frequency to isolate the load side. A new qZS structure was proposed in [10] which uses two additional switches which connects the positive point and negative point of load to negative dc point of converter to make the CMV constant. The work described in [11] proposes the use of active power filter to filter out high frequency oscillations in the CMV in single phase qZSI. In [12], it has been suggested to add 2 more IGBT-switches for the conventional single-phase qZSI and utilizing them during the freewheeling period to achieve low leakage current.

Though some power circuit configurations and PWM strategies are available for three-phase conventional qZSIs, the area of single-phase qZSI based MLIs has not been explored adequately. Most of the investigations carried out in the area of single-phase qZSI topologies, developed to reduce the leakage current, could only obtain three-levels in the output voltage. This is the motivating factor for the authors to propose a new power circuit configuration in this paper.

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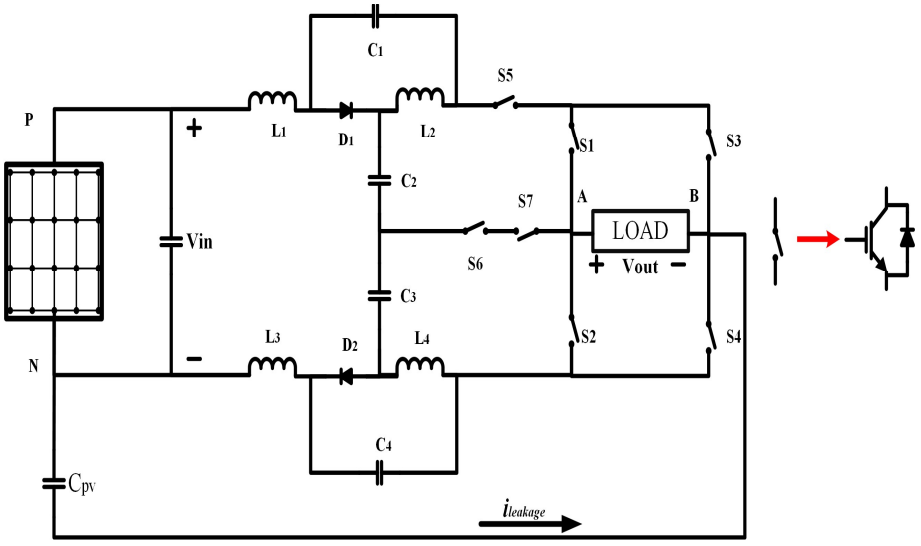

Fig. 1. The proposed converter

This paper introduces a new Tranformerless-qZSI topology, which displays benefits such as: (i) reduced leakage current, (ii) five-level voltage waveform, (iii) reduced number of switches, (iv) improved efficiency and (v) low voltage stress on the power semiconductor switching devices.

II. CONVERTER DESCRIPTION

A. The Proposed qZS Multilevel Inverter Topology

The proposed inverter is depicted in Fig. 1. The dual quasi z source is connected in an opposite fashion to create a neutral point structure [13], [14]. The proposed multilevel inverter consisting of 7 power semiconductor switches is cascaded to this dual quasi z source. The proposed topology consists of an improvised H5 structure, with an additional bidirectional switch. This bidirectional switch, which is connected to the midpoint of the dual qZS structure, increases the number of levels in the output voltage and clamps the CMV.

The proposed inverter outputs five voltage levels: 0, $\pm V_{DC}/2$, $\pm V_{DC}$. Modified level shifting carrier waveform is used to modulate the output of the proposed converter. The total dc-link voltage across the inverter is obtained by summing all of the capacitor voltages.

This circuit displays a total of 4 active states. These include a freewheeling state and a shoot-through state. The voltage boosting is obtained with the shoot-through technique. Fig. 2 shows all of the operating modes of the proposed inverter. Table I presents the switching states to obtain the required voltage levels. The working principle of the proposed converter is explained as follows:

Mode 1:

In this operating mode, the switches S6, S7 and S4 are turned on to generate the level $+V_{DC}/2$ in the output voltage for the proposed single-phase qZS-MLI. The equivalent circuit for this operating mode is shown in Fig. 2(a).

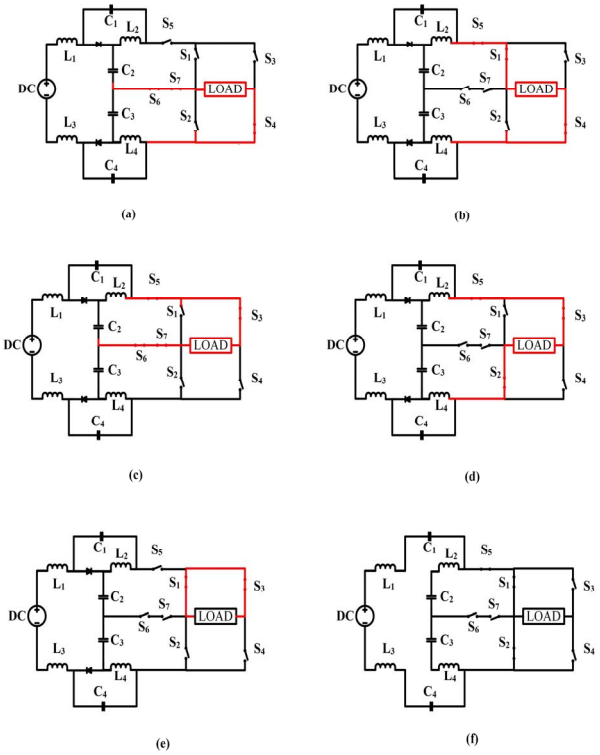

Fig. 2. Working modes of proposed inverter

Mode 2:

Switches S5 and S4 are turned on for the generation of $+V_{DC}$ level as shown in Fig. 2(b).

Mode 3:

Voltage level of $-V_{DC}/2$ is created by turning on the switches S5, S6, S7 and S3, which is shown in Fig. 2(c).

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Mode 4:

Switches S2, S3 and S5 are turned on to create the voltage level $-V_{DC}$, as presented in Fig. 2(d).

Mode 5:

This is the freewheeling mode, wherein S5 is turned off and S1 and S3 are turned on. Fig. 2 (e) depicts the current path.

Mode 6:

This mode is the shoot-through mode, which imparts the voltage boosting capability to the proposed qZS-MLI. In this mode, 3 switches, namely, S1, S3 and S5 are turned on. The path for current is shown in Fig. 2(f). The design of passive components is carried out by following the procedure described in [13] and [14]. The following equations are used for the calculation of passive components:

$$L = \frac{4*V_O^2*(1-2D_{SH})*T_S*D_{SH}}{(1-D_{SH})*K_L*P_O} \quad (1)$$

$$C_1 = C_4 = \frac{T_S*P_O*(1-D_{SH})^2}{4*k_{C1}V_O^2(1-2D_{SH})} \quad (2)$$

$$C_2 = C_3 = \frac{T_S*P_O*(1-D_{SH})*D_{SH}}{4*k_{C1}V_O^2(1-2D_{SH})} \quad (3)$$

where k_{C1} and k_L respectively denote the allowed ripples in capacitor voltages and inductor current.

The boost factor of the proposed inverter is the same as the conventional inverter. The corresponding voltage equations are:

$$B = \frac{1}{1-D_{SH}} \quad (4)$$

$$V_{out} = m * B * V_{in} \quad (5)$$

where, the symbols D_{SH} and 'm' respectively denote the shoot-through duty cycle and the modulation index.

B. Modified Modulation Scheme

The modulation scheme is so designed as to obtain 4 active states, 1 freewheeling state and 1 shoot through state. Also, the proposed converter is capable of supplying reactive power (both inductive and capacitive). *Level-Shifted* carrier waves are used to generate the gating signals for the semiconductor switching devices. Hence, the PWM scheme implemented in this work can be categorized under the label Level-Shifted PWM (LSPWM).

Fig 3 shows the carrier (shifted-triangular) and modulating (sinusoidal) waveforms pertaining to the implementation of the LSPWM scheme. The outputs of comparators, which compare the carrier and the modulating waves, are also shown in Fig.3 (signals A, B, C, and D). The duty signal 'G', which is obtained by comparing a variable dc voltage with the top or bottom carriers controls the shoot-through time period in each sampling time period. The operating principle of the proposed converter is similar to that of the H5 inverter, wherein the switch S5 isolates the AC and the DC sides. This isolation causes a significant reduction in the leakage current.

The five comparator outputs (A, B, C, D and G) are then translated into the actual gating signals for the seven-power semiconductor switching devices, using simple combinational logical expressions, which are given by:

$$S_1 = \bar{A}G + \bar{C}\bar{G} + B, S_2 = D, S_3 = \bar{G}, S_4 = A, S_5 = B + C, S_6 = C \oplus D + C\bar{G} + G, S_7 = A \oplus B + \bar{A}G + \bar{G} \quad (6)$$

TABLE I. SWITCHING STATES

Output level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Switching state
$+V_{DC}/2$	0	0	0	1	0	1	1	Active
$+V_{DC}$	1	0	0	1	1	0	0	Active
$-V_{DC}/2$	0	0	1	0	1	1	1	Active
$-V_{DC}$	0	1	1	0	1	0	0	Active
0	1	0	1	0	0	1	1	Zero
0	1	1	0	0	1	0	0	Shoot though

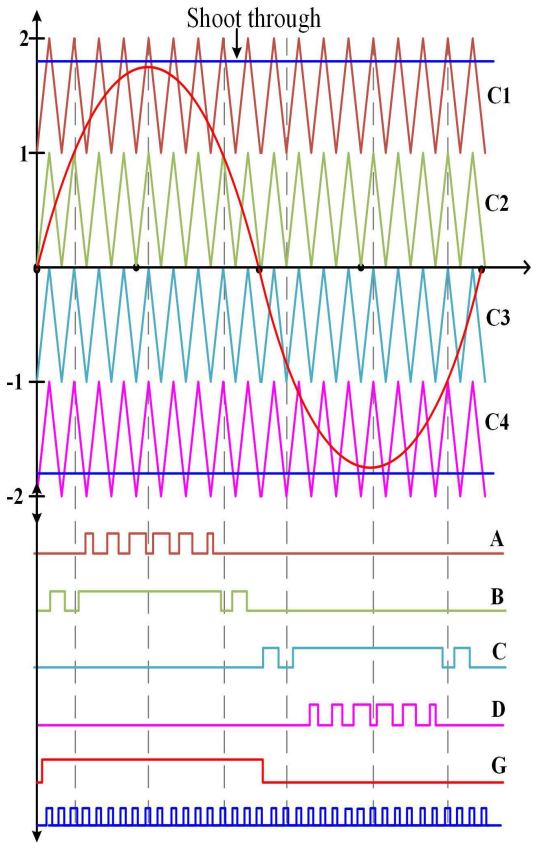

Fig. 3. Level shifting pulse width modulation method

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III. LEAKAGE CURRENT ANALYSIS

Leakage current is of major concern in PV based inverters from the standpoint of safety. The leakage current, as shown in Fig.1, flows through the parasitic capacitance formed between PV panels and electrical ground. As stated earlier, the leakage current is caused by the time rate of change of the CMV. Thus, the leakage current can be reduced either by avoiding oscillations of high-frequency or by keeping the CMV static (i.e. constant). The conventional H5 inverter, which outputs only a three-level voltage waveform, generates a constant CMV and therefore results in a low leakage current.

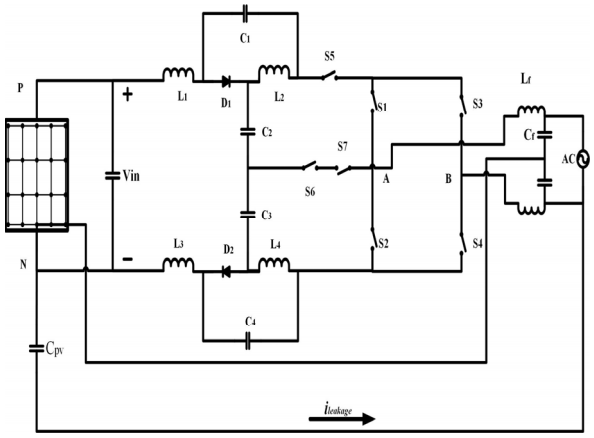

Fig. 4. Proposed inverter with active filter for leakage current reduction

In contrast, the proposed qZSI-MLI outputs a five-level voltage waveform. However, in this circuit, the CMV fluctuates from $+V_{DC}/2$ to $+V_{DC}/4$ at grid frequency. The shoot-through state used for boosting the voltage introduces an additional fluctuation in CMV, which needs to be filtered out. Hence, an active filter is used to remove the unwanted high frequency components in the CMV. Apart from this, the active filter also facilitates the proposed converter to output a sinusoidal waveform. Fig. 4 presents the complete system with active filter.

IV. SIMULATION RESULTS

Simulation studies have been carried out for the proposed qZSI-MLI using the MATLAB/Simulink tools to assess its effectiveness to mitigate the leakage current, while producing the 5-level output waveform. The circuit parameters and the operating conditions have been presented in Table II. The proposed power circuit is designed to deliver an output power of 500 W.

With the proposed system, maximum power point (MPP) can be attained by controlling the shoot-through duty cycle D_{SH}.

Fig 5(a) presentsvoltage waveform of the boosted dc-link, which is obtained by summing up all four capacitors of the qZS network. The 5-level output voltage and the corresponding load current are shown in Fig. 5(b). The current is amplified by a factor of 10 to make it visible on the chosen voltage scale. An output voltage of 110V (RMS) could be obtained when the input voltage is 100V. With a modulation index of 0.7 and the boost-factor of 2.3, the required shoot-through duty cycle is calculated to be 0.27.

The inductor current and the capacitor voltages are presented in Figs. 6(a), (b) and (c) respectively. These current and voltage waveforms are as expected of the behavior of the conceived converter.

The CMV and the voltage across the PV-leakage capacitor are shown in Figs. 7(a) and (b) respectively. It may be noted that the shoot-through time period, which is inserted within the null-vector time period, causes an additional fluctuation in CMV.

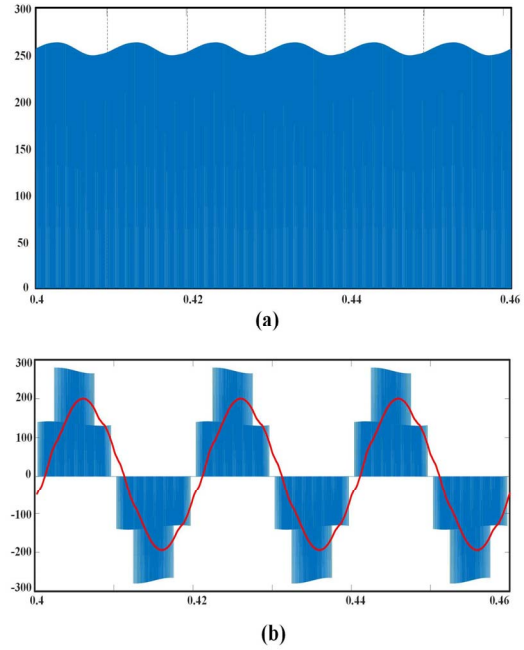

Fig. 5. (a) boosted dc link voltage, (b) Level voltage and current

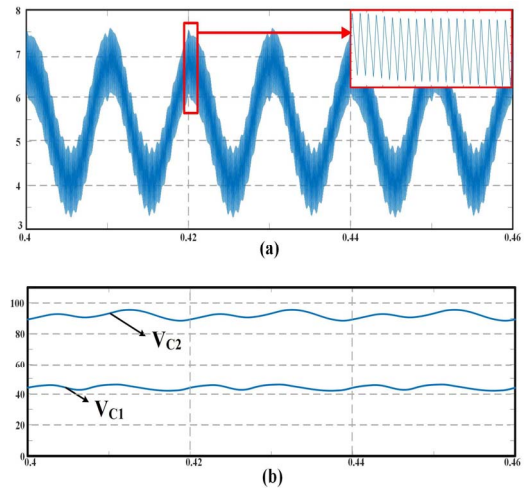

Fig. 6. (a) boosted dc link voltage, (b) Level voltage and current

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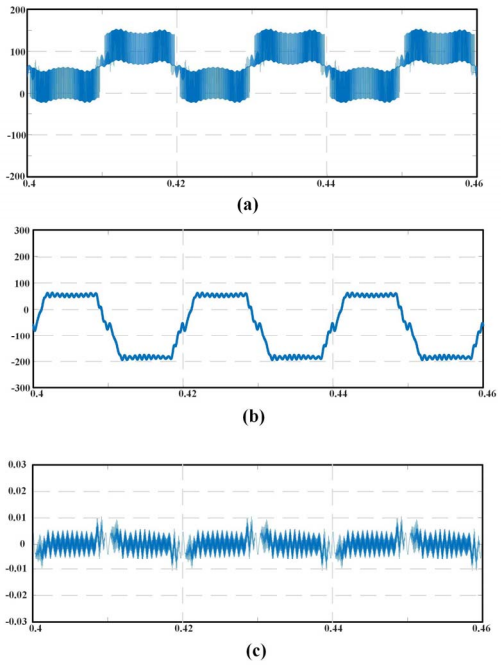

Fig. 7. (a) CMV of the proposed inverter
(b) Voltage waveform across parasitic capacitance C_{pv}
(c) Leakage current of the converter

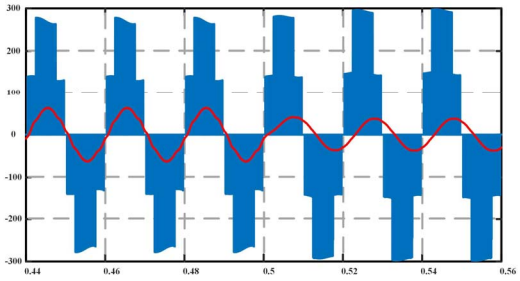

Fig. 8. Load voltage and current during change in power factor from 1 to 0.8 lagging.

TABLE II. PARAMETERS FOR SIMULATION

Parameters	Value
Power	500W
Input voltage	100V
Output voltage (RMS)	110V
Inductance Value	1mH
Capacitance value	1000μF
Operating frequency	10kHz

The active filter, employed at the output stage serves two purposes: (i) it filters out the high frequency components in the output voltage, and (ii) it reduces the CMV. Also, the waveform of the voltage across the parasitic capacitance (C_{pv}, Fig.1) is shaped trapezoidal. The trapezoidal voltage waveform does not only decrease the spike in the leakage current, but also decreases its value. Fig. 7(c) indicates that the resulting leakage current from the proposed inverter is only 3.5mA (RMS), which is well within the limits of international standards.

In the simulation result presented in Fig. 8, the converter initially feeds a resistive (UPF) load. At around 0.5s, the load on the converter is suddenly changed to 0.8 PF lagging load. While the resulting transient in the load current is significant, the waveform of the load voltage is not affected appreciably. In particular, the number of levels in the output voltage remains the same. This amply demonstrates the reactive power supporting capability of the proposed converter. A clear comparison with some of the popular five-level qZS topologies is provided in Table III. Thus, the proposed topology uses minimum number of switches of all the compared topology to provide a five-level voltage due to which it has a higher efficiency.

TABLE III. COMPARISON WITH OTHER TOPOLOGIES

Parameters	Proposed topology	[13]	[15]	[16]	[17]	[18]
Inductors	4	4	4	4	4	2
Capacitors	4	4	4	4	4	4
Switches	7	8	12	8	8	8
Efficiency	95.6	94	---	---	90	87

V. CONCLUSION

A new H5 circuit based five-level qZS inverter for PV applications has been presented in this paper. Two qZS networks are connected in an opposite fashion to create a neutral point. Improved H5 power circuit configuration has been proposed with a bidirectional structure, which results in a five-level output voltage waveform and clamps the CMV. Significant features of the proposed topology include: (i) reduced switch count, (ii) reduced leakage current, (iii) single stage boosting, (iv) reduced CMV and (v) reactive power supporting capability. The behavior of the proposed converter topology is assessed with simulation studies. Simulation results reveal that the resulting leakage current is 2mA (RMS), which is well within the limits of international standards.

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