Bi-Directional Clamping Based H5, HERIC and H6-Type Transformerless Inverter Topologies with Improved Modulation Technique

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***Abstract*—Transformerless inverters (TLIs) are well commercialized for Photovoltaic applications due to its small in size, less cost and high power conversion efficiency. However, the major challenge is to develop an inverter with reactive power capability and minimum leakage current. Therefore, in this paper, an improved H5, Heric, and H6-type topologies with bi-directional clamping branch are proposed to maintain constant common-mode voltage (CMV) during the freewheeling period. Thus, high-frequency variations due to switch junction capacitances in CMV are diminished and it further reduces the leakage current. Besides, an improved pulse width modulation scheme (PWM) provides a bi-directional current path during zero state to enhance the output waveform quality of the grid-connected inverter at different power factor conditions. Finally, the proposed concept is examined through the simulation results using Matlab software.**

Keywords—Transformerless Inverters, Common mode voltage, Leakage current.

I. Introduction

Power generation from photovoltaic's is the most promising solution to meet the world energy requirements. Majority of the PV installations are interfaced with grid due to its compactness, reduced cost and higher efficiency [1]. Moreover, these are operating in parallel to the utility grid which allows the flow of excess PV power into grid (i.e., when produced PV power is more than the local load demand). Therefore, this attracts the attention of people and policymakers to do in-depth research and development on grid-connected PV inverters [2].

Generally, PV inverters are categorized into isolated and non-isolated type based on the placement of transformer in the power processing stage. To achieve higher efficiency, compact size and reduced cost a bulky line frequency transformer (50/60 Hz) is eliminated in non-isolated PV inverters. Whereas, exclusion of the transformer and its isolation results in direct connection of grid and PV panel. In consequence, high-frequency CMV fluctuations generated by the switching of PV inverter can excite the resonant circuit formed between the parasitic capacitance of PV panels, filter and grid impedances. This contributes to excess leakage current through parasitic capacitance of PV panel. The leakage current flow in the circuit deteriorates the waveform quality, increases the electromagnetic compatibility (EMC) and also leads to poor safety [3].

A traditional full-bridge inverter with Unipolar and Bipolar PWM schemes is introduced in the early stage of symmetrical filter inductor based topologies. However, because of the higher leakage current, total harmonic distortion (THD) and switching losses it fails to satisfy grid codes and standards. To overcome these problems different topologies were published in the literature with AC and DC-based decoupling from grid to PV panel during the freewheeling period by incorporating additional circuitry. H5, Heric and H6 are the most popular and widely accepted inverter topologies in the market for transformerless operation. In H5 topology DC decoupling is achieved by adding switch in series with the source. AC decoupling is achieved in Heric topology by adding two switches in parallel to the grid. Either DC or AC decoupling is possible in H6 topology based on the placement of switches and diodes in series or parallel to the source and grid respectively [4].

All these topologies are recording more efficient in practice. However, the issue of leakage current is not fully diminished due to unequal or oscillatory terminal voltages during the freewheeling period. Consequently, excess leakage current will flow in the resonant circuit due to the excitation of PV parasitic capacitance; sometimes the leakage current magnitude exceeds the German VDE 0126-1-1 grid standards because of intermittent behavior of parasitic capacitance due to climate changes. To alleviate the leakage current problems and to improve the waveform quality in optimized way; a clamping branch and split DC-link capacitors were used to preserve constant CMV in all the operating modes of PV inverter [5].

Further, improved H5 topologies are proposed to clamp the inverter terminal voltages during the freewheeling period either by incorporating a diode or a switch respectively [6], [7]. In addition, Heric topology based different clamping circuits have been reported in [8]. All the above said topologies and their control schemes are quite successful in reducing the leakage current. Whereas most of the grid-connected topologies are derived for unity power factor operations. However, in modern days, reactive power capability is the major concern for transformerless PV inverters for grid-connected operation as per the VDE-AR-N4105 standard. To fill the gap, an improved modulation technique is proposed for basic H5 and Heric inverter topologies in [9]. Different inverter topologies are also proposed to serve the function of reactive power support in refs [10]-[11]. But, the effect due to switch junction

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capacitances and their resultant excess leakage current have not been addressed in the above topologies. Moreover, excess component count and passive filters are required to realize the reactive power capability of the inverter which results in increased size and cost of the system.

To address the above problems like constant CMV, reduced leakage current and reactive power capability demands an improvement in the topologies and modulation techniques for the power generation from PV systems. Therefore, in this paper an improved H5, Heric and H6-Type inverter topologies with bi-directional clamping branch (BDC) with split DC-link capacitors are proposed to maintain constant common-mode voltage (CMV) during the freewheeling period for unity, lagging, and leading power factors. The proposed circuit reduces the size of the additional common-mode filter. In addition, an improved PWM technique is introduced to achieve reactive power capability. Finally, the proposed concept is verified through simulation results.

II. Analysis of Leakage Current in TLI Topologies

The topological structures and gate pulse generation of the conventional H5, Heric, and H6-Type topologies are shown in Figs. 1 to 3 respectively. Where, V_{dc} is the equivalent PV voltage, namely, input DC voltage of the inverter, C_{PV} is the parasitic capacitance of the PV module. Positive and negative terminals of the input DC source are denoted as *P* and *N*. Similarly, phase and neutral terminals of the inverter are denoted as *A* and *B* respectively. A general expression used for the computation of common mode voltage 'V_{CM}' and differential mode voltage 'V_{DM}' are expressed in terms of inverter terminal voltages V_{AN} and V_{BN} are as follows;

$$V_{DM} = V_{AN} - V_{BN} \tag{1}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \tag{2}$$

Asymmetries in the filter impedances and parasitic capacitances among the power semiconductor switches to ground produce an extra component of CMV ($V_{CM\text{-}DM}$) as given in (3). Whereas, the total CMV (V_{TCMV}) and the leakage current are given in (4) and (5) as follows;

$$V_{CM-DM} = V_{DM} \cdot \frac{L2 - L1}{2(L2 + L1)} \tag{3}$$

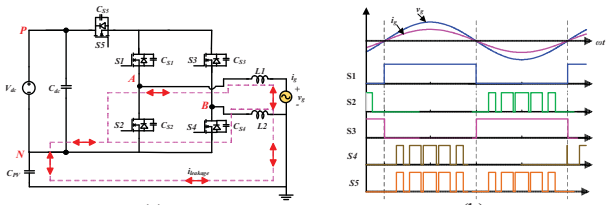
$$V_{TCMV} = V_{CM} + V_{CM-DM} \tag{4}$$

$$i_{leakage} = C_{PV} \frac{dV_{TCMV}}{dt} \tag{5}$$

If $L1$=$L2$, the voltage V_{TCMV}=V_{CM} (i.e., $V_{CM\text{-}DM}$= 0). It is evident that the leakage current depends on the variations in V_{TCMV} and the magnitude of equivalent parasitic capacitance C_{PV} [12]. Whereas, in all these topologies, the flow of leakage current in the resonant circuit is unavoidable due to the occurrence of high-frequency fluctuations in CMV.

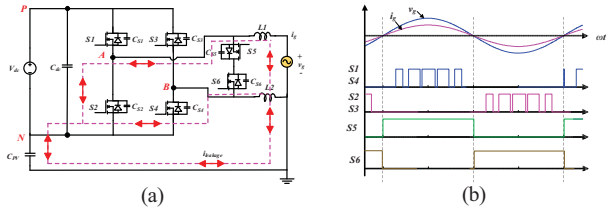
A. Analysis of Leakage Current with the Consideration of Switch Junction Capacitances

In real-time, the analysis of leakage current due to the switch junction capacitances of TLIs cannot be ignored. It



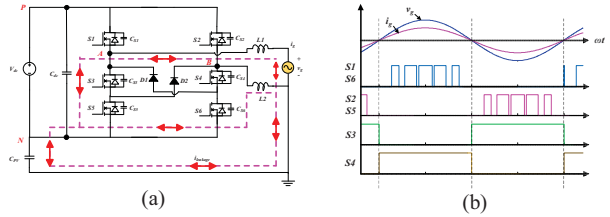
(a) (b)

Fig.1. H5 TLI: (a) circuit structure (b) gate pulses.



(a) (b)

Fig.2. Heric TLI: (a) circuit structure (b) gate pulses.



(a) (b)

Fig.3. H6-Type TLI: (a) circuit structure (b) gate pulses.

can be observed that V_{AN}= V_{dc}, V_{BN}= 0 and V_{CM}= V_{dc}/2 for the positive half cycle. Similarly V_{AN}= 0, V_{BN}= V_{dc} and V_{CM} = V_{dc}/2 for negative half cycle. Moreover, the CMV has maintained a constant value of V_{dc}/2 during the power transferring modes. Whereas in freewheeling mode, filter inductors current continuously freewheel through the grid and power cannot be transferred from the input DC source. Also, it is noticed that CMV is varying due to charging and discharging of the switch junction capacitances during the transition of inverter operation from power transferring modes to freewheeling modes. From the analysis given in refs [7], [8] and [13] the CMV derived during the freewheeling period as follows;

H5

$$V_{CM} = V_{AN} = V_{BN} = V_{DC} \cdot \frac{C_{S2} + C_{S5}}{C_{S2} + C_{S5} + C_{S4}} \tag{6}$$

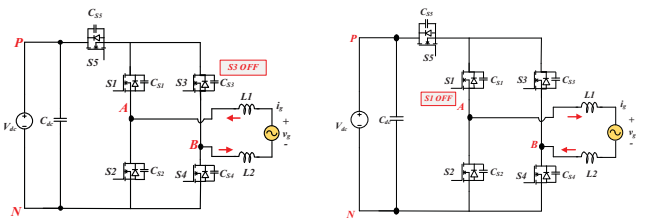
Heric

$$V_{CM} = V_{AN} = V_{BN} = V_{DC} \cdot \frac{C_{S1} + C_{S3}}{C_{S1} + C_{S2} + C_{S3} + C_{S4}} \tag{7}$$

H6-Type

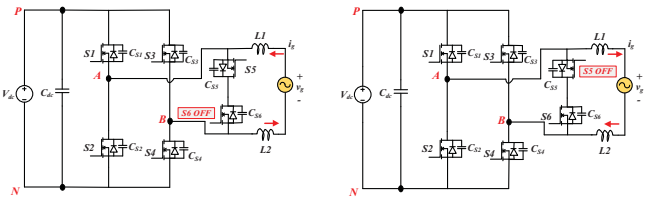
$$V_{CM} = V_{AN} = V_{BN} = V_{DC} \cdot \frac{C_{S1} + C_{S2}}{C_{S1} + C_{S2} + \frac{C_{S3} \cdot C_{S5}}{C_{S3} + C_{S5}} + C_{S4}} \tag{8}$$

From the above expressions; it is evident that V_{AN} and V_{BN} are not equal to V_{dc}/2 during freewheeling mode for all three topologies. Therefore, CMV cannot be kept constant in all the operating modes of the inverter which increases the magnitude of leakage current.



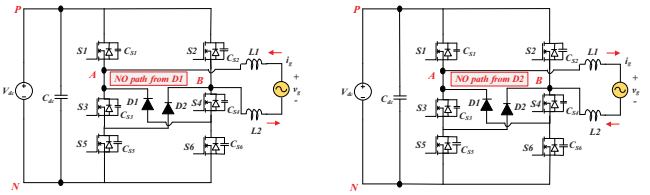
(a) (b)

Fig.4. H5 topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.



(a) (b)

Fig.5. Heric topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.



(a) (b)

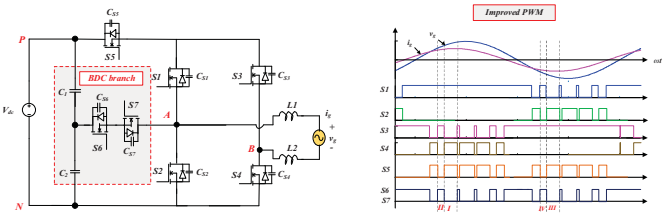
Fig.6. H6-Type topology during negative power region; (a) positive v_g and negative i_g, (b) negative v_g and positive i_g.

B. Analysis of Bi-directional current path in H5, Heric and H6-Type topologies while freewheeling period

The reactive power capability of the inverter is determined based on the bi-directional current path provided by the topology and its PWM technique. From Figs. 4, 5 and 6; it is observed that the conventional PWM technique applied for all three topologies are not providing a path for the current under negative power region during freewheeling period (i.e., positive v_g and negative i_g, negative v_g and positive i_g respectively). For example, in H5 topology switch, *S3* and *S1* are off during the negative power region hence there is no path for current as shown in Figs. 4(a) and 4(b) respectively. Thus, PWM logic applied to the H5 inverter should be modified in such a way that switches *S3* and *S1* to be turn-on under negative power region. Similarly, switches *S5*, *S6* in Heric and switches *S3*, *S4* in H6-Type inverter should be turn-on under negative power region to allow the current in both the directions during the freewheeling period as shown in Figs. 5 and 6 respectively.

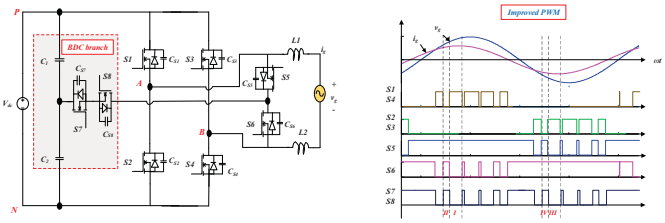
III. Proposed BDC based H5, Heric and H6-Type Topologies

In this section, a bi-directional clamping branch along with improved PWM techniques for H5, Heric and H6-Type are proposed. The BDC branch is obtained by connecting two cascaded MOSFETs switching devices with split DC-link capacitors. It provides a bi-directional current path and clamps the terminal voltages of the inverter equal to $V_{dc}/2$ during freewheeling period in positive as well as negative power regions. Figs. 7, 8 and 9 show the proposed BDC based H5, Heric and H6-Type topologies respectively.



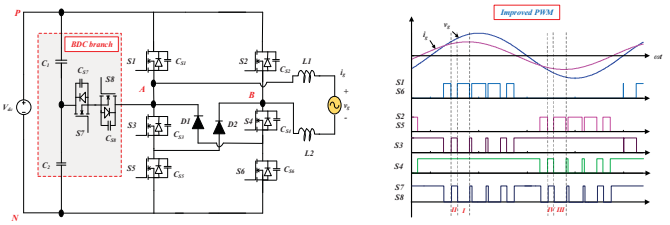
(a) (b)

Fig.7. BDC based H5TLI: (a) Circuit diagram, (b) improved PWM.



(a) (b)

Fig.8. BDC based Heric TLI: (a) Circuit diagram, (b) improved PWM.



(a) (b)

Fig.9. BDC based H6-Type TLI: (a) Circuit diagram, (b) improved PWM.

A. Operating states

Operating states of the inverters in both unity and non-unity power factor operations of the grid are explained in this section. Based on the voltage polarity the operation of the inverters are classified into three states (i.e., $V_{AB}=V_{dc}$, V_{AB}=zero and $V_{AB}=-V_{dc}$) and each state allows the current from source to grid and vice-versa. Besides, the operation of both conventional H5, Heric and H6-Type TLIs and proposed BDC based TLIs are same during positive power region. Furthermore, switching logic, terminal voltages and CMV calculations for BDC based H5, Heric and H6-Type topologies are given in Table I.

State 1: In this state, $V_{AB} = V_{dc}$, and the current flows either from source to grid or vice-versa as shown in Figs. 10(a), 11(a) and 12(a) respectively. During this state; in positive power region, current flows through MOSFETs and in the negative power region current flows through body diodes of MOSFETs. The inverter terminal voltages $V_{AN}=V_{dc}$, $V_{BN}=0$. Hence V_{DM} and V_{CM} become,

$$V_{DM} = V_{AN} - V_{BN} = V_{dc} \tag{9}$$

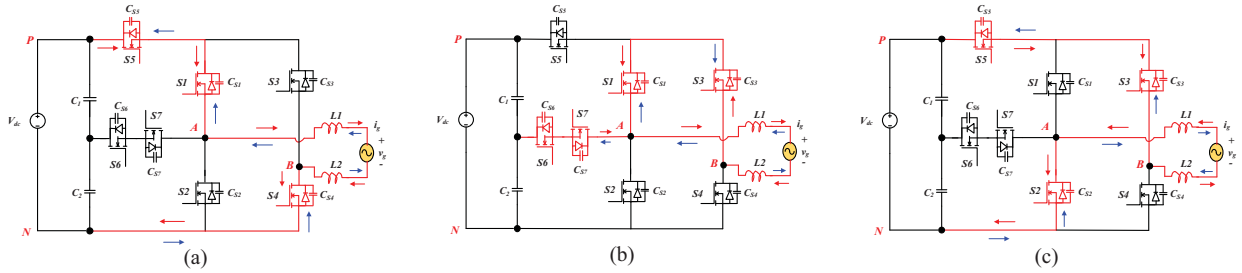
$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{dc}}{2} \tag{10}$$

State 2: In this state, $V_{AB} = 0$, and the current freewheels through the inductors and grid or vice-versa via power semiconductor switches as shown in Figs. 10(b), 11(b) and 12(b) respectively.

TABLE I. SWITCHING LOGIC AND CMV CALCULATIONS FOR BDC BASED TLIs

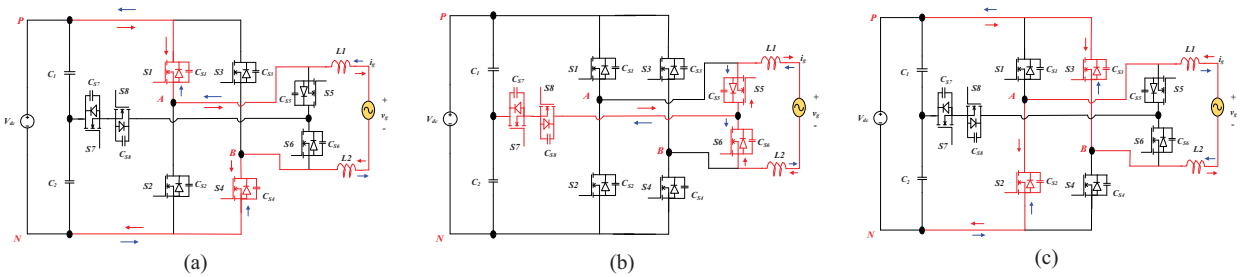
BDC based TLIs		*S1*	D_{S1}	*S2*	D_{S2}	*S3*	D_{S3}	*S4*	D_{S4}	*S5*	D_{S5}	*S6*	D_{S6}	*S7*	D_{S7}	*S8*	D_{S8}	*D1*	*D2*	V_{AN}	V_{BN}	V_{CM}
H5	$i_g>0$	1	0	0	0	0	0	1	0	1	0	0	0	0	0	-	-	-	-	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	1	0	1	0	0	0	0	-	-	-	-	V_{dc}	0	$V_{dc}/2$
H5	$i_g>0$	1	0	0	0	0	1	0	0	0	0	1	0	0	1	-	-	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	1	0	0	1	0	0	0	0	0	0	1	1	0	-	-	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H5	$i_g>0$	0	0	1	0	1	0	0	0	1	0	0	0	0	0	-	-	-	-	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	-	-	-	-	0	V_{dc}	$V_{dc}/2$
Heric	$i_g>0$	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	-	-	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-	-	V_{dc}	0	$V_{dc}/2$
Heric	$i_g>0$	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
Heric	$i_g>0$	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	-	-	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	-	-	0	V_{dc}	$V_{dc}/2$
H6-Type	$i_g>0$	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	V_{dc}	0	$V_{dc}/2$
$V_{AB}=V_{dc}$	$i_g<0$	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	V_{dc}	0	$V_{dc}/2$
H6-Type	$i_g>0$	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
$V_{AB}=0$	$i_g<0$	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H6-Type	$i_g>0$	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	V_{dc}	$V_{dc}/2$
$V_{AB}=-V_{dc}$	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	V_{dc}	$V_{dc}/2$

*D_{S1} to D_{S8} are the body diodes of switches *S1* to *S8* respectively.



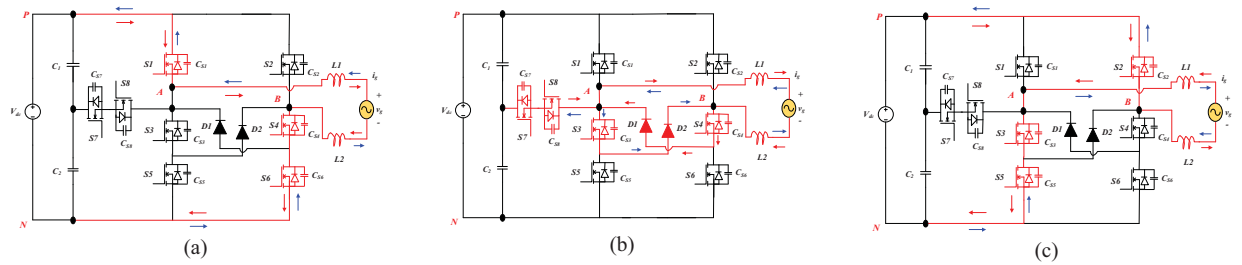
(a) (b) (c)

Fig.10. Operating modes of the BDC-H5 inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.



(a) (b) (c)

Fig.11. Operating modes of the BDC-Heric inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.



(a) (b) (c)

Fig.12. Operating modes of the BDC-H6-Type inverter (a) $V_{AB}= V_{dc}$, (b) $V_{AB}= 0$, (c) $V_{AB}=-V_{dc}$.

Improved modulation technique provides a bi-directional path for current to enhance the reactive power capability of the BDC based inverters. During this state; DC source is isolated from the grid and also the inverter terminal voltages are clamped to half of the DC-link voltage such as $V_{AN}=V_{dc}/2$, $V_{BN}= V_{dc}/2$. Hence V_{DM} and V_{CM} become,

$$V_{DM} = V_{AN} - V_{BN} = 0 \tag{11}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{dc}}{2} \tag{12}$$

State 3: In this state, V_{AB} = $-V_{dc}$, and the current flows either from source to grid or vice-versa as shown in Figs. 10(c), 11(c) and 12(c) respectively. During this state; in positive power region, current flows through MOSFETs and in the negative power region current flows through body diodes of MOSFETs. The inverter terminal voltages V_{AN}=0, $V_{BN}=V_{dc}$. Hence V_{DM} and V_{CM} become,

$$V_{DM} = V_{AN} - V_{BN} = -V_{dc} \tag{13}$$

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{dc}}{2} \tag{14}$$

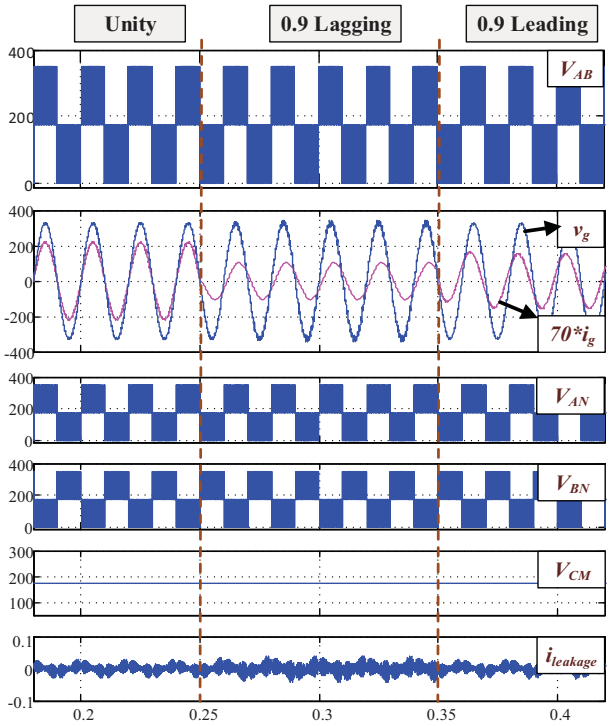


Fig.13. Differential mode and common mode results of the BDC based H5 inverter.

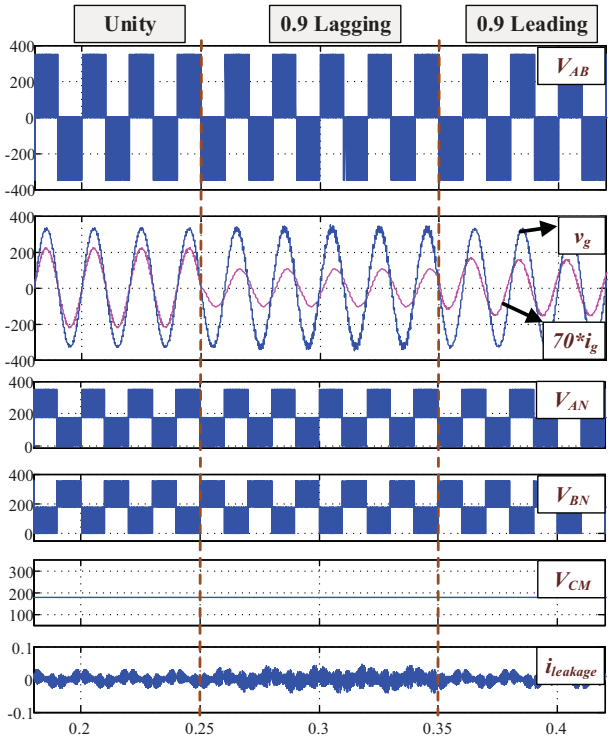


Fig.14. Differential mode and common mode results of the BDC based Heric inverter.

TABLE II. SIMULATION PARAMETERS

S. No	*Parameters*	*Value*
1	Input voltage	350 V
2	Inductor L_f	2 mH
3	Capacitors C_1, C_2, C_f	1 mF, 1 mF, 6 µF
4	AC output voltage	230V, 50 Hz
5	Switching frequency f_s	10 kHz
6	Output power	500W
7	C_P and R_g	30 nF, 10Ω

B. Improved PWM Strategies

Figs. 7(b), 8(b) and 9(b) illustrates the improved Unipolar based pwm strategies for BDC based H5, Heric and H6-Type topologies respectively. Here, a bi-directional current path is provided for the inverters by triggering switches *S1* and *S3* in H5, *S5* and *S6* in Heric and *S2* and *S4* in H6-Type topologies. Moreover, in zero states, only two switches and two diodes are conducting with respect to the current direction. In addition to that, the BDC branch clamps the inverter terminal voltages to half of the DC-link voltage.

V. SIMULATION RESULTS

To test the proposed concept simulations are performed in MATLAB/SIMULINK software and their corresponding specifications are given in Table II. A 150nF capacitor is connected across the terminals *P* and ground for the evolution of leakage current caused due to changes in CMV. Further, the reactive power capability of the proposed grid-connected inverters is tested for 0.9 lagging and 0.9 leading conditions. Fig. 13 shows the differential mode (V_{AB}, v_g and i_g) and common mode characteristics (V_{AN}, V_{BN}, V_{CM} and $i_{leakage}$) of BDC based H5 topology under various power factor conditions. It can be noticed that the proposed BDC branch effectively clamps the CMV to half of the *input DC voltage* in all the operating modes of the H5 inverter (i.e., high-frequency fluctuations due to switch junction capacitances are eliminated during the freewheeling states).

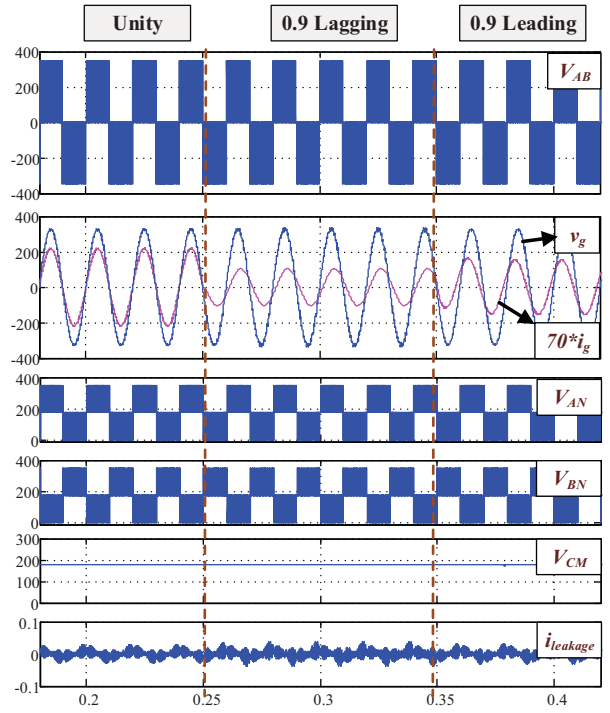


Fig.15. Differential mode and common mode results of the BDC based H6-Type inverter.

Moreover, improved PWM technique enhances the inverter operation under negative power region without losing waveform quality. Similarly, Figs. 14 and 15 illustrate the waveforms of BDC based Heric and H6-Type inverter topologies at unity, 0.9 lagging and 0.9 leading operations. Moreover, it enhances conventional H5, Heric and H6-Type TLI operations during negative power region. Figs. 16(a) and (b) shows %THD of the grid current at unity and 0.9 leading power factors operation respectively and the measured %THD is less than the IEEE 1547 grid standards.

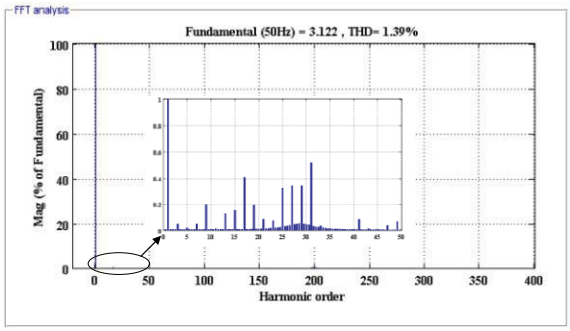


Fig.16. (a) FFT spectrum of grid current under unity power factor.

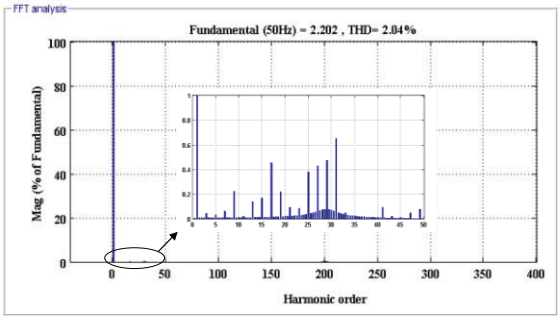


Fig.16. (b) FFT spectrum of grid current at 0.9 leading power factor.

Furthermore, the measured leakage current through PV parasitic capacitance is 10.24 mA(RMS) which is well below the VDE 0126-1-1 standards. Thus, from the simulation results, it is observed that the BDC based clamping and improved modulation techniques for all three topologies are well suitable to limit the leakage current below 11mA (approx.) and also enhances the inverter operation under real and reactive power injection. The experimental validation is underway to further prove the proposed concept and those results will be presented in the next version of the manuscript.

VI. Conclusion

In this paper, BDC based H5, Heric and H6-Type transformerless inverter topologies are proposed with the features of reduced leakage current and reactive power capability. It can be noticed that proposed BDC based topologies maintains constant CMV across the inverter terminals (half of the input DC voltage) and owns the merit of reduced common mode filter size. Moreover, the proposed modulation scheme enables the inverter to operate in both positive and negative power regions and improves the waveform quality. Finally, the performance of all three topologies is validated through simulation results.

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