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RESEARCH ARTICLE

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A three-phase inverter circuit using half-bridge cells and T-NPC for medium-voltage applications

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Summary

Three-phase single DC-source based multilevel inverter topologies play a pivotal role in industrial applications due to the reduced number of components and higher efficiency. This paper emphasizes the inverter for medium-voltage applications that employ a conventional three-phase T-type structure (T-NPC). The primary circuit of the proposed configuration consists of a T-NPC structure connected to the half-bridge cells at the top and the bottom sides of each phase. The secondary circuit consists of DC-link capacitors whose voltage balancing is attained through a separate voltage balancing circuit (VBC). Using the proposed configuration, the number of components and independent DC supplies are reduced compared with the conventional topologies such as a neutral point clamped (NPC) inverter, a flying capacitor (FC) inverter, and a cascaded H-bridge (CHB) inverter for the same number of output voltage levels. Hence, the proposed topology results in the reduction of weight, volume, and power losses of the inverter. A sine-triangle comparison method is employed in the field programmable gate array (FPGA) platform to generate the firing pulses of the circuit switches. The effectiveness of the proposed topology is verified with simulation studies and is experimentally validated with a scaled-down prototype.

KEYWORDS

efficiency, T-type inverter, two-level cells, voltage balancing circuit

1 | INTRODUCTION

Multilevel inverters (MLIs) consist of several DC voltage sources and power semiconductor devices to synthesize an AC output voltage waveform, which possesses a low harmonic content. They have become popular in various industrial drives, flexible alternating current transmission system (FACTs), and renewable applications due to their improved power quality, reduced electromagnetic interference, voltage stress (dv/dt) across the devices, and filter size.[1–4] The MLI technology started with the advent of three classical configurations: namely, neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). Though these topologies are standardized and can meet various applications, they all suffer from the drawback of the higher component count to generate more than three-levels.[5,6] The difficulty of DC-link capacitor voltage balancing and the necessity of clamping diodes limit the use of the NPC-MLIs for higher-level operations. On the other hand, the FC-MLIs require a more significant number of FCs and need higher switching

frequencies to balance the capacitor voltages. The CHB converter overcomes these limitations up to a certain extent, with its modular structure. However, it demands more independent DC sources for higher voltage levels. Therefore, in the recent literature,[7–15] several new MLI topologies are reported with a reduced component count, novel voltage balancing methods, and the reduced number of independent DC sources in comparison with the aforesaid conventional topologies. The topology proposed in Babaei et al[7] can produce a seven-level output with reduced component count as compared with CHB, but it has no common DC-link to operate for three phases. A novel three-section-based cascaded single-phase nine-level inverter is proposed in Tirupathi et al[8] with reduced component count and using a single DC source. This topology has the limitation of a higher number of conducting switches and demands separate DC sources to operate for three-phase. To address this problem, a novel three-phase, five-level (5-L) inverter is proposed with the combination of diode clamped and FC MLIs using a common DC-link with two DC sources of $V_{dc}/2$ each.[9] Another 3-phase 5-L topology with the limited component count is proposed in Masaoud et al.[10] However, the demand for a higher number of clamping diodes and DC power supplies increases the cost and complexity of these topologies.

Moreover, in most of the MLI topologies, the primary difficulty lies in balancing the DC-link and FC voltages. To alleviate this issue, a novel pulse width modulation (PWM) scheme is proposed in Lee et al.[11] It has not become popular due to the control complexity. In Sandeep and Udaykumar[12] and Yu et al,[13] it is demonstrated that the voltage balancing of the FCs could be achieved using redundant switching combinations. However, this method reduces the effective utilization of the DC-bus voltage due to the reduced fundamental output component because of the reduction in the modulation index. To alleviate this problem, the employment of front-end DC-DC converters is proposed for higher-level MLIs to achieve the reference DC-bus capacitor voltages. Consequently, the introduction of the DC-DC converter demands more semiconductor devices and reduces reliability.[14] A six-level inverter reported in Le and Lee[15] employs the combination of two two-level cells with an FC in each phase along with the DC-bus capacitors. In this topology, the DC-bus capacitor voltages are maintained constantly with the use of a VBC, and the FCs are charged using the redundant states. As a result, this circuit is more complex, and the initial charging of the FCs also needs special attention.

Recently, a modified 5-L hybrid inverter topology that is referred to as 5-L HFC was proposed in Dao and Lee,[16] which is similar to Le and Lee.[15] More conducting devices, complex control, and additional need for FCs increase the size and cost with a reduction in the efficiency of the system. Moreover, the requirement of a voltage sensing device in each phase of Le and Lee[15] and Dao and Lee[16] limits their applicability for a cost-effective prototype. A 5-L hybrid clamped (5-LHC) converter is reported in Wang et al[17] to avoid the series-connected switches and low-frequency ripples of the FC voltages. These features make the converter adaptable for medium-voltage applications. This topology demands more capacitor and switch count; hence, it is not preferable. A 5-L inverter based on a stacked cell approach is proposed in Karthik and Loganathan[18], this configuration requires a smaller number of capacitors compared with Wang et al.[17] But, it demands increased switch count per phase and two DC sources. A single DC-source based 5-L inverter using capacitor fed H-bridges is introduced in Davis and Dey.[19] This topology has the additional advantage of increasing the DC-bus utilization. Contrary to it, this configuration also requires additional voltage sensors to control the FC voltages similar to Wang et al[17] and Karthik and Loganathan.[18] Therefore, an optimized topology with reduced switch count using novel basic units and a T-type structure is proposed in Hota et al.[20] This topology avoids the FCs and DC-link capacitors while providing an output of better quality. But, the overall system cost is expensive due to the requirement of asymmetrical DC sources V_{dc} and $2V_{dc}$. A 5-L back-to-back E-type converter that is presented in Di Benedetto et al[21,22] without using FCs has the advantages of reduced switching losses. Consequently, it uses a complex auxiliary circuit with more devices to balance the capacitor voltages; this work also lacks design criteria and dynamic analysis of the configuration.

The shortcomings mentioned in these power circuit configurations demand further research. Authors are motivated from the reported literature to develop a single DC-source based, reduced switch count with less conducting switches of 3-phase, 5-L inverter topology. It is also aimed to eliminate the FCs to overcome the requirement of independent sensors in each phase. The recommended topology in this paper is configured by combining the T-NPC and half-bridge cells. The proposed work contributes to the reduction of device count compared with NPC and FC[9,17,23] and the reduction of conduction losses due to a lower number of conducting switches/phase. A minimum component count VBC is chosen from Rojas et al[24] to achieve the DC-link capacitor voltage balancing. The performance of the VBC in equalizing the two midpoint capacitor voltages is proposed in this work. The steady-state and dynamic behavior of the proposed topology and the application of VBC in balancing two midpoint capacitor voltages are stringently investigated by creating several disturbances in the control algorithm. Moreover, the significant advantages of the proposed topology include the following: (i) common DC-link for all the three phases, (ii) absence of FCs, (iii) a simple auxiliary circuit is used to

control the capacitor voltages; (iv) reduced component count and simple structure, and (v) higher efficiency compared with conventional MLIs.

Further, the proposed topology is evaluated in simulation and the results are validated using an experimental prototype at steady-state, as well as, dynamic conditions.

2 | PROPOSED HYBRID FIVE-LEVEL INVERTER

Figure 1 illustrates the proposed hybrid 5-L inverter of phase-A with the advantage of a reduced number of semiconductor devices. This structure has a common DC-link for all three phases and built by connecting a two-level cell at the top and the bottom capacitors. The T-NPC structure is located at the center that is connected to the midpoint of the DC-link with a four-quadrant switch (antiseries connection of two IGBTs with antiparallel diodes), as well as to the outputs of top and bottom two-level cells.

2.1 | Proposed configuration

Figure 2 shows the complete three-phase circuit along with the star-connected load at the output terminals of the T-NPC. The DC-bus capacitors are connected in series and charged from an isolated DC-source; each capacitor is charged to a voltage of $V_{dc}/4$ with the aid of a VBC. Five-level output voltage waveform can be produced at the output within the limits of $-V_{dc}/2$ to $+V_{dc}/2$, at a $V_{dc}/4$ step size, by properly triggering the semiconductor devices. The output voltage levels may vary from 5-L to 3-L by a decrease in modulation index (m_a).

The off-state voltage stress across the devices S_1, S_2, S_6, and S_7 is $V_{dc}/4$; across S_{51} and S_{52} is $V_{dc}/2$; and across S_3 and S_4 is $3V_{dc}/4$. From Figure 2, it can be noted that the proposed three-phase configuration consists of 12 switches with voltage stress of $V_{dc}/4$, six switches with $V_{dc}/2$, and six switches with $3V_{dc}/4$. Hence, the sum of the total voltage stress (TVS) of the inverter switches in the proposed circuit is $3.5V_{dc}$ per phase, which is less than $4.25V_{dc}$ in the topology, introduced in Tirupathi et al.[25] The TVS in the proposed configuration is reduced due to the difference in the inverter structure and avoidance of bi-directional voltage blocking switches, compared with Tirupathi et al.[25] The reduction in TVS of the switching devices decreases the switching power losses, which results in improved efficiency of the configuration. Moreover, in contrast with Tirupathi et al,[25] this paper provides the mathematical analysis for the design of inverter and balancing circuit components and analyzes the performance of the circuit to operate at medium-voltage

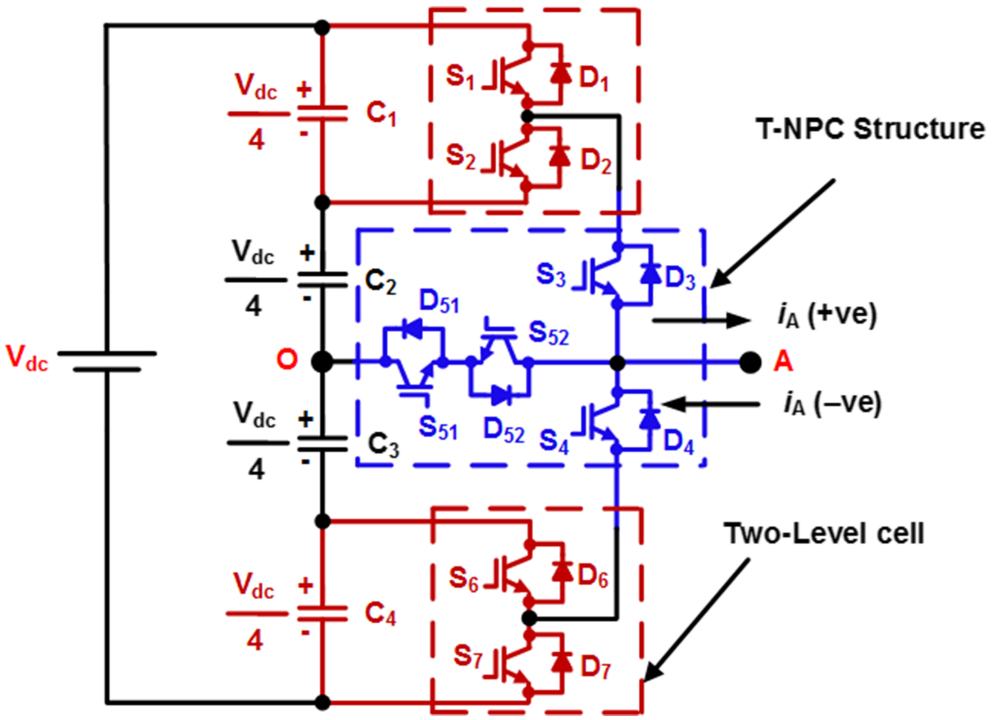

FIGURE 1 Proposed five-level configuration in phase-A [Colour figure can be viewed at wileyonlinelibrary.com]

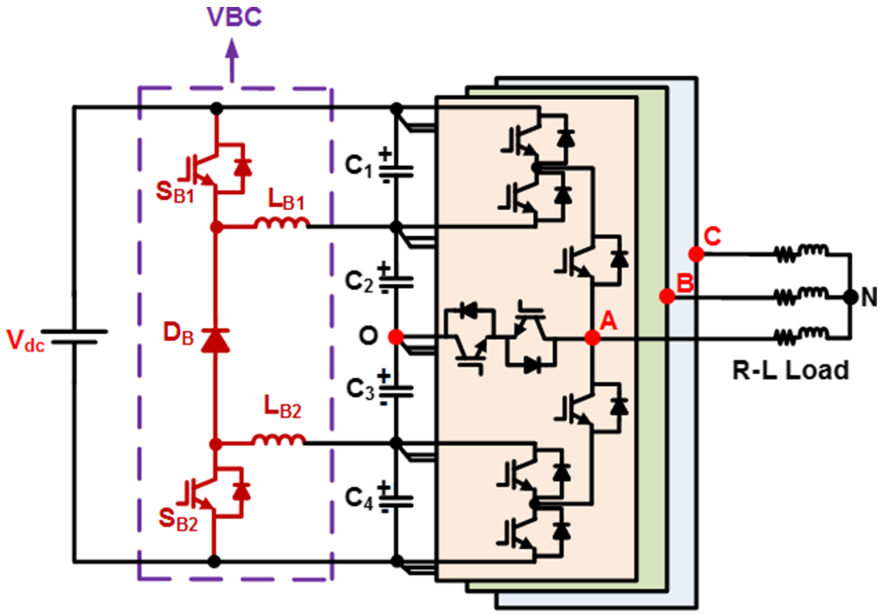

FIGURE 2 Three-phase structure of the proposed configuration [Colour figure can be viewed at wileyonlinelibrary.com]

and high power levels. Also, it investigates the ability of the circuit to withstand several transient disturbances and provides the efficiency comparison with respect to several other configurations.

2.2 | Modes of operation

The operation of the proposed 5-L inverter is described through five modes to achieve the various output voltage levels. The proposed MLI generates five levels in pole-voltage (V_{AO}), namely, $-V_{dc}/2$, $-V_{dc}/4$, 0, $V_{dc}/4$, and $V_{dc}/2$. Figure 3 illustrates the working modes and the conducting devices with respect to the line current (i_A) path.

Mode-0 [$V_{AO} = 0$]: During this mode, switches S_{51} and S_{52} are continuously gated for zero output voltage. One of the devices among switch or its body diode conducts that is determined by the path of i_A. If i_A is +ve, S_{51} and D_{52} conduct, on the other hand, when i_A is −ve, it flows through S_{52} and D_{51}.

Mode-1 [$V_{AO} = V_{dc}/4$]: If S_2 and S_3 are gated, $V_{AO} = V_{C2}$. Assuming that C_2 is initially charged to $V_{dc}/4$, then $V_{AO} = V_{dc}/4$. For +ve and −ve directions of i_A, the group of devices D_2, S_3 and D_3, S_2 conduct, respectively.

Mode-2 [$V_{AO} = V_{dc}/2$]: When the switches S_1 and S_3 are turned on, the sum of the voltages of the DC-link capacitors C_1 and C_2 appears across the load, ie, $V_{AO} = V_{C1} + V_{C2} = V_{dc}/2$. It may be noted that the devices S_1, S_3 conduct when i_A is +ve. Similarly, the devices D_3 and D_1 conduct when i_A is −ve.

Mode-3 [$V_{AO} = -V_{dc}/4$]: If S_4 and S_6 are gated, $V_{AO} = V_{C3}$. Assuming that C_3 is initially charged to $V_{dc}/4$, then $V_{AO} = -V_{dc}/4$. For +ve and −ve directions of i_A, the group of devices S_6, D_4 and D_6, S_4 conduct, respectively.

Mode-4 [$V_{AO} = -V_{dc}/2$]: By gating the devices S_4 and S_7, it is possible to make $V_{AO} = V_{C3} + V_{C4} = -V_{dc}/2$. It may be noted that the devices D_4 and D_7 conduct when i_A is +ve. Similarly, the devices S_4 and S_7 conduct when i_A is −ve.

3 | MODULATION AND DC-BUS CAPACITOR VOLTAGE CONTROL METHODS

Table 1 illustrates the switching order for 5-L output in the pole-voltage (V_{AO}). The switching states ON and OFF are shown by the digits "1" and "0," respectively. It can be observed that the number of conducting switches in the proposed topology during peak voltage levels ($\frac{\pm V_{dc}}{2}$) is only two. At $\frac{\pm V_{dc}}{2}$ level, four switching devices conduct for any direction of load current in 5L-NPC or 5L-FC topologies. Table 1 demonstrates that only 6 (ie, 2 × 3) switches from 24 conduct for a specified voltage level and the number of switching changes among any two voltage levels are only two. Therefore, higher efficiency can be expected from the proposed topology in view of the lower on-state and switching transition losses.

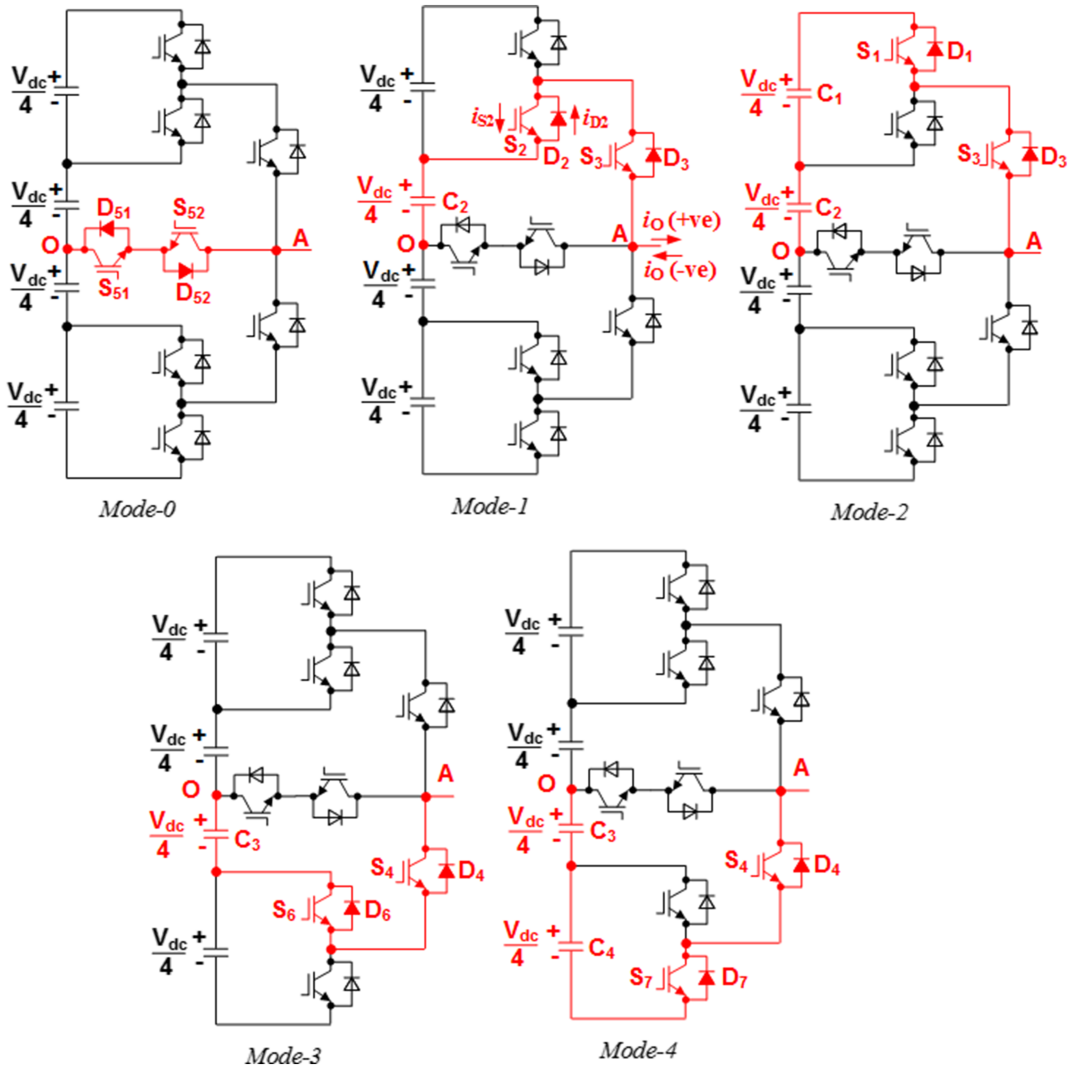

FIGURE 3 Operating states of the phase-A leg in a fundamental cycle [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1 Switching sequence of the proposed converter

V_{AO}	S_1	S_2	S_3	S_4	S_{51}	S_{52}	S_6	S_7	No. of Conducting Devices/Phase
$V_{dc}/2$	1	0	1	0	0	0	0	0	2
$V_{dc}/4$	0	1	1	0	0	0	0	0	2
0	0	0	0	0	1	1	0	0	2
$-V_{dc}/4$	0	0	0	1	0	0	1	0	2
$-V_{dc}/2$	0	0	0	1	0	0	0	1	2

3.1 | PWM technique

Several modulation and control techniques have been reported for MLIs such as sine PWM (SPWM), hybrid modulation technique, and space vector modulation. Whereas, the universally accepted level shifted in-phase disposition sinusoidal pulse-width modulation (LSIPD-SPWM) scheme[26,27] as shown in Figure 4 is used in the proposed topology. This method has the advantages of the lowest harmonic content[28] and reduced complexity in implementation. A fundamental sine wave is compared with four carrier waves to generate the control pulses at each voltage level in a fundamental cycle. FPGA Xilinx blocks are used to build suitable logic to drive the inverter switches. In this context, the modulation index (m_a) is defined as

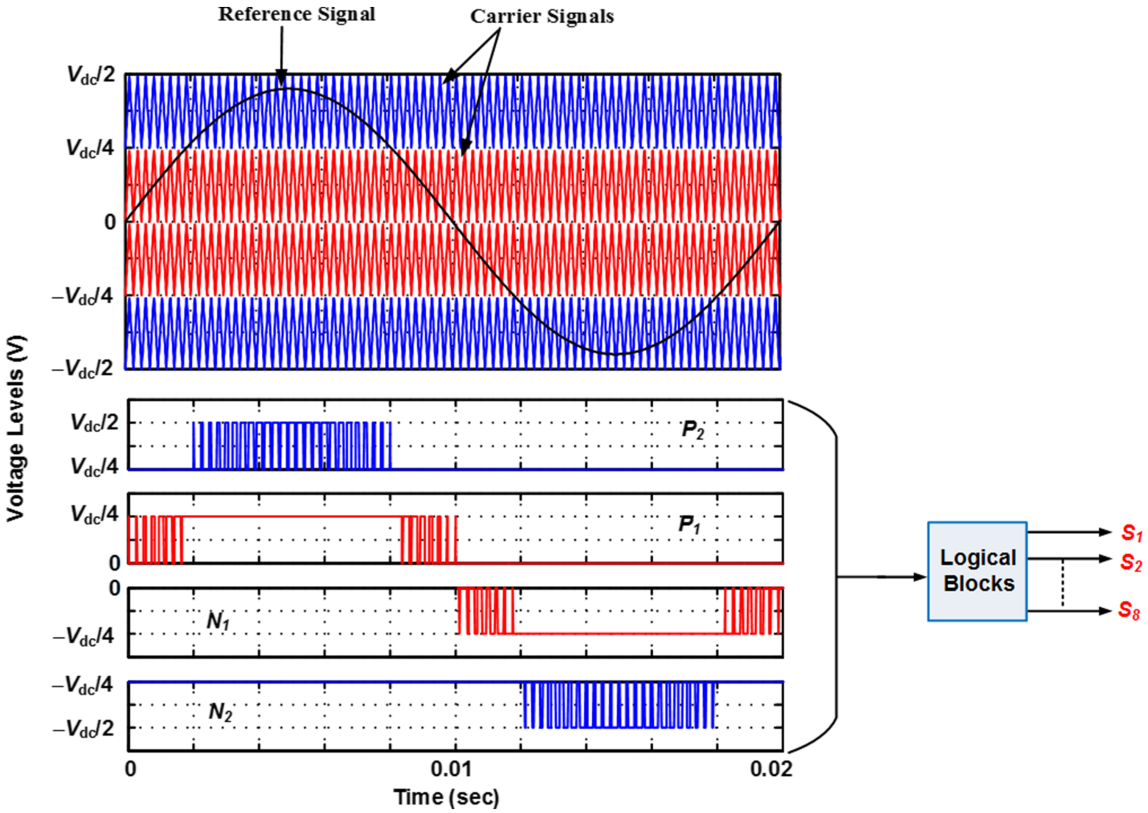

FIGURE 4 Sine-triangle modulation scheme [Colour figure can be viewed at wileyonlinelibrary.com]

$$m_a = \frac{A_r}{2A_c} \tag{1}$$

where A_r is amplitude of the reference signal and A_c is amplitude of the carrier signal.

3.2 | Capacitor voltage balancing

A voltage balancing circuit (VBC) is connected prior to the DC-link to solve the problem of capacitor voltage balancing. Figure 5 shows the auxiliary circuit constituted by two inductors and power switches with a diode. The VBC reported in previous studies[15,16,24] to control the single midpoint DC-bus capacitor voltage is employed in this work to balance two midpoint capacitor voltages.

The capacitor voltage balancing is achieved by simultaneous control of the VBC switches (S_{B1} and S_{B2}), by measuring the capacitor voltages V_{C2} and V_{C3} as shown in Figure 5. The VBC ensures the voltage regulation of C_2 and C_3 and also the voltage balancing of C_1 and C_4. Since C_2 and C_3 are located between C_1 and C_4, the charging and discharging currents of C_1 and C_4 should flow through C_2 and C_3. Thus, the direct voltage regulation of C_2 and C_3 results in an indirect voltage regulation across C_1 and C_4.[29] The complete operation of the balancing circuit consists of the following steps:

Step-1: The sum of the midpoint capacitor voltages, ie, $V_{C2} + V_{C3}$ is measured using a voltage sensor. This quantity (ie, $V_{C2} + V_{C3}$) is denoted as V_α.
Step-2: When $V_\alpha < V_{dc}/2$, S_{B1} and S_{B2} are turned on.
Step-3: When $V_\alpha = V_{dc}/2$, the balancing switches S_{B1} and S_{B2} are turned off.

The step-by-step operation of the VBC is also described in the form of a flow-chart, as shown in Figure 6B. It shows that after measuring the voltage "V_α" by a voltage sensor, it is compared with a voltage magnitude of $V_{dc}/2$. If it satisfies

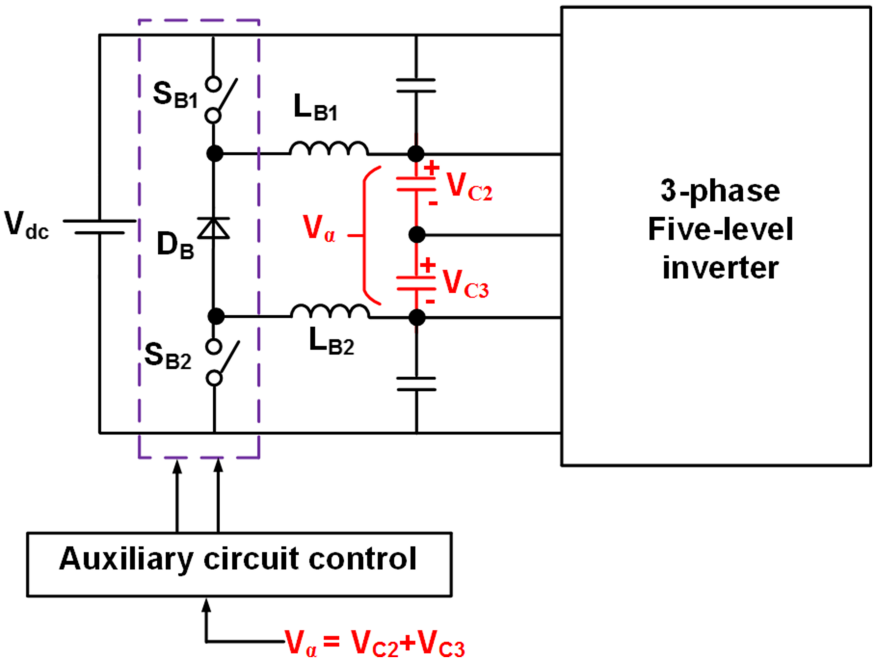

FIGURE 5 DC-link capacitor voltage control using voltage balancing circuit [Colour figure can be viewed at wileyonlinelibrary.com]

the condition ($V_\alpha = V_{dc}/2$), gate pulses to the balancing switches are withdrawn; otherwise, they are kept gated. Hence, this process is continuous and brings the voltage (V_α) approximately to $V_{dc}/2$. In the circuit shown in Figure 6A, if the initial voltage across the C_{eq} is assumed as V_0, it charges from V_{dc} source and attains its desired magnitude of $V_{dc}/2$.

The operation of the VBC is separated into two modes.

Mode-1: When $V_\alpha < \frac{V_{dc}}{2}$, S_{B1} and S_{B2} are turned-on.

During this period, the midpoint DC-bus capacitors get charged from the DC supply through the path V_{dc}-L_{B1}-C_2-C_3-L_{B2} as shown in Figure 7A. Inductors also store the energy during this period, due to the connection of the DC-source through the VBC switches.

Mode-2: When $V_\alpha = \frac{V_{dc}}{2}$, S_{B1} and S_{B2} are turned-off.

During this period, the inductors are disconnected from the DC-source; hence, they become source free. The stored energy in the inductors during Mode-1 is discharged and supplied to the midpoint capacitors through the path L_{B1}-C_2-C_3-L_{B2}-D_B as shown in Figure 7B. In this way, the midpoint capacitor voltages are maintained constantly.

When the stored energy in both the inductors is completely discharged, the midpoint capacitor voltages (V_{C2} and V_{C3}) tend to drift from their nominal values that cause $V_\alpha < \frac{V_{dc}}{2}$. By sensing this condition, the VBC switches are triggered at the same instant; this pulls the VBC to operate in Mode-1, which results in the repetition of the same cycle.

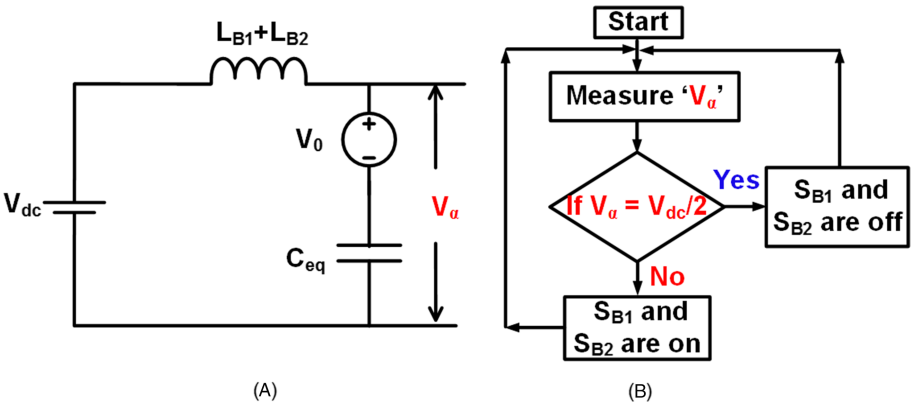

FIGURE 6 A, Equivalent circuit for DC-link capacitor voltage balancing. B, Flow-chart for capacitor voltage balancing algorithm [Colour figure can be viewed at wileyonlinelibrary.com]

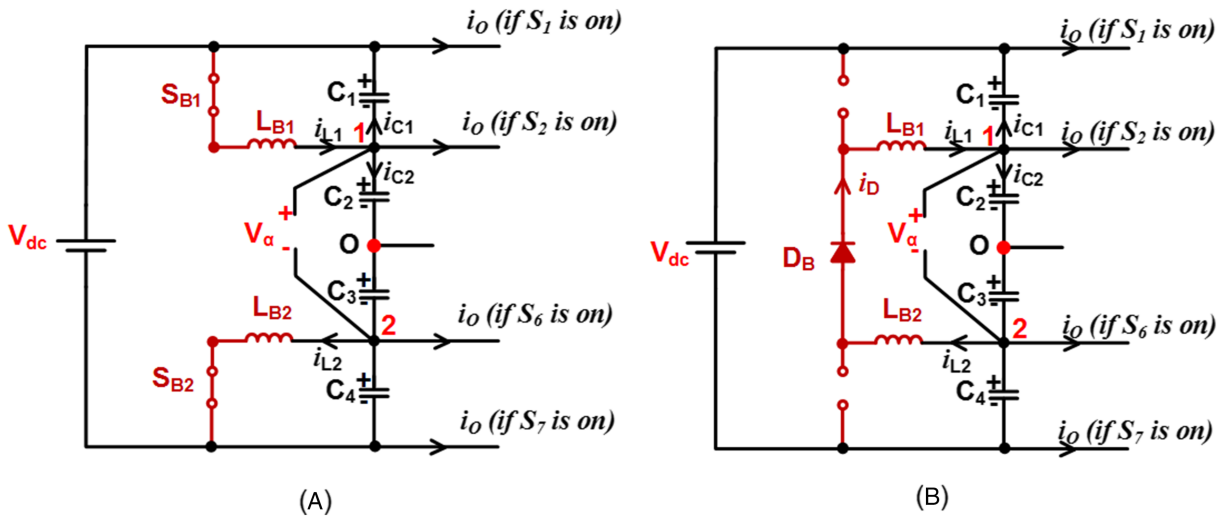

FIGURE 7 Operating modes of voltage balancing circuit: (A) Mode-1 and (B) Mode-2 [Colour figure can be viewed at wileyonlinelibrary.com]

4 | DESIGN OF CIRCUIT COMPONENTS

4.1 | DC-link capacitance

The size of the capacitors in the proposed topology is designed from the mathematical expression reported in Kjaer et al.[30] The size of each DC-link capacitor is designed as

$$C_d = \frac{P_O/V_C}{2 \times \omega_r \times \Delta V_C} \tag{2}$$

The value of the capacitors used in simulation studies and the experimental setup is designed based on the above expression.

The inverter output voltage (v_o), within a linear modulation range, can be expressed using Equation (1) as.

$$v_o = m_a V_{dc} \sin(\omega t) \tag{3}$$

where m_a is the modulation index, V_{dc} is the DC-link voltage, and ω is the fundamental angular frequency.

The inverter output current (i_o) can be expressed as

$$i_o = I_O \sin(\omega t - \varnothing) \tag{4}$$

where I_{O} is the output current amplitude and $\varnothing$ is the load power factor (PF) angle. By substituting Equations 3 and 4 in 2, and rewriting the equation for capacitor voltage ripple (ΔV_{C}),

$$\Delta V_C = \frac{m_a V_{dc} I_0 (\cos\varnothing - \cos(2\omega t - \varnothing))}{4\omega V_C C_d} \tag{5}$$

Equation 5 gives the dependency of capacitor voltage ripple on load current and load PF. It can be noted that the load current has a direct impact on capacitor voltage ripple; ie, if the load current increases, ΔV_{C} also increases. By testing at various values of load PFs, it is estimated that the load PF has an inverse relation with the ΔV_{C}; ie, if the load PF decreases, ΔV_{C} increases. The increase in ΔV_{C}, due to either an increase in load current or decrease in PF, can be controlled by either decreasing the modulation index (m_{a}) or increasing the size of the capacitance (C_{d}).

4.2 | Balancing inductors

The expression for the design of balancing inductors (L_{B1} and L_{B2}) based on the magnitude of ripple current (ΔI_L) and switching frequency[30] is as follows.

$$L_{B1} = L_{B2} = L_B = \frac{V_L D}{\Delta I_L f_{sw}} \tag{6}$$

where V_L is the voltage appearing across the inductor and D is the duty ratio of the VBC switches (S_{B1} and S_{B2}). It is to be noted that the S_{B1} and S_{B2} operate with the same duty ratio (D). The size of the inductors used in simulation and in experimentation is decided using the above formula.

The current rating $(i_L)_{\max}$ of the inductors can be estimated by applying kirchoff's current law (KCL) at node-1 in Figure 7A.

$$i_L = i_{C1} + i_{C2} + i_O \tag{7}$$

$$i_{C1} \cong i_{C2} = i_C \,(\text{in steady} - \text{state}) \tag{8}$$

$$V\text{AO} = V\text{dc}/4, i_o \cong \frac{(i_o)_{\max}}{2}$$

$$(i_L)_{\max} = 2C\frac{dV_C}{dt} + \frac{(i_o)_{\max}}{2} \tag{9}$$

By limiting the capacitor voltage ripple to 14% of its nominal value ($V_{\text{dc}}/4$),

$$(i_L)_{\max} = 2C \times 0.14 \times f_{sw}\frac{V_{dc}}{4} + \frac{(i_o)_{\max}}{2} \tag{10}$$

4.3 | Balancing switches and diode

The voltage stress across the switches (S_{B1} and S_{B2}) can be obtained by writing kirchoff's voltage law (KVL) equation in Figure 7A.

$$V_{\text{SB1}} = V_{\text{SB2}} = V_{\text{SB}} = \frac{V_{\text{dc}}}{4} + V_L \tag{11}$$

$$(V_{\text{SB}})_{\max} = \frac{V_{\text{dc}}}{4} + L_B\left(\frac{di_L}{dt}\right)_{\max} \tag{12}$$

$$(V_{\text{SB}})_{\max} = \frac{V_{\text{dc}}}{4} + L_B \times f_{sw} \times (i_L)_{\max} \tag{13}$$

The voltage across the balancing diode (D_B) can be obtained by writing KVL in Figure 7B.

$$V_{DB} = 2V_L + \frac{V_{dc}}{2} \tag{14}$$

By substituting the value of $(V_L)_{\max}$ obtained from Equation 13 in Equation 14.

$$(V_{\mathrm{DB}})_{\max} = 2L_B \times f_{\mathrm{sw}} \times (i_L)_{\max} + \frac{V_{\mathrm{dc}}}{2} \tag{15}$$

$$(V_{\mathrm{DB}})_{\max} = 2(V_L)_{\max} + \frac{V_{dc}}{2} \tag{16}$$

For the chosen values of L_B and f_{sw}, it is calculated theoretically and verified in the simulation that the maximum switching stress across the VBC switches and diode is approximately $2V_{\mathrm{dc}}/4$ and V_{dc}, respectively. The current rating of the VBC switches is to be determined during their conduction period. It is to be noted that both the switches carry equal current, when they are turned-on, due to the symmetrical nature of the circuit. Therefore,

$$i_{\mathrm{SB1}} = i_{\mathrm{SB2}} = i_{\mathrm{SB}} \tag{17}$$

When S_{B1} and S_{B2} are turned-on, the current carried by the switches is the same as the inductor currents; hence,

$$(i_{\mathrm{SB}})_{\max} = (i_L)_{\max} \tag{18}$$

When S_{B1} and S_{B2} are turned-off, the diode (D_B) joins into the conduction path of inductor currents; hence,

$$(i_{\mathrm{DB}})_{\max} = (i_L)_{\max} \tag{19}$$

It is to be noted that the maximum inductor current flowing through the VBC switches and diode is the charging current and the discharging current of the inductors respectively.

5 | ADVANTAGES AND COMPARISON OF THE PROPOSED TOPOLOGY

The requirement of clamping diodes and FCs in a NPC and FC inverters, respectively, results in an increased component count. In contrast, the proposed topology results in a compact system due to the absence of the clamping diodes and FCs. The advantage of using only one DC supply renders the proposed configuration suitable for grid-connected applications. The number of independent DC supplies in the proposed configuration reduces by 83% with respect to conventional CHB, 50% compared with topologies reported in Narimani et al[9] and Karthik and Loganathan[18] and 33% compared with Masaoud et al[10] and Sanchez-Ruiz et al.[23] The number of capacitors required in the proposed configuration is four, which are operated from a single DC source.

In order to control the capacitor voltages, the proposed circuit additionally requires two switches, two inductors, and a diode to form the VBC. A CHB inverter requires two independent DC sources per phase, ie, in total six independent sources to produce the three-phase 5-L output, which is not economical. Due to the presence of VBC in the proposed configuration, it appears that the total device count in the proposed configuration is more than a CHB inverter. However, the requirement of only one DC source and a few low-cost components of VBC in the proposed topology results in an economical, compact, and flexible system compared with a CHB inverter, which demands six independent DC sources.

Table 2 provides a comparative analysis of the proposed circuit with respect to the other MLIs in terms of the number of switching devices, device ratings, the number of DC sources, etc. Table 2 clearly shows that the proposed topology avoids the use of FCs, which are required in an FC inverter[9] and other circuit configurations reported in previous studies.[16–20,31] The avoidance of FCs eliminates additional voltage sensors and reduces the ripple content in the output voltage waveforms. The complexity in the operation of the circuit is reduced due to the lower number of devices. In addition, the proposed topology can be operated for higher modulation indices as compared with the configuration presented in.[13]

TABLE 2 Component comparison of the proposed MLI with respect to other MLIs

Component	Voltage Rating	NPC	FC	CHB	9	10	16	17	18	19	31	23	25	Proposed Topology
Switches	V_{dc}	--	--	--	--	6	--	--	--	6	--	--	6	--
	$3V_{dc}/4$	--	--	--	--	6	--	--	--	--	--	--	3	6
	$2V_{dc}/4$	--	--	--	--	2	6	6	12	6	12	24	3	6
	$V_{dc}/4$	24	24	24	24	2	18	24	8	12	12	--	12	12
Clamping diodes	V_{dc}	--	--	--	--	6	--	--	--	--	--	--	--	--
	$3V_{dc}/4$	6	--	--	--	--	--	--	--	--	--	--	--	--
	$2V_{dc}/4$	6	--	--	--	--	--	--	6	--	--	12	--	--
	$V_{dc}/4$	6	--	--	6	6	--	--	--	--	--	--	--	--
Flying capacitors	$3V_{dc}/4$	--	3	--	3	--	--	--	--	--	--	--	--	--
	$2V_{dc}/4$	--	3	--	--	--	--	3	--	--	--	--	--	--
	$V_{dc}/4$	--	3	--	6	--	3	3	2	3	3	--	--	--
DC sources	V_{dc}	1	1	--	--	--	1	1	--	1	1	3	1	1
	$2V_{dc}/4$	--	--	--	2	2	--	--	2	--	--	--	--	--
	$V_{dc}/4$	--	--	6	--	1	--	--	--	--	--	--	--	--
DC-link capacitors	$V_{dc}/4$	4	4	--	--	--	2	4	--	--	--	--	4	4
	$2V_{dc}/4$	--	--	--	2	--	1	--	--	2	2	6	--	--
Total components		47	38	30	43	31	31	41	30	30	30	45	29	29

6 | SIMULATION RESULTS

6.1 | Steady-state performance

In this paper, the proposed three-phase inverter and its control scheme are modeled with the MATLAB software using Xilinx blocks. In simulation studies, 6200 V of DC bus voltage is considered to produce 3.4 kV (L-L) at the output. The gating pulses are developed at a carrier switching frequency of 4 kHz. The proposed prototype is implemented at a power rating, PF, and modulation index of 1000 kW, 0.9, and 0.9, respectively. The load PF of 0.9 is obtained using restive-inductive (R-L) elements. Figure 8A–D shows the inverter output quantities consisting of the pole voltages, line voltage, 3-phase line currents, and steady-state DC-link capacitor voltage waveforms, respectively. In the proposed configuration, the mathematical expression for DC source current (I_{dc}) is defined as

$$I_{dc} = \text{Load current } (i_O) + \text{Capacitor charging current } (i_C) \tag{20}$$

It can be observed from Figure 8E that the peak value of I_{dc} is 310 A and its average value is measured as 165 A. From the peak value of I_{dc}, the load current share is 260 A from Figure 8C. The remaining 50 A of I_{dc} is used for charging the DC-link capacitors.

Figure 8F illustrates the harmonic spectrum of the synthesized inverter output pole-voltage waveform. The line-voltage and current THDs are observed in fast Fourier transform analysis and denoted in Figure 8B and 8C, respectively. It is observed that the current THD is 1.2%, which is below the nominal value as per the IEEE 1547 grid standard.

6.2 | Dynamic performance

The proposed 5-L converter and the balancing circuit are tested for several disturbances by a step-change in (i) load, (ii) load PF, and (iii) switching frequency (f_{sw}). A sudden change in load is applied at 0.8 seconds as shown in

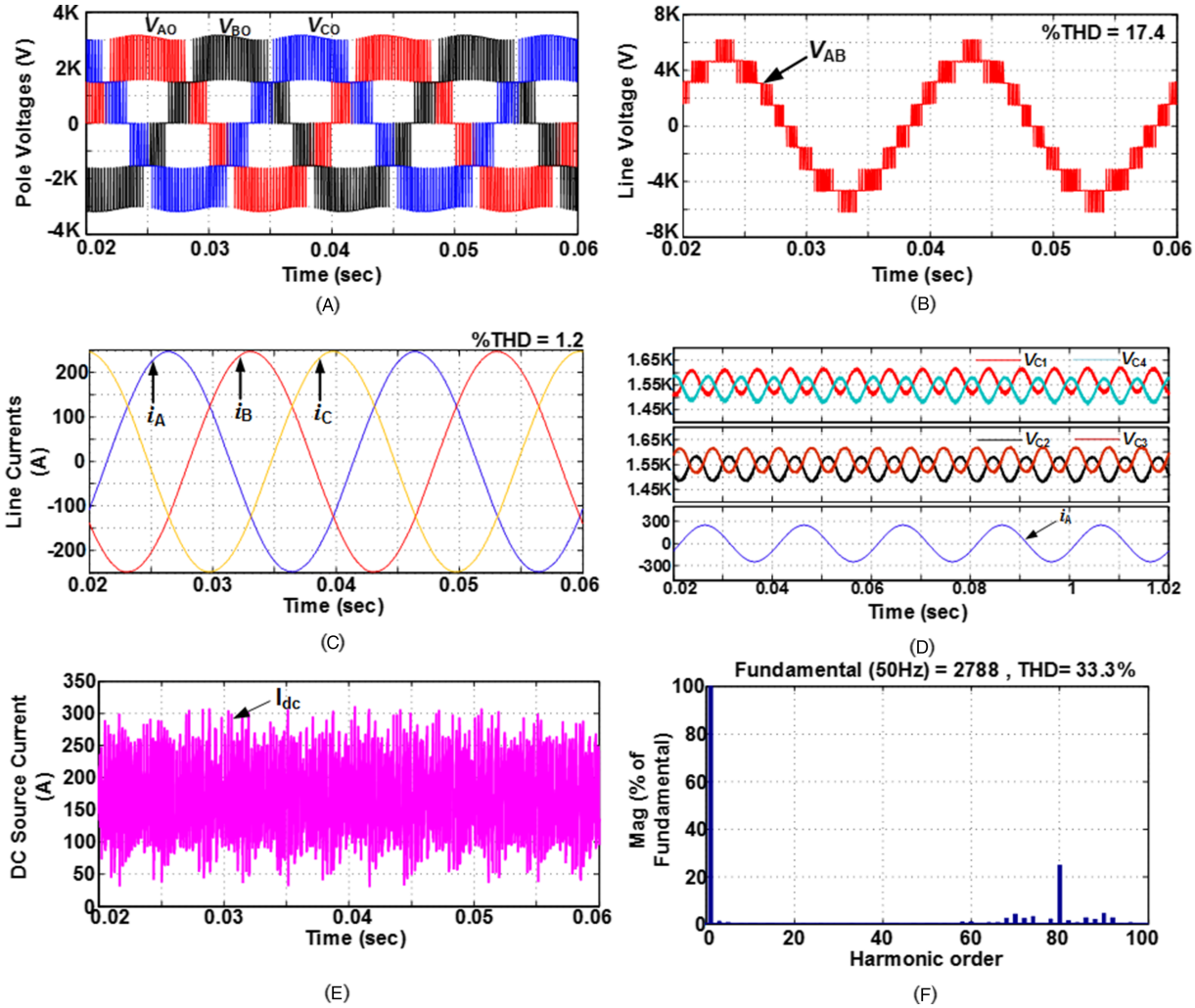

FIGURE 8 Simulation results for $m_a = 0.9$: (A) pole-voltages, (B) line-voltage (V_{AB}), (C) 3-ph line-currents, (D) steady-state capacitor voltages, (E) DC source current (I_{dc}), and (F) fast Fourier transform spectrum of pole-A voltage [Colour figure can be viewed at wileyonlinelibrary.com]

Figure 9A. To facilitate a better visualization, the zoomed waveforms of Figure 9A are shown in Figure 9B. It can be observed that the capacitor voltages are balanced constantly for a load change from 124 to 248 A. Figure 10 shows the variation of capacitor voltages for a step-change in switching frequency (f_{sw}). It is evident that the DC-link capacitor voltages are maintained constantly and the ripples are varying slightly with respect to change in f_{sw}. It is also evident from Figure 11 that the slight variation in capacitor voltage has a negligible effect on output voltage and currents.

7 | EXPERIMENTAL RESULTS

The proposed three-phase 5-L inverter is developed on a lower scale prototype to validate the simulation results using Digilent SPARTAN-6 (XC6SLX45) FPGA processor as shown in Figure 12. The detailed specifications of the proposed inverter components and controller parameters are given in Table 3. It can be seen that the proposed 5-L inverter comprises a power circuit, balancing circuit, control circuit, and driver circuit. The proposed model is tested at a power rating, PF, and m_a of 400 W, 0.9, and 0.9 respectively. A single DC power source is connected to the power circuit, and a four-channel DPO3034 Tektronix Oscilloscope is used for the measurement of various waveforms.

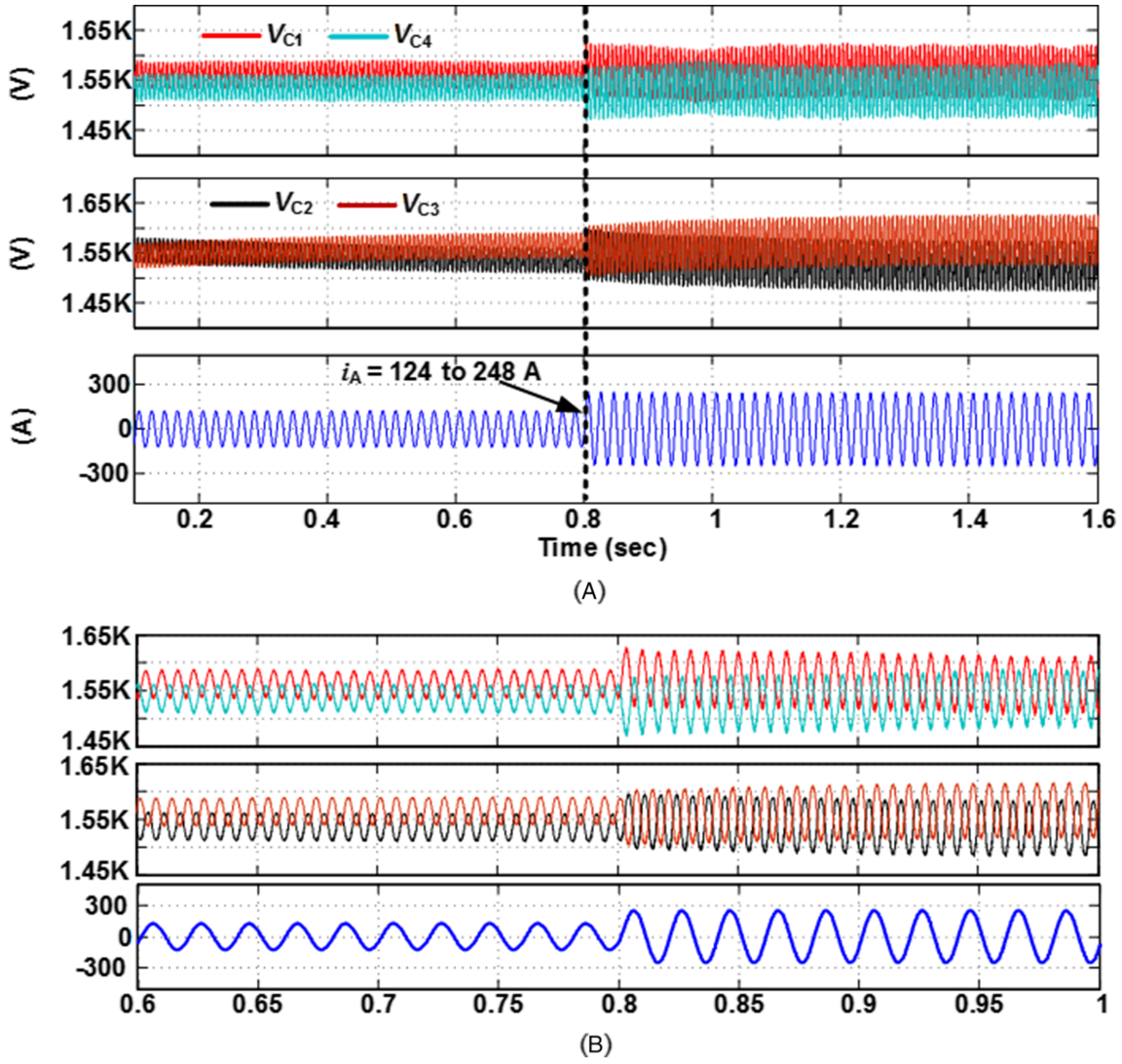

FIGURE 9 A, Capacitor voltages with respect to step-change in load. B, Zoomed waveforms of Figure 9A [Colour figure can be viewed at wileyonlinelibrary.com]

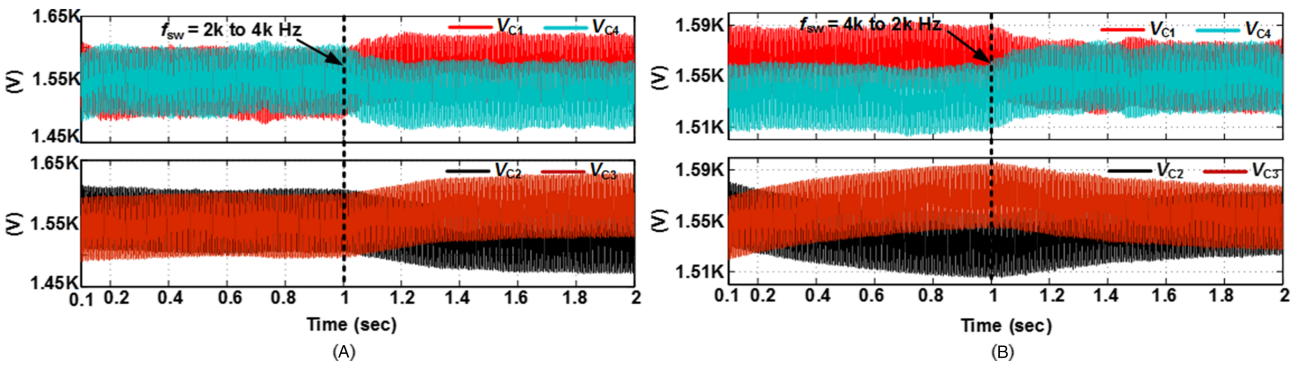

FIGURE 10 Capacitor voltages with respect to change in PWM frequency (f_{sw}): (A) 2 to 4 k Hz and (B) 4 to 2 k Hz [Colour figure can be viewed at wileyonlinelibrary.com]

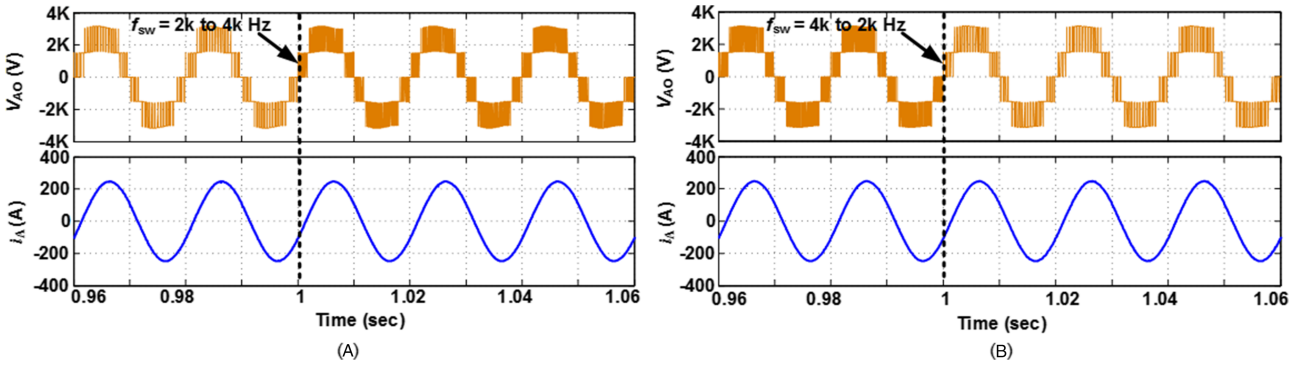

FIGURE 11 V_{AO} and i_A with respect to change in pulse width modulation frequency (f_{sw}): (A) 2 to 4 k Hz and (B) 4 to 2 k Hz [Colour figure can be viewed at wileyonlinelibrary.com]

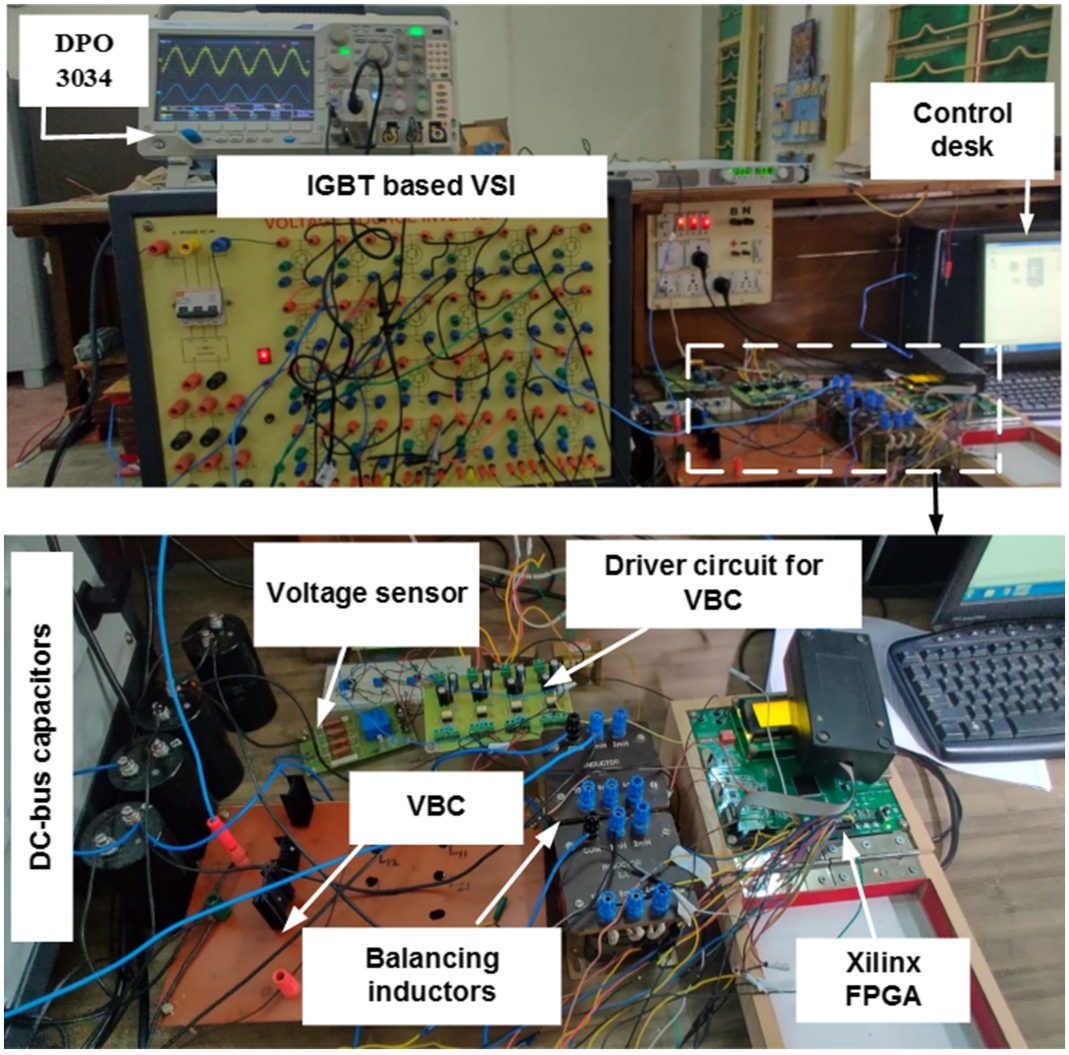

FIGURE 12 Experimental setup [Colour figure can be viewed at wileyonlinelibrary.com]

7.1 | Steady-state performance

Figure 13A,B illustrates the measured output waveforms of pole voltages, line voltage, and load current at a modulation index (m_a) of 0.9, respectively. Figure 13C depicts the steady-state capacitor voltages. It can be noted that the VBC effectively balances the capacitor voltages. Figure 13D depicts the experimentally obtained harmonic profile of pole-A

TABLE 3 Configuration parameters

Parameter/Device	Simulation	Experimentation
DC-bus voltage	6200 V	200 V
Capacitors (C_1, C_2, C_3, C_4)	2 mF/ C44UOGT7200G5SK	1 mF/ Electrolytic (450 V-DC)
Balancing inductors	1 mH/195C100	1 mH/CRNGO steel core (10 A)
Output power	1,000 kW	400 W
Switching frequency	4 kHz	4 kHz
Fundamental frequency (f_m)	50 Hz	50 Hz
IGBT switches	FF200R33KF2C	IKW40T120
Balancing diode (D_B)	DD200S33K2C	MUR1560
Load resistance (R)/phase	10 Ω	26 Ω
Load resistance (L)/phase	15 mH	10 mH

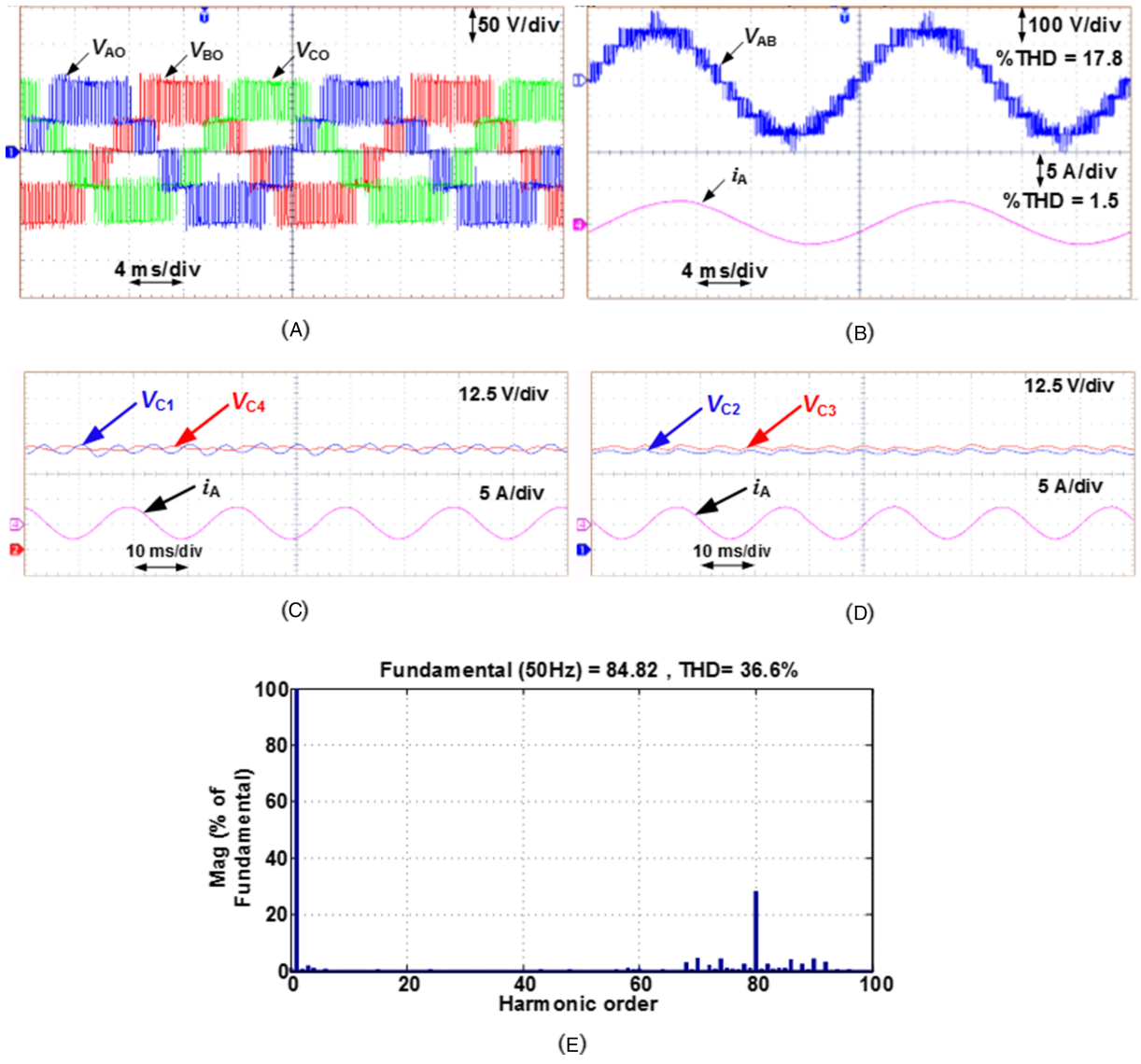

FIGURE 13 Experimental results at $m_a = 0.9$: (A) pole-voltages, (B) V_{AB} and i_A, (C) steady-state capacitor voltages with respect to i_A, and (D) fast Fourier transform spectrum of pole-A voltage [Colour figure can be viewed at wileyonlinelibrary.com]

voltage. The percentage total harmonic distortion (%THD) is 36.6% in the output pole-voltage, and the current THD is 1.5%, which is within the limits of IEEE 1547 grid standard. Moreover, the %THD and the order of harmonics are approximately equal in the simulation and the experimental results. The close agreement between the simulation and experimental results validates the developed prototype.

7.2 | Dynamic performance

The robustness of the proposed configuration and the ability of the VBC in controlling the capacitor voltages are tested by applying various disturbances in the control algorithm. Firstly, Figure 14A,B reveals the load-voltage (V_{AN}) and DC-bus capacitor voltages, respectively, for a load disturbance. It can be observed that V_{AN} remains relatively unaltered with respect to the change in load. The voltage ripple in the capacitors is small except that a small increment in the voltage ripple results when the load is increased. Figure 15A,B demonstrates the pole-voltage, load current, and voltage across capacitors, respectively, for a change in switching frequency (f_{sw}). It reveals that the increase or decrease in f_{sw} has a negligible impact on the operation of the converter. Figure 16A,B depicts

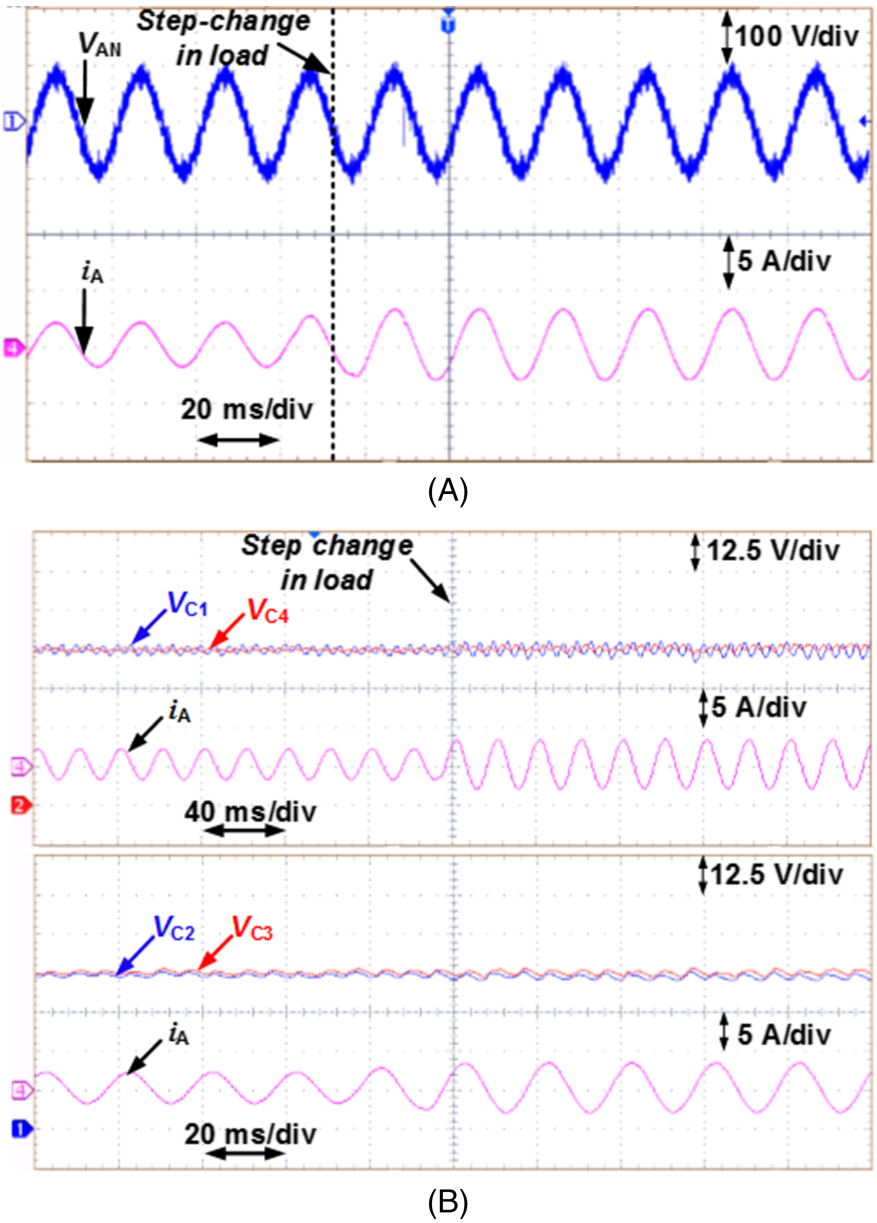

FIGURE 14 Dynamic results for a step-change in load: A, load-voltage (V_{AN}) with respect to load-current (i_A); B, DC-link capacitor voltages (V_{C1}, V_{C2}, V_{C3} and V_{C4}) with respect to i_A [Colour figure can be viewed at wileyonlinelibrary.com]

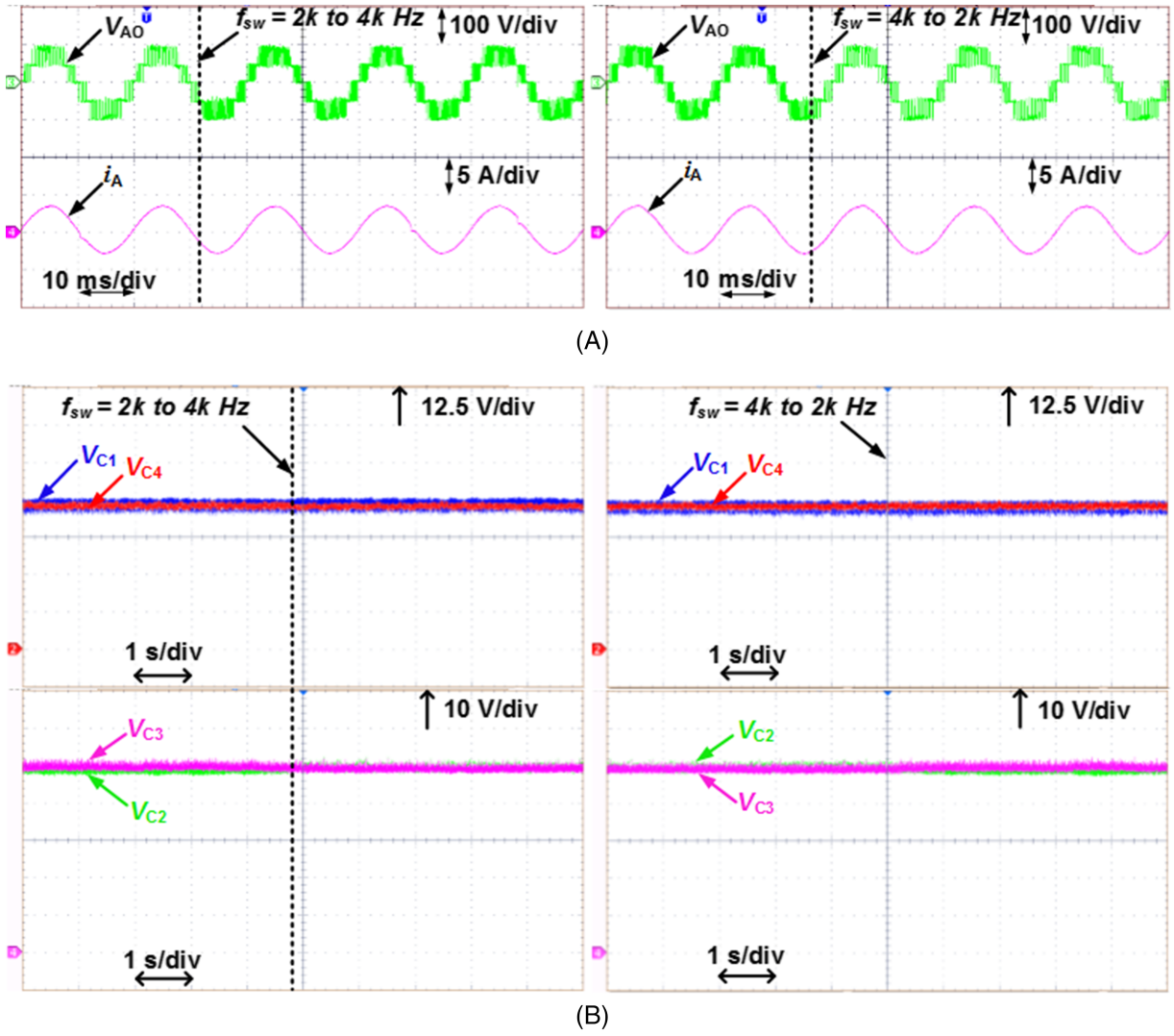

FIGURE 15 Dynamic results for a step-change in switching frequency (f_{sw}): A, pole-voltage (V_{AO}) and load-current (i_A); B, DC-link capacitor voltages (V_{C1}, V_{C2}, V_{C3}, and V_{C4}) [Colour figure can be viewed at wileyonlinelibrary.com]

the pole-voltage, load current, and capacitor voltages, respectively, for a change in the fundamental frequency (f_m). The decrease in f_m causes the increase in capacitor voltage ripple, which in turn affects the quality of the output voltages and currents. Therefore, it is recommended to operate the converter at higher fundamental frequencies to deliver an output of better quality. Finally, Figure 17A,B presents the converter pole-voltage, load current, and voltage across capacitors, respectively, for a change in modulation index (m_a). It is observed that the pole-voltage (V_{AO}) is varying from a 5-L to a 3-: output when m_a is decreased from 0.9 to 0.45. The voltage ripple in C_1 and C_4 decreases with the reduction in m_a, which is due to the reduction in the utilization of C_1 and C_4. Whereas, the voltage ripple in C_2 and C_3 is decreasing due to the decrease in load current. Therefore, it can be concluded that the proposed topology has the ability to tackle several types of disturbances, which verifies the adequacy of its dynamic behavior.

7.3 | Operating under highly inductive load

The performance of the converter and the ability of the VBC are tested during the extreme condition of 0.1 lagging PF load by using a highly inductive load. Figure 18A shows the line-voltage (V_{AB}) and the line-current (i_A)

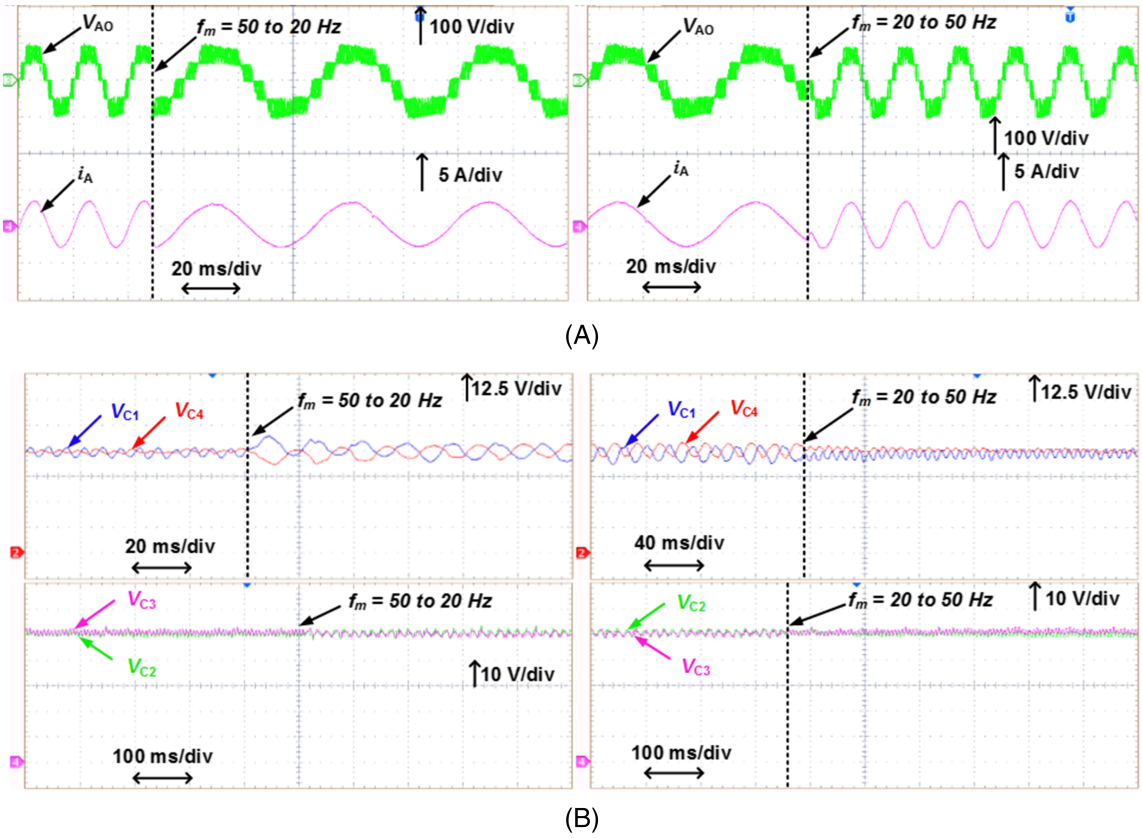

FIGURE 16 Dynamic results for a step-change in fundamental frequency (f_m): A, pole-voltage (V_{AO}) and load-current (i_A); B DC-link capacitor voltages (V_{C1}, V_{C2}, V_{C3}, and V_{C4}) [Colour figure can be viewed at wileyonlinelibrary.com]

during a low PF condition. It is evident that the current waveform is smooth and ripple-free approximating to a pure sinusoidal wave. Figure 18B demonstrates the charging currents of each capacitor during a low PF condition. It also presents the dynamic variations of charging currents when the VBC is switching from the off-state to the on-state. It may be noted that during the instant when the VBC is switched on, the set of currents i_{C1}, i_{C4} and i_{C2}, i_{C3} are increasing in opposite directions, which reduces the current supplied by the source to equalize the capacitor voltages.

8 | EFFICIENCY CALCULATION AND APPLICATIONS

The performance of the proposed MLI is evaluated for different output power conditions. The determination of efficiency from the low-scale prototype model is error-prone and impracticable for comparison on account of more losses at light-load conditions. As a result, simulation work is carried out to assess all losses and efficiency. Figure 19 illustrates the efficiency curves of various power circuit configurations. The efficiency curves for different topologies were plotted using PSIM[32] models by loading various characteristics of the required devices listed in Table 3. The determination of efficiency of all the topologies shown in Figure 19 is performed for an output voltage of 3.4 kV and a rated power of 1 MW. The losses incurred in all of the inverter components, including the losses in the VBC, are computed. It can be observed that a maximum efficiency of 95.8% is achieved in the proposed topology in comparison with the 5L-NPC, 5L-FC, and 5L-HFC MLIs. The higher efficiency in the proposed topology may be attributed to the elimination of clamping diodes and FCs involving high-frequency operated switching devices compared with NPC, FC, and HFC topologies, respectively.

The potential applications of the proposed inverter are listed as follows:

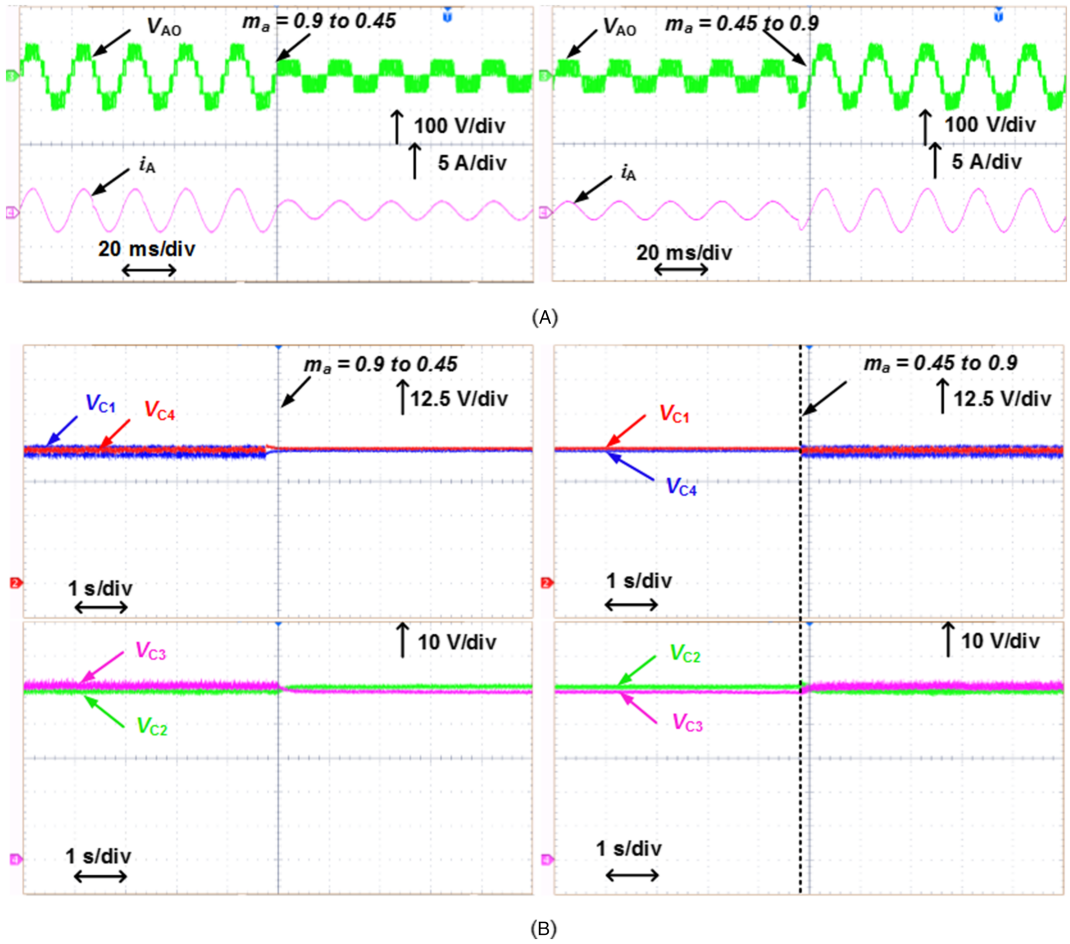

FIGURE 17 Dynamic results for a step-change in modulation index (m_a): A, pole-voltage (V_{AO}) and load-current (i_A); B, DC-link capacitor voltages (V_{C1}, V_{C2}, V_{C3}, and V_{C4}) [Colour figure can be viewed at wileyonlinelibrary.com]

1 The proposed topology has the capability to absorb or deliver the reactive power; hence, it is suitable for Static Var Compensators.[33]
2 The proposed topology can also use solar photovoltaic panels as the DC input to produce AC output from the inverter for grid integration. Hence, the proposed topology is suitable for grid integration of renewable energy sources.[34]
3 The input DC voltage can be scaled to higher values to produce an output voltage of 3.3 kV/6.6 kV, which makes the proposed topology suitable for medium-voltage industrial drives.[16]

9 | CONCLUSION

The presented work proposes a new circuit configuration of a 3-phase 5-L inverter suitable for medium-voltage level applications. This topology has been configured with the combination of half-bridge cells and the T-type structure with the aim of achieving a common DC-link, as well as to eliminate the FCs with reduced device count. The sinusoidal modulation and the voltage balance control schemes are implemented in a Xilinx processor to produce the 5-L output and to balance the capacitor voltages, respectively. The modes of operation, modulation technique, and the working of the balancing circuit of the proposed topology have been addressed in detail. The proposed topology has been compared with the traditional and recently proposed topologies, and its advantages have been explained in detail in terms of component count and other aspects. The viability of the proposed circuit is demonstrated through simulation and experimentation studies under steady-state and dynamic conditions.

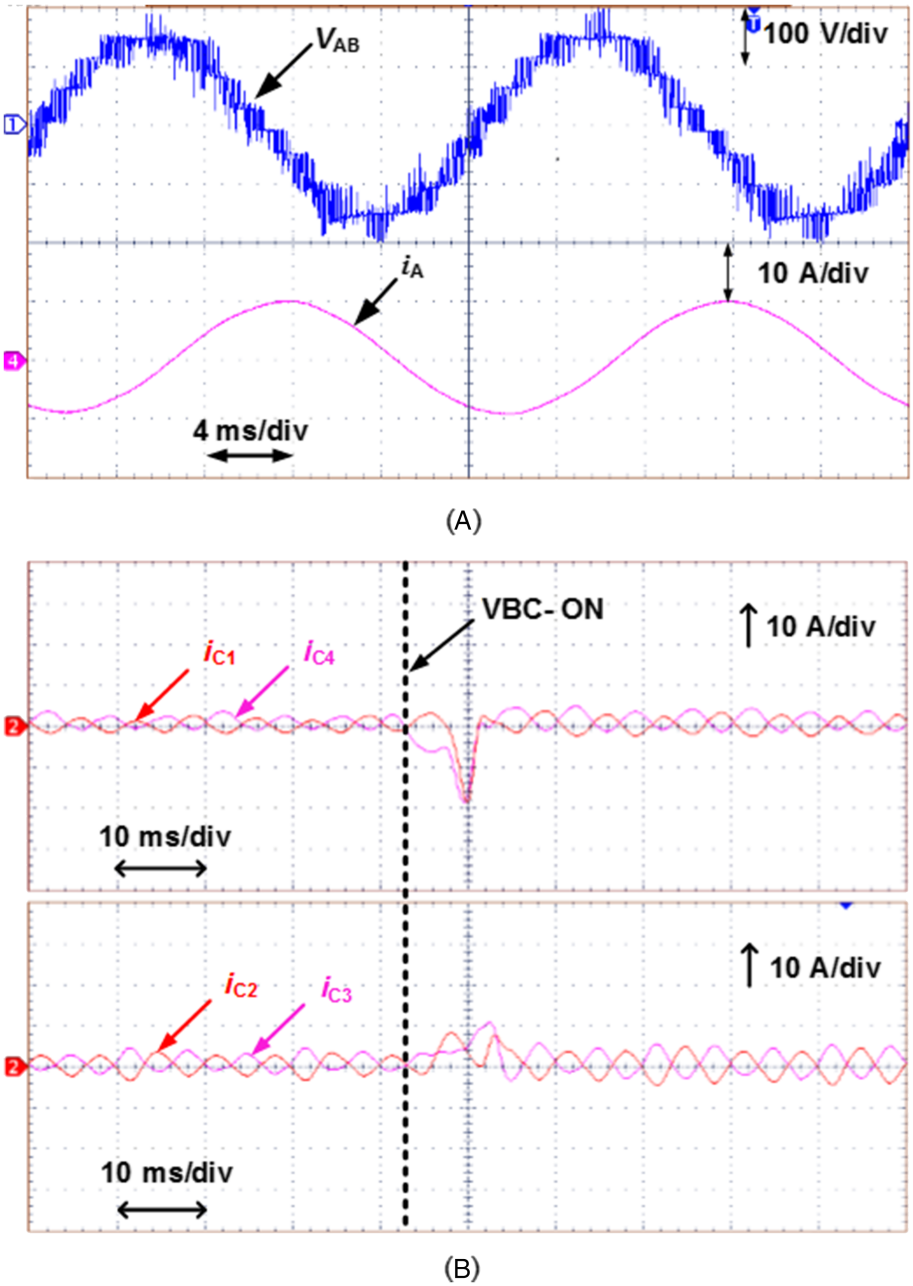

FIGURE 18 Inverter performance under a highly inductive load: A, line-voltage (V_{AB}) and load-current (i_A); B, DC-link capacitor currents (i_{C1}, i_{C2}, i_{C3}, and i_{C4}) [Colour figure can be viewed at wileyonlinelibrary.com]

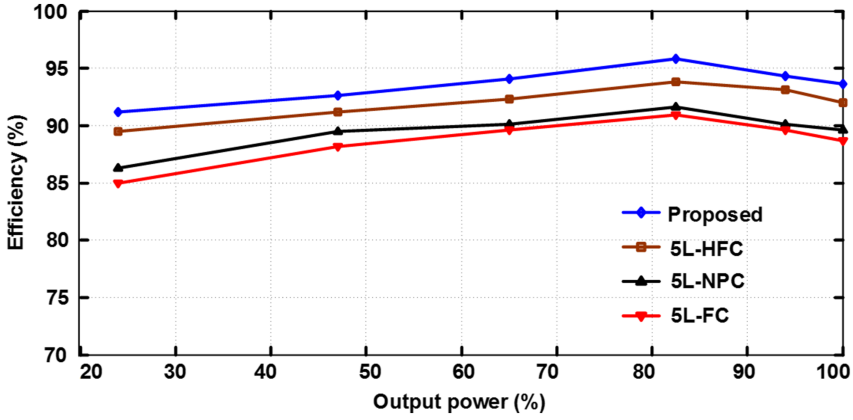

FIGURE 19 Simulated efficiency curves of the proposed and other topologies with respect to percentage output power [Colour figure can be viewed at wileyonlinelibrary.com]

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