Single-Phase Two-Stage Seven-Level Power Conditioner for Photovoltaic Power Generation System

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***Abstract*— This paper presents a new power conditioner with the inherent benefits of boosting, generation of seven-level output voltage with minimum leakage current in a grid-connected photovoltaic (PV) power generation system. The proposed power conditioner is an upgrade of a front-end multioutput dc–dc boost converter and an asymmetrical seven-level inverter. A high-frequency transformer (HFT) employed in front-end converter produces balanced dc-link voltages to generate the seven-level output voltage. The leakage current caused by the parasitic capacitance of the PV panel is minimized by providing a common-mode conducting path to the inverter. This results in a reduction of the leakage current well below the VDE0126-1-1 grid standards. Furthermore, the proposed configuration utilizes a minimum number of devices for every level generation, which reduces the control complexity and also improves the system efficiency. The dynamic performance of the system is tested for intermittent changes in the PV characteristics for grid-connected operation. The proposed power conditioner is simulated using MATLAB software, and a laboratory prototype of 750 W is developed to validate its feasibility. Finally, a comparison is made with other recently proposed seven-level inverters to highlight the benefits of this power conditioner over others.**

***Index Terms*— Common-mode voltage (CMV), dc–dc converter, grid interface, leakage current, multilevel inverter (MLI), power losses.**

I. Introduction

In RECENT years, power generation from photovoltaic (PV) sources has become inevitable due to its inherent advantages of such sources being clean, environment-friendly, and deployable at any location with suitable placement of PV arrays. This has motivated the researchers and policymakers to develop a compact, reduced cost, highly reliable, and efficient grid-connected PV system [1]. Based on the number of power processing stages, PV inverters are classified into single-stage inverter and two-stage inverter. Single-stage three-level inverters are widely popular in industrial and commercial applications because of its higher efficiency and simple structure. However, to meet the grid voltage requirement, more number of PV panels are essential to connect in series, which increases the complexities in maximum power point tracking (MPPT), creates the imbalance in power-sharing due to partial shading, which leads to overheating of nonshaded PV panel and lower safety of operation [2], [3]. Therefore, to avoid the above-mentioned drawbacks, two-stage inverters have become popular with boosting of input dc voltage.

Generally, two-stage inverter comprises front-end dc–dc converter followed by a dc–ac inverter. The front-end dc-dc power converter is used for boosting the PV voltage along with the maximum power extraction followed by a dc–ac inverter, which injects power into the grid. However, some challenges in the two-stage PV inverters, such as high efficiency, reduced filter components, and effective decoupling of the pulsating power delivered to the grid from the PV to minimize the leakage current [4]–[6]. The uncontrolled leakage current leads to the risk of electrical shock, increased power losses, and reduced reliability [7].

Detailed reviews on two-stage PV systems are given in [8]–[11]. Many topologies comprise the nonisolated-type boost converter and half-bridge or full-bridge inverter, but these inverters have the disadvantage of leakage current. To overcome this, the front-end boost converter is developed with a high-frequency transformer (HFT). However, all these two-stage three-level configurations have reduced the efficiency with total power-sharing by isolation transformer or HFT and also require large filter size to lower the total harmonic distortion (THD). Therefore, two-stage multilevel inverters (MLIs) with minimum leakage current are a better alternative to solve the problems associated with the three-level inverters.

The popular MLI configurations are diode clamped, flying capacitor, and cascaded H-bridge inverters [12]. High-frequency transitions in the common-mode voltage (CMV) excite the PV parasitic capacitance, which causes the flow of leakage current from the grid to the PV panel. Usually, variations in CMV depend on the topology structure and modulation technique. Leakage current in the diode clamped and flying capacitor MLIs is zero because of the direct connection of neutral to the negative terminal of PV panel [7], [11]. However, these topologies require higher dc-link voltage and more components to meet grid voltage requirements and to realize multilevel operation.

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Hence, cascaded H-bridge MLIs are attaining popularity to solve the above-mentioned drawbacks; but it requires more number of isolated dc sources and an isolation transformer to provide the galvanic isolation from the leakage current. The cascaded H-bridge inverter can be configured either with symmetric (equal) or with asymmetric (unequal) dc sources. The asymmetrical MLI generates more levels using fewer active semiconductor switches that lead to improvement in efficiency and reduction in cost as compared with traditional MLIs [13]–[15]. In [21] and [22], symmetrical based reduced switch MLIs and packed U cells seven-level inverter are presented. Both of these topologies utilize fewer switches and dc sources to realize multilevel operation in comparison with the traditional inverters. However, these single-stage inverters always buck in nature and demand higher dc-link voltage, which increases the rating of PV and also generates very high leakage current because of more oscillations in the CMV.

In [16], symmetrical seven-level inverter topology with a simple boost converter for grid-connected PV system is reported. The main disadvantages with this topology are more number of components, complexity in capacitor voltage balancing for level generation and requirement of a line frequency transformer (LFT) for isolation; this results in increased complexity, system size, and reduced efficiency. In [18], an asymmetrical seven-level inverter is proposed for PV application, which requires more conducting devices for multilevel operation and also extra passive components to boost the input PV voltage. Similarly, in [19] and [20], two different configurations of asymmetrical seven-level inverter for solar power generation system are presented with new modulation techniques to minimize the power losses due to switching algorithm. Both the topologies are developed with more switching devices, higher switching frequency operations with two-stage conversions to produce seven-level output. The topologies mentioned above are enough for the level generation with the limitations of increased device rating, conduction losses and lower efficiency due to more switches in operation at each level generation. Moreover, the researchers have focused mainly on the level generation but have not addressed the issue of CMV analysis and leakage current.

Therefore, this led to the authors to develop an efficient single-phase two-stage seven-level power conditioner suitable for PV power generation system. It comprises a front-end multioutput boost converter and an asymmetrical six switch MLI with CM filter. The front-end dc–dc converter uses an HFT to balance the capacitor voltages and also only 33% of total power transferred through it; hence, the complexity and power loss of the converter are reduced. Furthermore, an asymmetrical inverter produces seven-level output voltage with six MOSFETs for unity and non-unity power factor (UPF) operations of the grid. Out of six MOSFETs, only three are in conduction at any instant of operation. In addition to that, the operating frequency of the switches is inversely related to blocking voltage. For example, higher blocking voltage switches conduct with grid frequency, while lower blocking voltage switches conduct with switching frequency. Hence, the total switching and conduction loss of inverter switches are reduced. Furthermore, this paper presents an effective solution to minimize the leakage current for the above-mentioned two-stage MLIs below the VDE0126-1-1grid standard; this is done by providing CM path from split capacitor to the negative terminal of PV source. This avoids the use of extra switches and isolation transformer for limiting the magnitude of leakage currents.

The proposed model is built and studied in MATLAB software for grid-connected mode with intermittent changes in PV characteristics under different climatic conditions. An experimental setup is developed for 750 W and the controller for front-end dc–dc converter is implemented using DSP2812 processor in real-time workshop. Spartan-6 field-programmable gate array (FPGA) is also used to generate firing pulses for seven-level inverter operation. The simulation results are validated through experiment to establish a good correlation between them. The detailed organization of this paper is as follows. Sections II and III describe the detailed working principle, control of the proposed power conditioner, and their corresponding CMV analysis. Section IV presents the simulation and experimental validation of the proposed configuration. Section V shows a detailed comparison of various seven-level inverter topologies to prove the merit of the proposed power conditioner. Finally, Section VI presents the concluding remarks.

II. Proposed Power Conditioning System

Fig. 1 depicts the proposed power conditioner, which comprises a front-end dc–dc converter and an asymmetrical MLI. The front-end dc–dc converter boosts the output voltage of the PV source to the grid voltage level and also produces two isolated voltages of (2/3) $V_{\rm dc}$ and (1/3) $V_{\rm dc}$. The switching operation of the complementary switches in the boost converter and HFT ensures proper voltage balancing of the dc-link capacitors. Furthermore, the inverter generates a seven-level output voltage with six semiconductor switches. The *LC* and CM filters are connected across the output of the inverter to limit the variations in CMV, and it will be explained in Section III. The detailed operation of the proposed configuration is as follows.

A. Front-End DC–DC Boost Converter

The front-end dc–dc boost converter is derived from the conventional boost converter in combination with a (2:1 turns ratio) HFT to produce two different dc voltages. The front-end converter is operated in two distinct modes such as boosting mode and current fed forward converter mode to produce (2/3) $V_{\rm dc}$ and (1/3) $V_{\rm dc}$ voltages as shown in Fig. 2(a) and (b). In boost mode inductor L, diode $D1$ and switch $S1'$ are operated to produce a voltage across capacitor $C1$. Similarly, in current fed forward converter mode inductor L, HFT, diodes $D2$, $D3$, and switches $S1$, $S1'$ are operated to charge the capacitor $C2$.

Switches $S1$ and $S1'$ are complementary to each other. When switch $S1$ is off and the complementary switch $S1'$ is on, capacitor $C1$ is connected across the primary of the HFT through diode $D1$ and switch $S1'$ as shown in Fig. 2(b). The stored energy in the inductor and the input PV source charges

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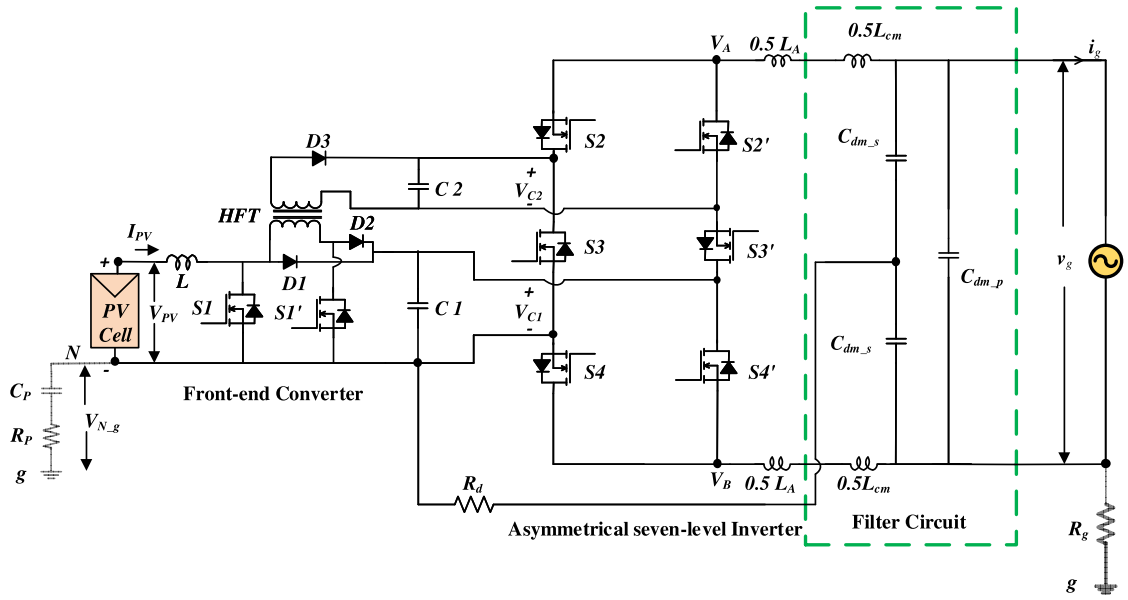

Fig. 1. Proposed single-phase two-stage power conditioner.

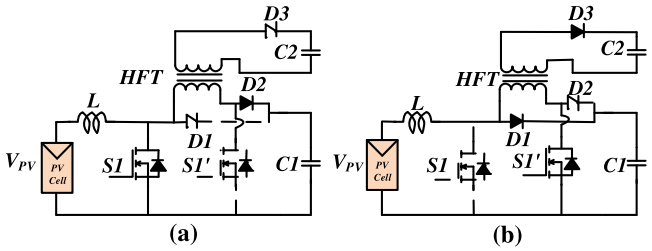

Fig. 2. Operation forward boost converter. (a) S1 is on. (b) S1 is off.

TABLE I
SWITCHING STATES AND CURRENT PATH FOR THE ACHB INVERTER

Modes	Switching Scheme						Source Combination
	S2	*S3*	*S4*	*S2′*	*S3′*	*S4′*	
Positive	1	0	0	0	1	1	V_{C2}
	0	0	1	1	1	0	V_{C1}
	1	0	1	0	1	0	$V_{C1}+V_{C2}$
Zero	0	0	0	1	1	1	*0*
	1	1	1	0	0	0	
Negative	0	1	0	1	0	1	$-(V_{C1}+V_{C2})$
	1	1	0	0	0	1	$-V_{C1}$
	0	1	1	1	0	0	$-V_{C2}$

capacitor *C*1. Since capacitor *C*2 is connected to the secondary of the HFT through diode *D*3, half of the primary voltage is applied to charge capacitor *C*2. Hence, the voltages across the two dc-link capacitors are maintained at V_{C1} and V_{C2}. From Fig. 2(a), when switch *S*1 is conducting, inductor "*L*" stores the energy from the source and magnetizes current in the transformer winding discharges through the capacitor *C*1 and diode *D*2. Since, the stored energy in the magnetizing inductance is transferred to the output capacitors *C*1 and not back to the source, the output power efficiency improves. Moreover, capacitors *C*1 and *C*2 are charged in parallel by using the HFT of the converter, which ensures the voltages to be in asymmetric (2:1) in nature [19]. Moreover, power transferred to the HFT is only 33% of rated power; this reduces the power rating and losses of the HFT. Assuming the converter is operating in continuous conduction mode (CCM), the voltage across the capacitors can be expressed as follows:

$$V_{C1} = \frac{1}{1-D} V_{\mathrm{PV}} \tag{1}$$

$$V_{C2} = \frac{1}{2*(1-D)} V_{\mathrm{PV}}. \tag{2}$$

B. Asymmetrical Seven-Level Inverter

In this paper, to realize the seven-level output, a popular asymmetrical MLI reported in [21] and [22] is considered. It consists of six active switches *S2, S2′, S3, S3′, S4′*, and *S4′*. Switches *S2′*, *S3′*, and *S4′* are complementary to switches *S*2, *S*3, and *S*4, respectively. Therefore, three independent states would give ($2^3 = 8$) eight active states. The asymmetrical seven-level inverter is fed with voltages V_{C1} and V_{C2} that are generated from the multioutput dc–dc boost converter. In any of the switching state, three switches are in conduction to realize the output ac voltage. Table I shows different switching states corresponding to each level generation. The voltage blocking capability of the switch pairs (*S*2, *S2′*), (*S*3, *S3′*), and (*S*4, *S4′*) is V_{C2}, $(V_{C1} + V_{C2})$, and V_{C1}, respectively. The control pulses to the inverter switches are produced using the sinusoidal-level shifted pulsewidth modulation (SLSPWM) technique.

C. Closed-Loop Control System

The development of suitable controller plays a major role in extracting maximum power from the PV source into grid. The basic functions of the controller are MPPT from PV, dc-link voltage balancing, generation of seven-level output voltage, and injecting current into the grid. Hence, two control loops are developed with proportional–integral (PI) and proportional–resonant (PR) controllers [23], [24]. The voltage control is performed by the outer loop PI controller,

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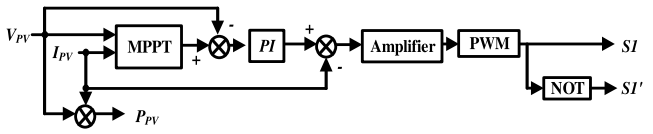

Fig. 3. MPPT control block.

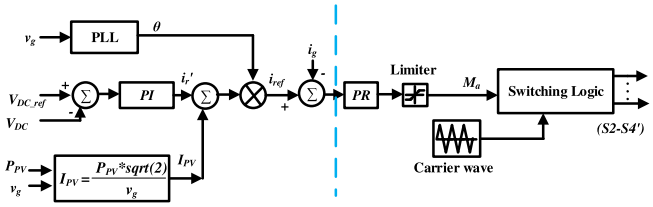

Fig. 4. Closed-loop control of inverter.

while the current control is achieved by the inner loop PR controller. Thus, the overall controller facilitates the regulation of intermittent variations in PV characteristics.

A simple perturb and observation (P and O) algorithm is used to extract the maximum power from the PV panel [25]. An inner loop current control and outer loop voltage control are developed to limit the inductor current ripple and capacitor voltage ripple, respectively, to improve the performance of MPPT with multioutput boost converter, as shown in Fig. 3. Furthermore, to inject generated PV current into grid by preserving constant dc-link voltage, a two loop controller is developed and is shown in Fig. 4. The dc-link voltage control gives the reference grid current and then improved PR controller generates the modulation index M_a, which is further fed to SLSPWM logic block to produce the switching pulses for inverter switches as shown in Table I. An improved PR controller [24] is used for injecting current into grid. It has the advantages of limiting the steady-state error and is also robust in the control of inverter voltage due to parameter variations. Thus, improved PR controller performance is far better when compared with the PI controller. Phase locked loop (PLL) circuit is used to generate in-phase current to grid voltage. The transfer function of PI and improved PR controller are given as follows:

$$G_{\mathrm{PI}}(s) = K_P + \frac{K_I}{S} \tag{3}$$

$$I_{\mathrm{PV}} = \frac{P_{\mathrm{PV}} * \sqrt{2}}{v_g} \tag{4}$$

$$G_{\mathrm{PR}}(s) = K_P + \frac{2K_r\omega_{\mathrm{PR}}s}{s^2 + 2\omega_{PRc}s + \omega_1^2}. \tag{5}$$

Furthermore, to show the closed-loop controller performance, the proposed power conditioner and its controller are developed in MATLAB environment for a maximum PV power capacity of 1.26 kW, and a simple P and O MPPT algorithm is used to track the maximum power from the PV source. The specifications considered for the PV source are as follows: voltage, current, and power at maximum power $V_{\mathrm{MP}} = 19.2$ V, $I_{\mathrm{MP}} = 3.64$ A, and $P_{\mathrm{MP}} = 70$ W, respectively. A total of three parallel rows of six panels are connected in series ($N_S = 6$, $N_P = 3$) to generate the power of 1.26 kW at a

TABLE II
SYSTEM PARAMETERS

Parameters	Specification
Power (P)	750 W
DC-link voltage (V_{dc})	380 V
AC output voltage (V_{load})	230 V
Fundamental frequency (f)	50 Hz
Switching frequency (f_s)	20 kHz
Inductors (L_A, L_{cm}, L)	2 mH, 2 mH, 3 mH
Capacitors (C_{dm_s}, C_{dm_p}, C_{DC_s}, C_p)	1 µF, 2 µF,1000 µF, 21 nF
Resistors (R_d, R_g, R_p)	2.2 Ω, 10 Ω, 2.2 Ω
High frequency transformer	Core type: ETD 42/21/15 Magnetizing inductance (L_m): 8.2 mH Leakage inductance referred to primary: 66 µH Turns ratio: 2:1

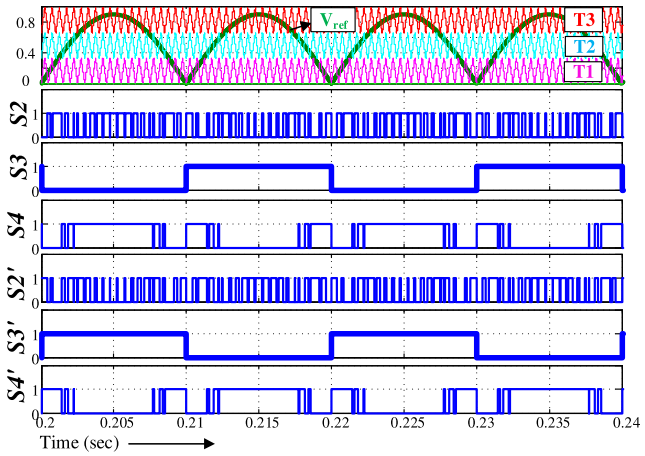

Fig. 5. Simulation waveforms of SLSPWM and corresponding gate pulses to the inverter switches.

standard temperature of 25 °C and insolation of 1000 W/m^2. Various details of the parameters considered for simulations are given in Table II and the design of LC and CM filter is given in [8] and [26]. Fig. 5 shows the gate pulses generated by SLSPWM technique for driving the inverter switches. To inject active power (P) into the grid, the inverter produces a voltage V_r having a phase and the same is given in (6) and (7). In the case of $P = 1.26$ kW, $V_{\mathrm{ac}} = 230$ V, $(L_f + L) = 5.25$ mH, $R = 0.1$ Ω, $V_r = 230.54$ V, $\delta = 0.039$ in radians [28]

$$\delta = \arctan\left(\frac{2\pi f(L_f + L)P}{V_{\mathrm{ac}}^2 + \mathrm{RP}}\right) \tag{6}$$

$$V_r = \left(V_{\mathrm{ac}} + \frac{\mathrm{RP}}{V_{\mathrm{ac}}}\right)\frac{1}{\cos\delta}. \tag{7}$$

Fig. 6 shows the simulation results of the proposed seven-level power conditioner with closed-loop control. Fig. 6(a)–(j) shows the waveforms corresponding to insolation changes from 1000 to 800 W/m^2 and vice versa. Fig. 6(a) and (f) shows the PV power versus voltage characteristics for various insolation changes. The variations in output PV power and the corresponding dc-link voltages are depicted in Fig. 6(b) and (g) and (c) and (h), respectively. It can be noted that the capacitor voltages of front-end dc–dc converter are maintained constant despite changes in the input voltage of

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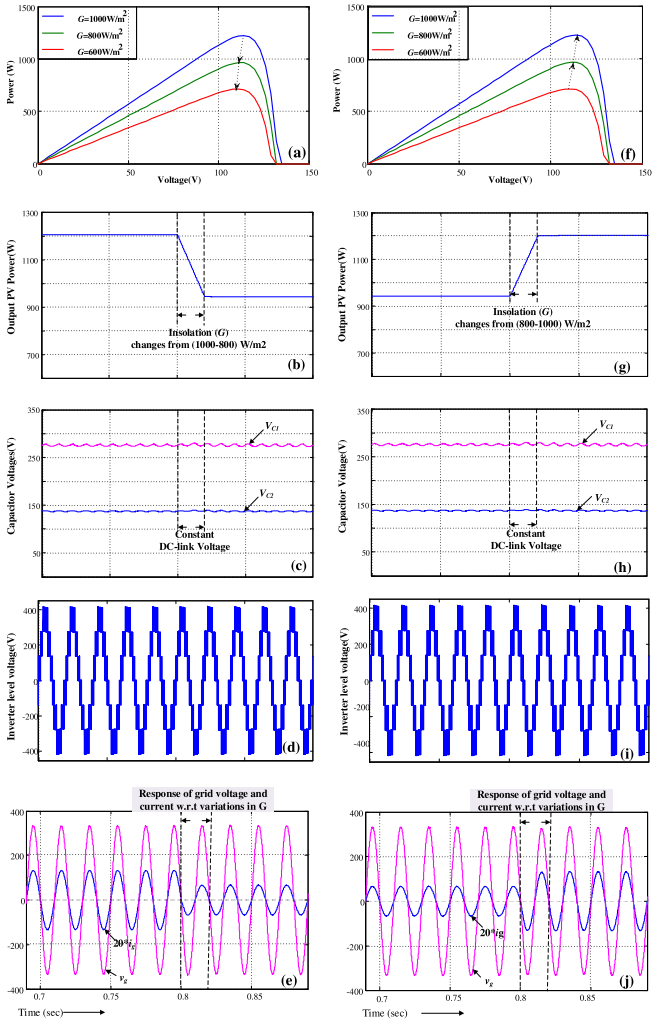

Fig. 6. Simulation results of the proposed power conditioner integrated with closed-loop control when input insolation varies from 1000 to 800 W/m^2 and vice versa. The subplot gives the waveforms of (a) and (f) PV characteristics, (b) and (g) output PV power, (c) and (h) balanced dc capacitor voltages, (d) and (i) seven-level output voltage of asymmetrical MLI, and (e) and (j) grid voltage and injected current.

the PV source due to insolation variations. The seven-level inverter output voltage, filtered output voltage, and phase current waveforms for UPF operation of the grid are given in Fig. 6(d) and (i) and (e) and (j), respectively. The variation of grid current at the constant voltage for insolation changes can be observed clearly in Fig. 6(e) and (j), which shows that the developed power conditioner and the closed-loop controller effectively inject power into the grid for intermittent changes in PV characteristics. For better visibility of the grid current waveforms shown in Fig. 6(e) and (j) are scaled to 20 times. In addition, Fig. 7 depicts the %THD of grid current as 2.39% at 800 W/m^2 PV insolation and it is within the limits of IEEE 1547 grid standard.

III. Leakage Current Analysis

One of the major issues in grid-connected PV inverter is the leakage current generated by the PV parasitic capacitors due to variations in CMV. To address the leakage current in

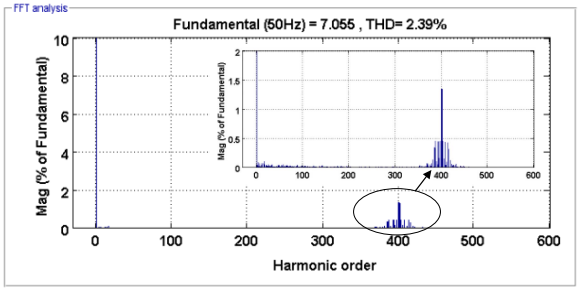

Fig. 7. Fast Fourier transform (FFT) spectrum of grid current.

the proposed converter, a passive LC filter and a CM choke are employed at the inverter side. The effect of variations in the CMV can be evaluated by generated CM and differential mode (DM) terminal voltages, which are defined in(8) and (9). V_{AN} and V_{BN} are the terminal voltages of the inverter with respect to the negative terminal of the PV source, as shown in Fig. 1

$$V_{\mathrm{DM}}(\omega) = [V_{\mathrm{AN}}(\omega) + V_{BN}(\omega)] \tag{8}$$

$$V_{\mathrm{CM}}(\omega) = 0.5[V_{\mathrm{AN}}(\omega) + V_{BN}(\omega)] \tag{9}$$

where V_{CM} and V_{DM} are CM and DM voltages, respectively. Generally, the variations in CMV are determined based on the topology and the control strategy. In this system, the CMV is associated with switching frequency as well as grid frequency variations. The switching frequency variations in CMV occur when there is a transition from one voltage level to another voltage level. The grid frequency variations in CMV occur during the transition between the positive half cycle to the negative half cycle. The midpoint of the split capacitors is connected to the negative terminal of the dc bus through a damping resistor R_d to provide a conducting path to CM current as shown in Fig. 1 [27]. Due to the symmetrical nature of the filter inductor, there is no effect on active and reactive power flows.

Furthermore, to analyze the CM characteristics of the asymmetrical MLI, an equivalent circuit is illustrated in Fig. 8(a) L_{CM} is the CM choke, $C_{\mathrm{DM\_}P}$ and two split capacitors $C_{\mathrm{DM\_}S}$ are used in the DM capacitor stage, $C_{\mathrm{dc\_}S}$ split dc-link capacitors, R_P and C_P are the parasitic elements of the PV source to ground, and R_g is the ground resistance. Fig. 8(b) depicts the simplified CM equivalent circuit for easy analysis of CMV and leakage current behavior.

In the simplified model, the passive components $C_{\mathrm{dc\_}S}$ and $C_{\mathrm{DM\_}S}$ and a small damping resistor R_d are added in series to the CM path. From Fig. 8(b), the effect of CMVs on PV source negative terminal V_{N_g} can be determined by (10). The resonant frequency ω_r of LC components is $(0.5L_A + L_{\mathrm{CM}})$ and $(2C_{\mathrm{DM\_}S} \,//\, 2C_{\mathrm{dc\_}S})$. Usually, the value of ω_r is higher than the ripple frequency (100 Hz) and much lower than switching frequency; thus, (10) can be simplified as (11). Smaller ω_r leads to higher attenuation to the CMV (V_{CM}). The CM path provided by the filter circuit attenuates variations in the CMV as per (12). The grid frequency variation in CMV causes a small spike in the leakage current. Hence, the rms value of the leakage current corresponding to grid frequency

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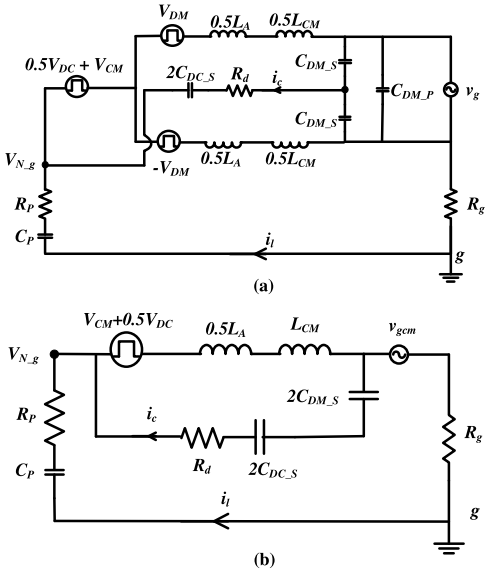

Fig. 8. (a) CM equivalent circuit. (b) Simplified CM equivalent circuit.

variations is very low in comparison with switching frequency variations. Voltages $V_{\rm dc}$, $V_{\rm ripple}$, and $V_{\rm gcm}$ have low effect on the PV terminal voltage due to lower operating frequencies. Moreover, additional CM noise current i_c, which is generated and circulated in the CM path provided by the ac filter, is shown in Fig. 8(a). From Fig. 8(b), this CM noise current can be calculated as per (13)

$$V_{N\_g} = \frac{-(V_{\rm CM}+0.5V_{\rm dc})}{1-\omega^2(0.5L_A+L_{\rm CM})(2C_{\rm DM\_S}//2C_{\rm DC\_S})}+V_{\rm gcm}$$

$$V_{N\_g} = \frac{-(V_{\rm CM}+0.5V_{\rm dc})}{1-\frac{\omega^2}{\omega_r^2}}+V_{\rm gcm} \tag{10}$$

$$V_{N\_g} = \frac{-V_{\rm CM}(\omega)}{1-\frac{\omega}{\omega_r^2}}-0.5V_{\rm dc}-0.5V_{\rm ripple}+V_{\rm gcm} \tag{11}$$

$$\text{Atten}(\omega) = 20\log_{10}\left(\left|1-\frac{\omega^2}{\omega_r^2}\right|\right). \tag{12}$$

It shows that i_c is mainly decided by: 1) switching frequency components (ω) and grid frequency component; 2) resonant frequency component (ω_r); and 3) twice the grid frequency (100 Hz) component. Since ω_r is much smaller than ω, almost all the high-frequency noise is applied to $L_{\rm CM}$. Therefore, a factor $k(\omega)$ as given in (14) is applied to $V_{\rm CM}$, so that the total variations in V_{N_g} are minimized. Furthermore, (15) shows that the leakage current flows in the parasitic elements of the PV source. Finally, the magnitude of leakage current can be effectively limited by an additional CM filter. The filter circuit does not introduce extra components, but it restructures passive components of ac. Thus, inverter operation and reliability are guaranteed

$$i_c = V_{\rm CM}(\omega)*k(\omega)+0.5V_{\rm ripple}*k(2\pi*100) \tag{13}$$

$$k(\omega) = \frac{\omega}{1-\frac{\omega^2}{\omega_r^2}}(2C_{\rm DM\_S}//C_{\rm DC\_S}) \tag{14}$$

$$i_l = C_{\rm PV}\frac{{\rm d}V_{N\_g}}{dt} \tag{15}$$

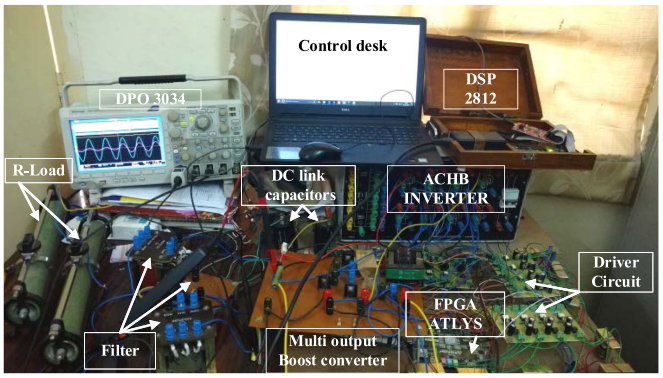

Fig. 9. Experimental prototype for the proposed power conditioner.

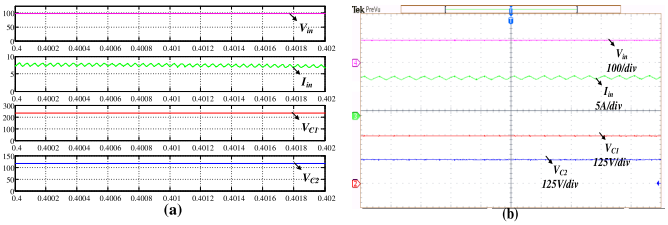

Fig. 10. Input voltage, current, and dc-link voltage waveforms of (a) simulation and (b) experiment.

IV. Simulation and Experimental Setup

In this section, simulation and experimental results are presented and they are given side by side to validate the feasibility of the proposed topology. The fabricated experimental setup with various components is shown in Fig. 9. Various parameters considered for the simulations and experimental setup are given in Table II, and the design of *LC* and CM filter is given in [8] and [26]. The experimental setup is developed using IRFP460 MOSFETs, MUR1560 diodes, copper-based printed circuit board (PCB), and connecting wires as per the availability in lab. The PWM pulses required for the boost converter and asymmetrical inverter are generated with the use of DSP2812 processor and DIGILENT ATLYS Spartan-6 FPGA board, respectively. TLP250-based driver circuit is used for driving the MOSFETs. A regulated dc power supply is used as an input source to the front-end boost converter. The output of the asymmetrical MLI is connected to load resistance through *LC* and CM filter. To measure the leakage current, parasitic capacitance C_P in series with R_P is connected at node *N* as shown in Fig. 1. The waveforms are captured using DPO3034 with the help of current probe TCP0030 and differential voltage probe TMDP0200.

From Fig. 10, it is observed that the input voltage is 96 V and the input current of the multioutput boost converter is continuous in nature; which confirms that the conduction mode of operation is continuous and also the voltages across capacitors *C*1 and *C*2 are balanced and preserved corresponding to the turns ratio (2:1) of HFT. It is essential to deal with high penetration of power into grid and reactive power capability in the future PV inverters [28]. Therefore, a newly designed inverter should allow the reactive power flow without affecting

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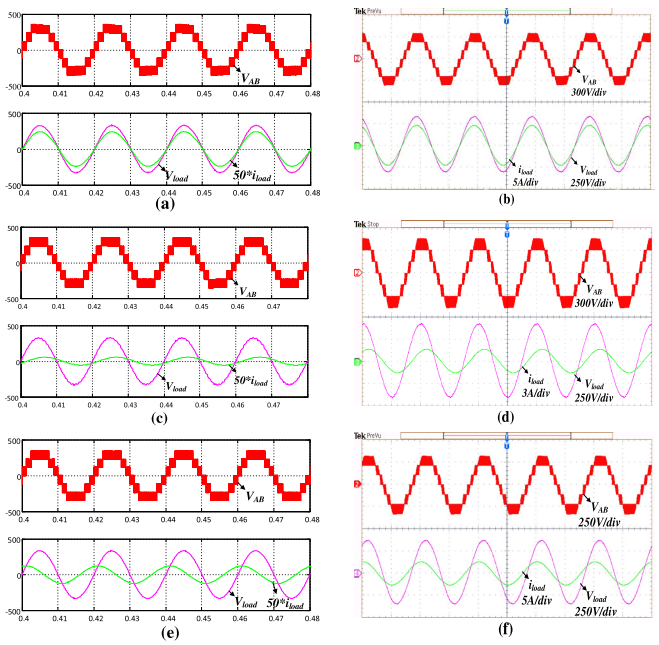

Fig. 11. Simulation and experimental results of seven-level voltage, load voltage, and current. (a) and (b) UPF. (c) and (d) (0.9) Lagging power factor. (e) and (f) (0.9) Leading power factor.

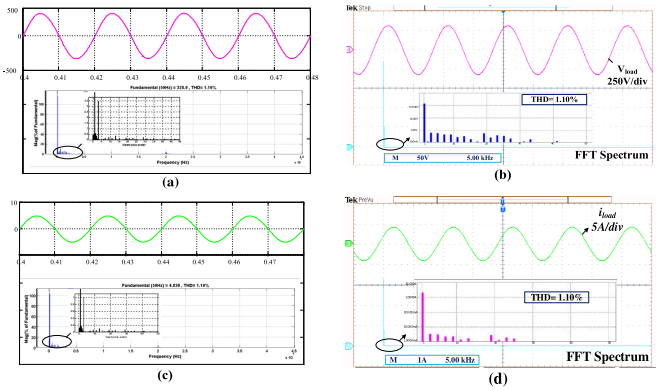

Fig. 12. Simulation and experimental FFT spectra for UPF operation. (a) and (b) Load voltage. (c) and (d) Load current.

the levels in the output. From Fig. 11, it is noted that the waveforms of seven-level voltage, load voltage, and current for unity, 0.9 lagging power factor (200 Ω, 300 mH), and 0.9 leading power factor (135 Ω, 50 μF) loads, respectively; it is evident that the proposed power conditioner and its modulation scheme suitable for both real and reactive powers.

The experimental THD of load voltage and currents is measured using DPO3034 and YOKOGOWA WT310E digital power analyzer, as given in Fig. 12. The measured %THD of the filtered output voltage and current is 1.10%, which is well below the IEC61000-3-2 standard [29]. Fig. 13(a) and (b) illustrates the simulation and experimental results of the inverter terminal voltages (V_{AN}, V_{BN}) and CMV (V_{CM}). It is observed that the CMV has both switching and grid frequency variations. In order to eliminate the switching frequency components and to reduce the leakage current magnitude below the grid standards, a CM filter is connected across the terminal of

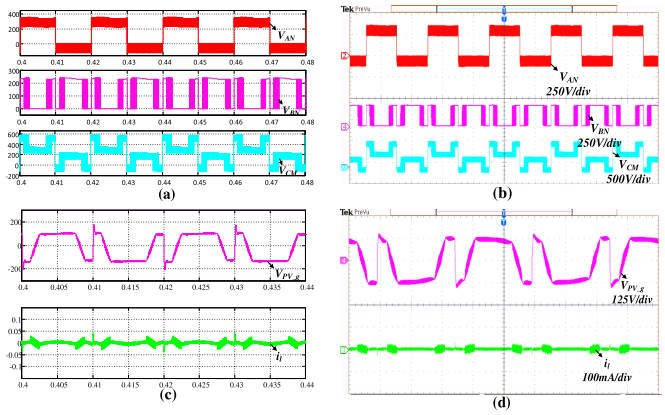

Fig. 13. Simulation and experimental waveforms of the (a) and (b) terminal voltages V_{AN}, V_{BN}, and V_{CM} and (c) and (d) V_{N-g} and leakage current.

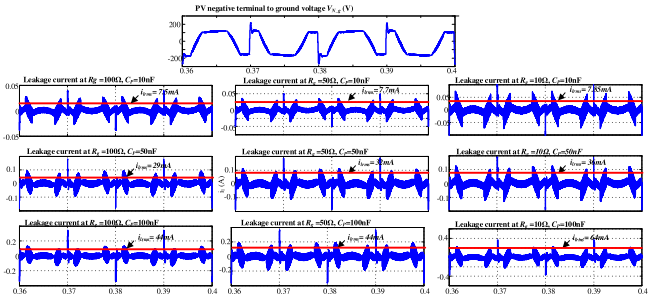

Fig. 14. Simulation results of V_{N-g} and leakage current.

the inverter, which forms a low-pass filter circuit as explained Section III. Fig. 13(c) and (d) depicts the measured waveforms of PV terminal voltage and leakage current in both simulation and experimentation, it is observed that high-frequency voltage transitions in V_{N_g} are attenuated and the rms magnitude of leakage current is limited to 14 mA, which indicates the effectiveness of the proposed power conditioner along with CM filter.

Furthermore, to demonstrate the practical limitation of the leakage current, three different grounding resistances and parasitic capacitances are considered as per [30] to evolve the leakage current magnitude. From Fig. 14, it is noted that in all nine cases, the rms leakage current magnitude does not exceed VDE 126-1-1 grid standards. Therefore, the proposed topology along with the CM filter is effective in limiting the leakage current.

Fig. 15 illustrates the comparison of leakage currents and the corresponding PV terminal voltages for different configurations presented in [18]–[20]. The simulation study for all the configurations is carried out for the same conditions as given in Table II. Based on the configuration and PWM control strategy, the PV terminal to ground voltage V_{N_g} contains switching frequency or grid frequency or both of different amplitudes. From Fig. 15(a), it is noted that V_{N-g} of the configuration reported in [18] contains only grid frequency variations of two different amplitudes; hence, the resultant value of rms leakage current is 38 mA. Fig. 15(b) and (c) depicts V_{N-g} and i_l of the configurations reported in [19]

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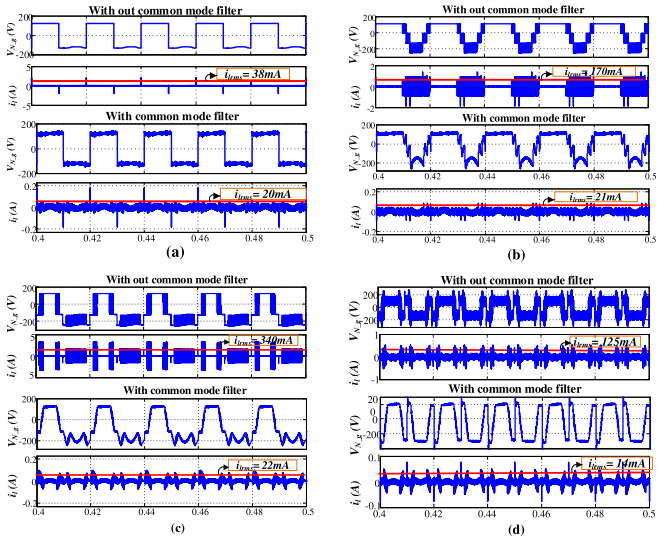

Fig. 15. Comparison of V_{N_g}, leakage current i_l, and its rms value without and with CM filter. (a) Reference [18]. (b) Reference [19]. (c) Reference [20]. (d) Proposed topology.

and [20]. It is noted that both switching frequency and grid frequency variations of four different amplitudes are present in V_{N-g}, which result in the leakage current of 170 and 340 mA, respectively. From Fig. 15(d), it is observed that V_{N-g} of the proposed power conditioner consists of both switching and grid frequency variations of three different amplitudes; hence, the resultant value of rms leakage current is 125 mA.

All these inverters with such leakage currents are not feasible for PV applications directly without providing isolation. Therefore, a CM filter is connected across terminals of the inverter by employing CM path from split capacitor to the negative terminal of PV source for attenuating high-frequency variations in the CMV as explained in Section IV. Hence, the leakage current is reduced to 20, 21, and 22 mA for the topologies reported in [18]–[20], respectively, as shown in Fig. 15. However, the proposed power conditioner has a leakage current of 14 mA. In addition to that, the overall component count and cost of the proposed power conditioner are low and the efficiency is more as compared with other topologies. Therefore, from the above discussion, it can be emphasized that the proposed power conditioner along with CM filter limits the leakage current well below the grid standards with lower component count and higher efficiency for unity and non-UPF conditions.

Furthermore, the dynamic performance of the proposed power conditioner is tested to ascertain the intermittent changes in PV characteristics. Thus, a simple PI controller is used to maintain constant dc-link voltage by regulating the duty cycle of the switches $S1$ and $S1'$, despite variations in the input voltage and load current. The closed-loop control of the front-end converter is evolved with DSP2812 processor using embedded code generation tool in MATLAB. The capacitor voltages are in the ratio of 2:1 with the HFT, and hence, the control of $C1$ voltage automatically regulates the total dc-link voltage. To maintain the dc-link voltage of 350 V, capacitor voltage $C1$ is sensed and compared with

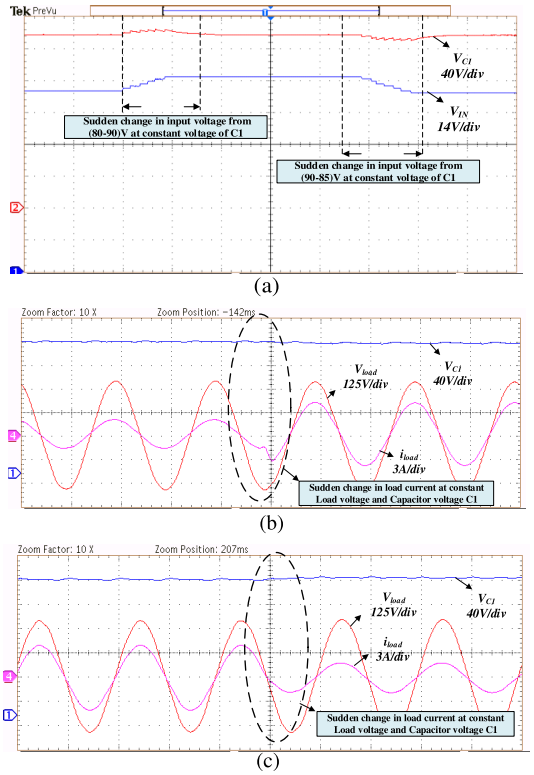

Fig. 16. Experimental waveforms of (a) capacitor voltage (V_{C1}) with respect to changes in input voltage and (b) and (c) load voltage, capacitor voltage (V_{C1}) response with respect to step change in load.

a set reference value of 230 V; then the error is fed to the PI controller, which produces the required duty ratio. For generating the driving pulses to switches $S1$ and $S1'$, the duty ratio is compared with a triangular wave of frequency 20 kHz. Fig. 16(a) shows the constant capacitor voltage $C1$ despite changes to the input voltage from 80 to 90 V and then to 85 V. It can be noted that the capacitor voltage $C1$ reaches steady state immediately after a slight deviation during the transitions in input voltage. From Fig. 16(b) and (c), it is evident that the output voltage and capacitor voltages are maintained constant for a step change in load current by 40%. From the above discussion, it can be concluded that the dynamic performance of the proposed power conditioner is capable of feeding the power into the grid under intermittent changes of PV characteristics.

V. Evaluation of Losses and Comparisons

This section deals with the evaluation of losses and comparisons of different two-stage seven-level PV inverters to highlight the merits of the proposed system. The losses are calculated using steady-state equations referred in [31]–[34], and PSIM thermal module simulations have also been performed to validate the losses obtained. Based on the ON-state resistance and blocking voltage, various switches and diodes selected for the evaluation of losses and they are given in Table III. The expressions used for the calculation of switching and

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TABLE III
SELECTION OF SWITCHES AND DIODES

Device	Part number	Rating
MOSFET	FCA76N60N	400V/76A
	IRF300P227	300V/50A
	IRFP4127PbF	250V/75A
Diode	RUR1S1560S	600V/15A

conduction losses of the MOSFET are as follows:

$$P_{\mathrm{SW\_}I} = \frac{1}{2\pi}\frac{V_b(t_{\mathrm{ON}}+t_{\mathrm{OFF}})}{2T_c}\int_{\theta_{S2}}^{\theta_{S1}}|i_L|d\theta \tag{16}$$

$$P_{\mathrm{SW\_}B} = \frac{1}{2}\mathrm{I}V_b(t_{\mathrm{ON}}+t_{\mathrm{OFF}})f_{\mathrm{SW}} + \frac{1}{2}C_{\mathrm{oss}}V_b^2 f_{\mathrm{SW}} \tag{17}$$

$$P_C = \frac{1}{2\pi}\int_0^{\pi} i(t)V_{\mathrm{SW}}(t)d_{\mathrm{SW}}(t)d(\omega t) \tag{18}$$

where $P_{\mathrm{SW\_}I}$ and $P_{\mathrm{SW\_}B}$ are the switching losses of MOSFET for inverter and front-end boost converter, respectively. V_b denotes the blocking voltage of the switch, T_c, t_{ON}, and t_{OFF} denote inverter switching period and operating times of the switches, θ_{S1} and θ_{S2} are angles of the starting and the ending of an interval with switching losses, $|i_L| = i_{\max}M_a \sin\theta$, M_a is the modulation index, $i_{\max}$ is the maximum load current. I, C_{oss} are the average current and output capacitance. Where P_C is the conduction loss of the MOSFET, $i(t) = I_M \sin\omega t$, $v_{\mathrm{SW}}(t) = i(t)R_{ds}$, $d_{\mathrm{SW}}(t) = M_a \sin\omega t$. The expressions used for the calculation of conduction and reverse-recovery losses of the diodes are as follows:

$$P_{C\_D} = \frac{1}{2\pi}\int_0^{\pi} i(t)V_d(t)D_{\mathrm{diode}}(t)d(\omega t) \tag{19}$$

$$P_{d\_\mathrm{SW}} = \frac{1}{2\pi}\int_0^{\pi} (0.5V_{bd})(0.5I_{\mathrm{rr}})f_s t_b d(\omega t) \tag{20}$$

P_{C_D} and P_{d_sw} denote the conduction and reverse-recovery losses in diode, respectively. Where $i(t) = I_M \sin(\omega t)$, $V_d(t) = V_f + i(t)R_{ak}$, $D_{\mathrm{diode}}(t) = 1\text{--}M\sin(\omega t)$, V_f is the voltage drop in diode under off condition, R_{ak} is the ON-drop resistance, V_{db} is the blocking voltage of the diode, I_{rr} is the reverse-recovery current and t_b is turn-off time of the diode. Table IV elaborates the operation of switches in various seven-level inverter topologies for grid-connected PV systems. It has been observed that the proposed topology has least component count and the number of switching devices at each output level generation is low, which results in high efficiency of the proposed topology compared to other topologies. Fig. 17 depicts a comparison of the blocking voltage of each switching device used in various inverters. Fig. 18 illustrates the comparison of loss distribution among various components for different MLI configurations.

From Fig. 18, it is clearly evident that the efficiency of the proposed two-stage configuration is higher in comparison with other recently proposed topologies presented in [18]–[20]. The power transferred by HFT is less than the one-third of the total output of the PV source in all the above-mentioned topologies. Hence, the degradation of power efficiency with the use of HFT is not a serious problem. In order to validate the

TABLE IV
OPERATION OF VARIOUS SWITCHES IN DIFFERENT TOPOLOGIES

S.No	Reference number	I	II		III		IV		V		VI	
			S	D	P	N	P	N	P	N	P	N
1	Ref [18]	4	9	3	14	14	3	3	2	2	4	4
2	Ref [19]	3	8	5	15	15	6	6	0	0	2	2
3	Ref [20]	4	10	3	15	15	6	6	0	0	2	2
4	Proposed Topology	3	8	3	13	13	4	4	2	2	2	2

I – Number of switches and diodes in conduction during freewheeling period
II – Total number of devices used in the given topology
S -switches; D -Diodes
III – Number of diodes and switches in conduction during one cycle of two-stage system
P- Positive cycle; N- Negative cycle
IV – Number of switches operating at higher switching frequency loss of the two-stage system
V – Number of switches operating at medium switching frequency loss of the two-stage system
VI – Number of switches operating at lower switching frequency loss of the two-stage system

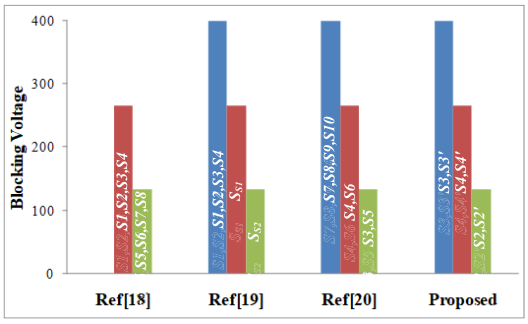

Fig. 17. Blocking voltages of the switches used in various MLI topologies.

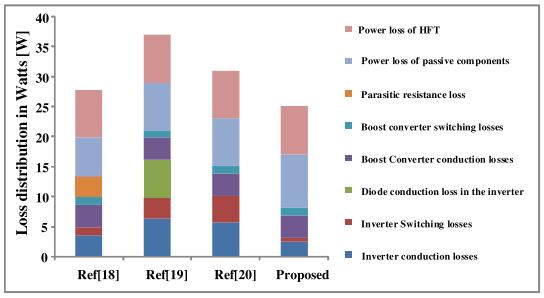

Fig. 18. Loss distribution in various topologies at 750 W of output power.

theoretical losses, a PSIM thermal module is developed and simulated at various loading conditions. The PSIM thermal module enables a quick way of estimating the switching and conduction losses of semiconductor switches based on real device characteristics [35], [36]. Finally, Fig. 19(a) and (b) depicts the efficiency curve of the proposed power conditioner based on theoretical and PSIM thermal module analysis. Both the results are very close to each other and also it is noted that a slight increase in efficiency of the configuration for the input voltage changes from 80 to 100 V. This ensures that the efficiency of the proposed configuration is more than 90% at different input voltages. Furthermore, detailed comparisons with the existing two-stage seven-level inverters are given

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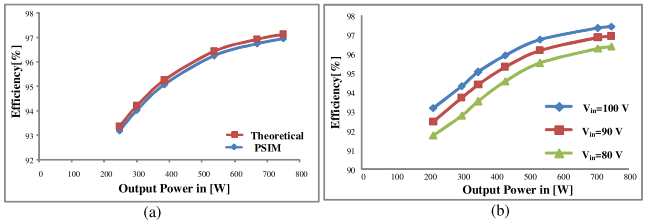
TABLE V
COMPARISON OF DIFFERENT SEVEN-LEVEL INVERTER TOPOLOGIES

Parameter		Ref [16]	Ref [18]	Ref [19]	Ref [20]	Proposed
MOSFETS	LF	2	4	2	2	2
	OLF	5	5	6	8	6
Diodes		9	3	5	3	3
DC capacitors		3	2	2	2	2
HFT		-	1	1	1	1
Reactive power capability		Yes*	Yes	No	Yes	Yes
Leakage current	Without CMF	165mA	38mA	170mA	340mA	125mA
	With CMF	18mA	20mA	21mA	22mA	14mA
Blocking Voltage	MOSFET	$6.5V_{dc}$	$4V_{dc}$	$5V_{dc}$	$6V_{dc}$	$4V_{dc}$
	Diode	$5V_{dc}$	$1.35V_{dc}$	$1.65V_{dc}$	$1.65V_{dc}$	$1.65V_{dc}$

LF=line- frequency, OLF= other than line-frequency, Yes*=possible with modified modulation technique, CMF=common mode filter, V_{dc}=Total DC-link voltage.



(a) (b)

Fig. 19. Efficiency curves. (a) Theoretical and PSIM. (b) Different input voltages.

in Table V to highlight the merits of the proposed power conditioner; it is observed that the total component count, leakage current, and blocking voltages are less compared with the topologies in [16], [19], and [20]. On the other hand, the leakage current and blocking voltages of [18] are close to the proposed topology; however, it is augmented with an extra semiconductor device and parasitic resistance losses as shown in Fig. 19. Moreover, the use of bulky and low-frequency transformer at ac side is eliminated. Furthermore, the proposed CM filter solution can be employed for the topologies reported in [16]–[20] to minimize the leakage current.

VI. CONCLUSION

In this paper, a new single-phase two-stage seven-level power conditioner suitable for PV power generation system is presented. The proposed single-phase seven-level power conditioner employs a front-end dc–dc boost converter and an asymmetrical seven-level inverter. This topology uses very few power semiconductor switches in comparison with other topologies for the realization of seven-level output, which leads to improved efficiency. The proposed power conditioner ensures guaranteed balancing of dc-link capacitor voltages with simple control. In addition, the leakage current is limited effectively within the VDE0126-1-1 grid standards. The developed controller shows better performance by regulating the output voltage and injecting current into the grid for intermittent changes in PV. The experimental results are in good correlation with the simulation results, which prove the capability of the proposed topology.

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