Bidirectional Clamping-Based H5, HERIC, and H6 Transformerless Inverter Topologies With Reactive Power Capability

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***Abstract*—Transformerless inverters (TLIs) are competently accepted for photovoltaic (PV) applications because of their high efficiency, reduced size, and lower cost. But in the absence of a transformer, there exists a galvanic connection between the PV array to ground and it results in the flow of hazardous leakage current. Several TLI topologies have been proposed in the literature with decoupling circuits to reduce the leakage current. Among those H5, Heric, and H6 topologies are the most popular and widely accepted TLIs. Nevertheless, the effect of switch junction capacitances was not considered in the common-mode voltage analysis, which inevitably causes excess leakage current. Also, reactive power capability cannot be accomplished with traditional pulsewidth modulation (PWM) schemes due to the absence of a bidirectional current path during the freewheeling period. Therefore, in this article, a bidirectional clamping (BDC) based H5, Heric, and H6 TLI topologies are proposed with improved PWM schemes. BDC branch reduces the leakage current by clamping the inverter terminal voltages to half of the dc-link voltage during the freewheeling period and the improved PWM schemes ensure the bidirectional current path while operating in negative power region. The performance of both traditional and proposed topologies is tested with MATLAB simulations and further justified with experimental results.**

***Index Terms*—Common-mode voltage (CMV), leakage current, transformerless inverter (TLI).**

I. Introduction

POWER generation from solar photovoltaics (PV) is the most favorable solution to meet the increased energy requirements. The majority of the PV installations are interfaced with the grid due to its compactness, reduced cost, and higher efficiency. Moreover, these are operating in parallel to the utility grid, which allows the flow of excess PV power into the grid (i.e., when produced PV power is more than the local load demand). Therefore, this attracts the attention of people and policymakers to do in-depth research and development on grid-connected PV inverters [1].

Generally, PV inverters are categorized into isolated types and nonisolated types based on the placement of the transformer in the power processing stage. To achieve higher efficiency, compact size, and reduced cost, a bulky line frequency transformer (50/60 Hz) is eliminated in nonisolated type PV inverters. But the exclusion of the transformer results in the formation of a resonant circuit between the parasitic capacitance of PV panels, filter inductors, and grid impedances. High-frequency common-mode voltage (CMV) oscillations generated by the switching of the PV inverter excite the resonant circuit and also contribute to the leakage current. Consequently, it will deteriorate the waveform quality, increase the electromagnetic compatibility (EMC), and also lead to poor safety [2], [3]. The full-bridge inverter with bipolar pulsewidth modulation (BPWM) and unipolar pulsewidth modulation (UPWM) schemes is introduced in the early stage of symmetrical filter inductor-based topologies. Even though the BPWM scheme is successful in the limitation of leakage current, increased total harmonic distortion (THD), EMC noise, and switching losses limit its application in transformerless inverters (TLIs). The above-said drawbacks can be overcome by the UPWM scheme. But it fails to limit the leakage current due to high-frequency oscillations in CMV. Thus, both of the pulsewidth modulation (PWM) schemes with the conventional full-bridge inverter do not satisfy the grid codes and standards [4].

To overcome these problems, different topologies were published in the literature [5]; either dc- or ac-based decoupling is provided from grid to PV panel during the freewheeling period by incorporating additional circuitry to the full-bridge inverter. Among those, H5, Heric, and H6 are the most popular and widely accepted TLI topologies in the industry for PV power applications. In H5 topology [6], dc decoupling is achieved by adding a switch in series with the source. AC decoupling is achieved in Heric topology by adding two switches in parallel to the grid. Either dc or ac decoupling is possible in H6 topology based on the placement of switches and diodes in series or parallel to the source and grid, respectively [7], [8]. Even though the above-said topologies are recording more efficiency, the decoupling circuits solitary cannot preserve constant CMV due to the effect of switch junction capacitances during the freewheeling period. Consequently, the potential difference in

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CMV is produced by charging and discharging switch junction capacitances. The magnitude of this junction capacitances varies from several pico to few nanofarads, which cannot be neglected. Thus, it causes more oscillations in the CMV and also results in the flow of excess leakage current. To alleviate the leakage current problems and to improve the waveform quality in an optimized way, a passive or active clamping branch with split dc-link capacitors was used to preserve constant CMV during the freewheeling period of PV inverters [9].

In this circumstance, different full-bridge-based TLI topologies were proposed to clamp the terminal voltages to $V_{\rm dc}/2$ (i.e., half of the dc-link voltage) during the freewheeling period. González *et al.* [10] proposed a modified full-bridge TLI topology by adding two switches and two diodes for attaining dc decoupling and passive clamping, respectively. An H-bridge zero-voltage state rectifier–diode topology is proposed in [11], where one switch and six diodes are used for both ac decoupling and passive clamping, respectively. Similarly, in [12] and [13], a family of modified full-bridge TLI inverter topologies are proposed to obtain ac decoupling and active clamping by adding extra switches and diodes. All the above-said topologies and their PWM schemes are only designed to operate at a unity power factor (UPF) condition of the grid. But in modern days, the reactive power capability of the TLI is much important to pierce a large amount of PV power into the grid as per the VDE-AR-N4105 standard [14]. To fill the gap, Freddy *et al.* [15] proposed an improved modulation technique for basic H5 and Heric inverter topologies. In addition to that, different inverter topologies are also proposed in [16] and [17] to serve the functions of high efficiency and reactive power support with an increased component count. However, the clamping of the inverter terminal voltages during the freewheeling period is not considered in [15]–[17], which results in more oscillations in CMV. Consequently, excess leakage current will flow in the resonant circuit and it further increases the size of common-mode filter (CMF). Furthermore, increased component count and passive filters to realize the reactive power control will hike the overall cost and also enlarge the size of the system.

To resolve the above problems, such as constant CMV, reduced leakage current and reactive power control capability demand some improvements in both inverter topologies and their PWM schemes. Therefore, in this article, a bidirectional clamping (BDC) based H5, Heric, and H6 TLI topologies are proposed with improved PWM schemes. BDC branch clamps the inverter terminal voltages to half of the dc-link voltage during the freewheeling period. Thus, CMV is maintained constant in all the operating modes of an inverter to reduce the leakage current. Furthermore, improved PWM schemes ensure the bidirectional current path while operating in a negative power region; it confirms the reactive power control capability of the proposed TLI topologies without effecting the waveform quality. Furthermore, the effect of switch junction capacitances on CMV and bidirectional current path during the freewheeling period for traditional H5, HERIC, and H6 topologies is discussed in detail. The performance of both traditional and proposed topologies is tested with MATLAB simulations and further justified with experimental results.

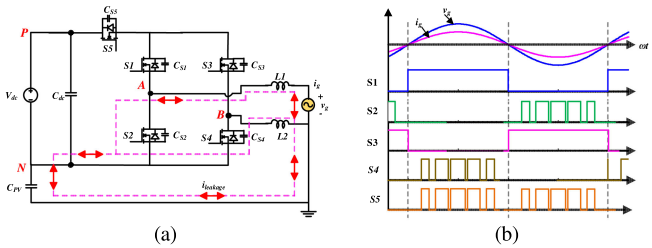

Fig. 1. H5 TLI. (a) Circuit structure. (b) Gate pulses.

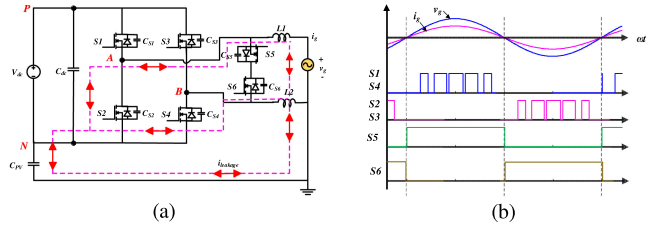

Fig. 2. Heric TLI. (a) Circuit structure. (b) Gate pulses.

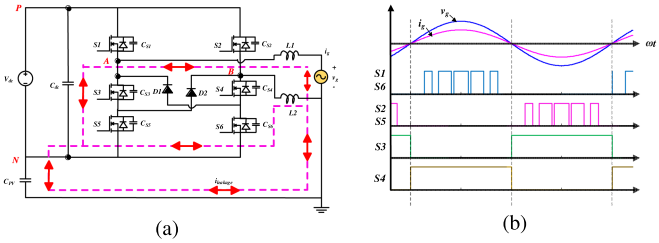

Fig. 3. H6 TLI. (a) Circuit structure. (b) Gate pulses.

The organization of the article is as follows. The analysis of leakage current, oscillations in CMV, and reactive power capability of the traditional H5, Heric, and H6 topologies are given in Section II. Operating states and improved modulation schemes of the proposed topologies are discussed in Section III. Simulation results are presented in Section IV. Experimental validation of both traditional and proposed topologies is given in Section V. Finally, the conclusion is made in Section VI.

II. Analysis of Leakage Current

The topological structures and gate pulses of the traditional H5, Heric, and H6 TLIs are shown in Figs. 1–3, respectively, where $V_{\rm dc}$ is the equivalent PV voltage, namely, input dc voltage of the inverter, and $C_{\rm PV}$ is the parasitic capacitance of the PV module. Positive and negative terminals of the input dc source are denoted as P and N. Similarly, phase and neutral terminals of the inverter are denoted as A and B, respectively. General expressions used for the computation of CMV "$V_{\rm CM}$" and differential-mode voltage "$V_{\rm DM}$" are indicated in terms of inverter terminal voltages V_{AN} and V_{BN} are as follows:

$$V_{\rm DM} = V_{AB} = V_{AN} - V_{BN} \tag{1}$$

$$V_{\rm CM} = \frac{V_{AN} + V_{BN}}{2}. \tag{2}$$

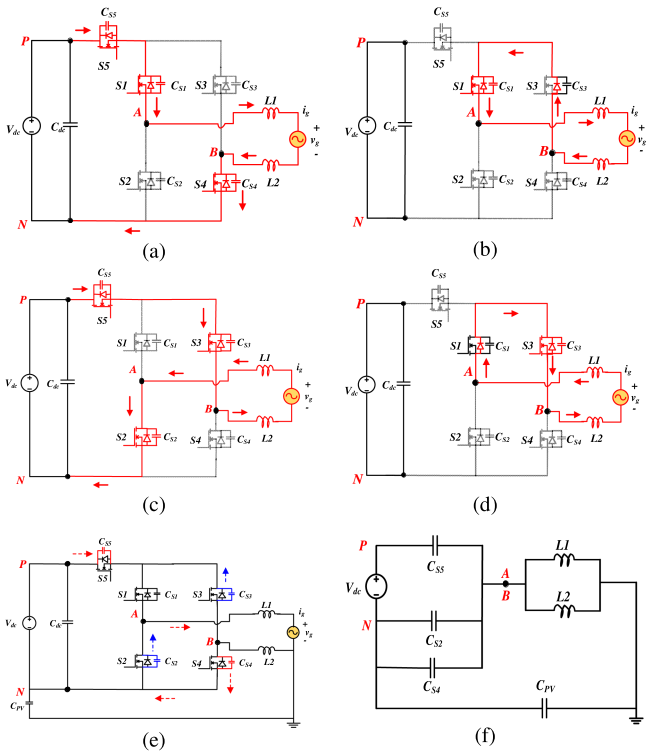

Fig. 4. Operating states, the charging and discharging of switch junction capacitances of H5 topology in the positive power transferring mode. (a) Positive half cycle. (b) Freewheeling period during the positive half cycle. (c) Negative half cycle. (d) Freewheeling period during the negative half cycle. (e) Charging and discharging of switch junction capacitances during the positive half cycle. (f) Simplified circuit.

Asymmetries in the filter inductors produce an extra component of CMV ($V_{\text{CM-DM}}$), as given in (3), whereas, the total CMV (V_{TCMV}) and the leakage current are given in (4) and (5) as follows.

$$V_{\text{CM-DM}} = V_{\text{DM}} \cdot \frac{L2 - L1}{2\,(L2 + L1)} \tag{3}$$

$$V_{\text{TCMV}} = V_{\text{CM}} + V_{\text{CM-DM}} \tag{4}$$

$$i_{\text{leakage}} = C_{\text{PV}} \frac{dV_{\text{TCMV}}}{dt}. \tag{5}$$

From (3), if $L1 = L2$ (i.e., for a well-designed magnetic circuit), the voltage $V_{\text{TCMV}} = V_{\text{CM}}$ [12]. From (5), it is evident that the magnitude of C_{PV} and oscillations in V_{TCMV} are controlling the leakage current. Eventually, the magnitude of C_{PV} is depended on the environmental conditions and it is not controllable. Therefore, the ultimate option to reduce the leakage current is to eliminate the oscillations in V_{TCMV}. Usually, these oscillations depend on the topology and PWM scheme employed for the switching of an inverter.

A. Analysis of Oscillations in CMV Due to Junction Capacitances of the Switches

In real time, the analysis of leakage current due to junction capacitances of the MOSFETs cannot be ignored. From Fig. 4(a), $V_{AN} = V_{\text{dc}}$, $V_{BN} = 0$, and $V_{\text{CM}} = V_{\text{dc}}/2$ for positive half cycle. Similarly, from Fig. 4(c), $V_{AN} = 0$, $V_{BN} = V_{\text{dc}}$, and $V_{\text{CM}} = V_{\text{dc}}/2$ for a negative half cycle. It is observed that the CMV is constant (i.e., $V_{\text{dc}}/2$) in both the half cycles, whereas in the freewheeling mode, filter inductor currents continuously freewheel through the grid and power cannot be transferred from the input dc source, as shown in Fig. 4(b) and (d). While transferring from positive half cycle to freewheeling period, switches *S4* and *S5* are switched OFF synchronously. During the transient period junction, capacitances of the switches *S4* and *S5* are charging and the switches *S2* and *S3* are discharging, as depicted in Fig. 4(e). After completion of the transition, the body diode of *S3* will conduct to provide the freewheeling path. Also, the terminal voltage V_{AN} increases and V_{BN} decreases due to the charging and discharging of junction capacitances [5]. From the simplified circuit depicted in Fig. 4(f), the terminal voltages can be evaluated by (6) using Kirchhoff's current law. The steady-state terminal voltages during the freewheeling period are regulated by the junction capacitances of the MOSFETS, as shown in (6). Therefore, V_{CM} of the H5 inverter is not constant throughout the whole period, which results in abrupt leakage current. Similarly, the terminal voltages of the Heric and H6 inverter topologies are given in (7) and (8), respectively [18], [19].

$$V_{AN} = V_{BN} = \frac{C_{S2} + C_{S5}}{C_{S2} + C_{S5} + C_{S4}} V_{\text{dc}} \tag{6}$$

$$V_{AN} = V_{BN} = \frac{C_{S1} + C_{S3}}{C_{S1} + C_{S2} + C_{S3} + C_{S4}} V_{\text{dc}} \tag{7}$$

$$V_{AN} = V_{BN} = \frac{C_{S1} + C_{S2}}{C_{S1} + C_{S2} + \frac{C_{S3}.C_{S5}}{C_{S3}+C_{S5}} + C_{S4}} V_{\text{dc}}. \tag{8}$$

From the above expressions, it is evident that V_{AN} and V_{BN} are not equal to $V_{\text{dc}}/2$ during the freewheeling period for all three topologies. Therefore, CMV cannot be kept constant in all the operating modes of the inverter and it will further increase the magnitude of leakage current. Moreover, in this analysis, the effect of parasitic capacitances formed between the heat sink and the ground (C_{1g}, C_{2g}) is ignored because of its lower magnitude and fundamental frequency of operation [20].

B. Analysis of Bidirectional Current Path in H5, Heric, and H6 Topologies

The reactive power control capability of the inverter is determined based on the bidirectional current path provided by the topology and its PWM technique. From Figs. 5–7, it is observed that the conventional PWM technique applied for all three topologies is not providing a bidirectional current path during the freewheeling period under the negative power region. For example, in H5 topology, switch *S3* is turn-OFF during positive v_g and negative i_g, as shown in Fig. 5(a). Similarly, switch *S1* is turn-OFF during negative v_g and positive i_g, as shown in Fig. 5(b).

Thus, reactive power control capability cannot be realized with the traditional PWM scheme applied to the H5 topology. In the same way, switches *S6* $(+v_g\ and - i_g)$ and *S5* $(-v_g\ and + i_g)$ in Heric and switches *S3* $(+v_g\ and - i_g)$ and *S4* $(-v_g\ and + i_g)$ in the H6 inverter are turn-OFF under negative

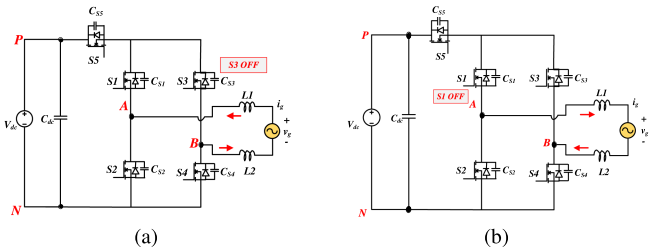

Fig. 5. H5 topology during negative power region. (a) Positive v_g and negative i_g. (b) Negative v_g and positive i_g.

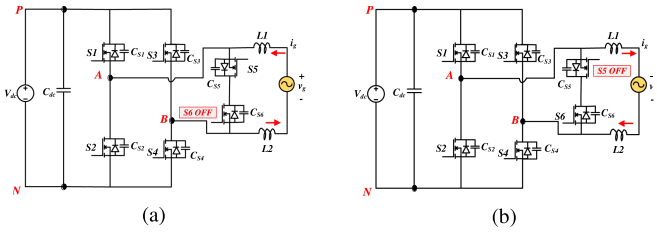

Fig. 6. Heric topology during negative power region. (a) Positive v_g and negative i_g. (b) Negative v_g and positive i_g.

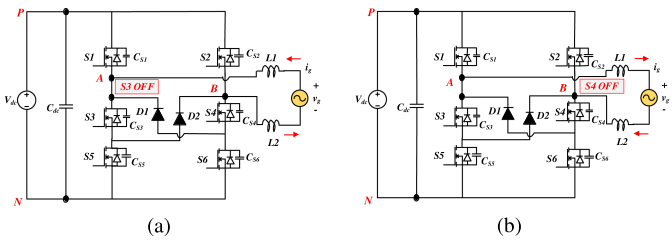

Fig. 7. H6 topology during negative power region. (a) Positive v_g and negative i_g. (b) Negative v_g and positive i_g.

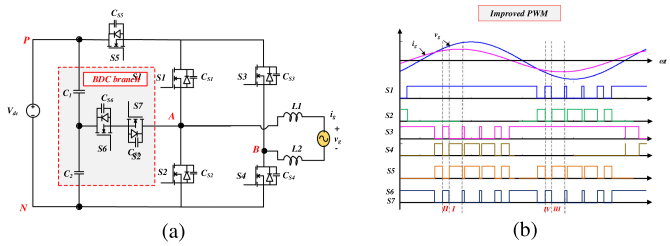

Fig. 8. BDC-H5 TLI. (a) Circuit diagram. (b) Improved PWM.

power region, as shown in Figs. 6 and 7, respectively. Therefore, PWM schemes applied to the traditional H5, Heric, and H6 topologies should be improved to support the bidirectional current path during the freewheeling period.

III. Proposed BDC-Based H5, Heric, and H6 Topologies

To solve the above-mentioned issues, a BDC branch is integrated along with improved PWM schemes for the traditional H5, Heric, and H6 topologies, as shown in Figs. 8–10, respectively. The BDC branch is obtained by connecting two source connected MOSFETs with split dc-link capacitors to clamp the

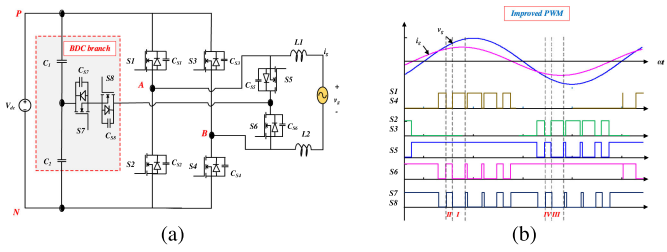

Fig. 9. BDC-Heric TLI. (a) Circuit diagram. (b) Improved PWM.

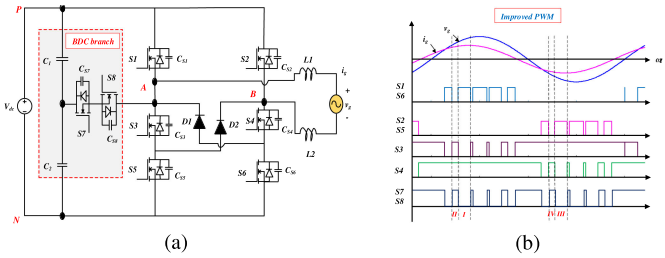

Fig. 10. BDC-H6 TLI. (a) Circuit diagram. (b) Improved PWM.

terminal voltages of the inverter to $V_{\rm dc}/2$ during the freewheeling period. Moreover, improved PWM schemes are allowing the current in both directions to support the reactive power control during the freewheeling period.

A. Operating States

Operating states of the inverters in both unity and non-UPF operations of the grid are explained in this section. Based on the voltage polarity, the operation of the inverters is classified into three states (i.e., $V_{AB} = V_{\rm dc}$, $V_{AB} = 0$, and $V_{AB} = -V_{\rm dc}$) and each state allows the current from source to grid and vice versa. The operation of both traditional and BDC-based H5, Heric, and H6 TLI topologies is the same during the positive power region. Furthermore, switching logic, terminal voltages, and CMV calculations for BDC-based H5, Heric, and H6 topologies are given in Table I.

State 1: In this state, $V_{AB} = V_{\rm dc}$, and the current flows either from source to grid or vice versa, as shown in Figs. 11(a), 12(a), and 13(a), respectively. During this state, in positive power region, current flows through MOSFETS and in the negative power region, current flows through body diodes of MOSFETS. The inverter terminal voltages $V_{AN} = V_{\rm dc}$ and $V_{BN} = 0$. Hence, $V_{\rm DM}$ and $V_{\rm CM}$ become

$$V_{\rm DM} = V_{AN} - V_{BN} = V_{\rm dc} \tag{9}$$

$$V_{\rm CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{\rm dc}}{2}. \tag{10}$$

State 2: In this state, $V_{AB} = 0$, and the current freewheels through the inductors and grid or vice versa via MOSFETs or body diodes of MOSFETs, as shown in Figs. 11(b), 12(b), and 13(b), respectively. During this state, dc source is isolated from the grid and also the inverter terminal voltages are clamped to half of the dc-link voltage, such as $V_{AN} = V_{\rm dc}/2$ and $V_{BN} =$

TABLE I
SWITCHING LOGIC AND CMV CALCULATIONS BDC-BASED H5, HERIC, AND H6 TLI TOPOLOGIES

BDC based TLIs		*S1*	D_{S1}	*S2*	D_{S2}	*S3*	D_{S3}	*S4*	D_{S4}	*S5*	D_{S5}	*S6*	D_{S6}	*S7*	D_{S7}	*S8*	D_{S8}	*D1*	*D2*	V_{AN}	V_{BN}	$V_{TCMV}=V_{CM}$
H5 $V_{AB}=V_{dc}$	$i_g>0$	1	0	0	0	0	0	1	0	1	0	0	0	0	0	-	-	-	-	V_{dc}	*0*	$V_{dc}/2$
	$i_g<0$	0	1	0	0	0	0	0	1	0	1	0	0	0	0	-	-	-	-	V_{dc}	*0*	$V_{dc}/2$
H5 $V_{AB}=0$	$i_g>0$	1	0	0	0	0	1	0	0	0	0	1	0	0	1	-	-	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
	$i_g<0$	0	1	0	0	1	0	0	0	0	0	0	1	1	0	-	-	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H5 $V_{AB}=-V_{dc}$	$i_g>0$	0	0	1	0	1	0	0	0	1	0	0	0	0	0	-	-	-	-	*0*	V_{dc}	$V_{dc}/2$
	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	-	-	-	-	*0*	V_{dc}	$V_{dc}/2$
Heric $V_{AB}=V_{dc}$	$i_g>0$	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	-	-	V_{dc}	*0*	$V_{dc}/2$
	$i_g<0$	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-	-	V_{dc}	*0*	$V_{dc}/2$
Heric $V_{AB}=0$	$i_g>0$	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
	$i_g<0$	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	-	-	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
Heric $V_{AB}=-V_{dc}$	$i_g>0$	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	-	-	*0*	V_{dc}	$V_{dc}/2$
	$i_g<0$	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	-	-	*0*	V_{dc}	$V_{dc}/2$
H6 $V_{AB}=V_{dc}$	$i_g>0$	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	V_{dc}	*0*	$V_{dc}/2$
	$i_g<0$	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	V_{dc}	*0*	$V_{dc}/2$
H6 $V_{AB}=0$	$i_g>0$	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
	$i_g<0$	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0	0	1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
H6 $V_{AB}=-V_{dc}$	$i_g>0$	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	*0*	V_{dc}	$V_{dc}/2$
	$i_g<0$	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	*0*	V_{dc}	$V_{dc}/2$

*D_{S1}–D_{S8} are the body diodes of switches *S*1 to *S*8, respectively.

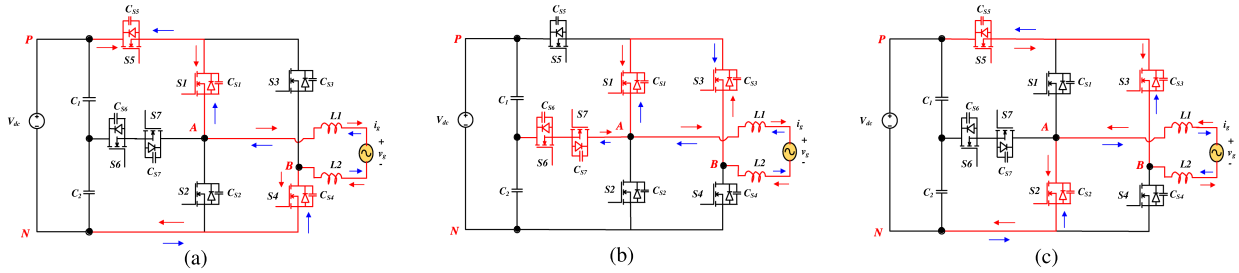

Fig. 11. Operating modes of the BDC-H5 inverter. (a) $V_{AB} = V_{\rm dc}$. (b) $V_{AB} = 0$. (c) $V_{AB} = -V_{\rm dc}$.

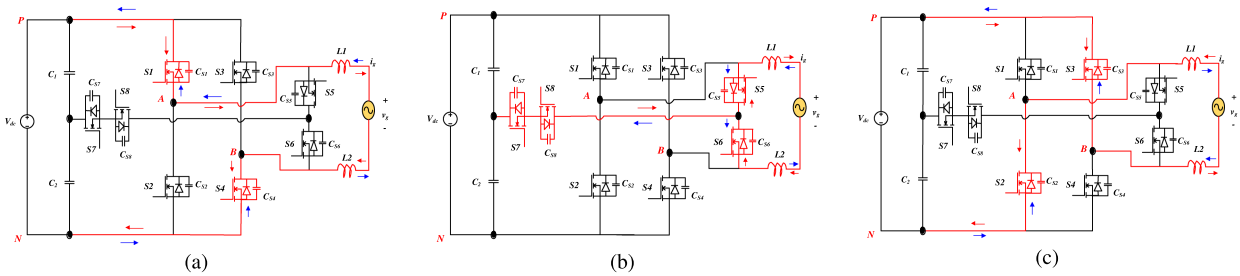

Fig. 12. Operating modes of the BDC-Heric inverter. (a) $V_{AB} = V_{\rm dc}$. (b) $V_{AB} = 0$. (c) $V_{AB} = -V_{\rm dc}$.

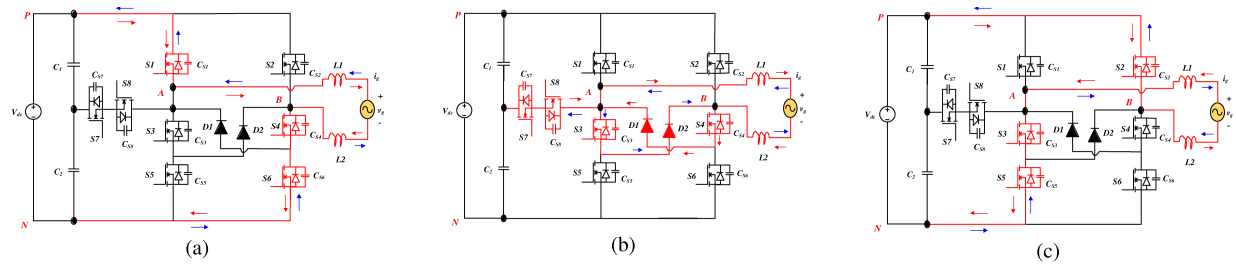

Fig. 13. Operating modes of the BDC-H6 inverter. (a) $V_{AB} = V_{\rm dc}$. (b) $V_{AB} = 0$. (c) $V_{AB} = -V_{\rm dc}$.

TABLE II
SYSTEM PARAMETERS

S. No	Parameters	Value
1	Input voltage	400 V
2	Inductor L_1, L_2	4 mH
3	Capacitors C_1, C_2, C_f, C_{PV}	1 mF, 1 mF, 2 μF, 42 nF
4	AC output voltage	230 V, 50 Hz
5	Switching frequency f_s	10 kHz
6	Output power	500 W
7	Ground resistance R_g	10 Ω
8	Mosfet	IRFP460N
9	Diode	MUR1560

$V_{\rm dc}/2$. Hence, $V_{\rm DM}$ and $V_{\rm CM}$ become

$$V_{\rm DM} = V_{AN} - V_{BN} = 0 \tag{11}$$

$$V_{\rm CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{\rm dc}}{2}. \tag{12}$$

State 3: In this state, V_{AB} = -$V_{\rm dc}$, and the current flows either from source to grid or vice versa, as shown in Figs. 11(c), 12(c), and 13(c), respectively. During this state, in positive power region, current flows through MOSFETS and in the negative power region, current flows through body diodes of MOSFETS. The inverter terminal voltages $V_{AN} = 0$ and $V_{BN} = V_{\rm dc}$. Hence, $V_{\rm DM}$ and $V_{\rm CM}$ become

$$V_{\rm DM} = V_{AN} - V_{BN} = -V_{\rm dc} \tag{13}$$

$$V_{\rm CM} = \frac{V_{AN} + V_{BN}}{2} = \frac{V_{\rm dc}}{2}. \tag{14}$$

From (9)–(14), it is observed that the $V_{\rm CM}$ is maintained constant in all the operating modes of BDC-based TLI topologies. Therefore, the effect of switch junction capacitance is eliminated by clamping the terminal voltages to $V_{\rm dc}/2$. Consequently, the magnitude of leakage current and thr size of the CMF are reduced in the proposed TLI topologies [5].

B. Improved PWM Strategies

Figs. 8(b), 9(b), and 10(b) illustrate the improved UPWM schemes for BDC-based H5, Heric, and H6 topologies, respectively. Here, a bidirectional current path is provided for the inverters by turning ON the switches *S1* and *S3* in H5, *S5* and *S6* in Heric, and *S3* and *S4* in H6 topologies during the freewheeling period. Moreover, in zero states, only two switches and two diodes are conducting with respect to the current direction. Furthermore, the proposed BDC branch clamps the V_{AN} and V_{BN} to $V_{\rm dc}/2$, which ensures constant CMV during the freewheeling period in both UPF and nonUPF operations of the grid. The closed-loop control of the proposed TLI topologies is verified by using a proportional resonant controller given in [17].

IV. SIMULATION RESULTS

To test the proposed concept, simulation studies are carried out as per the specifications listed in Table II by using MATLAB/SIMULINK software. An equivalent capacitance of 42 nF is placed between the terminals of dc power source to the ground for the evolution of leakage current caused due to oscillations

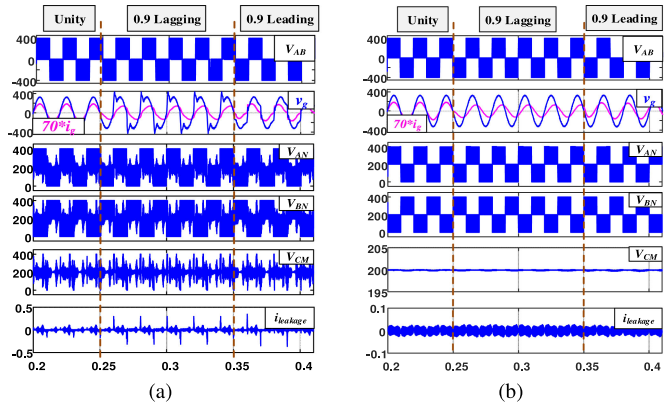

Fig. 14. Differential-mode and common-mode results. (a) H5. (b) BDC-H5 inverter.

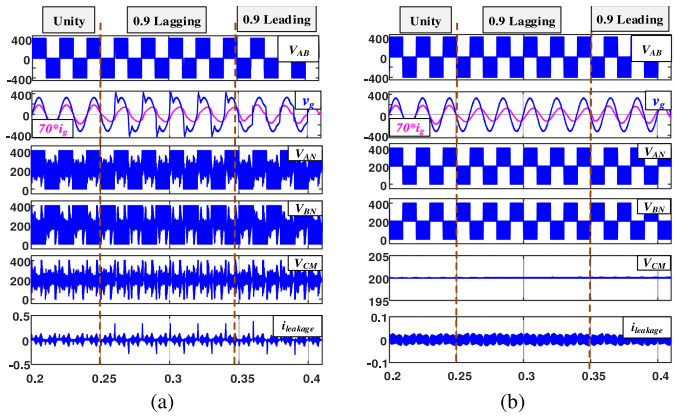

Fig. 15. Differential-mode and common-mode results. (a) Heric. (b) BDC-Heric inverter.

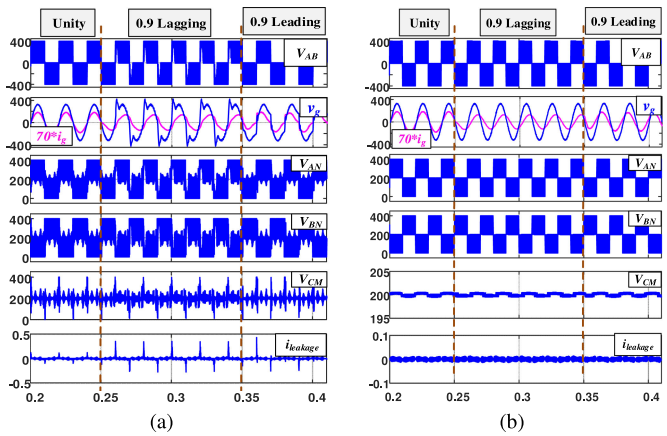

Fig. 16. Differential-mode and common-mode results. (a) H6. (b) BDC-H6 inverter.

in CMV. Furthermore, the reactive power control capability of the proposed grid-connected inverters is tested for 0.9 lagging and 0.9 leading conditions. Fig. 14 shows the differential-mode (V_{AB}, v_g, and i_g) and common-mode characteristics (V_{AN}, V_{BN}, $V_{\rm CM}$, and $i_{\rm leakage}$) of both traditional and BDC-based H5 topologies under unity, 0.9 lagging, and 0.9 leading power factor conditions. Similarly, Figs. 15 and 16 illustrate the waveforms of both

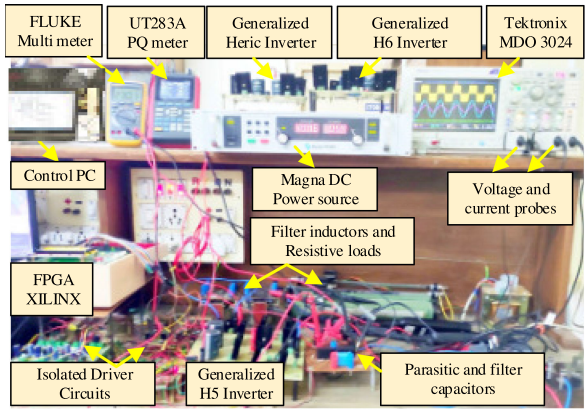

Fig. 17. Experimental test setup.

traditional and BDC-based Heric and H6 inverter topologies. From the simulation results, it can be observed that the improved PWM schemes provide the reactive power support to enhance the inverter operation in all the operating modes without losing the waveform quality [21]. Moreover, the additional BDC branch effectively clamps the CMV to $V_{\rm dc}/2$ in all the operating modes of the proposed inverter topologies. Therefore, high-frequency oscillations due to the junction capacitance of the switches are eliminated in $V_{\rm CM}$ during the freewheeling states, which result in the reduction of leakage current.

V. Experimental Results

To prove the effectiveness of the proposed TLI topologies, a 500 W experimental setup is built and tested based on the available resources in the laboratory, as shown in Fig. 17. The design of the various passive components is evaluated using the formulas given in [3] and [22]. The system parameters used for the testing of both traditional and BDC-based topologies are listed in Table II. The performance of all the topologies is tested under unity, 0.9 lagging, and 0.9 leading conditions to validate the reactive power control capability. Also, an equivalent capacitance of 42 nF is placed between the terminals of dc power source to the ground for measuring the magnitude of leakage current caused due to oscillations in CMV. Differential voltage (V_{AB}), load voltage (v_l), load current (i_l), and leakage current ($i_{\rm leakage}$) are shown in a single window to affirm the identical CMV behavior in all the operating modes of proposed TLI topologies. MDO3024 and UT283A power quality meters were used to measure the leakage current magnitude and THD, respectively.

Figs. 18–20 illustrate differential-mode (V_{AB}, v_l, and i_l) and common-mode (V_{AN}, V_{BN}, $V_{\rm TCMV}$, and $i_{\rm leakage}$) characteristics of both traditional and BDC-based H5, Heric, and H6 topologies, respectively. Moreover, the performance evaluation of all the topologies is listed in Table III. Differential-mode characteristics of both traditional and BDC-H5 topology are similar while operating under UPF condition, as shown in Fig. 18(a) and (f).

From Fig. 18(b) and (c), it is observed that the output waveforms of the traditional H5 topology are distorted while operating in non-UPF conditions due to the absence of bidirectional

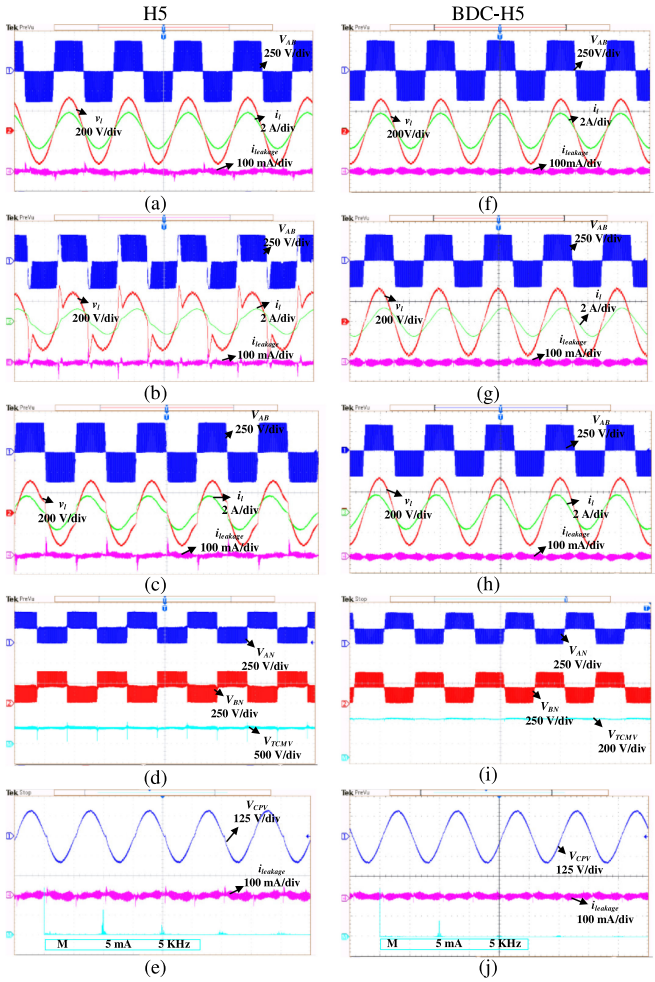

Fig. 18. Differential-mode and common-mode characteristics of H5 and BDC-H5 topologies.

current path during the freewheeling period, whereas in BDC-H5 topology, reliable output waveforms can be observed, as shown in Fig. 18(g) and (h) due to the presence of a bidirectional current path provided by the improved PWM scheme (as per the analysis given in Section III). Furthermore, common-mode characteristics of the traditional H5 topology are illustrated in Fig. 18(d) and (e). Due to the effect of junction capacitance of the switches during the freewheeling period, there exist oscillations in the total CMV. Moreover, these oscillations can excite the resonant circuit formed by the parasitic capacitance connected to the dc source and result in excess leakage current (as per the analysis given in Section II), whereas, in BDC-H5 topology, an additional BDC branch is connected to clamp the $V_{\rm TCMV}$ to $V_{\rm dc}/2$ and result in a complete abolishment of such oscillations, as shown in Fig. 18(i). Also, it further reduces the leakage current magnitude, as shown in Fig. 18(j).

Similarly, the experimental results of Heric, BDC-Heric and H6, BDC-H6 topologies are presented side by side for easy comparison and also their performance evaluation results are listed in Table III. Furthermore, Fig. 21 shows the THD measurement of output current waveforms at unity, 0.9 lagging, and 0.9 leading power factors of both traditional and BDC-H5

TABLE III
PERFORMANCE EVALUATION OF THE TRADITIONAL AND BDC-BASED TOPOLOGIES

Features		H5	BDC-H5	Heric	BDC-Heric	H6	BDC-H6
PWM		Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
Total No.of MOSFETs		5	7	6	8	6	8
Total No.of Diodes		0	0	0	0	2	2
Total No.of components conducting in one cycle		10	14	8	12	10	14
Total blocking voltage		4.5*V_{dc}	5.5*V_{dc}	6*V_{dc}	7*V_{dc}	7*V_{dc}	8*V_{dc}
Unity power factor	$i_{leakage\_RMS}$	16.4 mA	8.52 mA	21.9 mA	8.67 mA	12.4 mA	8.36 mA
	% THD	1.43 %	1.44 %	1.45 %	1.53 %	1.47 %	1.54 %
Lagging power factor	$i_{leakage\_RMS}$	22.5 mA	9.28 mA	27.6 mA	9.38 mA	18.05 mA	9.13 mA
	% THD	11.8 %	2.59 %	11.38 %	2.59 %	11.50 %	2.07 %
Leading power factor	$i_{leakage\_RMS}$	17.95 mA	8.55 mA	22.6 mA	8.7 mA	15.48 mA	8.06 mA
	% THD	9.20 %	1.58 %	10.76 %	1.68 %	11.28 %	1.71 %
Size of the CMF		Large	Small	Large	Small	Large	Small
Reactive power capability		No	Yes	No	Yes	No	Yes
CMV		Oscillating	Constant	Oscillating	Constant	Oscillating	Constant
Bi-directional current path during negative power region		Not present	Present	Not present	Present	Not present	Present

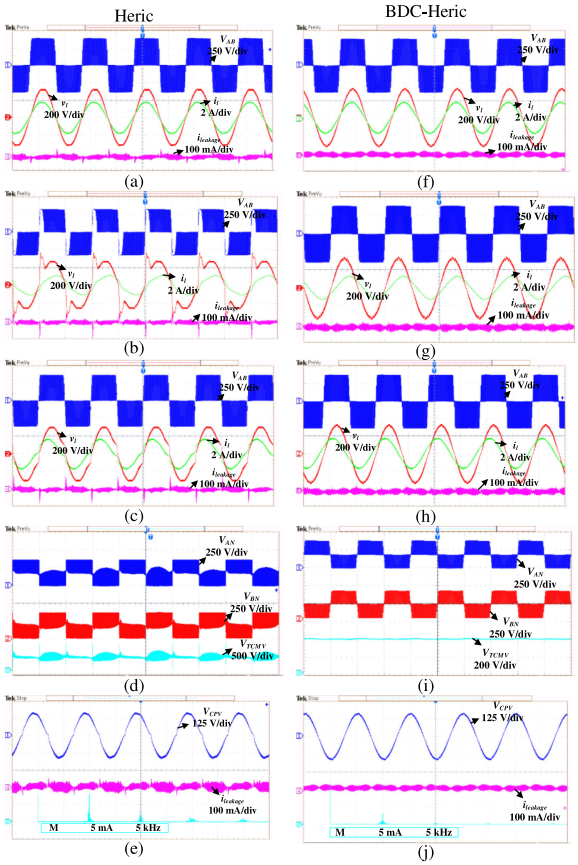

Fig. 19. Differential-mode and common-mode characteristics of Heric and BDC-Heric topologies.

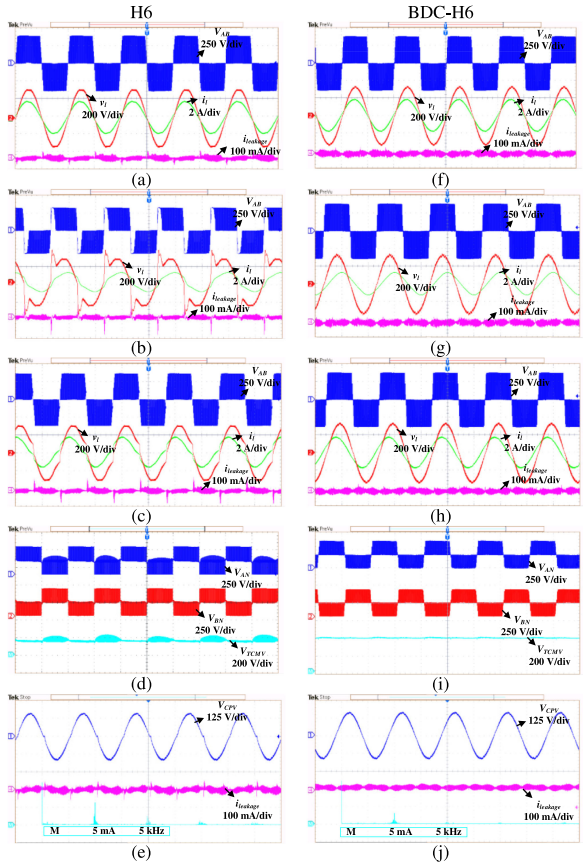

Fig. 20. Differential-mode and common-mode characteristics of H6 and BDC-H6 topologies.

topology, respectively. From the data given in Table III, it is noticed that the measured %THD of the proposed topologies is less than the IEC61000-3-2 standard for all the operating conditions. Moreover, the RMS value of the leakage current is also less for BDC-based topologies under different power factor conditions in comparison with traditional topologies. Therefore, both reactive power control capability and leakage current reduction are achieved by improving the modulation schemes and traditional topologies with the BDC branch, respectively.

Furthermore, closed-loop operation of the proposed BDC-H5 topology is tested for different power factor conditions of the grid by using a real-time validation platform, named OPAL-RT OP4500 modules [23]. Fig. 22(a) illustrates the step change in

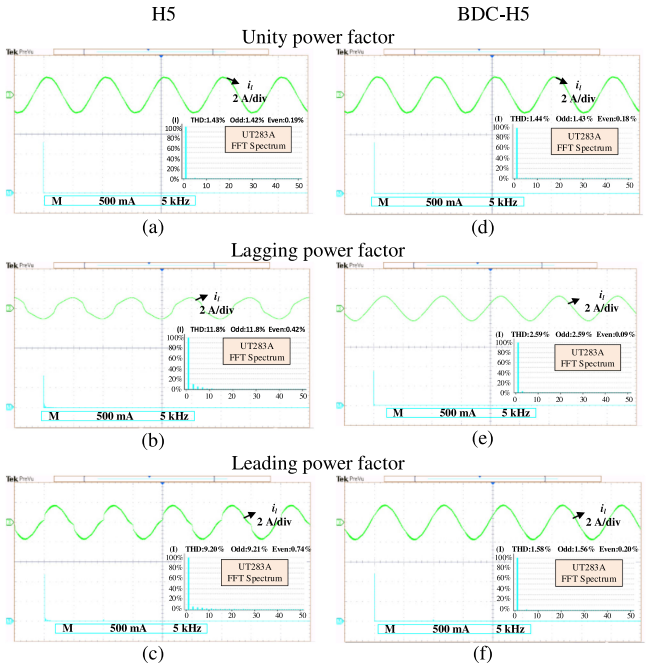

Fig. 21. THD measurement of current waveforms for H5 and BDC-H5.

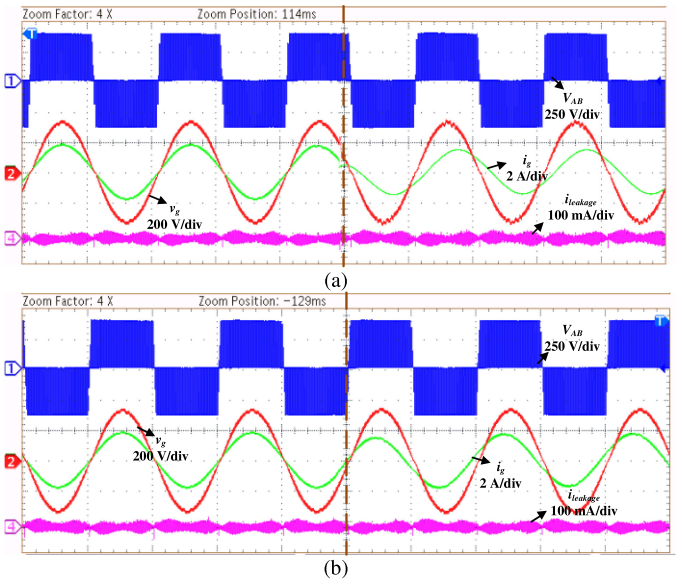

Fig. 22. (a) Step change in power factor from unity to 0.9 lagging. (b) Step change power factor from unity to leading.

power factor from unity to 0.9 lagging (i.e., by changing reference active and reactive power). Similarly, Fig. 22(b) shows a step change in power factor from unity to 0.9 leading. From both the figures, it can be observed that the BDC-based topologies are capable of supporting the reactive power control with the superior quality of waveforms in comparison with the traditional topologies. Moreover, the controller implementation is the same for the other two proposed topologies. Finally, the efficiency curves of both traditional and BDC-based H5, Heric, and H6 topologies are drawn in Fig. 23. Because of the increased power

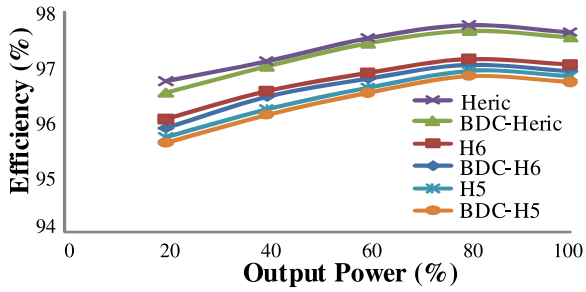

Fig. 23. Efficiency curves.

losses in the additional BDC branch, the proposed topologies register slightly lower efficiency in comparison with the traditional topologies. However, the leakage current reduction and reactive power control capability of the proposed topologies attract the attention of researchers in the future PV power generation systems.

VI. Conclusion

In this article, BDC-based H5, Heric, and H6 TLIs are proposed with the features of reactive power control capability and reduced leakage current. Improved modulation schemes enable the inverters to operate in both unity and non-UPF conditions without losing waveform quality. Moreover, the additional BDC branch maintains constant CMV (half of the input dc voltage) in all the operating modes of the inverter. Thus, the magnitude of leakage current is reduced in the proposed topologies. Finally, the performance of both traditional and BDC-based topologies is validated through simulation and experimentation and also their results are compared to highlight the novelty of proposed configurations.

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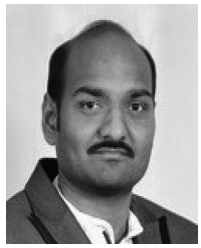

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