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# A three-phase transformer based T-type topology for DSTATCOM application

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**ABSTRACT**

Among the various reduced switch count multilevel inverter (RSC-MLI) topologies, T-type is the simplified configuration with appreciable reduction in switch count and, posses an ability to serve an alternative to cascaded H-bridge (CHB) MLI. However, extreme reduction in switch count of T-type topology has limited its switching redundancies and created critical dc-link voltage balancing issues in closed-loop applications. In addition, conventional multi-reference PWM scheme reported for T-type produces poor line-voltage total harmonic distortion (THD). Therefore, in this paper, a five-level T-type topology is presented, which involves only one-third dc source requirement of conventional T-type and CHB. This will greatly reduce the dc-link voltage balancing issues and cost. Further, to improve the harmonic performance of conventional multi-reference PWM, a simple carrier-based modulation scheme is proposed. The open and closed performance on the proposed scheme is validated on Simulink and experimental environment considering five-level T-type configuration. To evaluate the dynamic performance of developed T-type configuration, a three-phase three-wire (3P3W) distributed static compensator (DSTATCOM) application is considered, where its ability to eliminate source current harmonics, reactive power and load unbalance is investigated. To promote the superiority of the developed T-type topology, its cost comparison with conventional T-type and CHB is presented.

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**KEYWORDS**
Cascaded H bridge (CHB); diode clamped multilevel inverter (DCMLI); multi-reference PWM; level shifted PWM (LSPWM); total harmonic distortion (THD) and T-type topology

## 1. Introduction

For high power, medium voltage applications, power converters involving dc-link are very successful over direct AC-AC converters. Based on the arrangement of dc-link and the nature of switching devices, these converters are classified as current source (CSI) and voltage source (VSI) converter/inverter. However high efficiency, low initial cost, and small physical size of VSI acted as pre-dominant factors over CSI, and gathered more attention. The poor harmonic performance, high device ratings and requirement of large input/output filters limited the implementation of two-level inverters for high power, medium-voltage applications. Alternative solutions reported for high-power converters with

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reduced filtering requirements can be broadly divided into two categories, i.e., Multi-pulse and Multi-level inverters (Singh et al., 2004). Multi-pulse inverters require complex phase-shifting transformers, which increases its size, cost and complexity and thus limiting its applications. On the other hand, multilevel inverters (MLI) use the concept of adding multiple small dc-voltage sources through appropriate switching action, to produce a staircase output voltage of higher magnitude. The advent of self-commutating devices provoked the ability to MLI to cope up for high/medium power application with matured medium power electronic devices, boosting their market penetration. MLIs offer multiple advantages such as is reduction in d$v$/d$t$, electromagnetic interference and Total Harmonic Distortion, reduced common mode voltages and reduced filtering requirements (Franquelo et al., 2008; Parker et al., 2013; Rodriguez et al., 2009, 2007; Young et al., 2013).

MLIs are used for wide range of applications like medium-voltage drives, front end converters, grid connected/PV systems, active power filters and custom power devices (Singh et al., 1999). In literature, Cascaded H bridge (CHB), Diode clamped (DCMLI) and Flying capacitor (FCMLI) are the widely accepted classical Topologies of MLIs which gathered much attention both from academia & industry (Baker, 1980; Baker & Bannister et al., 1975; Debnath et al., 2015; Nabae et al., 1981). Various modulation techniques are developed to implement these classical topologies (Meynard & Foch, 1992; Rashid, 2013), among which Sinusoidal pulse width modulation (SPWM) turned to be more popular, due to its simplified carrier-based switching strategy (Mohan & Undeland et al., 2003; Sreenivasarao et al., 2014). Even though MLIs are applicable for any level, in practice its application is limited to five-level in motor drives and, eleven-level in medium/high voltage grid-connected systems and active filters applications. This is due to increase in the switch count with increase in number of levels, increases not only the requirements of power circuit but also effects the gate drive requirements such as protection circuits, heat sinks and controller requirements. Further turns the topology complex and raises the overall cost of the inverter.

From past two decades, there is an extreme exploration carried out to evolve newer MLI topologies with reduced switch count (Babaei, 2008; Babaei et al., 2015; Bana et al., 2019; Behara, Sandeep, Yaragatti et al., 2018a, 2018b; Ceglia et al., 2006; Gui-Jia, 2005; Gupta & Jain, 2014; Gupta et al., 2016; Li et al., 2012; Méllo & Jacobina, 2018; Naik et al., 2018; Najafi & Yatim, 2012; Omer et al., 2020; Park et al., 2003; Rahim et al., 2011; Rahul Sanjeevan et al., 2016; Salmon et al., 2009; Samadaei et al., 2016; Sanjeevan et al., 2016; Satish Naik et al., 2018). Among them, T-type is the most simplified configuration with appreciable reduction in switch count (Ceglia et al., 2006). The structural arrangement of T-type involves dc-link connected with bi-directional switches is followed by half/full bridge structure (Ceglia et al., 2006). It is to be noted that self-commutating switching devices available for high-power medium voltage applications such as MLIs are only unidirectional devices. These unidirectional devices possess unidirectional current conducting and bi-directional voltage blocking ability. However in RSC-MLIs, popular switch arrangement to meet the requirement of bi-directional switch is by connecting two unidirectional switches (such as IGBT) in anti-series combination.

A single-phase seven-level T-type (full-bridge structure) converter for grid-connected system is reported in (Ceglia et al., 2006). A three-phase three-level (half-leg) T-type MLI for renewable energy system is reported in (Behara, Sandeep, Yaragatti et

al., 2018a). A three-phase three-level (half-leg) T-type topology using space vector modulation with fault-tolerant control strategy is reported in (Choi et al., 2015; Do et al., 2020; Martins et al., 2006; Zhou et al., 2020). Among T-type half and full-bridge structures, the full-bridge structure offers magnificent reduction in switch count of around 25% for five-level and at least 41% for higher levels. On average, T-type provides 37.5% reduction as compared to the classical topologies (Gupta et al., 2016; Mohan & Undeland et al., 2003; Sreenivasarao et al., 2014). This configuration is well reported for grid-connected PV applications (Bana et al., 2019; Ceglia et al., 2006; Gupta et al., 2016; Omer et al., 2020). It is to be noted that though T-type with full-bridge configuration is very well implemented for single-phase systems, however its implementation to three-phase involves a separate dc-link for each phase, which increases the requirement of dc-sources.

In literature, to reduce the requirement of dc-source and switch count, various transformer-based configurations are reported in (Babaei et al., 2015; Li et al., 2012; Naik et al., 2018; Park et al., 2003; Salmon et al., 2009; Samadaei et al., 2016; Satish Naik et al., 2018). In (Park et al., 2003; Samadaei et al., 2016), transformer-based two-phase configurations are reported; where a Scott connected transformer is incorporated following a topology with two-phase structure. The incorporated Scott transformer converts obtained two-phase voltages (from topology) to three-phase. Excluding the Scott transformer, these configurations are effective with simplified topological structure. However, involvement of Scott transformer imposes design constraints and increases inverter cost and complexity for medium/high voltage applications. In (Li et al., 2012; Naik et al., 2018; Satish Naik et al., 2018), transformer-based configurations are reported to reduce the dc-source requirement by incorporating an isolation transformer on each phase of the converter. In detail, these configurations attempt to connect the dc-bus of all phases to a common dc-link, by incorporating a single-phase transformer on AC-side of each phase. These configurations neither effect topological modularity nor imposes design constraints.

This paper is motivated by the concept of transformer-based configurations where an isolation transformer is incorporated on each phase of the topology to reduce the requirement of dc-sources. This paper considers T-type full-bridge configuration and refers as generic word of T-type topology. On the other hand, appreciable reduction in switch count T-type has limited the switching redundancies such that, popular SPWM of MLIs can no more be applicable to RSC-MLI. In literature multi-reference modulation scheme is used to implement the Single-phase T-type MLI topology, but it is observed that implementation of multi-reference control to three-phase T-type topology results in more THD compared to the classical topologies with LSPWM (Gupta et al., 2016; Behara, Sandeep, Yaragatti et al., 2018b; Méllo & Jacobina, 2018).

Therefore with the keen review of the literature, it can be stated that,

(1) Appreciable reduction in switch count of T-type has drastically limited the switching redundancies, and imposed dc-link voltage balancing issues.
(2) Though, LSPWM-IPD is the most popular scheme among classical MLIs such as DCMLI and CHB, its implementation to RSC-MLI such as T-type is limited due to the absence of redundancies in the configuration (Gui-Jia, 2005).
(3) Popular multi-reference PWM reported for T-type is scalable for higher levels, but produces poor line-voltage THD performance (Gui-Jia, 2005).

(4) Modified multi-reference PWM technique reported in Behara, Sandeep, Yaragatti et al. (2018b) produces improved harmonic profile, however, it is difficult to implement for closed-loop applications.
(5) The novel reduced carrier PWM technique reported in Behara, Sandeep, Yaragatti et al. (2018b) produces improved harmonic profile but the selected carrier frequency must be a multiple of three.
(6) Though T-type has effective reduction in switch count, involvement of separate dc-link for each phase increases its control complexity for DSTATCOM applications.

To address the above issues, this paper presents a transformer-based three-phase five-level T-type RSC-MLI by including an isolation transformer at AC-side is incorporated on each phase. This imposes a common dc-link for all phases reducing the required dc-sources by 2/3$^{rd}$ with respect to the conventional T-type configurations. Further to improve the degraded harmonic performance of conventional scheme (multi reference) of T-type, an alternate multi-carrier scheme is proposed in this paper.

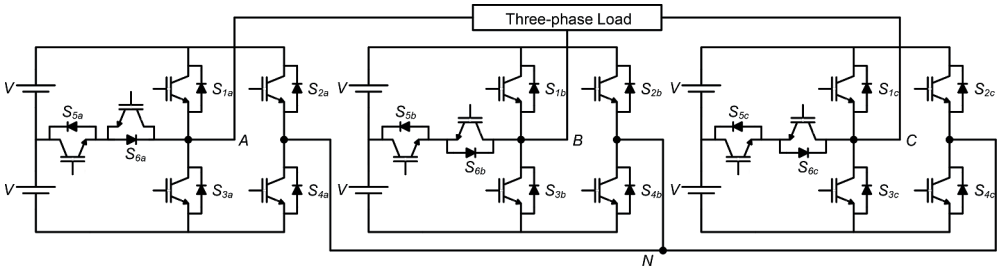
The key contributions of this work are

(1) A transformer-based five-level T-type configuration with reduced dc-source requirement is presented.
(2) The observation of degraded harmonic profile of conventional scheme of T-type i.e., multi-reference is presented.
(3) A simplified carrier-based PWM scheme is proposed, which can be easily scalable and produces good harmonic profile as similar to LSPWM-IPD.
(4) Superior performance of the proposed scheme over the conventional multi-reference is validated both on Simulink and experimental environment.
(5) The closed loop performance of the considered topology with proposed scheme is demonstrated for three-phase four-wire DSTATCOM application.

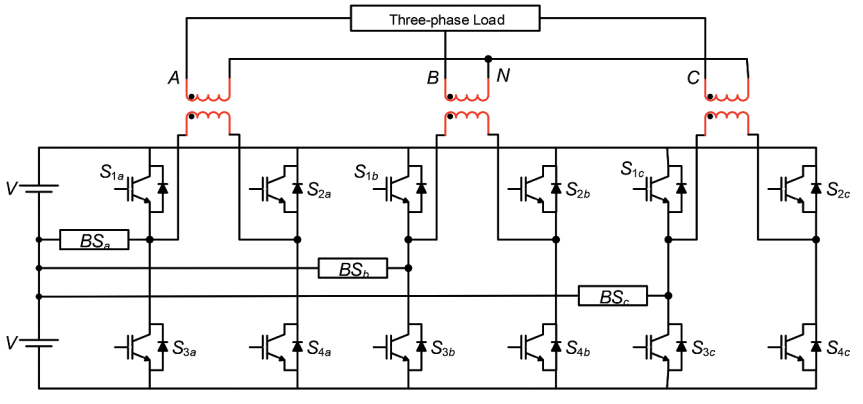
The organisation of this paper is as follows. In Sec-II, the topological configuration of five-level T-type RSC-MLI with reduced dc-source arrangement is presented and its operation is explained. In Sec-III, the degraded line THD performance of conventional multi-reference PWM is addressed, and the proposed modulation scheme and its implementation for five-level are presented. Also the improved harmonic performance of the proposed scheme is validated on both Simulink and experimental environment. In Sec-IV, a three-phase four DSTATCOM is developed to estimate the closed performance of the proposed scheme. Finally in Sec-V, the closed performance of the consider topology with conventional and proposed schemes, for dynamic variation in load is demonstrated in MATLAB environment.

## 2. T-type Topology

The Structural arrangement of five-level T-type configuration is shown in Figure 1(a). Depending on the way dc-link is connected, there are two possible configurations of three-phase T-type (full-bridge topology). The structural arrangement of these five-level T-type configurations is shown in Figure 1(a) and (b). This T-type topology is the congregation of bidirectional and uni-directional switches. Four unidirectional switches $S_1$, $S_2$,




(a) A five-level conventional T-type arrangement.




(b) Modified five-level T-type arrangement with common dc link.

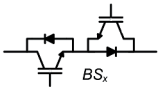



**Figure 1.** Three-phase five-level T-type topologies and bidirectional switch arrangement.

$S_3$, and $S_4$ are connected to form an H-bridge as shown in Figure 1(a) & 1(b). The dc supply is connected to H-bridge through the bidirectional switches. Equivalent of bidirectional switch (BS) is shown in Figure 1(c). Increase in the number of dc source and bi-directional switches increases the voltage levels, but the switches in H-bridge remain unaltered. However, the performance of both the configurations remains same, but the selection of the configuration should be wisely made depending on the application.

***Separate DC link for each phase:*** Each phase is fed from separate dc source, and the three-phase load can be connected as shown in Figure 1(a). All the three phases operate independently and this configuration will be best suited for grid-connected photovoltaic (PV) applications. This topology has an advantage of obtaining independent operation of the three phases and has the flexibility to connect three-phase load directly without the requirement of any auxiliary devices.

***Common DC link***: As the levels increase, not only the requirement of switches increases, but also the requirement of the dc voltage sources (capacitors) also increases. So, here an attempt is made to reduce the requirement of voltage sources, by feeding all the three phases from the same dc supply, which is shown in Figure 1(c). Since the T type operates all the phases independently, a neutral point on the load side should be formed such that voltage obtained on the one phase should not ruin the voltage of other. Therefore, an

Table 1. Switching operation of five-level T-type RSC-MLI.

| Switches in conduction | Voltage level ($v_{an}$) |
|---|---|
| $S_{5a}$ and $S_{4a}$ | $+V$ |
| $S_{1a}$ and $S_{4a}$ | $+2\ V$ |
| ($S_{1a}$ and $S_{2a}$) or ($S_{3a}$ and $S_{4a}$) | 0 |
| $S_{6a}$ and $S_{2a}$ | $-V$ |
| $S_{3a}$ and $S_{2a}$ | $-2\ V$ |

isolation transformer of 1:1 ratio is introduced to connect three-phase load. Intention of this transformer is to operate all the phases independently and to create a load neutral point through isolation, reducing the dc-source requirement. This prime advantage of Figure 1(b) is its reduction in dc source requirement by 2/3$^{rd}$ with respect to Figure 1(a), offering an alternative for DCMLI configurations for DSTATCOM applications.

***Operation of five-level T-topology:*** For five-levels in phase voltage, the levels to be obtained are 2 *V*, *V*, 0, –*V*, –2 *V*, where *V* is the voltage across each DC each source (Hari Priya et al., 2017). In every phase $S_4$ and $S_2$ are responsible for obtaining positive and negative levels respectively. To obtain the 2 *V*, –2 *V* levels $S_1$ and $S_3$ are operated respectively. +*V* and –*V* are obtained by operating $S_5$ and $S_6$ respectively. Levels obtaining by operating switches in phase-*a* are shown in Table 1. Operation of all the three phases is identical with its phase voltage displaced by 120° with each other.

To obtain '*m*' levels in phase voltage and (2 *m*–1) levels in line, (4+(*m*–3)) switches are required for each phase. Here, 4 indicates number of uni-directional switches to form H-bridge and, (*m*–3) indicates the required number of bi-directional switches.

## 3. Modulation Scheme

Absence of switching redundancies in T-type configuration limits its implementation with conventional SPWM such as LSPWM and PSPWM schemes. In addition, multi-reference modulation scheme popularly reported to control this T-type configuration, is generalised modulation scheme, which can be scalable for any number of levels. However this scheme is proved to produce produces poor line-THD performance. This is demonstrated by comparative line-voltage THD performance shown in Figure 2, where the performance of conventional multi-reference modulation scheme on a five-level T-type with respect to the LSPWM-IPD scheme on five-level DCMLI for $m_f = 30$ at different modulation indices ($m_a$) is presented. The degraded performance of multi-reference PWM is due to its inherent switching operation due to carrier arrangement is similar to LSPWM-OPD (Gui-Jia, 2005).

Therefore, a simple multi-carrier PWM with LSPWM-IPD carrier arrangement is proposed in this paper, and its switching action is modified such that the proposed scheme is easily scalable like multi-reference PWM and, provides improved harmonic performance like LSPWM-IPD.

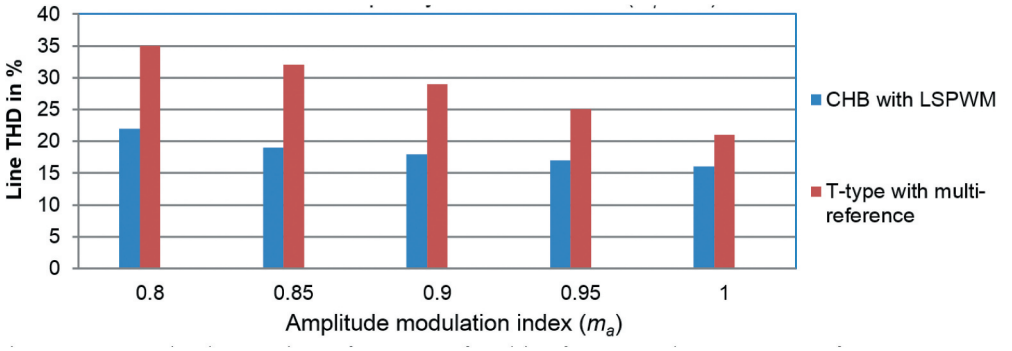



Figure 2. Comparative harmonic performance of multi-reference and LSPWM-IPD for $m_f = 30$.

### 3.1 Proposed switching logic with multiple level shifted carriers

The proposed multi-carrier modulation scheme uses ($m$–1) carrier signals and one reference signal to obtain '$m$' levels in phase voltage. Position of carriers is similar to LSPWM; however, the switching logic is modified to meet the required switching operation of the T-type configuration.

***Implementation for five-level***: Arrangement of carrier of this PWM to a five-level inverter is shown in Figure 3, considering carrier frequency as 1.5 kHz and $m_a$ as 0.95. In this scheme, the switching action is modified such that pulses obtained by comparing carrier and reference signal remains active only the reference is in the carrier limits of respective carrier. With this switching logic, the active switching band obtained by comparing carrier$_2$ and reference is responsible to produce a voltage band between V and 2 V in phase-voltage. Similarly, active switching band obtained by comparing carrier$_1$ and reference produces a band between 0 and V in phase-voltage. Similar switching action is carried out for carrier$_3$ and carrier$_4$ to produce the voltage levels 0 to –V and, –V to –2 V in output voltage. This switching logic to attain five-level phase voltage is shown in Figure 4, and application of these extracted pulses to obtain desired operation T-type converter is shown in Table 2.

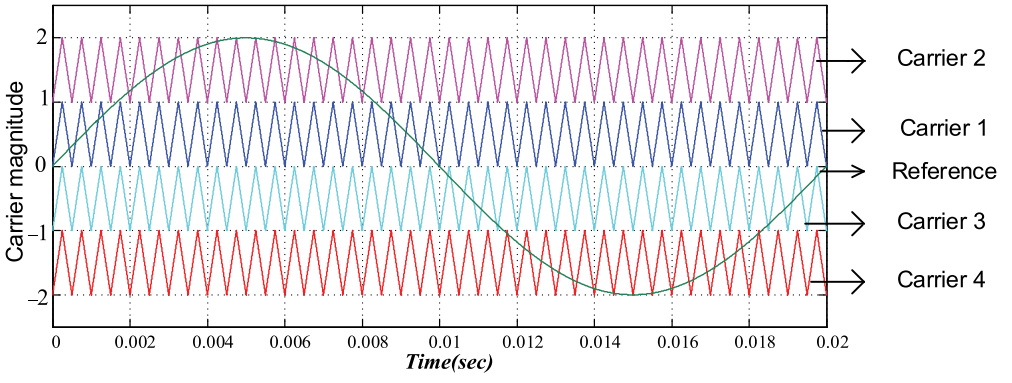



Figure 3. Carrier arrangement for the proposed multi-carrier modulation scheme for five-level inverter.

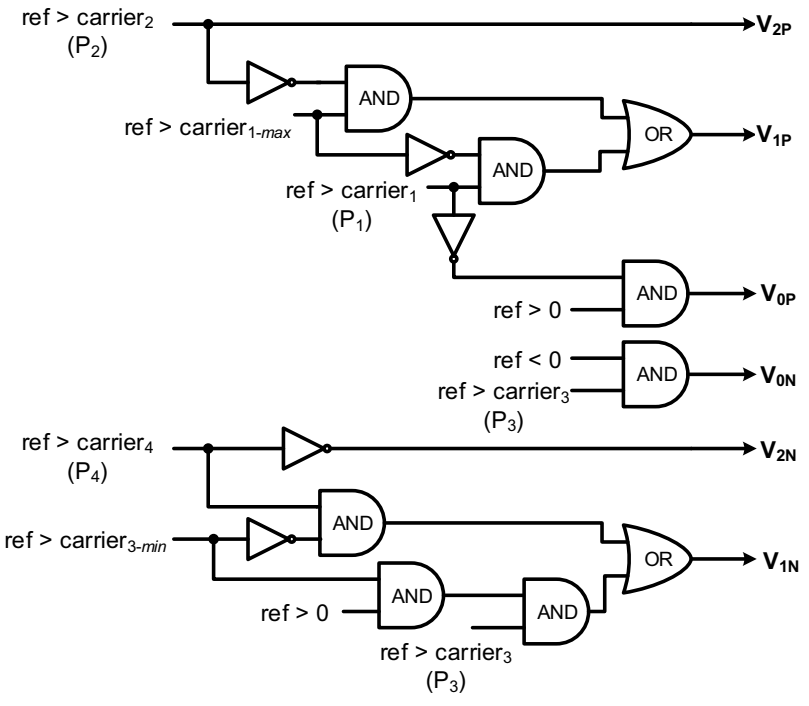



Figure 4. Proposed switching logic to obtain switching pulses to control a five-level inverter.

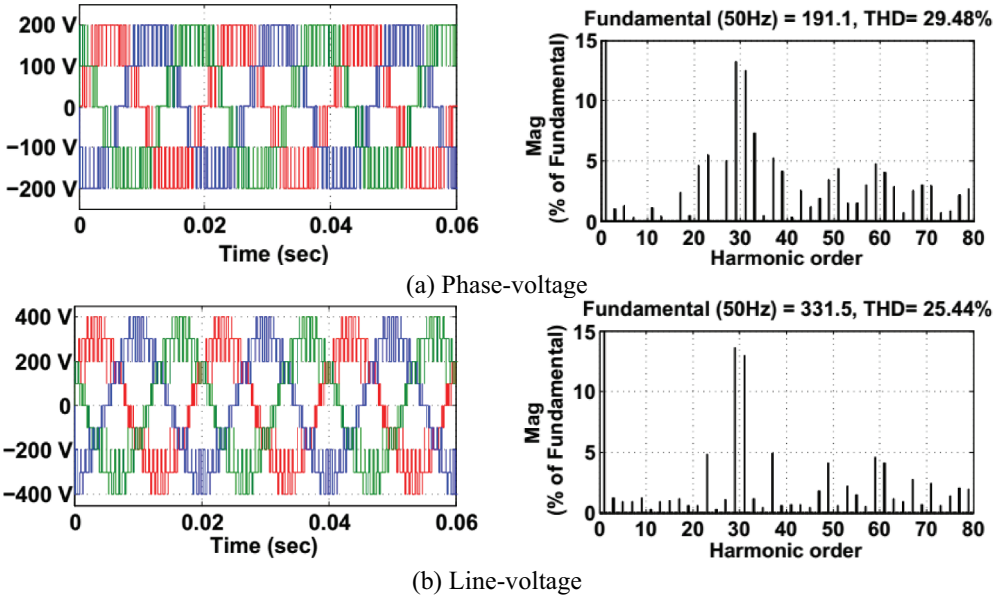
Table 2. Direction of obtained switching pulses (proposed PWM) to control five-level T-type inverter.

| Switch | Pulse applied | Remarks: Switch purpose – level involved |
|---|---|---|
| $S_1$ | $P_2 + P_{0n}$ | $S_1$ responsible for +2 V and zero level in phase-voltage. $S_1$ should be ON either if $P_2$ is high or $P_{0n}$ is high. |
| $S_2$ | $P_n$ | $S_2$ responsible for negative levels in phase-voltage. $S_1$ should be ON, if $P_n$ is high |
| $S_3$ | $P_4 + P_{0p}$ | $S_3$ responsible for 2 V and zero level in phase-voltage. $S_3$ should be ON, either if $P_4$ is high or $P_{0p}$ is high. |
| $S_4$ | $P_p$ | $S_2$ responsible for positive levels in phase-voltage. $S_1$ should be ON if $P_p$ is high |
| $S_5$ | $P_1$ | $S_5$ responsible for +V level; $S_5$ should be ON if $P_1$ is high |
| $S_6$ | $P_3$ | $S_6$ responsible for V level; $S_6$ should be ON if $P_3$ is high |

### 3.2 Simulation Performance of proposed modulation scheme

To investigate the performance of proposed switching logic and validate its superior performance with the conventional multi-reference modulation scheme, a three-phase five-level T-type inverter shown in Figure 1(b) is simulated in MATLAB. Each dc source voltage of 100 V and an *RL* load of 2 kW, 0.9 power factor (PF) are considered. Simulation is carried out at amplitude modulation index ($m_a$) of 0.95 and ($m_f$) as 30.

The line and voltage performance of considered configuration with conventional and proposed switching scheme are shown in Figure 5 and Figure 6 respectively. Further their comparative line-harmonic performance for various modulation indices is shown in Figure

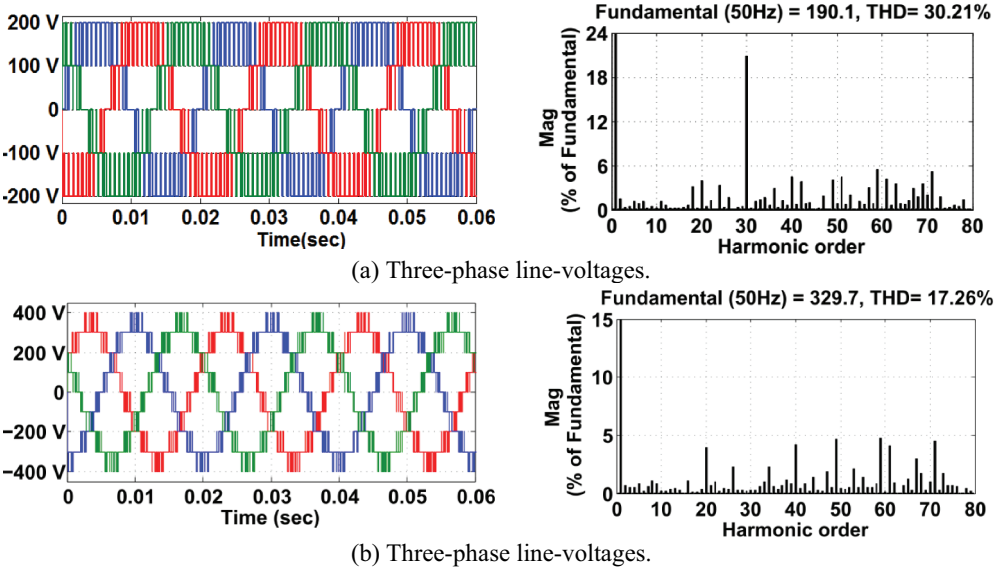



(a) Phase-voltage

(b) Line-voltage

Figure 5. Performance of five-level T-type RSC-MLI with multi-reference modulation scheme.

7. Figs. 5, 6 and 7 infer the superior harmonic performance of proposed multi-carrier modulation scheme over the conventional multireference PWM scheme.




(a) Three-phase line-voltages.

(b) Three-phase line-voltages.

Figure 6. Performance of five-level T-type RSC-MLI with proposed modulation scheme.

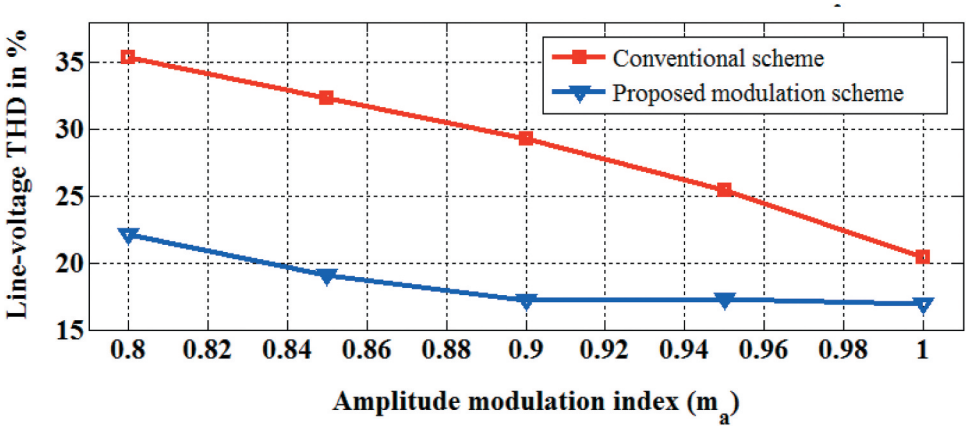



Figure 7. Comparative THD performance of proposed and conventional schemes on a three-phase five-level T-type inverter for $m_f = 30$.

### 3.3 Experimental Performance of proposed modulation scheme

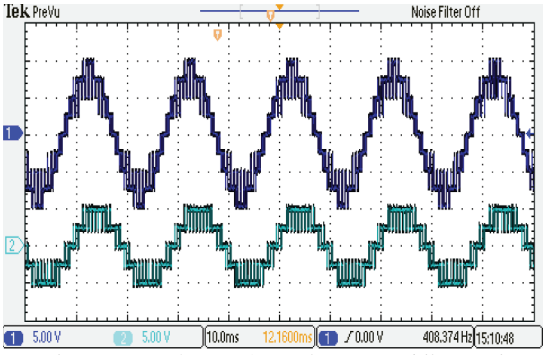
To validate the performance of proposed scheme experimentally, a prototype of a five-level T-type RSC-MLI is developed with generalised 24 switch IGBT inverter module. The considered experimental parameters to develop a prototype of five–level T-type RSC-MLI are given in Table 3.

Firing pulses for switching devices are obtained from dPSACE-1104 R&D controller with dead-time delay of 1 $\mu$s. The input dc voltage to the prototype is provided by isolated dc regulated power supplies (RPS). The experimental results are recorded for $m_f = 30$, $m_a = 0.95$ and controller sampling period of 50 $\mu$s. Experimental Performance of the developed three-phase five-level T-type inverter with the conventional and scheme is given in Figs. 8 and 9.

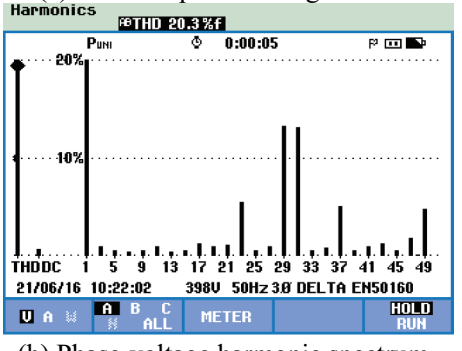
The experimental performance is shown in Fig. 8(a) and 9(a) infers that line-voltage levels obtained with proposed scheme remain clean and uniform, when compared to the conventional multi-reference PWM. Also as the experimental results are recorded at $m_f = 30$, the side band harmonics in the obtained phase and line-voltages are centred at $m_f$. Figure 9(b) shows the presence of dominant harmonic in phase-voltage at $m_f$ and, the magnitude of this dominant harmonic is suppressed in line-voltage shown in Figure 9 (c). This further reflects an appreciable difference in THD of phase-voltage (23.2%) and line-voltage (7.3%), however it is not in the case of multi-reference PWM. Further, comparing Figure 8(c) and Figure 9(c), infers that superior line-voltage voltage performance proposed scheme (7%) with respect to conventional scheme (23.4%).

Table 3. Experimental parameters.

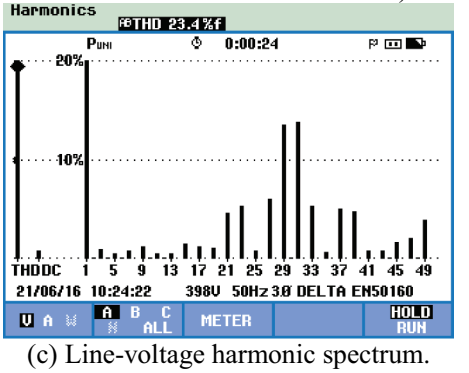
| Circuit | Component | Specification – Type |
|---|---|---|
| Input dc voltage | Isolated Regulated dc power supplies. | 25 V/5 A |
| Power circuit | Switching device (IGBT) with anti-parallel diode | 1200 V/40 A |
| Controller | dSPACE | DS1104 R&D Controller Board |
| | Sampling time | 50 $\mu$s |
| THD measurement | Power quality analyser | Fluke 435 Series II |




(a) Line and phase-voltage waveforms (X-axis: 10 ms/div. and Y-axis: 100 V/div.).




(b) Phase-voltage harmonic spectrum.




(c) Line-voltage harmonic spectrum.

Figure 8. Experimental performance of conventional multi-reference modulation scheme on five-level.

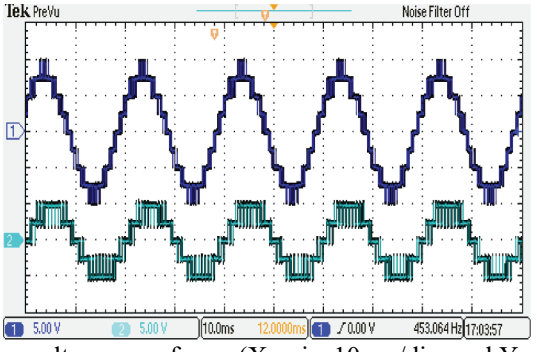
To estimate the closed loop performance of the proposed modulation scheme and to observe the dynamic performance of the three-phase five-level T-type topology, its implementation to three-phase four wire DSTATCOM application is considered in the next section.

## 4. Closed-loop performance: DSTATCOM Application

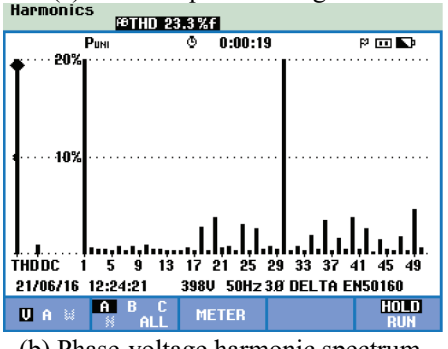
DSTATCOM is mostly used in distribution systems for the improvement of power quality when a nonlinear and unbalanced load is connected (Aboutaleb et al., 2019; Akagi, 1996; Akagi & Wantanble et al., 2017; Jian et al., 2019; Moreno-munoz, 2007; Singh et al., 2009). The efficient compensation depends on the extraction of the compensator reference currents.

### 4.1. Topology

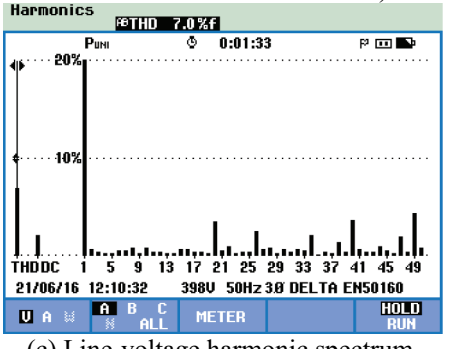
To track the reference currents effectively and to maintain the required dc-link voltage, multilevel inverters can be incorporated. Advantages of MLI in DSTATCOM are clearly reported (Akagi, 1996; Singh et al., 2009). A three-phase five-level T-type topology shown in Figure 1(c) is incorporated for implementing three-phase four-wire DSTATCOM as shown in Figure 10.




(a) Line and phase-voltage waveforms (X-axis: 10 ms/div. and Y-axis: 100 V/div.).




(b) Phase-voltage harmonic spectrum.




(c) Line-voltage harmonic spectrum.

**Figure 9.** Experimental performance of proposed PWM scheme on five-level T-type inverter.

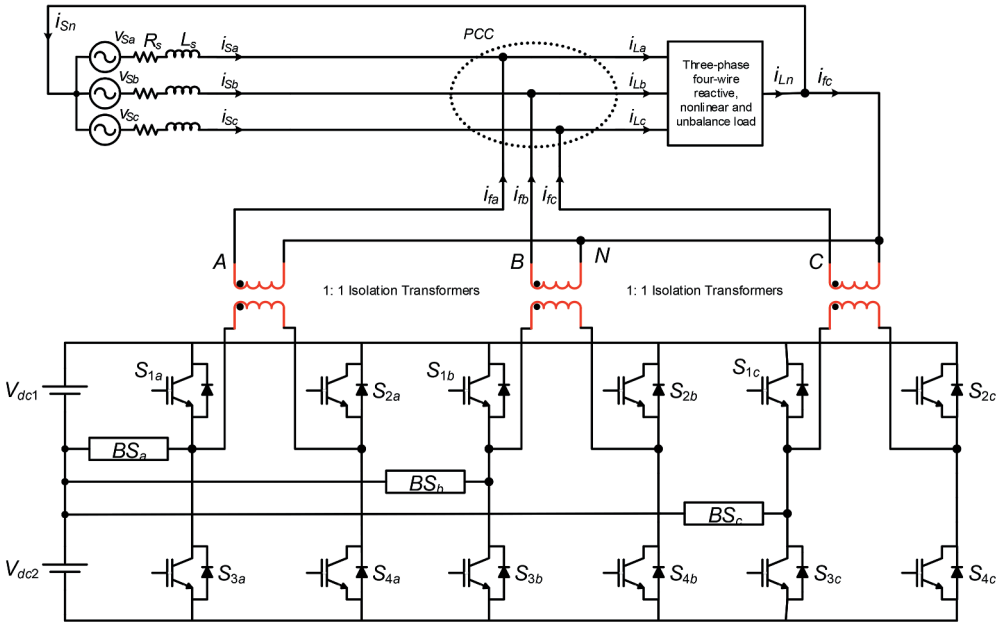



**Figure 10.** A three-phase four-wire DSTATCOM based on three-phase five-level T-type topology.

### 4.2. Control strategy

To extract the reference currents effectively, there are many control strategies reported in the literature (Behara, Sandeep, Yaragatti et al., 2018b; Choi et al., 2015; Martins et al., 2006; Méllo & Jacobina, 2018). Instantaneous *p-q* theory is used here, due to its simple methodology in extracting reference currents (Akagi & Wantanble et al., 2017).

***Instantaneous P-Q theory***: Power calculations through instantaneous values of voltage and current are introduced and time-domain analysis is performed to analyse the system non-linearity. Let $v_a$,$v_b$ and $v_c$, are the Instantaneous load voltages and $i_a$, $i_b$ and $i_c$ be the load Instantaneous currents which are converted to the $v_\alpha$, $v_\beta$ and $v_0$ and $i_\alpha$, $i_\beta$ and $i_0$ respectively by Clark's transformation and Instantaneous powers are calculated. DSTATCOM will compensate for the load reactive power component and regulates the dc-link voltage.

$$i_{f0} = i_0 \tag{1}$$

$$i_{f\alpha} = \frac{p_f v_\alpha + v_\beta q_f}{v_\alpha v_\alpha + v_\beta v_\beta} \tag{2}$$

$$i_{f\beta} = \frac{p_f v_\beta - v_\alpha q_f}{v_\alpha v_\alpha + v_\beta v_\beta} \tag{3}$$

Filter currents in *αβ0* given in equation (1), (2) & (3) are converted to *abc* reference frame, using inverse Clark's transformation. These currents $i^*_{fa}$, $i^*_{fb}$ and $i^*_{fc}$ are the compensator reference currents or DSTATCOM reference currents. To compensate the load reactive component, compensator (DSTATCOM) currents should track the reference compensator currents.

### 4.3. Modulation scheme

Error between the reference compensator currents ($i^*_{fa}$, $i^*_{fb}$ and $i^*_{fc}$) and the actual DSTATCOM currents ($i_{fa}$, $i_{fb}$and $i_{fc}$) is processed through the PI controller to obtain the modulating signals for each phase respectively. This modulating signal acts as the reference signal for the PWM controller and the switching pattern is produced by comparing the carrier signal and the reference signal (modulating signal) by using proposed multi-carrier modulation scheme. Switching operation of the power semiconductor devices automatically forces the DSTATCOM currents to follow the reference compensator currents. Closed loop performance of the proposed modulation scheme for DSTATCOM application is analysed in the next section.

## 5. Simulation Results

Simulink implementation of the three five-level T-type topology with proposed multi-carrier modulation scheme for three-phase four-wire DSTATCOM application carried out and its performance is analysed for various loading conditions. System parameters and loads considered for the implementation of DSTATCOM are given in Table 4 and Table 5.

Table 4. Parameters considered for the Simulink implementation of DSTATCOM.

| Parameter | Value |
|---|---|
| Dc-link voltage | 3 kV |
| Dc capacitor | 4000 μF |
| Coupling Inductor (provided by transformer) | 2 mH |
| Switching frequency | 2 kHz |
| $K_p$ and $K_i$ (dc link voltage regulation loop) | 2 and 1 |
| Source line voltage (RMS) | 2.3 kV |
| Supply frequency | 50 Hz |
| Source impedance | $R$ = 0.1 Ω and $L$ = 1 μH |

Table 5. Linear and Non-Linear loads for the Simulink implementation of DSTATCOM.

| Parameter | Value |
|---|---|
| 3-ph full controlled converter with *RL* load ($\alpha$ = 30°) | $R$ = 200 Ω & $L$ = 150 mH |
| 3-ph diode bridge rectifier with *RL* load | $R$ = 50 Ω & $L$ = 50 mH |
| 1-ph full controlled converter (b-n) with *RL* load ($\alpha$ = 30°) | $R$ = 70 Ω & $L$ = 50 mH |
| 1-ph fully controlled converter (c-n) with *RL* load ($\alpha$ = 30°) | $R$ = 70 Ω & $L$ = 48 mH |
| *RL* load (A ph – N) | $R$ = 150 Ω & $L$ = 300 mH |
| *RL* load (B ph – N) | $R$ = 100 Ω |
| *RL* load (C ph – N) | $R$ = 50 Ω & $L$ = 50 mH |

Combinations of various linear and non-linear loads are considered to analyse the dynamic performance of the DSTATCOM. Initially all the loads are considered (except three diode bridge rectifier load) to be acting on the system. Variations in load condition are created by switching the three-phase diode bridge rectifier load.

### 5.1 Performance of DSTATCOM is analysed for various load conditions

For the simulation time of 0.6 s, various loads are conditions and the steady-state and dynamic state performance is analysed with and without compensator. Sample time is considered as 1 μs.

#### 5.1.1 Case I: Steady-state performance

The steady performance of the overall system shown in Figure 11 carried out before and after compensation can be explained under two cases.

##### 5.1.1.1 Without compensator: $0 < t < 0.05$ s

In this case, system performance is observed without compensator. Load is assumed to be the combination of unbalanced linear and nonlinear loads. Initially, all the loads are assumed to be connected to the system except three-phase diode bridge rectifier load. So, the loads connected are a three-phase full controlled converter, single-phase full controlled converter (between b phase and neutral), single-phase fully controlled converter (between c phase and neutral), and an unbalanced linear *RL* load. During this period, since the compensator is not connected to PCC, the source currents are equal to load currents and compensator (actual) currents are zero. This can be observed in Figure 11(b), 11(c), 11(d). Also as there is no compensation, source neutral current is equal to the load neutral current which can observed from Figure 11(e) & 11(f). Voltage across the dc

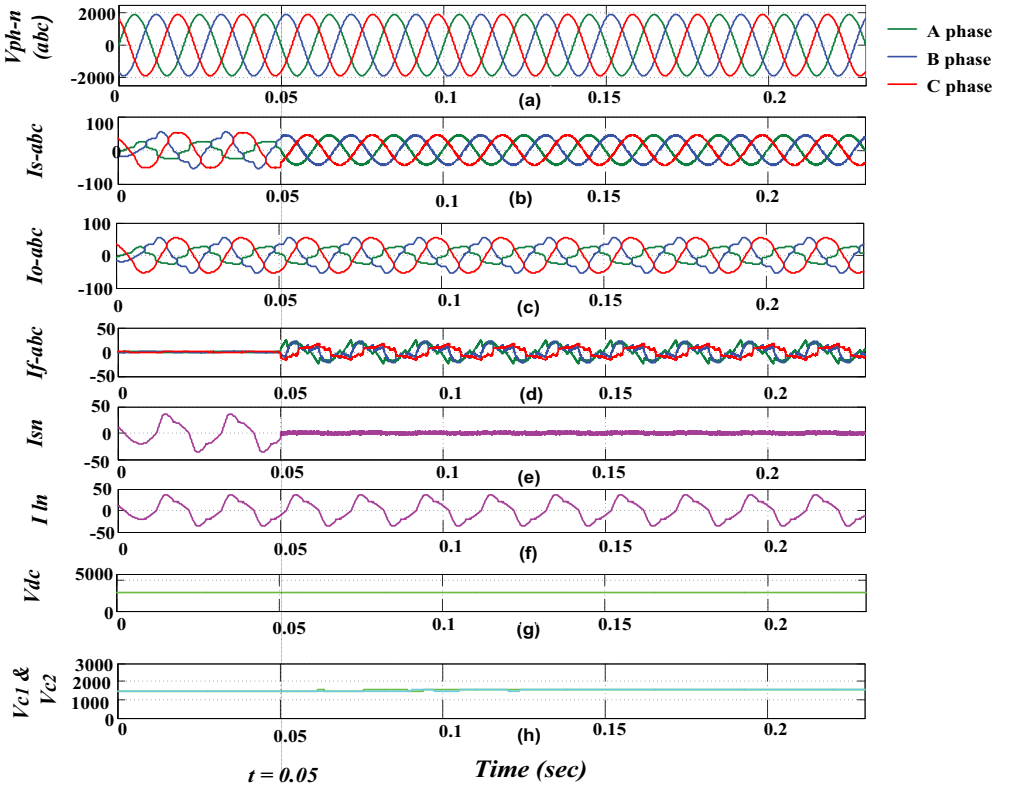



Figure 11. Steady-state performance of five-level T-type based DSTATCOM with proposed modulation scheme. (a) Three-phase supply voltages (b) Source currents (c) Load currents (d) DSTATCOM currents (e) Supply neutral current (f) Load neutral current (g) dc-link voltage and (h) Voltage across dc-link capacitors.

link is maintained to be 1.6 times of $V_{ph\text{-}peak}$ . Voltage across DC link capacitors is considered to be pre-charged to 95% of $V_{dc}$ as shown in Figure 11(g) with its dc-link capacitors balanced Figure 11(h).

#### *5.1.1.2 With Compensator:* 0.05 s < t < 0.24 s

At t = 0.05 s, compensator is switched on without any load change, i.e., load in this case remains to be same as in the previous case. By the instant compensator is switched on, switches in the compensator are operated such that the filter currents tracks the reference currents. Figure 11(b) depicts that compensator takes less than half a cycle to make the supply currents balanced and supports the load reactive component. From Figure 11(e) and 11(f) shows the decrease in the source neutral current after connecting DSTATCOM and dc-link capacitors remains to be balanced refer to Figure 11(e) and 11(f).

The closed performance of the proposed modulation scheme for DSTATCOM application is shown in Figure 12. This is the switching comparison observed for one cycle (T = 0.02 s) in phase-A, after the DSTATCOM is turned on in *case*-1. Error between the reference filter current and actual filter current of phase-A acts as a reference signal for the modulation scheme.

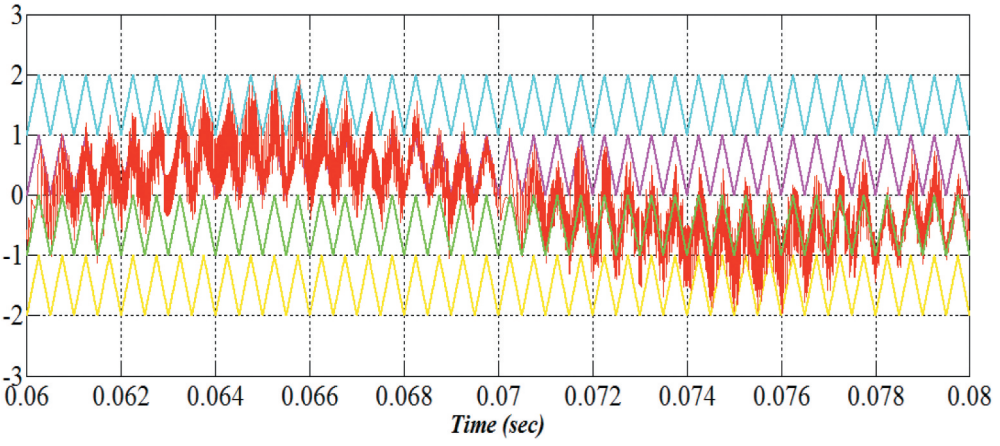



Figure 12. Performance of the proposed modulation scheme in DSTATCOM application.

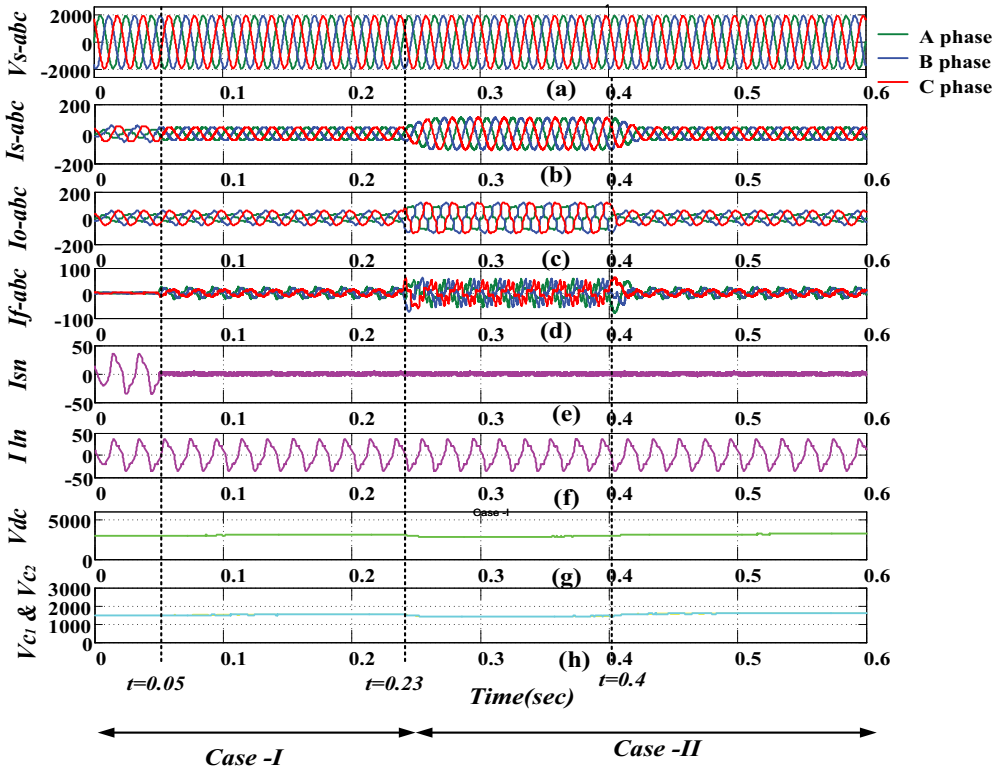



Figure 13. Simulation results for three-phase five-level T-type topology with proposed modulation in three-phase four-wire DSTATCOM for variation loads: (a) Three-phase supply voltages, (b) Source currents, (c) Load currents, (d) DSTATCOM currents, (e) Supply neutral current, (f) Load neutral current, (g) Dc-link voltage and (h) Voltage across dc-link capacitors.

***Case II: Dynamic performance of DSTATCOM with load variations:*** Figure 13 depicts the dynamic performance of the system for load variation. Variation in load is created by

Table 6. Source-current (shown for phase-a) harmonic Performance of five-level T-type DSTATCOM with conventional and proposed schemes.

| Modulation scheme | without DSTATCOM | with DSTATCOM | | |
|---|---|---|---|---|
| | THD of phase-*a* | 0 < t < 0.24 s THD of phase-*a* | 0.23 s < t < 0.4 s THD of phase-*a* | 0.4 s < t < 0.6 s THD of phase-*a* |
| Multi reference PWM | 25% | 3.12% | 2.03% | 3.19% |
| Proposed PWM | 25% | 1.5% | 0.61% | 1.62% |

the addition of the three-phase diode bridge rectifier load before and after compensation is explained here under.

#### *5.1.1.3 Compensator with decrease in load: 0.24 s < t < 0.4 s*

At $t = 0.24$ s, three-phase diode bridge rectifier is connected (in parallel), to observe the dynamic performance of the compensator by sudden reduction in the load. This can be observed by increase in the magnitudes of load and source currents (Figure 13(c) & 13(b)). Voltage across both the dc-link capacitors remains to be balanced (Figure 13(h)) but in dc-link voltage drops by 5–8% (acceptable range) due to the sudden change in the load Figure 13(g).

#### *5.1.1.4 Compensator with increase in load: 0.4 s < t < 0.6 s*

At $t = 0.4$ s, load is increased, with the disconnection of three-phase diode bridge rectifier. This can be observed by decrease in the magnitudes of load current and source current (Figure 13(c) &13(b)). Voltage across the dc-link capacitors remains to be balanced Figure 13(h).

### *5.2 THD analysis for load variation*

THD analysis of source currents in three-phase four-wire DSTATCOM involving T-type configuration operating with conventional and proposed switching scheme is carried out and is shown in Table 6. It is observed that proposed modulation scheme provides better compensation in THD than the conventional multi-reference scheme, for same system parameters and loading conditions.

## 6. Cost comparison with cascade H-bridge and conventional T-type based DSTATCOM

The proposed three-phase modified T-type DSTATCOM configuration is compared with cascade H-bridge and conventional T-type approaches. The cost comparison of modified T-type with cascade H-bridge and conventional T-type-based DSTATCOMs are given in Table 7. From this Table it is observed that the proposed modified T-type D-STATCOM requires less cost when compared to conventional T-type and CHB-based DSTATCOMs. A five-level CHB-based DSTATCOM require 24 switching devices and 6 dc capacitors with their associated voltage measuring sensors. The conventional T-type approach requires only 18 switches but it requires 6 dc capacitors with voltage sensors. Moreover, controlling the six capacitors in conventional T-type is a tedious task due to the absence of switching redundancies. Even though, the modified T-type approach also requires 18

Table 7. Cost comparison of five-level cascade H-bridge, conventional T-type and modified T-type based DSTATCOM configurations.

| Configuration | Five-level cascade H-bridge | Five-level conventional T-type | Modified T-type D-STATCOM |
|---|---|---|---|
| IGBT semi pack switch (SKM50GB12V, 1200 V and 50 A) | 5800*4*3 = 69,600 | 5983*3*3 = 53,847 | 5983*3*3 = 53,847 |
| DC capacitors with voltage sensor (4700 μF/450 V) B43743A5478M000 | 7288*6 = 43,728 | 7288*6 = 43,728 | 7288*2 = 14,576 |
| Heat sink cost (KL-2855, P3/300 mm) | 4000 | 3000 | 3000 |
| Skyper board (SKHI 10/12 R,1200 V and 8 A) | 9600*4*3 = 1,15,200 | 9600*3*3 = 86,400 | 9600*3*3 = 86,400 |
| Snubber capacitor (MP-4 1 F/1200 V dc H1 AD) | 400*4*3 = 4,800 | 400*3*3 = 3,600 | 400*3*3 = 3,600 |
| Coupling inductors (3 mH, 10A) | 2400*3 = 7,200 | 2400*3 = 7,200 | Not required |
| Isolation transformers (10 kVA, 1-phase, 1.6 kV/1.6kV) | Not compulsory | Not compulsory | 3*6000 = 18,000 |
| Total cost (INR) | 2,44,528 | 1,97,775 | 1,79,423 |

**Reference**: **https://www.semikron.com**. **(Apr. 2020)**

switching devices but only two dc capacitors are required. This will greatly reduce the control complexity of dc-link capacitors. The excess cost due to the presence of isolation transformer can be masked by the absence of coupling inductors and reduced cost of dc-link capacitors and voltage sensors.

## Conclusion

This paper presented a simplified carrier-based PWM scheme along with a three-phase T-type RSC-MLI topology with minimum dc-source requirement in closed-loop applications. The main conclusions are given below.

- This transformer-based T-type configuration effectively reduced the dc-link capacitors to one-third of conventional T-type and CHB topologies of same level.
- The presented simplified carrier-based PWM scheme addressed the degraded line-voltage THD performance of the conventional modulation scheme. This scheme can be easily extended to higher levels and applicable for any RSC-MLI topology.
- The simulation and experimental results proved the efficacy of the proposed PWM scheme.
- As the dc-link capacitors are reduced, in closed-loop applications such as DSTATCOM, an effective voltage balance among these capacitors was achieved with less computation burden.
- The obtained Simulink performance of five-level 3P4W DSTATCOM with proposed PWM scheme demonstrated the effective dynamic performance in balancing capacitor voltages and meeting the control objectives of DSTATCOM.
- The overall cost of the proposed DSTATCOM is reduced due to the reduction in number of switching devices, coupling inductors, reduction in dc-link capacitors and their associated voltage measuring sensors.

## Disclosure statement

No potential conflict of interest was reported by the authors.

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