A Two-Stage T-Type Hybrid Five-Level Transformerless Inverter for PV Applications

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***Abstract*—This article presents a two-stage T-type hybrid five-level transformerless inverter (TLI) for grid-connected photovoltaic (PV) applications. The proposed T-type hybrid five-level inverter and its level-shifted pulsewidth modulation scheme offers reduced leakage current by eliminating the high-frequency variations and sudden transitions in the voltage across PV parasitic capacitance C_{PV} and a path for the negative current in all the modes of operation under unity and nonunity power factor conditions of the grid without degrading the waveform quality. Moreover, in this article, the proposed inverter is integrated with a traditional three-level boost converter (3LBC) for boosting the lower PV voltage to higher dc-link voltage and also to extract maximum power from the PV source. The 3LBC provides high efficiency and reduced input inductor size for the same power rating over the conventional boost converter. The simulation results of the proposed system are presented using MATLAB software, and a 500-W experimental prototype is constructed and tested in the laboratory to validate the feasibility of the proposed configuration. Finally, a comparison of the proposed inverter with other five-level TLI topologies is presented to highlight its merits.**

***Index Terms*—Common-mode voltage (CMV), leakage current, level-shifted pulsewidth modulation (LSPWM), transformerless multilevel inverter (MLI).**

I. Introduction

RENEWABLE energy sources are gaining popularity to satisfy the increasing power demands while having a low impact on the ecosystem. Among all the renewable energy sources, photovoltaic (PV) power generation has acquired much more importance due to its rooftop implementation ability in small and medium power scales connected to the 1-φ grid. A line frequency transformer (LFT) is the most generally used device in the grid-connected PV applications for providing voltage boosting and galvanic isolation. However, the cost and bulkiness of the overall system increase with a reduction in efficiency [1], [2]. Therefore, many researchers have focused on transformerless operation, but it will introduce the issue of leakage current due to the parasitic capacitance C_{PV} of the PV source with respect to the ground. Generally, C_{PV} varies in the ranges of few tens of nanofarads to microfarads and depends on the environmental conditions and technology employed in PV cell manufacturing. The voltage that appears across C_{PV} causes the flow of leakage current into the system, which will introduce electromagnetic interference, affects the power quality and also endangers the operator's safety [3]. Therefore, it is essential to highlight the issue of leakage current in the absence of LFT for the PV power generation system.

To address the abovementioned problem, several transformerless inverters (TLIs) have been discussed in [4] and [5]. But very few inverters are associated with multilevel operation. Multilevel inverters (MLI) have significant advantages such as the high quality of power output by lowering the total harmonic distortion (THD), reduced losses with the reduction in voltage stress of the switches, reduced filter size, and increased modularity [6]. It is much more advantageous to have such benefits in PV power generation systems along with a reduction in leakage current. Various MLI topologies were proposed in [7], [8] to limit the leakage current in transformerless PV power generation systems. All these topologies employ two different methods for the reduction of leakage current. One approach is based on the elimination of high-frequency voltage variations across C_{PV}, while the other way is obtaining the sinusoidal voltage variation across C_{PV} by maintaining constant common-mode voltage (CMV).

In this context, a five-level full-bridge neutral-point-clamped (FBNPC) [9] TLI topology is proposed based on the elimination of high-frequency voltage variations across C_{PV}, as shown in Fig. 1(a). In this topology, CMV and the asymmetrical voltage generated by the placement of filter inductors (i.e., $L1 = L_{\mathrm{ac}}$ and $L2 = 0$) are added to nullify the high-frequency voltage variations across C_{PV}. However, the topology suffers from the disadvantages of more component count and increased power losses due to the conduction of at least four devices in each mode of the operation. Based on a similar concept, Vazquez *et al*. [10], [11] have proposed two different five-level TLI topologies named the H5-Heric and derived Heric topologies to reduce the leakage current and to improve the efficiency, as shown in Fig. 1(b) and (c), respectively. In both H5-Heric and derived Heric topologies, the high-frequency voltage variations across C_{PV} are eliminated as similar to the five-level FBNPC. Moreover, both the topologies utilize the same number of devices in the positive power transferring mode and also requires only one diode and one MOSFET during the freewheeling period. Therefore, these two topologies achieve higher efficiency as

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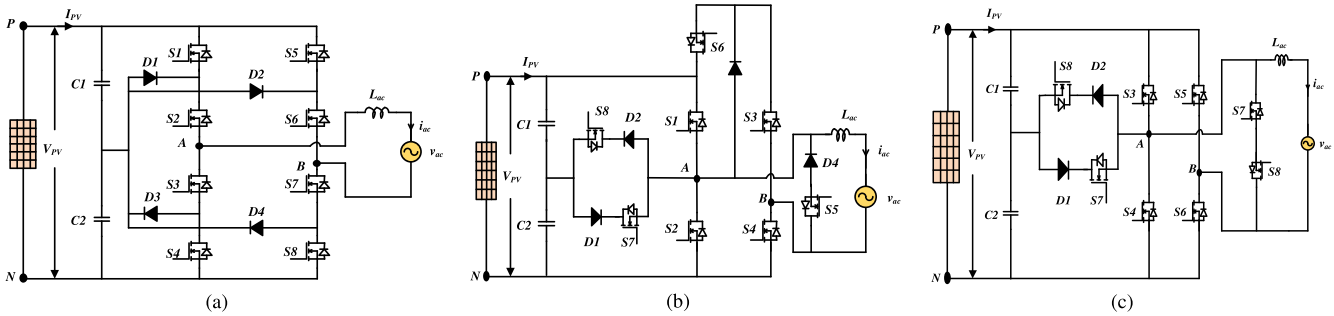


Fig. 1. Asymmetrical five-level TLI topologies. (a) FBNPC [9]. (b) H5-Heric [10]. (c) Derived Heric [11].

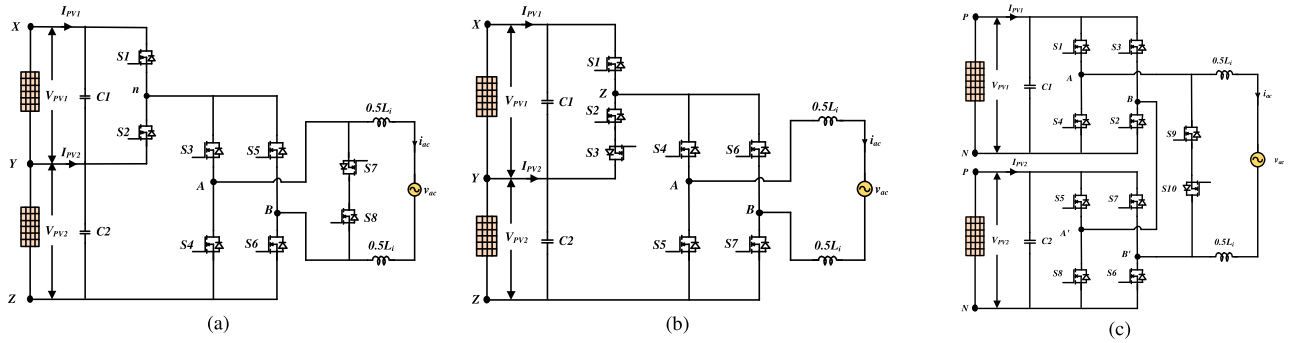


Fig. 2. Symmetrical five-level TLI topologies. (a) CMLI-1 [12]. (b) CMLI-2 [13]. (c) Derived CHB [14].

compared with the five-level FBNPC by reducing the conduction and switching losses of the power electronic devices.

However, in all the above three topologies, due to sudden transitions in the voltage across $C_{\rm PV}$ (i.e., from "$V_{\rm PV}$" to "0" and vice versa) with grid frequency variations causes a larger spike in the leakage current. Sometimes, the peak value of the leakage current exceeds DIN VDE0126-1-1 grid standard because of the large value of $C_{\rm PV}$ due to the intermittent nature of environmental conditions. Moreover, a bulky and expensive filter inductor is required to limit the high-frequency switching ripple in the grid current.

Another important method to reduce the leakage current is obtaining the sinusoidal voltage variation across $C_{\rm PV}$ by maintaining constant CMV. Two such interesting solutions are proposed by Jain *et al.* [12], [13], as shown in Fig. 2(a) and (b), respectively. In these two topologies, a novel pulsewidth modulation (PWM) strategy is proposed to obtain the near sinusoidal voltage variation across $C_{\rm PV}$ for minimizing the leakage current. Moreover, these MLIs are reliable candidates for high efficiency and reduced component count. However, the presence of sudden transitions in the voltage across $C_{\rm PV}$ while transferring from $\pm 0.5V_{\rm dc}$ level to $\pm V_{\rm dc}$ level and vice versa results in unwanted spikes in the leakage current. In addition, the proposed PWM switching scheme results in higher THD and output filter size. Based on a similar concept, another elegant solution is proposed by Moghaddam and Iman-Eini [14], as shown in Fig. 2(c). In this topology, two additional switches are added to the conventional cascaded H-bridge (CHB) inverter for obtaining the sinusoidal voltage variations across $C_{\rm PV}$ by using redundant states during the freewheeling period. However, this configuration has the disadvantage of increased component count and power losses.

Furthermore, the topologies proposed in [12]–[14] require two isolated PV sources for realizing the multilevel output, which increases the cost and complexity of the control system for tracking maximum PV power. Furthermore, all the above-said topologies [9]–[14] are mainly focused on the level generation and leakage current reduction for grid-connected PV system under unity power factor conditions only. However, the reactive power capability of the inverter is also an important requisite to penetrate the considerable amount of PV power into the grid as per the recent grid standards VDE-AR-N4105 [15].

From the above discussion, the authors are motivated to develop a new multilevel TLI for achieving minimum leakage current and reactive power control capability. The salient features of the proposed T-type hybrid five-level TLI and its modulation scheme are as follows:

1) clamps the inverter terminal voltages to half of the dc-link voltage during the freewheeling period for limiting the amplitude of high-frequency variations in CMV;
2) provides a common-mode conducting path from the midpoint of filter capacitors to the negative terminal of PV source for attenuating all the high-frequency variations and sudden transitions in voltage across $C_{\rm PV}$;
3) it allows a path for the negative current in all the modes of operation for providing reactive power control without affecting the quality of output waveforms;
4) a single PV source is sufficient to realize the five-level output. Thus, cost and control complexities in maximum power tracking (MPPT) are minimized;

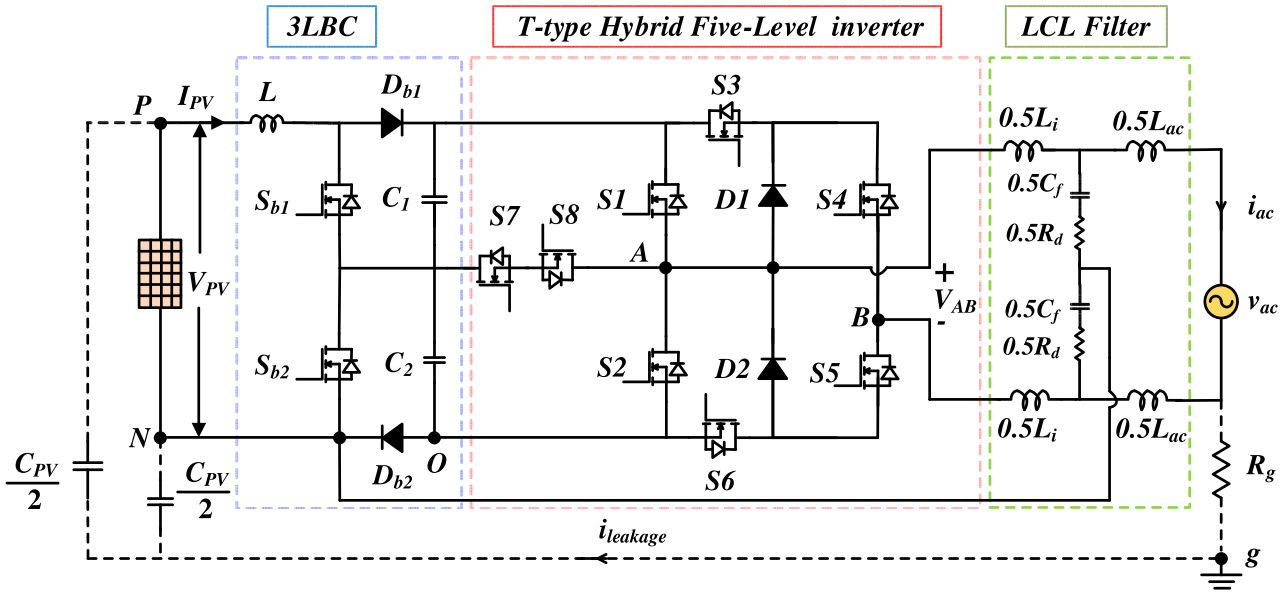


Fig. 3. Proposed two-stage T-type hybrid five-level TLI.

5) moreover, the proposed topology is an optimal tradeoff among other inverter topologies [9]–[14] in terms of leakage current reduction, reactive power control capability, and power losses in the semiconductor devices.

In addition to the above, the proposed inverter is integrated with a conventional three-level boost converter (3LBC) for boosting the lower PV voltage to higher dc-link voltage and also to extract maximum power from the PV source. Moreover, the two-stage operation of the inverter eliminates the demerits of single-stage systems, such as poor MPPT, imbalance in the power sharing of PV panels, and lower operational safety [16].

Furthermore, the manuscript is organized as follows. A brief description of the proposed two-stage system and front-end 3LBC is explained in Section II. Operating modes and control of the proposed inverter are discussed in Section III. CMV analysis is discussed in Section IV. Simulation results are presented in Section V. The experimental results of the proposed configuration are described in Section VI. The comparison of the proposed T-type hybrid five-level inverter with other recently proposed multilevel TLI topologies is presented in Section VII. Finally, the conclusion drawn from the article is discussed in Section VIII.

II. Proposed Two-Stage TLI

Fig. 3 depicts the schematic arrangement of the proposed two-stage inverter configuration. It comprises of a 3LBC followed by a proposed T-type hybrid five-level TLI with the symmetrical placement of the filter circuit. The 3LBC serves the functions of both voltage boosting and MPPT by employing a simple closed control system. Furthermore, the proposed inverter produces the output ac voltage by switching MOSFETs using level-shifted pulsewidth modulation (LSPWM) scheme, which enhances the inverter operation at all power factors without affecting the CMV. Moreover, the symmetrical placement of the *LCL* filter circuit provides a common-mode conducting path to the inverter for limiting the magnitude of leakage current below the grid standards. The operation and control of 3LBC are explained as follows.

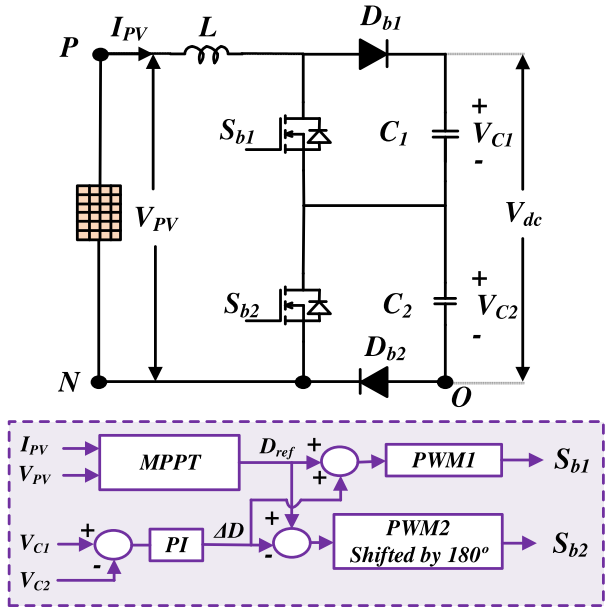


Fig. 4. Block diagram of 3LBC with PI control.

A. Front-End 3LBC

Fig. 4 depicts the front-end 3LBC, as given in [17], which comprises of boost inductor L, two dc-link capacitors C_1 and C_2, and two switches S_{b1} and S_{b2}. Depending on switching states, the 3LBC has four modes of operation, as shown in Fig. 5;

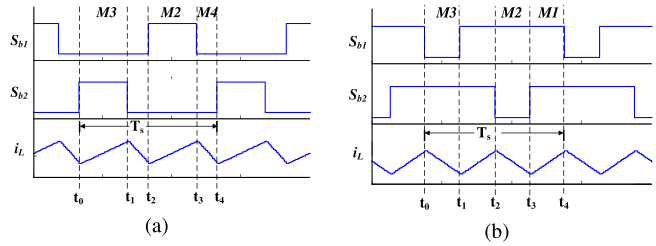


Fig. 5. Gate pulses and inductor current of 3LBC. (a) Region 1. (b) Region 2.

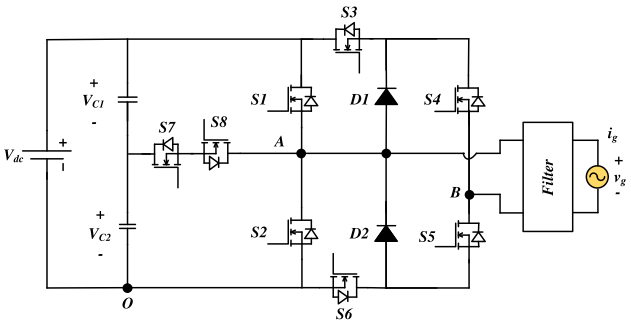


Fig. 6. Proposed T-type hybrid five-level TLI.

Mode 2 and Mode 3 occur when either S_{b1} or S_{b2} is turned ON. Mode 1 and Mode 4 occur when S_{b1} and S_{b2} are turned ON or OFF, respectively. It is noticed that there are two operating regions based on the value of duty ratio D. In region1, R1 ($0 < D < 0.5$) allows the converter to operate in Modes 2, 3, and 4. In region2, R2 ($0.5 < D < 1$) allows the converter to operate in Modes 1, 2, and 3.

The control pulses for the switches S_{b1} and S_{b2} are generated with a simple control circuit, as depicted in Fig. 4, where the reference duty cycle (D_{ref}) is generated from the MPPT controller to track maximum PV power. Furthermore, to balance the dc-link capacitor voltages, duty ratio $\triangle D$ is produced with a simple proportional–integral (PI) controller and then it is passed through the PWM circuit to generate the control pulses S_{b1} and S_{b2}. The following equation gives the relation between input PV voltage and dc-link voltage, where V_{PV} and V_{dc} indicate the PV source voltage and total dc-link voltage, respectively:

$$V_{\text{dc}} = \frac{V_{\text{PV}}}{(1-D)}. \tag{1}$$

III. Proposed T-Type Hybrid Five-Level TLI

A. Structure of the Proposed TLI

The proposed five-level TLI, as depicted in Fig. 6, comprises a half-bridge leg *(S1, S2),* a neutral point clamping (NPC) branch *(D1, D2, S3, S4, S5,* and *S6),* and a T-type bidirectional clamping branch *(S7, S8)*. The combination of half-bridge leg and NPC branch forms a hybrid structure and it is further enhanced with a T-type bidirectional clamping branch to build a T-type hybrid five-level inverter. Hybrid structure generates the polarity, and the bidirectional MOSFET branch enables the capacitor selection for five-level output and also clamps the inverter terminal voltages to $V_{\text{dc}}/2$ during the freewheeling period.

TABLE I
Switching Logic of the Inverter

State	*Voltage (V_{AB})*	*S1*	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*
State 1	(V_{C1}+V_{C2})	1	0	0	0	1	1	1	0
State 2	0.5 V_{C2}	0	0	0	0	1	1	1	1
State 3	0	0	0	0	1	1	0	1	1
State 4	- 0.5 V_{C1}	0	0	1	1	0	0	1	1
State 5	- (V_{C1}+V_{C2})	0	1	1	1	0	0	0	1

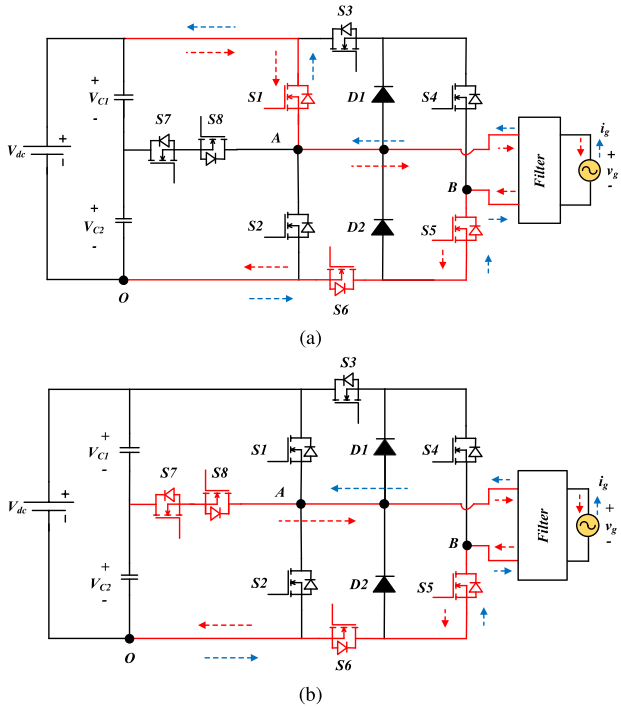


Fig. 7. Operating states of the inverter. (a) State 1 ($V_{AB} = (V_{C1} + V_{C2})$). (b) State 2 ($V_{AB} = V_{C2}$).

B. Operating States of the Proposed TLI

Table I gives the operating states of the proposed inverter topology. State 1 and State 2 correspond to $(V_{C1} + V_{C2})$ and V_{C2}, State 3 corresponds to zero-voltage level of the inverter, and State 4 and State 5 correspond to $-V_{C1}$ and $-(V_{C1} + V_{C2})$, respectively.

State 1: In this state, $V_{AB} = (V_{C1} + V_{C2})$, and the current flows either from 3LBC to grid or vice versa, as shown in Fig. 7(a). When the current flows from 3LBC to the grid, switches *S1*, *S5,* and *S6* are in conduction. If the current flows from the grid to 3LBC, body diodes of the switches *S1*, *S5,* and *S6* are in conduction. Throughout this state, the dc-link capacitors are in series and they are connected in parallel to the grid.

State 2: In this state, $V_{AB} = V_{C2}$, and the current flows either from 3LBC to grid or vice versa, as shown in Fig. 7(b). When current flows from 3LBC to the grid, switches *S5*, *S6*, and *S7* and body diode of *S8* are in conduction. If the current flows from the grid to 3LBC, switch *S8* and body diodes of the switches *S5*,

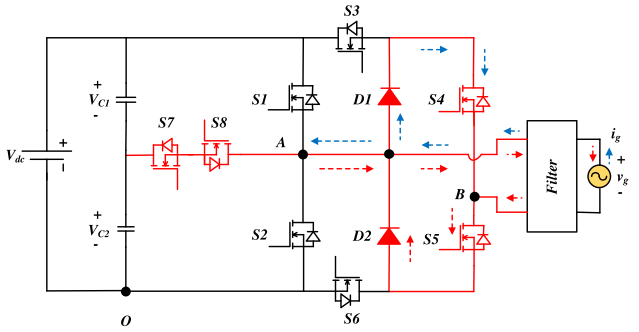


Fig. 8. Operation of the inverter during State 3 ($V_{AB} = 0$).

S6, and *S7* are in conduction. Throughout this state, the dc-link capacitor *C2* is connected parallel to the grid.

State 3: In this state, $V_{AB} = 0$, which provides a freewheeling path in the positive as well as negative half cycles of the grid. Switches *S4*, *S5*, *S7*, *S8*, *D1,* and *D2* are turned ON, as shown in Fig. 8. During this state, any of two above-said switches and two diodes will conduct based on the direction of the current. Moreover, throughout this state, PV source is isolated from the grid and also the potentials of V_{AO} and V_{BO} are clamped to the midpoint of dc-link capacitors.

Therefore, the effect of switch junction capacitance and the amplitude variations in CMV is reduced [18]. The detailed explanation of CMV behavior for the proposed system will be given in Section IV.

State 4: In this state, $V_{AB} = -V_{C1}$ and the current flows either from the grid to 3LBC or vice versa, as shown in Fig. 9(a). When current flows from the grid to 3LBC, switches *S3*, *S4*, and *S8* and body diode of *S7* are in conduction. If the current flows from 3LBC to the grid, switch *S7* and body diodes of the switches *S3*, *S4,* and *S8* are in conduction. Throughout this state, dc-link capacitor *C1* is connected parallel to the grid.

State 5: In this state, $V_{AB} = -(V_{C1} + V_{C2})$, and the current flows either from the grid to 3LBC or vice versa, as shown in Fig. 9(b). When the current flows from the grid to 3LBC, switches *S2*, *S3,* and *S4* are in conduction. If the current flows from 3LBC to the grid, body diodes of the switches *S2*, *S3,* and *S4* are in conduction. Throughout this state, dc-link capacitors are in series and they are connected parallel to the grid.

From all operating states of the inverter, it is observed that switches *S1* and *S2* are conducting only in the top levels of the output voltage. *S3* and *S6* are conducting in the negative and positive cycles except for zero level, respectively. *S4* and *S5* are conducting in the negative and positive half cycles of the grid, respectively. *S7* and *S8* are conducting according to the selection of voltage levels. Usually, switches *S4*, *S5* and *D1*, *D2* are enough to provide zero state, but it will float the terminal voltages of the inverter, which causes an imbalance in the CMV due to junction capacitances of the switches. Therefore, to clamp the CMV at $V_{dc}/2$, switches *S7* and *S8* are also in conduction during zero state. Moreover, this provides a path for current in any direction to realize the reactive power control capability of the inverter with similar CMV behavior. Therefore, the proposed

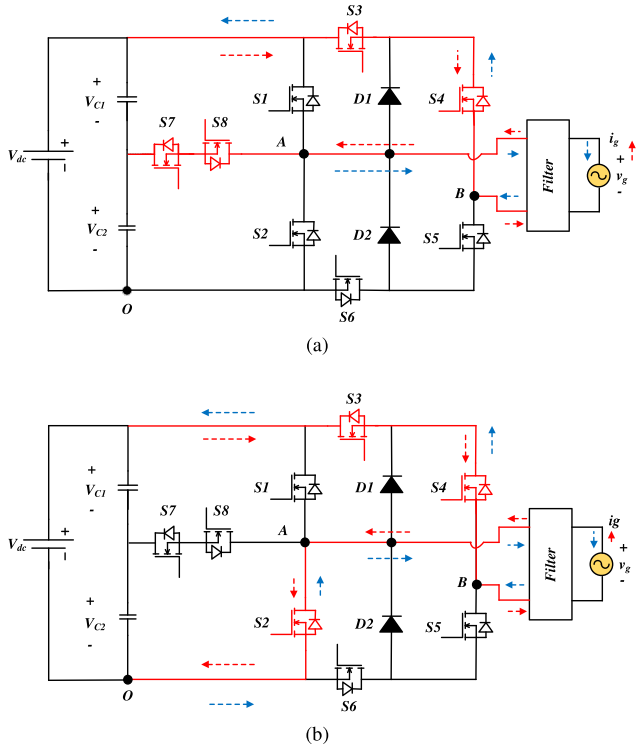


Fig. 9. Operating states of the inverter. (a) State 4 ($V_{AB} = -V_{C1}$). (b) State 5 ($V_{AB} = -(V_{C1} + V_{C2})$.

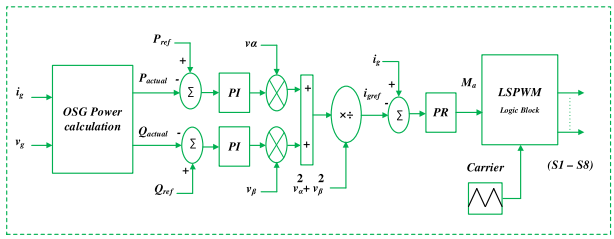


Fig. 10. Closed-loop control of the proposed inverter topology.

T-type hybrid five-level inverter is capable of producing voltage levels in the output under different power factor conditions of the grid without affecting the waveform quality.

C. Control of T-Type Hybrid Five-Level Inverter

The reactive power capability of the proposed two-stage system is tested by using the closed-loop control technique referred in [19], as depicted in Fig. 10. It comprises of an orthogonal signal generator (OSG) based power calculator, improved proportional–resonant controller [20], and LSPWM logic block for generating control pulses (*G1–G8*) to the inverter switches, as shown in Fig. 11.

IV. CMV Analysis for the Proposed TLI

Leakage current flow is one of the major problems in grid-connected TLI for PV power generation systems. High-frequency oscillations present in the CMV will electrify the resonant circuit and leads to the flow of leakage current i_{leakage}

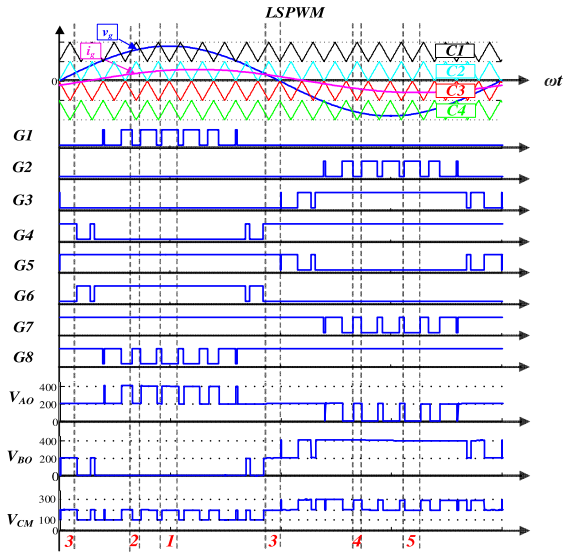


Fig. 11. Switching pulse generation corresponding to its operating states of the proposed inverter.

from the grid to the PV source. To analyze the CMV behavior, an equivalent circuit of the proposed inverter is drawn in Fig. 12(a), where V_{AO} and V_{BO} are the inverter terminal voltages with respect to *O*, as shown in Fig. 6. From the definitions [19], the CMV and differential-mode voltage (DMV) are expressed as follows:

$$V_{\mathrm{CM}} = \frac{V_{AO} + V_{BO}}{2} \tag{2}$$

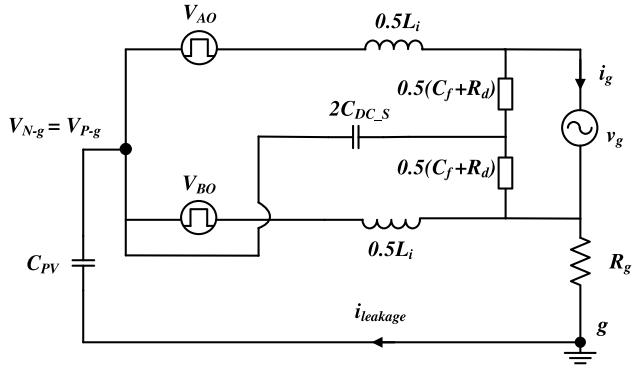
$$V_{\mathrm{DM}} = V_{AB} = V_{AO} - V_{BO} \tag{3}$$

$$V_{\mathrm{CM-DM}} = V_{\mathrm{DM}} \cdot \frac{L2 - L1}{2\,(L2 + L1)} \tag{4}$$

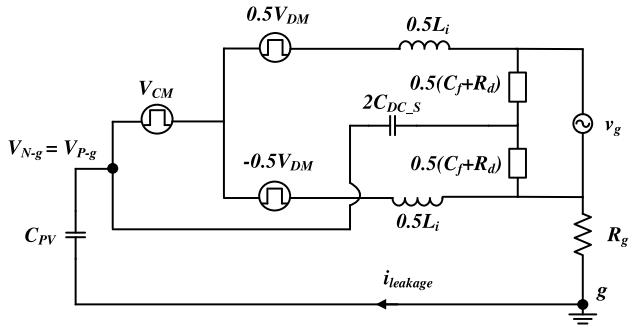
$$V_{\mathrm{TCMV}} = V_{\mathrm{CM}} + V_{\mathrm{CM-DM}} \tag{5}$$

where V_{CM} and V_{DM} are the CMV and DMV, respectively. Usually, the variations in the CMV depend on the structure and control scheme employed for the switching of an inverter. Moreover, depending on the placement of filter inductors, an additional CMV ($V_{\mathrm{CM-DM}}$) exists and it is given in (4). Thus, total CMV V_{TCMV} consists of both V_{CM} and $V_{\mathrm{CM-DM}}$, as expressed in (5). If the filter inductors are placed asymmetrically, such as $L1 = L_f$ and $L2 = 0$, $V_{\mathrm{CM-DM}} = -0.5V_{\mathrm{DM}}$ and $V_{\mathrm{TCMV}} = V_{BO}$. In opposite to that, if $L1 = L2 = 0.5L_f$ (for a well-designed inductor with symmetrically structured magnetic), $V_{\mathrm{CM-DM}} = 0$, and $V_{\mathrm{TCMV}} = V_{\mathrm{CM}}$. Equivalent circuit of the inverter in terms of CMV and DMV is depicted in Fig. 12(b). According to the operating states of the proposed inverter and ON–OFF positions of the switches presented in Section III-B, the variations in V_{TCMV} ($= V_{\mathrm{CM}}$) can be evaluated in each state of operation as follows:

$$\text{State 1}: \; V_{\mathrm{TCMV}} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(V_{\mathrm{dc}} + 0\right) = \frac{1}{2}V_{\mathrm{dc}} \tag{6}$$



(a)



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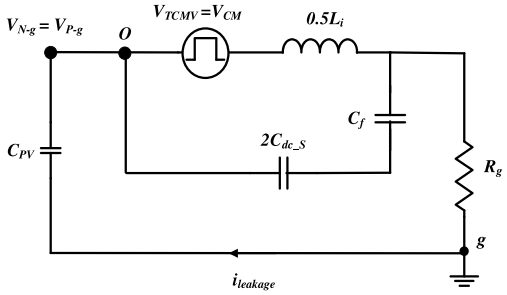

(c)

Fig. 12. (a) Common-mode equivalent circuit of the proposed TLI. (b) Equivalent circuit in terms of CMV and DMV. (c) Simplified circuit.

$$\text{State 2}: \; V_{\mathrm{TCMV}} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(\frac{V_{\mathrm{dc}}}{2} + 0\right) = \frac{1}{4}V_{\mathrm{dc}} \tag{7}$$

$$\text{State 3}: \; V_{\mathrm{TCMV}} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(\frac{V_{\mathrm{dc}}}{2} + \frac{V_{\mathrm{dc}}}{2}\right) = \frac{1}{2}V_{\mathrm{dc}} \tag{8}$$

$$\text{State 4}: \; V_{\mathrm{TCMV}} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(\frac{V_{\mathrm{dc}}}{2} + V_{\mathrm{dc}}\right) = \frac{3}{4}V_{\mathrm{dc}} \tag{9}$$

$$\text{State 5}: \; V_{\mathrm{TCMV}} = \frac{1}{2}\left(V_{AO} + V_{BO}\right) = \frac{1}{2}\left(0 + V_{\mathrm{dc}}\right) = \frac{1}{2}V_{\mathrm{dc}}. \tag{10}$$

From (6)–(10), it is noted that the variations in V_{TCMV} for the proposed topology are restricted from (1/4)$^*V_{\mathrm{dc}}$ to (3/4)$^*V_{\mathrm{dc}}$

due to clamping of inverter terminal voltages to half of the dc-link voltage during zero state. Moreover, the difference in amplitude of V_{TCMV} is only (1/4)*V_{dc} while transferring from one state to another state and vice versa, as shown in Fig. 11. But the high-frequency variations in V_{TCMV} will directly affect the voltage across C_{PV} (i.e., V_{N-g}) and also results in higher leakage current, as shown in (11). To reduce the effect of V_{TCMV} on V_{N-g}, in the proposed topology, a common-mode conducting path is provided for the inverter from split filter capacitors to the negative terminal of dc source, as shown in Fig. 3. The low-frequency components, such as grid voltage (50 Hz), ripple voltage (100 Hz), and DMV, have no effect on leakage current. Hence, they are neglected in the simplified circuit of the proposed TLI, as shown in Fig. 12(c) [21]. A small value of damping resistor (R_d) is also ignored for easy analysis

$$i_{\mathrm{leakage}} = C_{\mathrm{PV}} \frac{dV_{N-g}}{dt} \tag{11}$$

$$V_{N-g} = \frac{-V_{\mathrm{TCMV}}(\omega)}{1-\omega^2(0.5L_i)(2C_{\mathrm{dc\_}S}//C_f)}$$

$$V_{N-g} = \frac{-V_{\mathrm{TCMV}}(\omega)}{1-\frac{\omega^2}{\omega_r^2}} \tag{12}$$

$$A(\omega) = 20\log\left(\left|1-\frac{\omega^2}{\omega_r^2}\right|\right). \tag{13}$$

From the simplified circuit, as shown in Fig. 12(c), the total voltage variations in V_{N-g} are determined by (12), where ω and ω_r are the switching and resonant frequencies in rad/sec, respectively. The attenuation factor *A(ω)* is applied to the V_{TCMV}, as shown in (13). Smaller ω_r leads to higher attenuation on V_{TCMV}. Thus, the major contributor for voltage variations in V_{N-g} is attenuated with a factor *A(ω)*. Also, the *LC* circuit formed by the common-mode conducting path of the inverter results in the trapezoidal waveform of V_{N-g} with the fundamental frequency. Hence, the magnitude of leakage current is limited below the grid standards for the proposed topology. Furthermore, the proposed solution does not affect the active and reactive power injection into the grid due to the symmetrical placement of the filter inductors [22].

V. Simulation Results

MATLAB/Simulink results are presented to validate the performance of the proposed two-stage system integrated with closed-loop control under dynamic changes in both active and reactive powers. Various system parameters used for the proposed configuration in both simulation and experimentation are given in Table II. The PV panel is modeled with a 200 V dc source and the capacitance of 60 nF is connected between the terminals of dc source to the ground for emulating the PV parasitic capacitance. In Fig. 13, active power (*P*) is changing by maintaining reactive power (*Q*) as constant, and in Fig. 14, it is vice versa. Subplots of Figs. 13 and 14 consist of reference and actual active and reactive powers, dc-link voltage, and individual capacitor voltages, V_{AB}, v_g, and i_g, and also CMV (V_{CM}) of the inverter, respectively.

TABLE II
System Parameters

S. No	Parameters	Value
1	Power rating	500 W
2	Input voltage	200 V
3	AC output voltage	230 V, 50 Hz
4	Switching frequency f_s	10 kHz
5	Inductor L, L_i, L_{ac}	3 mH, 6 mH, 1.2 mH
6	Capacitors *C1*, *C2*, C_f, C_{PV}	1 mF, 1mF, 2 μF, 60 nF
7	R_d and R_g	5 Ω and 10 Ω
8	MOSFET	IRFP460N
9	Diode	RURP1560

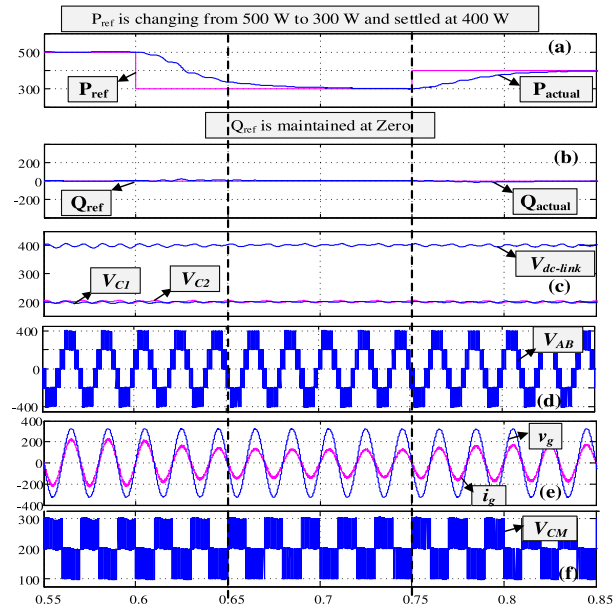

Fig. 13. Simulation results of the proposed two-stage system when P_{ref} is changing from 500 to 300 W and settled at 400 W. (a) Sudden changes in P_{ref}. (b) Constant Q_{ref}. (c) Total dc-link voltages and capacitor voltages *C1* and *C2*. (d) V_{AB}. (e) v_g. 70*i_g. (f) V_{CM}.

Grid current i_g is scaled by a factor of 70 for better visibility during reference power changes.

From Figs. 13 and 14, it is observed that the active and reactive powers effectively tracked the reference powers by maintaining constant and balanced dc-link voltage. Moreover, the bidirectional current path provided by the LSPWM scheme enables the inverter to operate in a reactive power region without having any spikes in grid voltage and current.

Furthermore, the common-mode characteristic curves of the proposed topology are depicted in Fig. 15. Subplots of Fig. 15 consist of V_{AO}, V_{BO}, V_{CM}, V_{N-g}, and i_{leakage}, respectively. Due to clamping of the inverter terminal voltages during the freewheeling period, the difference in amplitude variations of V_{TCMV} is restricted to (1/4)*V_{dc} while transferring from one state to another state and vice versa. Moreover, to attenuate such high-frequency and low-amplitude variations in V_{TCMV}, a common-mode conducting path is provided for the inverter. Therefore, the total high-frequency variations and sudden transitions are absent in V_{N-g}, which results in the reduction of leakage current, as shown in the subplot of Fig. 15. The rms value of leakage current 16.6 mA is measured from the simulations

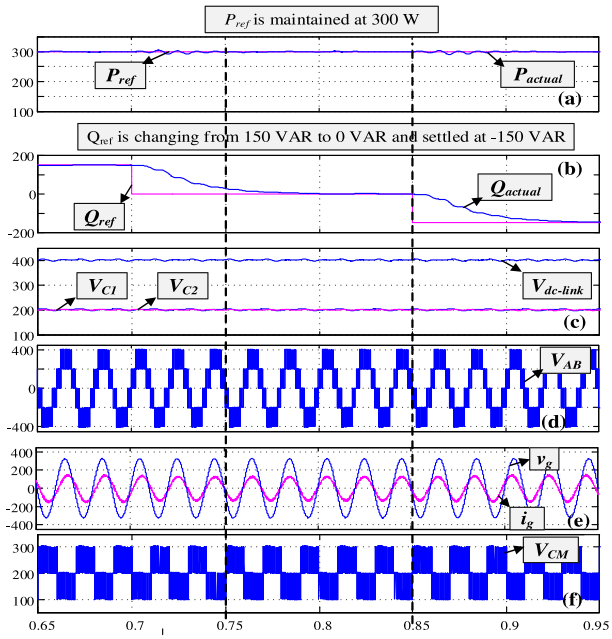

Fig. 14. Simulation results of the proposed two-stage system when Q_{ref} is changing from 150 to 0 VAR and settled at -150 VAR. (a) Constant P_{ref}. (b) Sudden changes in Q_{ref}. (c) Total dc-link voltages and capacitor voltages *C1* and *C2*. (d) V_{AB}, (e) v_g, and $70^{*}i_g$. (f) V_{CM}.

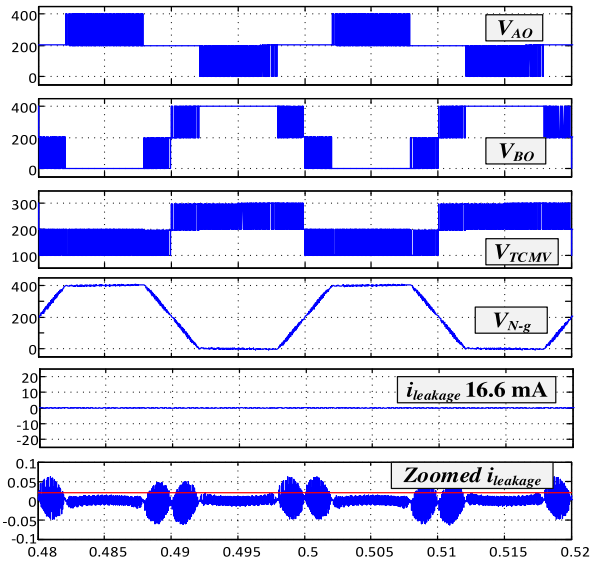

Fig. 15. Common-mode characteristics of the proposed TLI topology.

of the proposed symmetrical TLI for the specifications given in Table II, and also, it is well below the grid standards.

VI. Experimental Results

To validate the simulation studies of the proposed two-stage system, a 500-W experimental test setup is built based on the available lab facility and it is shown in Fig. 16. Various passive components employed for the development of the prototype are designed based on the calculations given in [23] and [24]. The parameters and components used for the experimental setup are

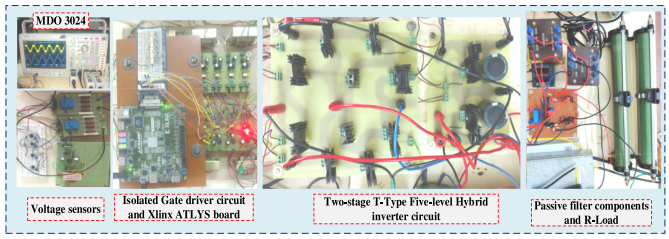

Fig. 16. Experimental prototype.

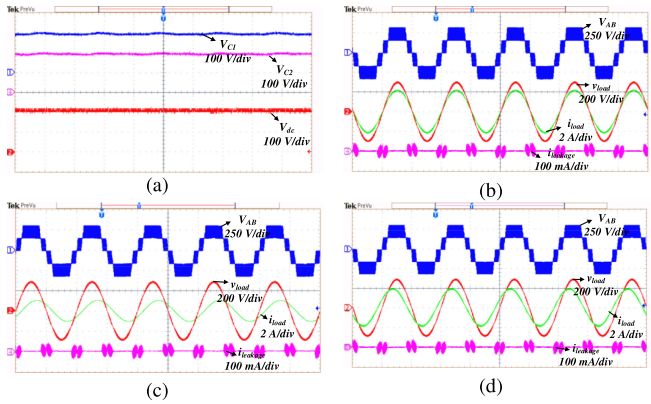

Fig. 17. (a) Input voltage, dc voltages waveforms of 3LBC. Five-level voltage (V_{AB}), load voltage V_{load}, load current i_{load}, and leakage current i_{leakage} under (b) unity power factor, (c) lagging power factor, and (d) leading power factor.

given in Table II. To show the leakage current flow with C_{PV} due to oscillations in CMV, an equivalent capacitor is modeled and connected across the dc terminal and ground. Fig. 17(a) shows the balanced voltages across the dc-link capacitors obtained from the simple control, as shown in Fig. 4, implemented using the ATLYS Spartan-6 FPGA board.

Fig. 17(b)–(d) shows the output waveforms of the inverter under unity, 0.9 lagging (200 Ω, 300 mH), and 0.9 leading (135 Ω, 50 μF) power factor conditions, respectively, which confirms the effectiveness of the proposed modulation scheme and topology for controlling the reactive power without affecting the waveform quality and multilevel operation. Moreover, THD% of the load current, represented in Fig. 18(b)–(d), is measured using comma-separated values' data obtained from MDO 3024 and which is less than IEC61000-3-2 standard.

Fig. 19 shows the CMV behavior of the proposed configuration. The terminal voltage V_{AO}, V_{BO}, and V_{CM} waveforms are given in Fig. 19(a). By observing the PV terminal voltage V_{N_g} in Fig. 19(b), it is confirmed that the common-mode path introduced by the *LCL* filter effectively limits the high-frequency variations and sudden transitions in the voltage across C_{PV}. The measured value of the rms leakage current is 17.42 mA, which is very close to the simulation value and also well below than 200 mA as per German DINVDE0126-1-1 standard. Moreover, the leakage current reduction is guaranteed irrespective of the operating power factor because of the similar CMV characteristics at all three power factor conditions.

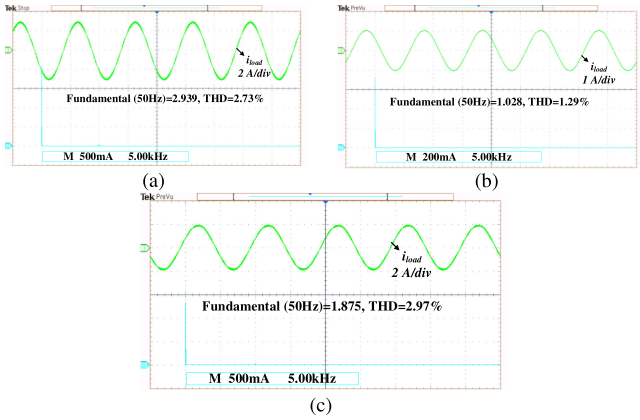

Fig. 18. FFT spectrums of load current under (a) unity power factor, (b) lagging power factor, and (c) leading power factor.

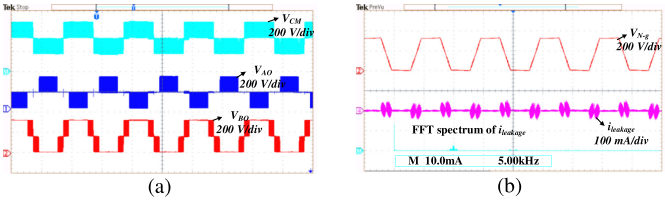

Fig. 19. (a) Inverter terminal voltages V_{AO}, V_{BO}, and $V_{\rm CM}$. (b) PV negative terminal to ground voltage V_{N_g} and leakage current $i_{\rm leakage}$.

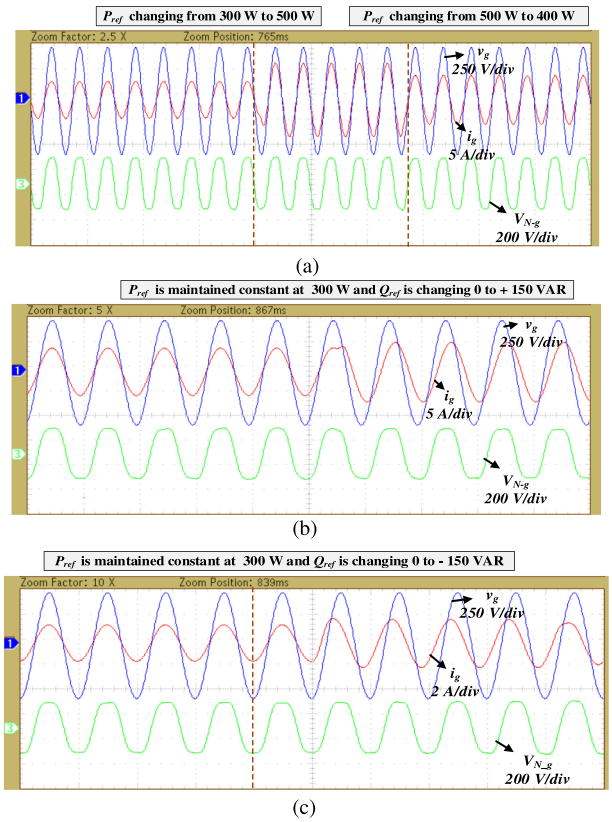

Fig. 20. (a) Dynamic performance of the proposed two-stage system. (a) Step change in real power and step change in reactive power. (b) Lagging. (c) Leading.

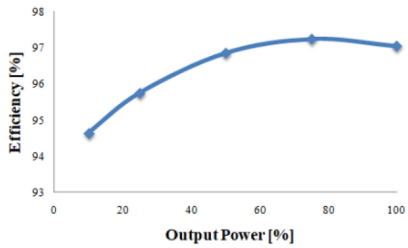

Fig. 21. Efficiency curve.

Furthermore, the dynamic performance of the proposed two-stage system under different power factor conditions of the grid is verified using real-time validation with OPAL-RT OP4500 modules [25]. Fig. 20(a) shows the step change in reference power from 300 to 500 W and then settled at 400 W. Fig. 20(b) and (c) shows the step-change reactive power from 0 to $\pm$150 VAR, respectively, for grid-connected operation.

It can be noticed that the inverter is capable to provide reactive power support at all power factors without degrading the quality of output waveforms. Furthermore, the efficiency versus the output power curve of the proposed two-stage system is evaluated using steady-state formulas referred in [23]. The maximum efficiency of 97.24% is attained for the proposed two-stage system, as shown in Fig. 21.

VII. Comparisons of the Proposed TLI With Other Five-Level TLI Topologies

In this section, a comparison of the proposed topology with other recently reported five-level TLI topologies is presented. Simulations are performed using powersim (PSIM) thermal module real-time devices (MOSFET-FCA76N60N and Diode-MUR1560) for obtaining the common-mode characteristics, fast Fourier transform (FFT) of leakage current, and loss distribution among various devices. Fig. 22 illustrates the comparison of PV terminal voltage (V_{N-g}) and leakage current for different topologies reported in [9]–[14] with the proposed topology, respectively. All the topologies are simulated under the same test conditions, as given in Table II. Generally, the variations in V_{N-g} depend on the topology structure and the modulation scheme employed for the switching of an inverter.

From (11), it is evident that the magnitude of leakage current is directly proportional to the total variations in V_{N-g} and size of the $C_{\rm PV}$. Fig. 22(a) shows the waveforms of V_{N-g} and $i_{\rm leakage}$ for topologies presented in [9]–[11]; it is observed that V_{N-g} is varying suddenly from $V_{\rm dc}$ to 0 while transferring from positive half-cycle to negative half-cycle. Fig. 22(b) shows the waveforms of V_{N-g} and $i_{\rm leakage}$ for the topologies presented in [12] and [13], where V_{N-g} has sudden variations while transferring from $\pm 0.5V_{\rm dc}$ level to $\pm V_{\rm dc}$ level and vice versa. This sudden variations of V_{N-g} result in more spikes in the leakage current. Fig. 22(c) depicts the waveforms of V_{N-g} and $i_{\rm leakage}$ for the topology presented in [14], where the redundant states formed by the derived CHB inverter eliminates both high frequency

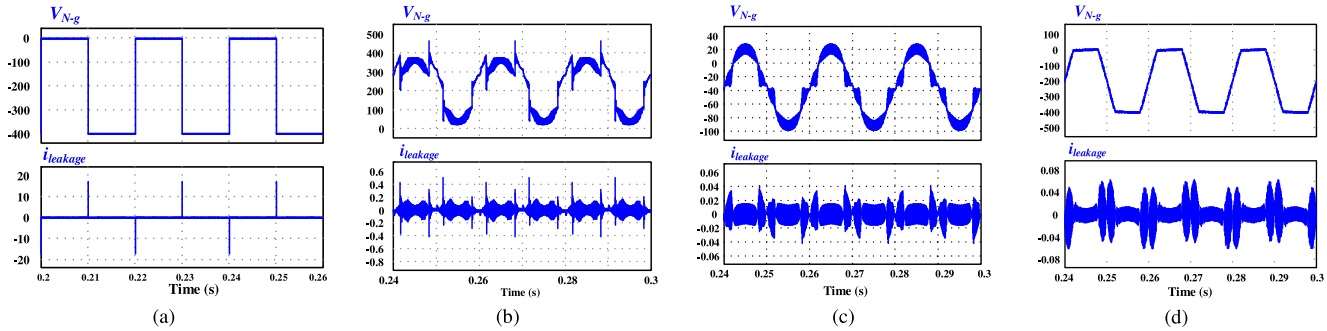

Fig. 22. Voltage across C_{PV} and leakage current of the (a) topologies [9]–[11], (b) topologies [12] and [13], (c) topology [14], and (d) proposed topology.

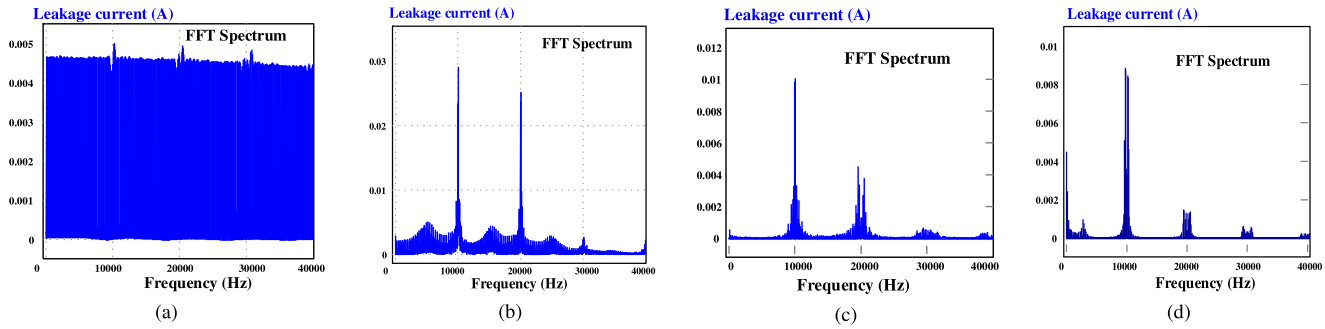

Fig. 23. FFT spectrum of the (a) topologies [9]–[11], (b) topologies [12] and [13], (c) topology [14], and (d) proposed topology.

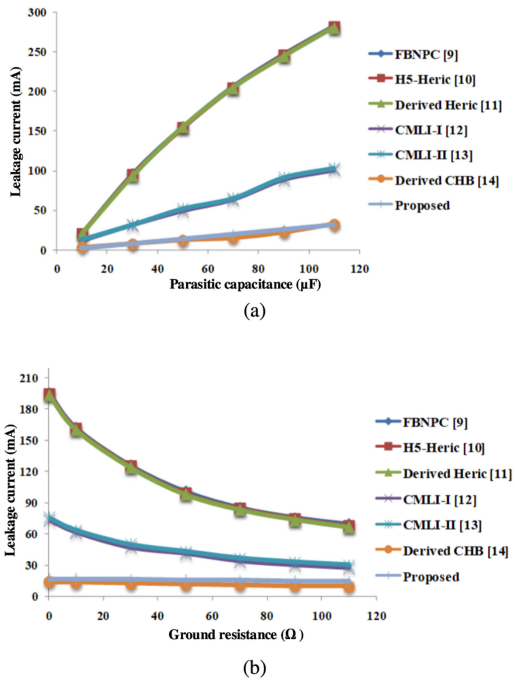

Fig. 24. (a) Parasitic capacitances versus leakage current curve. (b) Ground resistance versus leakage current.

and sudden transitions in V_{N-g}. Similarly, V_{N-g} and i_{leakage} of the proposed inverter topology are depicted in Fig. 22(d), where clamping of the inverter terminal voltages to half of the dc-link voltage and common-mode conducting path of the inverter eliminates both high frequency and sudden transitions in V_{N-g}.

Moreover, the measured rms values of the leakage current for the topologies reported in [9]–[11] are 180 mA, topologies reported in [12] and [13] are 57 mA, topology published in [14] is 13 mA, and for the proposed topology is 16 mA, respectively. Thus, the size of the additional common-mode filter is significantly reduced [5] for the proposed topology and derived CHB topology in comparison with the others. Usually, the low-impedance path offered by C_{PV} at resonant frequency causes higher leakage current and the same is noticed in the FFT spectrum, as illustrated in Fig. 23.

Furthermore, to realize the practical limitation of leakage current under various environmental conditions, the topologies were simulated at different parasitic capacitances and grounding resistances, as shown in Fig. 24(a) and (b), respectively. From the abovementioned discussion and simulation (see Figs. 22–24), it is concluded that the derived CHB and the proposed inverter topology offer very less leakage current in comparison with other five-level topologies proposed in [9]–[13].

Furthermore, detailed comparisons of the proposed topology with other five-level topologies are given in Tables III and IV in terms of device count, leakage current magnitude, reactive power capability, etc. It is noticed that the total number of PV sources required for the proposed topology is less than the cascaded multilevel inverter (CMLI)-I [12], CMLI-II [13], and derived CHB topologies. Also, the total number of components is less in comparison with the FBNPC [9], H5-Heric [10], and

TABLE III
COMPARISON OF VARIOUS MULTILEVEL TLI TOPOLOGIES WITH PROPOSED CONFIGURATION

Topology	FBNPC [9]	H5-Heric [10]	Derived Heric [11]	CMLI-1 [12]	CMLI-II [13]	Derived CHB [14]	Proposed
No.of PV Sources	1	1	1	2	2	2	1
MOSFETs	8	8	8	8	7	10	8
Diodes	4	4	2	0	0	0	2
Filter inductor placement	Asymmetrical	Asymmetrical	Asymmetrical	Symmetrical	Symmetrical	Symmetrical	Symmetrical
Voltage across C_{PV}	Square	Square	Square	Close to sine	Close to sine	Sine	Trapezoidal
Leakage current (RMS)	181.4 mA	181 mA	180.3 mA	56.5 mA	57.1 mA	13.7 mA	16.7 mA
Size of the CMF	Large	Large	Large	Medium	Medium	Small	Small
Reactive power capability	Yes	No	No	No	No	No	Yes
Freewheeling states during negative power transfer	Realized	Not Realized	Not Realized	Not Realized	Not Realized	Not Realized	Realized

TABLE IV
COMPARISON OF CONDUCTING DEVICES AND BLOCKING VOLTAGES FOR VARIOUS MULTILEVEL TLI TOPOLOGIES WITH PROPOSED CONFIGURATION

Topology			FBNPC [9]	H5-Heric [10]	Derived Heric [11]	CMLI-1 [12]	CMLI-II [13]	Derived CHB [14]	Proposed
No.of MOSFETs conducting	PP	V_{dc}	4	2	2	3	3	4	3
		$0.5*V_{dc}$	4	2	2	2	3	3	3
	FP	0	4	1	1	1	1	1	1
	NP	$-0.5*V_{dc}$	4	3	2	2	3	3	3
		$-V_{dc}$	4	3	2	3	3	4	3
No.of diodes conducting	PP	V_{dc}	0	0	0	0	0	0	0
		$0.5*V_{dc}$	1	1	1	1	1	1	1
	FP	0	0	1	1	1	1	1	1
	NP	$-0.5*V_{dc}$	1	1	1	1	1	1	1
		$-V_{dc}$	0	0	0	0	0	0	0
Total devices conducting in one cycle			22	14	12	14	16	18	16
Total blocking voltage	MOSFET		$4*V_{dc}$	$7*V_{dc}$	$7*V_{dc}$	$7*V_{dc}$	$6*V_{dc}$	$6*V_{dc}$	$6*V_{dc}$
	Diode		$2*V_{dc}$	$3*V_{dc}$	V_{dc}	0	0	0	$2*V_{dc}$

*PP = Positive period, **FP = Freewheeling period, ***NP = Negative period.

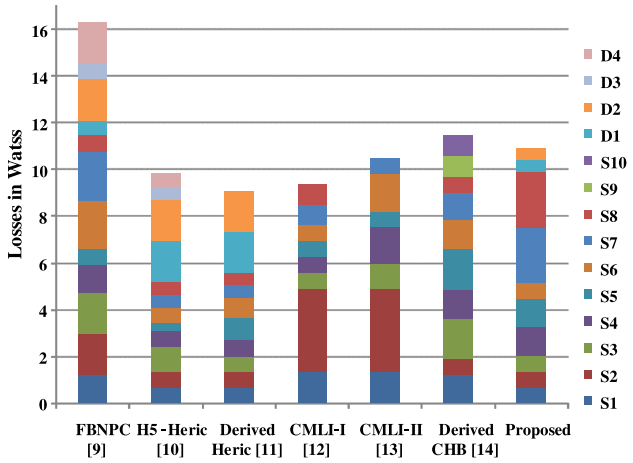

Fig. 25. Loss distribution of the various TLIs with the proposed topology.

derived CHB [14] topologies. Moreover, the proposed inverter structure and its modulation scheme effectively minimizes the leakage current and also supports the reactive power control. From Table IV, it is observed that the proposed topology requires fewer conducting devices in comparison with the FBNPC and derived CHB. Thus, the proposed T-type hybrid five-level TLI is expected to show lower losses and high efficiency.

Evaluation of the switching and conduction losses of each power device is carried out by using PSIM thermal module [26] under the same operating conditions, as given in Table II. Also, the loss distribution of various power switches and diodes for different topologies is illustrated in Fig. 25. It can be visualized that total losses for the proposed topology are lower than FBNPC and derived CHB and higher than H5-Heric, derived Heric, CMLI-1, and CMLI-II. However, it offers minimum leakage current, reactive power capability, and a reduced number of PV sources in comparison with the other inverter topologies. Therefore, the proposed inverter topology is an optimal tradeoff in comparison with other topologies and also a reliable candidate for future PV power generation systems.

VIII. CONCLUSION

In this article, a single-phase two-stage T-type hybrid five-level inverter is presented, which provides boosting, multilevel operation, reactive power control, and also offers minimum leakage current for transformerless PV applications. The 3LBC balances the dc-link capacitors by using a simple control algorithm, which reduces the control complexity of the inverter. The proposed inverter topology and its LSPWM technique provide a path to the current at different power factor conditions without affecting the CMV behavior. Moreover, the leakage current flowing through C_{PV} is limited by clamping the terminal voltages of the inverter to half of the dc voltage during zero states and also by introducing a common-mode path to the inverter using an *LCL* filter. Both simulation and experimental results are presented to

justify claims of the proposed configuration. Finally, a detailed comparison with the existing single-stage TLI topologies is given to focus on the merits of the proposed configuration.

REFERENCES

[1] J. Jana, H. Saha, and K. D. Bhattacharya, "A review of inverter topologies for single-phase grid-connected photovoltaic systems," *Renewable Sustain. Energy Rev.*, vol. 72, pp. 1256–1270, May 2017.

[2] M. Obi and R. Bass, "Trends and challenges of grid-connected photovoltaic systems—A review," *Renewable Sustain. Energy Rev.*, vol. 58, pp. 1082–1094, May 2016.

[3] O. P. Mahela and A. G. Shaik, "Comprehensive overview of grid interfaced solar photovoltaic systems," *Renewable Sustain. Energy Rev.*, vol. 68, pp. 316–332, Feb. 2017.

[4] Z. Özkan and A. M. Hava, "Classification of grid connected transformerless PV inverters with a focus on the leakage current characteristics and extension of topology families," *J. Power Electron.*, vol. 15, no. 1, pp. 256–267, Jan. 2015.

[5] W. Li, Y. Gu, H. Luo, W. Cui, X. He, and C. Xia, "Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4537–4551, Jul. 2015.

[6] A. El-Hosainy, H. A. Hamed, H. Z. Azazi, and E. E. El-Kholy, "A review of multilevel inverter topologies, control techniques and applications," in *Proc. 19th Int. Middle East Power Syst. Conf.*, Dec. 2017, pp. 1265–1275.

[7] O. Lopez, R. Teodorescu, and J. Doval-Gandoy, "Multilevel transformerless topologies for single-phase grid-connected converters," in *Proc. 32nd Annu. Conf. IEEE Ind. Electron.*, Nov. 2006, pp. 5191–5196.

[8] G. Buticchi, E. Lorenzani, and G. Franceschini, "A five-level single-phase grid-connected converter for renewable distributed systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, Mar. 2013.

[9] S. Iturriaga-Medina *et al.*, "A comparative analysis of grid-tied single-phase transformerless five-level NPC-based inverters for photovoltaic applications," in *Proc. 13th Int. Conf. Power Electron.*, Jun. 2016, pp. 323–328.

[10] G. Vazquez, P. R. Martinez-Rodriguez, J. M. Sosa, G. Escobar, M. A. Juarez, and A. A. Valdez, "H5-HERIC based transformerless multilevel inverter for single-phase grid connected PV systems," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2015, pp. 1026–1031.

[11] G. Vázquez, J. M. Sosa, M. A. Juarez, P. R. Martinez-Rodriguez, and G. Escobar, "A modulation strategy for a single-phase transformerless multilevel inverter with dual bidirectional switch," in *Proc. AEIT Int. Annu. Conf.*, Oct. 2018, pp. 1–6.

[12] S. Jain and V. Sonti, "A highly efficient and reliable inverter configuration based cascaded multilevel inverter for PV systems," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2865–2875, Apr. 2017.

[13] V. Sonti, S. Jain, and S. Bhattacharya, "Analysis of the modulation strategy for the minimization of the leakage current in the PV grid-connected cascaded multilevel inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1156–1169, Feb. 2017.

[14] F. K. Moghaddam and H. Iman-Eini, "Reliable simple method for suppression of leakage current in grid-connected CHB inverters," *IET Power Electron.*, vol. 11, no. 13, pp. 2170–2177, Nov. 2018.

[15] T. K. S. Freddy, J. H. Lee, H.-C. Moon, K.-B. Lee, and N. A. Rahim, "Modulation technique for single-phase transformerless photovoltaic inverters with reactive power capability," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6989–6999, Sep. 2017.

[16] W. Li and X. He, "Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[17] C. Balakishan, N. Sandeep, and M. V. Aware, "Design and implementation of three-level DC-DC converter with golden section search based MPPT for the photovoltaic applications," *Adv. Power Electron.*, vol. 2015, Feb. 2015, Art. no. 587197.

[18] L. Zhou, F. Gao, and T. Yang, "Neutral-point-clamped circuits of single-phase PV inverter: Generalized principle and implementation," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2015, pp. 442–449.

[19] M. Islam, N. Afrin, and S. Mekhilef, "Efficient single phase transformerless inverter for grid-tied PVG system with reactive power control," *IEEE Trans. Sustain. Energy*, vol. 7, no. 3, pp. 1205–1215, Jul. 2016.

[20] N. Zhang, H. Tang, and C. Yao, "A systematic method for designing a PR controller and active damping of the LCL filter for single-phase grid-connected PV inverters," *Energies*, vol. 7, no. 6, pp. 3934–3954, Jun. 2014.

[21] E. Gubia, P. Sanchis, A. Ursua, J. Lopez, and L. Marroyo, "Ground currents in single-phase transformerless photovoltaic systems," *Prog. Photovolt., Res. Appl.*, vol. 15, no. 7, pp. 629–650, Nov. 2007.

[22] K. Sateesh kumar, A. Kirubakaran, and N. Subrahmanyam, "A novel two-stage hybrid T-type five-level transformerless inverter," in *Proc. Innov. Power Adv. Comput. Technol.*, Mar. 2019, pp. 1–6.

[23] S. K. Kuncham, K. Annamalai, and S. Nallamothu, "Single-phase two-stage seven-level power conditioner for photovoltaic power generation system," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 794–804, Mar. 2020.

[24] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, and C. L. Bak, "A review of passive power filters for three-phase grid-connected voltage-source converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54–69, Mar. 2016.

[25] G. E. Gowd, P. C. Sekhar, and D. Sreenivasarao, "Real-time validation of a sliding mode controller for closed-loop operation of reduced switch count multilevel inverters," *IEEE Syst. J.*, vol. 13, no. 1, pp. 1042–1051, Mar. 2019.

[26] S. M. Sreechithra, P. Jirutitijaroen, and A. K. Rathore, "Impacts of reactive power injections on thermal performances of PV inverters," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2013, pp. 7175–7180.

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