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RESEARCH ARTICLE

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Fault-tolerant multi-level inverter topologies for open-end winding induction motor drive

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Summary

This paper presents two nine-level inverter topologies for open-end winding induction motor drive with fault-tolerance for all possible switch faults. The proposed topologies are designed with three voltage-source inverters each with eight switches, an isolated DC source and a capacitor. The number of components and the scheme of connection employed for phase windings in both the topologies are identical. The voltage across the capacitors is controlled using the phase currents and hence does not require any additional pre-charging circuit. The direction of phase currents flowing through the capacitors determines their charging and discharging states. Hence the proposed topologies are categorized as flying-capacitor leg based topology (FCLBT) and switched-capacitor based topology (SCBT) considering the technique employed for generating intermittent voltages. Although these topologies require three sources, the output voltage peak across each phase winding would be twice the source voltage, hence lower rating renewable energy sources can be employed as input sources. Conventional level-shifted carrier sinusoidal pulse width modulation technique (SPWM) is employed for generating switching pulses. The proposed topologies employ reduced number of devices compared to existing similar nine-level topologies and also exhibit fault-tolerance for switch faults. The post-fault operation of the proposed topologies does not require any additional hardware but necessitates the modifications of switching pulses. Simulations are performed in the MATLAB/Simulink environment and results are presented. A prototype is constructed to validate the performance of the proposed topologies and experimental results are presented.

KEYWORDS

fault tolerant, flying-capacitor, multi-level inverter, open-end winding, pulse width modulation

List of Symbols and Abbreviations: ACHB, Asymmetrical CHB; CHB, Cascaded H-bridge; DSP, Digital signal processors; DSPACE, Digital signal processing and control engineering; FCLBT, Flying-Capacitor leg based topology; FC, Flying-Capacitor; FFT, Fast Fourier Transform; IM, Induction motor; NPC, Neutral point clamped; OEWIM, Open-end winding induction motor; OC, Open-circuit; lp, Maximum value of load phase current; Ma, Modulation Index; MLI, Multilevel inverter; MSL, Modified switching logic; Q, Charge; T, Time-period; THD, Total harmonic distortion
SC, Short-circuit; SCBT, Switched-Capacitor based topology; SPWM, sinusoidal pulse width modulation technique; VSI, voltage-source inverter
V/F, Volts per Hertz; VB, Blocking Voltage; Z, Load Impedance; δT, Inverter switching time period; δV, Maximum permissible voltage ripple.

1 | INTRODUCTION

In recent days, multi-level voltage-source inverters (VSIs) have been receiving greater acceptance from the industry in the range of medium- and high-power induction motor (IM) drive applications. Owing to the certain advantages of multi-level inverters (MLIs) such as operation with higher DC-link voltages using lower rating semiconductor switching devices and producing output voltage with superior harmonic profile mark their importance in industrial applications.[1,2] Conventional topologies such as (a) neutral point clamped (NPC) inverter, (b) flying-capacitor (FC) inverter and (c) cascaded H-bridge (CHB) inverter belong to early era of MLIs and are employed in applications with lower levels of output voltage. These topologies have their own advantages and disadvantages based on their control and operation. NPC and FC topologies will have capacitor voltage balancing issues and require complex control techniques when designed for higher levels in the output. CHB topology can be designed for any level of output voltage but requires increased number of isolated sources. Although these topologies can be configured for the increased number of levels in the output, the power and control circuit complexity increases as the number of switching devices required are high. Hence this provides the scope of research for developing MLI topologies with reduced complexity in power and control circuits. A comprehensive MLI topology combining NPC and FC inverter topologies is presented,[3]in which the self-balancing of the capacitor voltages is achieved without complex algorithms but this topology requires additional capacitors and several active switches to produce the multi-level output voltage. A modified topology designed for a single-phase system employing CHB with single DC source and an FC is proposed.[4]This topology can deliver multi-level output voltage but the floating-capacitor voltage gets unbalanced with change in modulation range and requires a complex control scheme. Recent years have witnessed vast research in areas of MLI topologies and many of such topologies that are present in the literature are the blend of conventional topologies.[5-7] Several topologies were proposed to satisfy the desires of the industry such as reduced device count and fault-tolerance.[8-13]

Certain MLI topologies are designed based on the application, such as the topologies for open-end winding induction motor (OEWIM) drive. The three-phase stator winding terminals of IM are brought out and are fed from both ends to achieve multi-level output voltage across the phase windings.[14] Several effective and efficient modulation techniques were proposed for three-level and four-level operation of the dual inverter fed OEWIM drive configuration.[15-17] Apart from dual inverter configuration with conventional two-level inverters, several topologies were proposed for OEWIM drive with increased number of levels in the output voltage. MLI topologies employing conventional three-phase VSIs and FC connected H-bridges are proposed to generate nine- and seven-level output voltage. These topologies employ an increased number of components, complex modulation technique and deliver a peak output voltage equal to the magnitude of a single source voltage.[18,19]A modular fault-tolerant seven-level inverter topology configured with conventional two-level and NPC inverters for OEWIM drive is also proposed. This topology exhibits better fault-tolerance with reduced modulation range during switch faults but employs a large number of components and complex control scheme.[20] A 17-level inverter topology with low-switch count for OEWIM drive is presented. This topology employs DC sources of unequal magnitude and a complex modulation scheme for operation.[21] A nine-level inverter topology for OEWIM drive is proposed with minimum component count and employs a simple control scheme. This topology provides fault tolerance to switch faults but cannot produce average sinusoidal output voltage in post-fault operation.[22]

MLIs with a high number of levels in the output voltage are desired in drive applications as the increase in the number of levels decreases harmonic distortions and hinders the need for expensive and bulky filters. However, the increase in the levels of the output voltage is obtained at a cost of an increased number of components, hence the industry is reluctant for a higher number of levels as it makes the system bulky, less reliable and complex. Therefore, there is a necessity to attain an increased number of levels in the inverter output voltage without an enormous rise in the number of components, and reliability of the system is also important. The power circuit complexity can be reduced with lower switching devices and hence control complexity can be reduced proportionally. As the component count of MLIs increases, the reliability of the system decreases. Failure of any one switch may lead to a complete shutdown of the system. Thus, fault tolerant reduced device topologies find importance in the MLI family.[23,24] A fault-tolerant MLI topology with reduced switching devices for OEWIMs that can be controlled by conventional sinusoidal pulse width modulation (SPWM) techniques is also presented.[25]

Hence, this paper presents two nine-level inverter topologies for OEWIM drive with fault-tolerance capability to switch fault conditions. The proposed topologies are designed with a minimum number of switching devices. The two nine-level inverter topologies proposed are envisioned for an IM with open-end stator winding construction. In these topologies, the six terminals of the three-phase windings of the IM are fed from three three-phase VSIs along with the FCs. The modulation techniques employed can effectively charge and discharge the capacitors to realize middle voltage

levels throughout its modulation range. The proposed topologies employ a reduced number of switches and lower voltage rating isolated DC sources than conventional topologies.

The content of this paper is organised as follows: the working principle of the proposed topologies is detailed in Section 2, modulation scheme employed is presented in Section 3; comparative analysis and determination of capacitance value are presented in Sections 4 and 5, respectively. Operation of the proposed topologies during normal condition, with switch faults and with fault-tolerant strategy along with simulation results, is illustrated in Section 6. Experimental results and conclusions are presented in Sections 7 and 8 respectively.

2 | DESCRIPTION OF PROPOSED TOPOLOGIES

The proposed topologies are designed to feed an OEWIM with lower-rated voltage sources. These inverters are configured to feed the three-phase IM stator windings from both the ends to yield nine-level voltage across each phase winding. This configuration produces increased voltage levels with reduced devices and the output voltage peak will be twice the magnitude of input source voltage. This allows us to employ lower-voltage renewable energy sources as input elements. The scheme of connection employed exhibits inherent fault tolerance for switch faults as well. The scheme of connection employed for the proposed topologies is illustrated in Figure 1.

Figure 1A presents an FC-leg based topology (FCLBT) and Figure 1B presents a switched-capacitor based topology (SCBT). The FCLBT is designed with three inverters, in which each inverter consists of an FC leg and a conventional H-bridge and are connected across an isolated DC source. SCBT is designed with three three-phase inverters and each of these inverters are fed from an isolated DC source and also are provided with a capacitor with two series-connected switches across it. In the proposed topologies, switches S_{1A} through S_{8A} constitute inverter-A. Similarly, switches S_{1B} through S_{8B} constitute inverter-B and switches S_{1C} through S_{8C} constitute inverter-C.

In FCLBT, the circuit configuration for inverter-A is done in the following manner: the series connection of switches S_{1A}, S_{2A}, S_{3A} and S_{4A} constitute a leg of the inverter and a capacitor is connected across the switches S_{2A} and

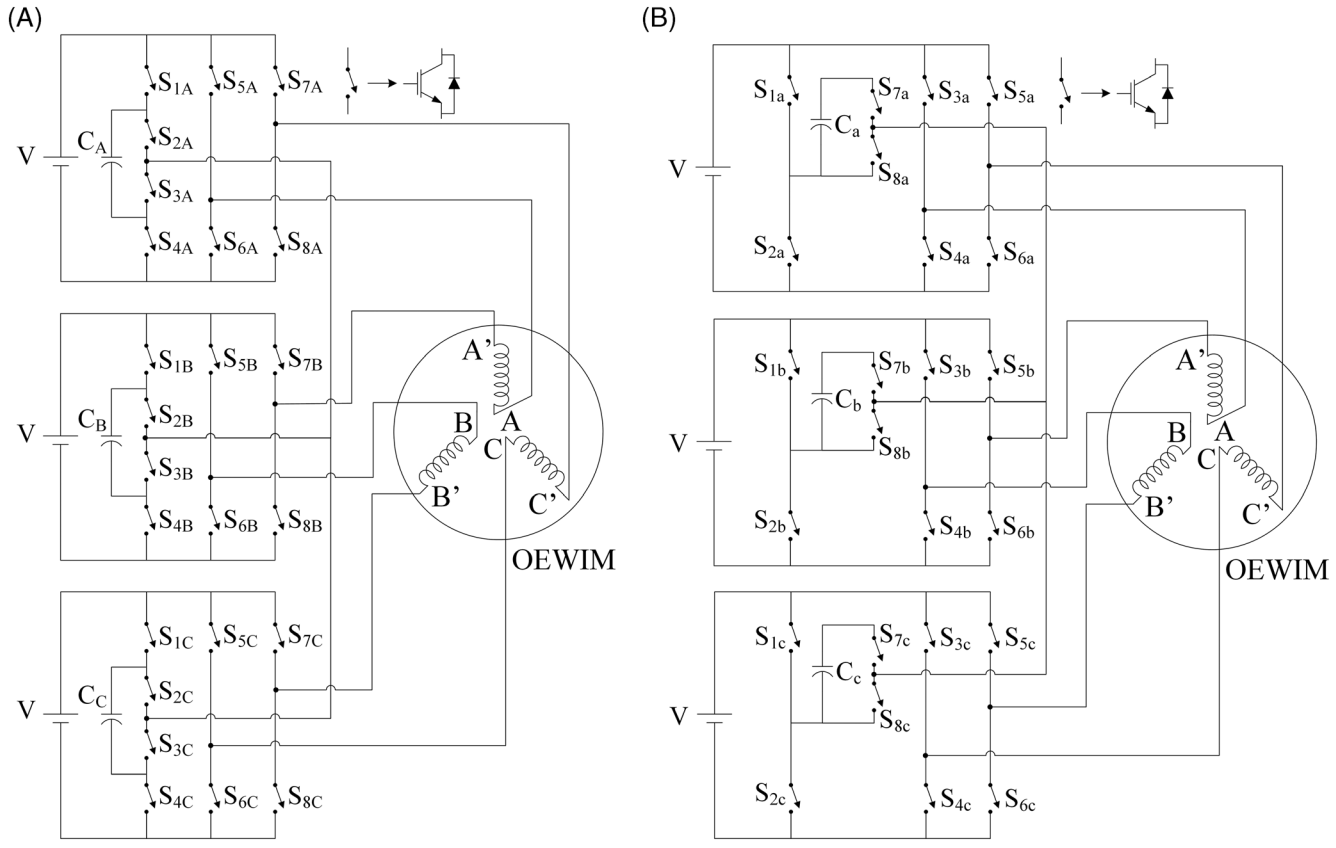


FIGURE 1 Proposed topologies: A, flying-capacitor leg based topology (FCLBT); B, switched-capacitor based topology (SCBT)

TABLE 1 Possible switching states to generate different voltage levels for FCLBT.

	Inverter-A			Inverter-B			
Voltage level	**S_{1A}**	**S_{2A}**	**S_{5A}**	**S_{1B}**	**S_{2B}**	**S_{7B}**	**Capacitor state**
2 V	0	0	1	1	1	0	No change
3 V/2	0	0	1	1	0	0	C_B-charging
	0	1	1	1	1	0	C_A-charging
V	0	0	1	0/1	0/1	0/1	No change
	0/1	0/1	0/1	1	1	0	
V/2	0	0	1	1	0	1	C_B-charging
	0	1	0	1	1	0	C_A-charging
0	1	1	1	0/1	0/1	0/1	No change
	0	0	0	1/0	1/0	1/0	
−V/2	0	1	0	0/1	0/1	0/1	C_A-discharging
	0/1	0/1	0/1	1	0	1	C_B-discharging
−V	1	1	0	0/1	0/1	0/1	No change
	0/1	0/1	0/1	0	0	1	
−3 V/2	1	1	0	1	0	1	C_B-discharging
	0	1	0	0	0	1	C_A-discharging
−2 V	1	1	0	0	0	1	No change

S_{3A}. The mid-point of switches S_{2A} and S_{3A} is taken as output terminal-1 of inverter-A. Similarly, the mid-point of switches S_{5A} and S_{6A} is considered as output terminal-2 and mid-point of switches S_{7A} and S_{8A} is considered as output terminal-3. In SCBT, the switches S_{1a} and S_{2a} constitute a leg of the inverter and to the point between these two switches the negative terminal of the capacitor is connected. The switches S_{7a} and S_{8a} constitute a leg and are connected across the capacitor. The mid-point of switches S_{7a} and S_{8a} is taken as output terminal-1 of inverter-a. Similarly, the mid-point of switches S_{3a} and S_{4a} is considered as output terminal-2 and mid-point of switches S_{5a} and S_{6a} is considered as output terminal-3. Hence, in both the proposed topologies, each inverter has three output terminals and output terminal-1 of all the three inverters is shorted to form a neutral connection. The phase-A winding of OEWIM is connected between output terminal-2 of inverter-a and output terminal-3 of the inverter-b. Similarly, the phase-B and phase-C windings are connected in the same configuration. The scheme of connection and the components required for both the topologies are the same.

The proposed topologies are proficient of generating output voltage across any phase winding with nine levels, namely ±2 V, ±3 V/2, ±V, ±V/2, 0. The possible switching states to generate nine-level output voltage across the terminals of phase winding A-A′ of OEWIM are presented in Table 1 for FCLBT and in Table 2 for SCBT. However, the reduction in the number of switching devices has a divergent influence on the number of overall redundant switching states as evident from Tables 1 and 2. However, an observation of switching tables depicts the information that the charging and discharging times of FC in both the proposed topologies are equivalent over one complete cycle of output voltage.

Considering the output voltage and also current have half-wave symmetry, the average current (Average$[i_c]$) that flow through the capacitor during output voltage levels ±3 V/2 and ±V/2 with the load impedance of Z can be given as follows:

$$\text{Average}\left[i_c^+\right]_{V_{/2}} = \frac{V - v_c}{Z}; \tag{1}$$

$$\text{Average}\left[i_c^-\right]_{3V_{/2}} = \frac{V + v_c}{Z}; \tag{2}$$

$$\text{Average}\left[i_c^+\right]_{3V_{/2}} = \frac{2V - v_c}{Z}; \tag{3}$$

TABLE 2 Possible switching states to generate different voltage levels for SCBT

	Inverter-a			Inverter-b			
Voltage level	S_{1a}	S_{3a}	S_{7a}	S_{1b}	S_{5b}	S_{7b}	**Capacitor state**
2 V	0	1	0	1	0	0	No change
3 V/2	0	1	1	1	0	0	C_a-charging
	0	1	0	0	0	1	C_b-discharging
V	0	1	0	0/1	0/1	0	No change
	0/1	0/1	0	1	0	0	
V/2	0	1	1	1	1	0	C_a-charging
	0	0	0	0	0	1	C_b-discharging
0	0	0	0	0/1	0/1	0	No change
	1	1	0	0/1	0/1	0	
−V/2	0	1	1	0	0	1	C_a-discharging
	0	0	1	0	0	0	C_b-charging
−V	1	0	0	1/0	1/0	0	No change
	0/1	0/1	0	0	1	0	
−3 V/2	0	0	1	0	1	0	C_a-discharging
	1	0	0	0	1	1	C_b-charging
−2 V	1	0	0	0	1	0	No change

$$\text{Average}\left[i_c^-\right]_{V_{/2}} = \frac{V_c}{Z}. \tag{4}$$

Therefore, the net charge (Q) absorbed/supplied for a time period (T) can be expressed as follows:

$$Q = \left\{\text{Average}\left[i_c^+\right]_{V_{/2}} + \text{Average}\left[i_c^+\right]_{3V_{/2}} - \text{Average}\left[i_c^-\right]_{V_{/2}} - \text{Average}\left[i_c^-\right]_{3V_{/2}}\right\} * T = \left\{\frac{2V - 4v_c}{Z}\right\}. \tag{5}$$

Owing to the symmetric property of the output current in steady-state, the average charge Q over a complete cycle is zero, substituting charge (Q) as zero in Equation (5) will result in a relation of $v_c = 0.5$ V. The voltage across the FC is maintained as 0.5 V where V is the voltage rating of each source in the proposed topologies. This self-balancing property of maintaining voltage 0.5 V across the FC is achieved without any additional circuitry or closed-loop control that expedites lowered overall inverter design cost.

The voltage at the output terminals is reliant on the switching states of the power switches. Considering the switches as ideal, let the binary variables 0 and 1 represent their blocking and conduction states, respectively. In other words,

that is, if $S_{vu} = 0$ then $S_{wu} = 1$; switch S_{vu} is OFF and switch S_{wu} is ON

if $S_{wu} = 0$, then $S_{vu} = 1$; switch S_{wu} is OFF and switch S_{vu} is ON.

- Where u ε A, B, C and v ε 1, 2, 5, 7 and w ε 4, 3, 6, 8 for FCLBT.
- Where u ε a, b, c and v ε 1, 3, 5, 7 and w ε 2, 4, 6, 8 for SCBT.

With this depiction and considering $\hat{S}_{1A} = S_{4A}$, $\hat{S}_{2A} = S_{3A}$, $\hat{S}_{5A} = S_{6A,}$ $S_{5A} = S_{7A}$ and $\hat{S}_{7A} = S_{8A,}$ for FCLBT and similarly $\hat{S}_{1a} = S_{a2}$, $\hat{S}_{3a} = S_{4a}$, $\hat{S}_{5a} = S_{6a}$, $S_{3a} = S_{5a}$, $S_{4a} = S_{6a}$ and $\hat{S}_{7a} = S_{8a}$ for SCBT, the output voltage across the terminals of OEWIM for the proposed topologies can be written as follows:

For FCLBT

$$V_{AA'} = V\begin{bmatrix} S_{5A}\left(\hat{S}_{1A}\hat{S}_{2A} + 0.5\hat{S}_{1A}S_{2A}\right) + \hat{S}_{7B}\left(S_{1B}S_{2B} + 0.5\hat{S}_{1B}S_{2B}\right) \\ -\hat{S}_{5A}\left(S_{1A}S_{2A} + 0.5\hat{S}_{1A}S_{2A}\right) - S_{7B}\left(\hat{S}_{1B}\hat{S}_{2B} + 0.5\hat{S}_{1B}S_{2B}\right) \end{bmatrix}. \tag{6}$$

For SCBT

$$V_{AA'} = V\begin{bmatrix} S_{3a}\left(\hat{S}_{1a}\hat{S}_{7a} + 0.5\hat{S}_{1a}S_{7a}\right) + \hat{S}_{5b}\left(S_{1b}\hat{S}_{7b} + 0.5\hat{S}_{1b}S_{7b}\right) \\ -\hat{S}_{3a}\left(S_{1a}\hat{S}_{7a} + 0.5\hat{S}_{1a}S_{7a}\right) - S_{5b}\left(\hat{S}_{1b}\hat{S}_{7b} + 0.5\hat{S}_{1b}S_{7b}\right) \end{bmatrix}. \quad (7)$$

The proposed topologies are capable of providing balanced three-phase output voltage even under switch fault conditions. This makes the proposed topologies reliable when used for low-voltage medium-power applications such as feeding motors in an electrical vehicle. For operation of the proposed topologies during switch fault conditions does not require any additional hardware, but requires modification of switching pulses. To obtain balanced output voltage across all the phases, the switching of the inverters should also be identical. Hence when switch fault occurs in any of the switches, some of the healthy switches are also turned-off in post-fault operation to ensure symmetrical switching of the inverters. Under normal operation of the proposed topologies, nine-level voltage is fed to the windings of the OEWIM drive, whereas with switch fault, the levels in the output voltage reduce to five and the power delivered will also be reduced to half for most of the switch faults. The output power supplied might be reduced during switch fault conditions but it ensures continuity in operation of the OEWIM drive.

3 | MODULATION SCHEME

The gate pulses for the switches in the proposed topologies are produced by the conventional SPWM technique. A fundamental frequency sinusoidal reference signal, V_{Ref} is compared with the high-frequency level shifted triangular carrier signals to generate the gate pulses. In general, the magnitude of the sinusoidal reference signal is taken as unity that represents the modulation index, Ma = 1, where the magnitude of the level-shifted carriers is half the reference

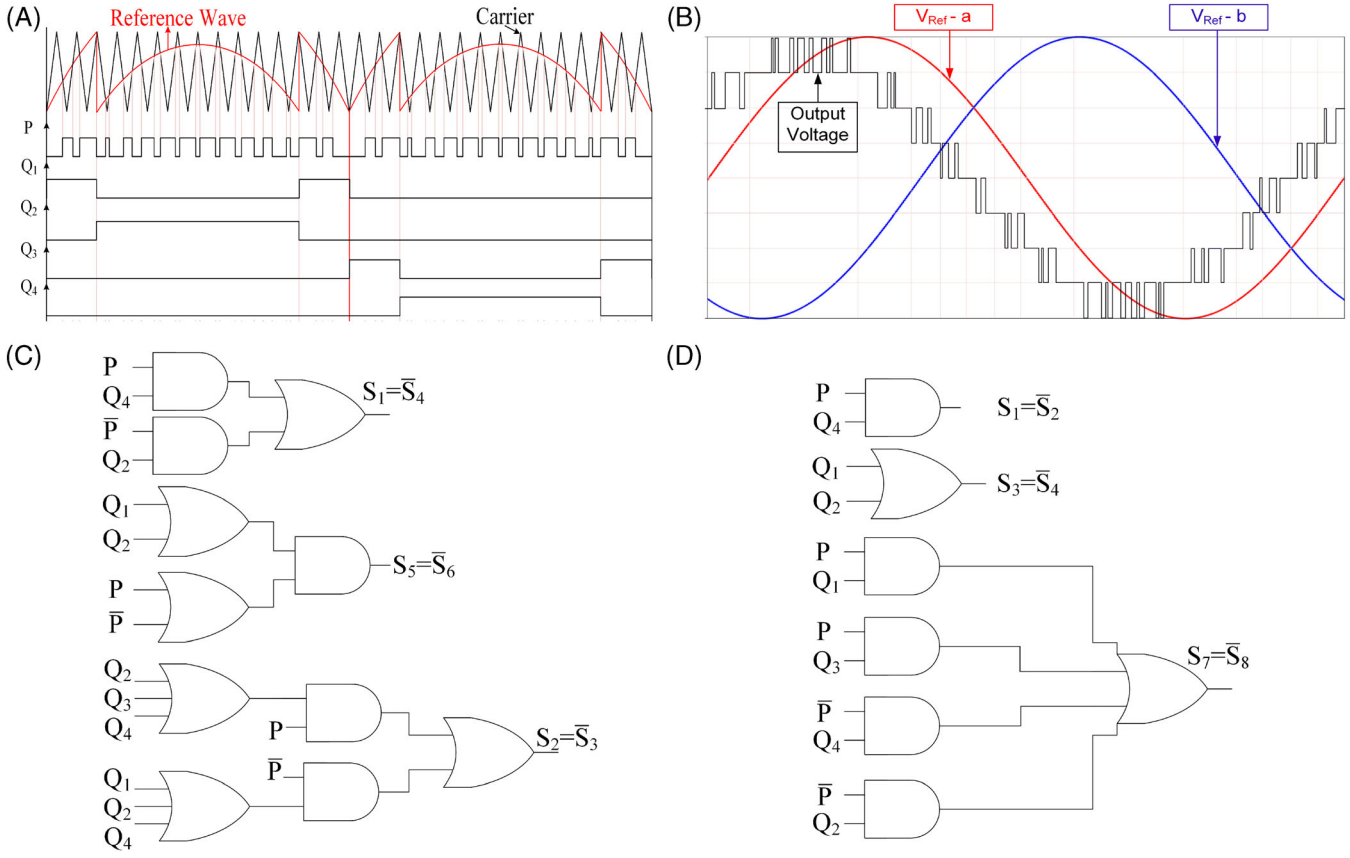


FIGURE 2 Modulation scheme employed to generate gate pulses for the proposed topologies: A, modified reference wave with a single carrier wave to generate gate pulses; B, representation of nine-level generation with two reference signals, $V_{Ref\text{-}a}$ and $V_{Ref\text{-}b}$; C, switching logics for switches in FCLBT; D, switching logics for switches in SCBT

voltage magnitude. For such a modulation scheme, the number of level-shifted carriers required for an N-level inverter will be $(N-1)$. To reduce the number of carrier signals required, the reference wave can be modified in such a way that the negative cycle is flipped as positive cycle, which reduces the number of carrier waves required.[26] The reference wave can be further modified as shown in Figure 2A, in such a way that the number of carriers required is only one.[27] This reduces the computational burden on the controllers while implementing on digital platforms like dSPACE and digital signal processors (DSP). The gate pulses for the proposed topologies are generated using dSPACE 1104.

The connection of phase windings is done such that two ends of each winding are fed from two different inverters. For example, considering SCBT, the phase winding terminal-A is connected to inverter-a and winding terminal-A′ is connected to inverter-b. Similarly, phase winding terminals B-B′ are also connected between two different inverters. Three inverters are operated by gate pulses generated by SPWM technique. The reference waves used for three inverters are displaced by 120°. Therefore, each terminal of every phase winding is operating with a phase difference of 120° with respect to its other terminal. This scheme of connection permits the phase winding to experience the output voltage with nine levels with maximum output voltage as twice the source voltage. The modified reference PWM used to produce gate pulses for the proposed topologies is illustrated in Figure 2A. Figure 2B illustrates the logic of generating nine levels in the output voltage with two reference waveforms displaced by 120°. The switching logics employed for FCLBT and SCBT are presented in Figure 2C,D, respectively.

TABLE 3 Comparison of proposed topologies with other similar topologies feeding OEWIM drives

	Active switches		DC capacitors		Clamping diodes		Sources	
Type of inverter	***N***	***V_B***	***N***	***V_B***	***N***	***V_B***	***N***	**Rating**
NPC	48	0.25 V_{DC}	8	0.125 V_{DC}	42	6 diodes—0.125 V_{DC} 6 diodes—0.25 V_{DC} 6 diodes—0.375 V_{DC} 6 diodes—0.5 V_{DC} 6 diodes—0.625 V_{DC} 6 diodes—0.75 V_{DC} 6 diodes—0.875 V_{DC}	1	V_{DC}
FC	48	0.25 V_{DC}	108	0.125 V_{DC}	0	—	1	V_{DC}
Conventional CHB (CCHB)	48	V_{DC}	0	—	0	—	12	$V_{DC}/8$
Asymmetrical CHB (ACHB)	24	12 switches—0.75 V_{DC} 12 switches—0.25 V_{DC}	0	—	0	—	3 3	3 $V_{DC}/8$ $V_{DC}/8$
[18]	36	12 switches—V_{DC} 12 switches—0.5 V_{DC} 12 switches—0.25 V_{DC}	6	—	0	—	2	V_{DC}
[19]	36	12 switches—V_{DC} 24 switches—0.33 V_{DC}	6	0.33 V_{DC}	0	—	2	V_{DC}
[20]	48	0.166 V_{DC}	6	0.0833 V_{DC}	12	0.083 V_{DC}	6	$V_{DC}/12$
[21]	36	12 switches—0.125 V_{DC} 12 switches—0.375 V_{DC} 12 switches—0.75 V_{DC}	9	3 Cap's-0.125 V_{DC} 3 Cap's-0.375 V_{DC} 3 Cap's-0.75 V_{DC}	0	—	3 3	3 $V_{DC}/4$ $V_{DC}/4$
[22]	24	18 switches—V_{DC} 6 switches—0.5 V_{DC}	6	0.5 V_{DC}	0	—	3	$V_{DC}/2$
FCLBT	24	12 switches—V_{DC} 12 switches—0.5 V_{DC}	3	0.5 V_{DC}	0	—	3	$V_{DC}/2$
SCBT	24	18 switches—V_{DC} 6 switches—0.5 V_{DC}	3	0.5 V_{DC}	0	—	3	$V_{DC}/2$

Abbreviations: Cap's, capacitors; N, number; V_B, blocking voltage.

4 | COMPARISON OF THE PROPOSED TOPOLOGIES

The proposed topologies are compared with other similar topologies in terms of blocking voltage capability (V_B) of switches, DC capacitors, clamping diodes and number of sources required along with their rating, and are presented in Table 3. The comparison is done based on the assumption that the voltage blocking capability of the components is calculated when all these topologies are excited with a source voltage of V_{DC} and the actual source voltages required with their rating are mentioned under the sources column. From Table 3, it is evident that the proposed topologies employ least number of switches as that used in ACHB and topology in Reference 22, out of the total switches used in FCLBT half of the switches have a blocking voltage equal to 0.5 V_{DC} and the other half have a blocking voltage of 0.25 V_{DC}. Whereas in SCBT three-fourth of the switches have a blocking voltage equal to 0.5 V_{DC} and rest have a blocking voltage of 0.25 V_{DC} (since the source voltage used for the proposed topologies is only 0.5 V_{DC}). It implies that the total switch count is low and that the rating required is also low for the proposed topologies.

5 | DETERMINATION OF CAPACITANCE

The proposed topologies are designed based on FC. So, it is important to determine the value of capacitance of such a capacitor that depends upon the peak value of load current, ripple voltage and discharging period. Capacitors designed for lower ripple will yield lower power loss and work with higher efficiency.

The value of capacitance of the FC can be determined as[28]

$$I_p = C\frac{dv}{dt} = C\frac{\Delta V}{\Delta T},$$

$$C = I_p\frac{\Delta T}{\Delta V} = \frac{I_p}{\Delta V * f_{sw}}, \tag{8}$$

where C is the minimum capacitance of FC required, I_p is the maximum value of load phase current, ΔT is the inverter switching time period (T_s) and ΔV is the maximum permissible peak-to-peak voltage ripple in the FC. For a switching frequency of 1.5 kHz, if the capacitor peak-to-peak ripple voltage has to be limited to 4 V, capacitance required is 666 μF. To be on the safe side, the capacitance for the experimental prototype is taken as 1000 μF.

6 | OPERATION OF THE PROPOSED TOPOLOGIES

To demonstrate the viability of the proposed topologies and the control scheme, the models are developed and simulated in the MATLAB/Simulink environment. The simulation results of three-phase output voltage and currents, total harmonic distortion (THD) of the phase voltage and current, FC voltages during normal operating conditions of FCLBT and SCBT are presented in Figures 3 and 4, respectively. The parameters considered for the simulation and experimentation are presented in Table 4.

6.1 | Inverter operation during switch faults

The proposed topologies employ three-phase inverters, and the total number of switches employed is 24 for each topology. Each winding is associated with six switches, at least, to deliver the output power. The switches in the inverters can be faulted either with an open-circuit (OC) or with a short circuit (SC). The proposed topologies can still be operated under such switch fault conditions with rated or reduced output power depending upon the switch under fault and the type of fault (SC or OC). Simulation results for various switch OC faults in the proposed topologies are presented in Figures 5 and 6. From the results presented in Figures 5 and 6, it is evident that both the topologies behave identical during switch faults (introduced at time 0.04 seconds) as well depending upon the switch position in their respective topologies. The switches S_{2A} and S_{3A} in FCLBT are identical to switches S_{7a} and S_{8a} in SCBT and are meant for charging and discharging of the FC. And switches S_{1A} and S_{4A} in FCLBT are

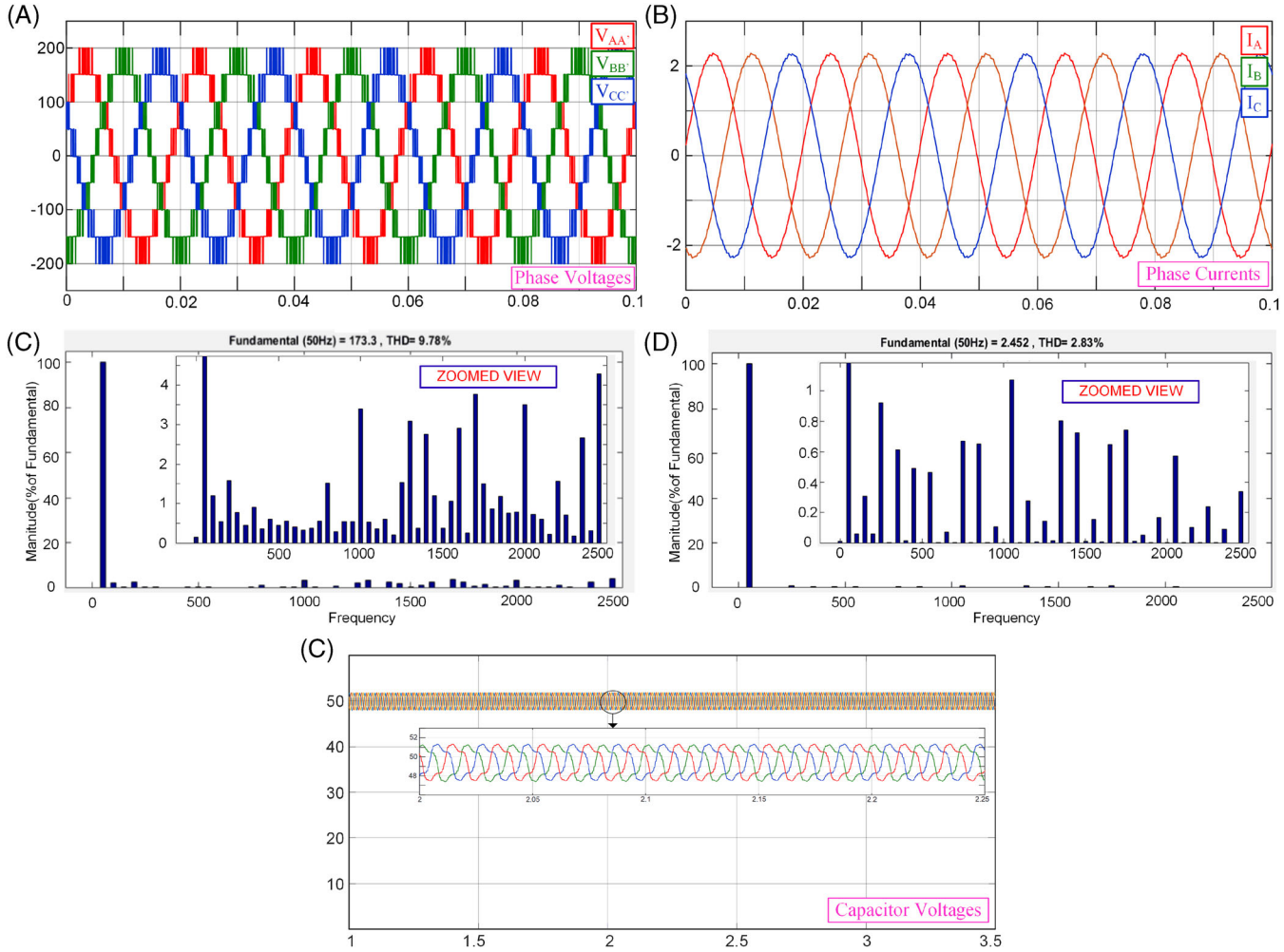


FIGURE 3 Simulation results of FCLBT. A, Three-phase output voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$; B, three-phase currents IA, IB and IC; C, THD for phase voltage; D, THD of phase current; and E, voltages across the capacitor in each inverter

identical to switches S_{1a} and S_{2a} in SCBT and are meant for neutral connection. Hence OC fault in such switches will yield similar output voltages and currents and hence experimental validation can be done with any of the topologies.

In FCLBT, switch S_{1A} operates in complimentary with S_{4A} and switch S_{2A} operates in complimentary with S_{3A}. Hence the results are presented only for S_{1A} and S_{2A} OC faults. Similarly, switches S_{5A} and S_{7A} operate in complementary with S_{6A} and S_{8A}, respectively. Therefore, waveforms of output voltage and current for switches S_{5A} and S_{7A} OC fault are presented. The output waveforms for OC faults in switch S_{6A} (or S_{8A}) would be the same as the vertical flip of the results presented for OC fault of switch S_{5A} (or S_{7A}). Similarly, in SCBT, switches S_{1a}, S_{3a}, S_{5a} and S_{7a} are operated in complementary with switches S_{2a}, S_{4a}, S_{6a} and S_{8a}, respectively. Hence waveforms for OC faults in switches S_{1a}, S_{3a}, S_{5a} and S_{7a} are presented in Figure 6.

6.2 | Fault-tolerant operation

The proposed topologies are capable of operating even under switch fault conditions. The switching logic has to be modified when a fault occurs in a switch in any of the inverters. If the fault occurred in the switch is an OC fault, then the switching strategy is that the gate pulses of the faulty switch are to be withdrawn and the switching logic has to be designed for the available healthy switches only. For the proposed topologies, out of the 24 switches, if any of the switches is either open-circuited or short-circuited, then the modulation index has to be reduced to half (ie, $M_a = 0.5$) and the

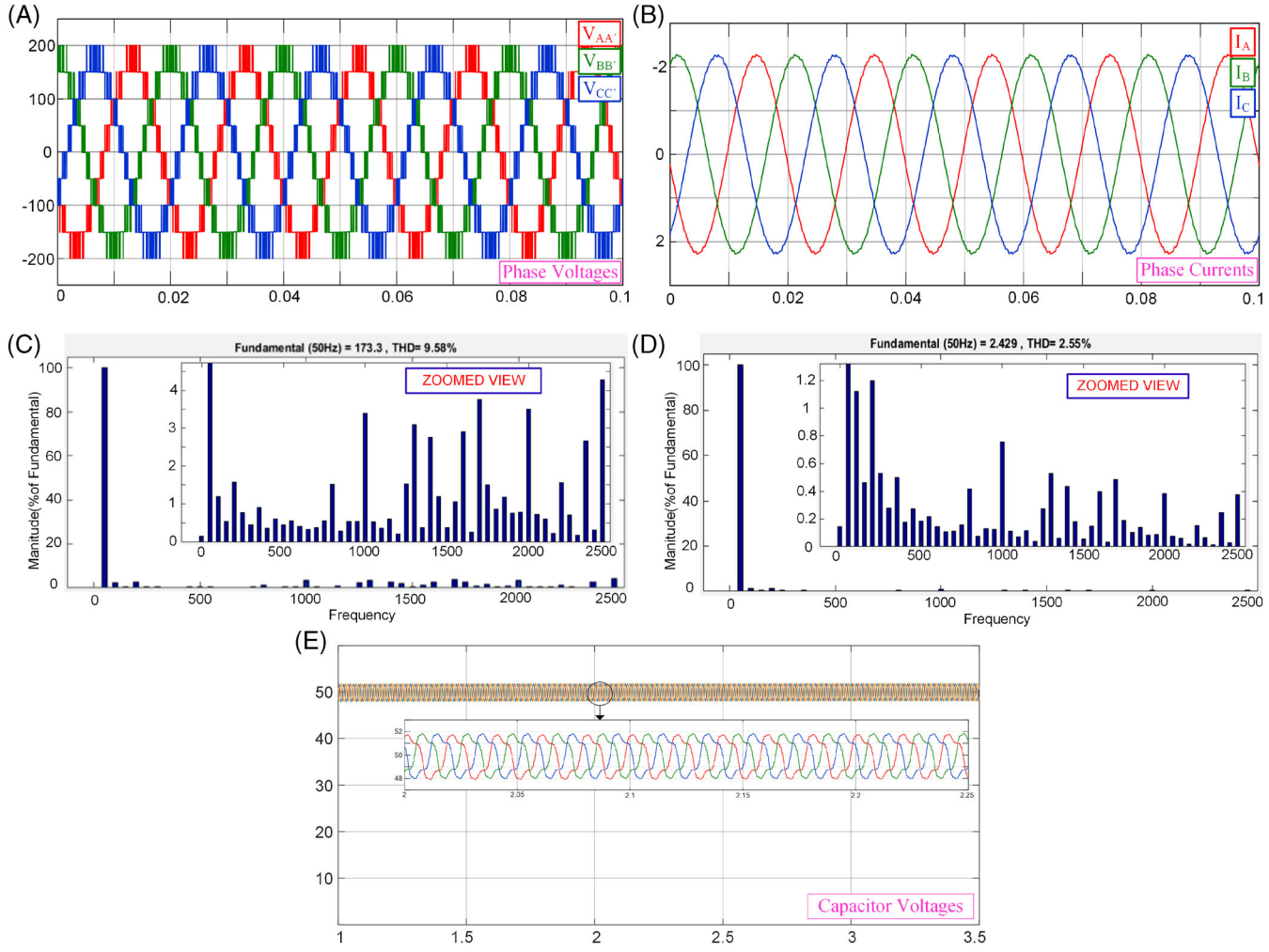


FIGURE 4 Simulation results of SCBT. A, Three-phase output voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$; B, Three-phase currents IA, IB and IC; C,THD for phase voltage; D,THD of phase current; and E, Voltages across the capacitor in each inverter

TABLE 4 Circuit parameters used for simulation and experimentation

Particulars	Value	
Source voltage	100 V	
Flying capacitors	1000 μf	
Fundamental frequency	50 Hz	
Switching frequency	1500 Hz	
Load	Open-end winding induction motor	
	Specifications	3-phase, 4 Pole, 50 Hz, 400 V, 1440 rpm, 1 hp
	Rated torque	3.5 Nm
	Stator and rotor resistance	2.23 Ω and 2.13 Ω
	Stator and rotor leakage inductance	0.032 H and 0.032 H
	Mutual inductance	0.219 H
	Moment of inertia	0.05 kg/m^2

inverter continues to operate as five-level inverter with modified switching logic (MSL). For example, if the switches S_{xa} or S_{yA} (where x ϵ 2 or 3, y ϵ 7 or 8), are faulty, still the rated output power can be delivered with five levels in the output

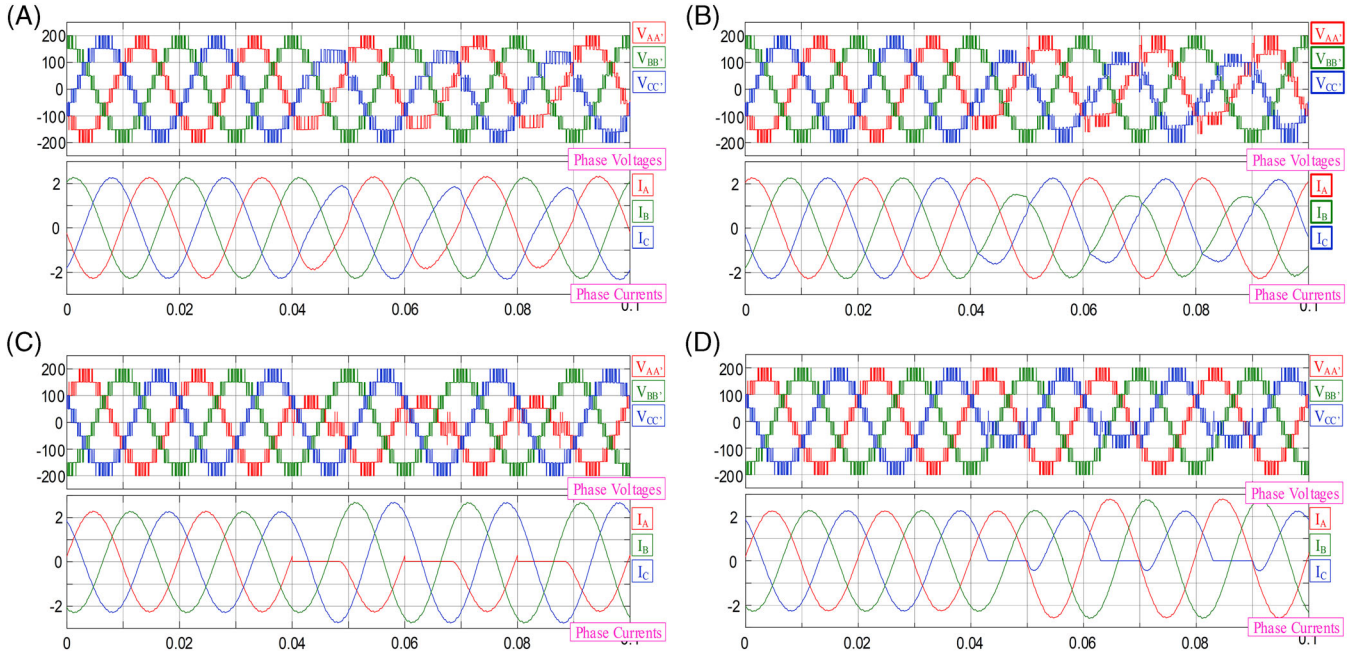


FIGURE 5 Simulation results of three-phase voltages and currents of FCLBT with open-circuit fault in switch: A, S_{1A}; B, S_{2A}; C, S_{5A}; D, S_{7A}

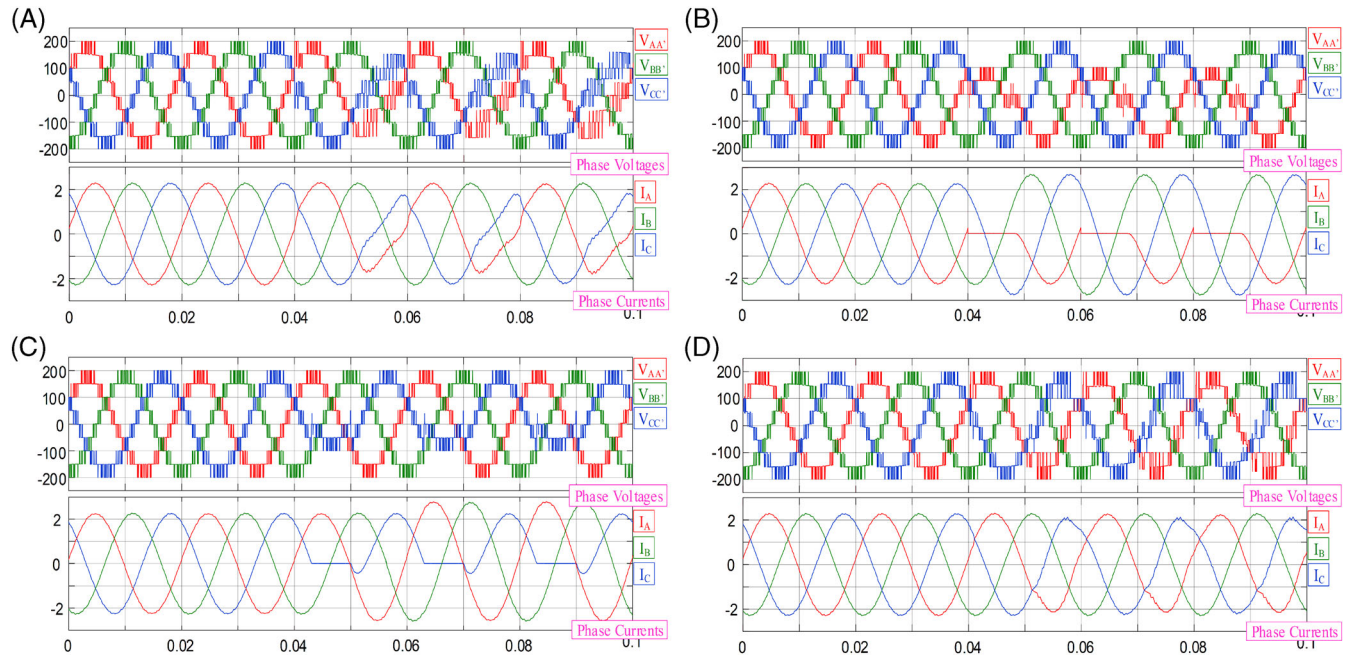


FIGURE 6 Simulation results of three-phase voltages and currents of SCBT with open-circuit fault in switch: A, S_{1a}; B, S_{3a}; C, S_{5a}; D, S_{7a}

voltage, and for faults in any other switches than these, the power delivered will decrease. The maximum output voltage is restricted to source voltage (V) under these conditions. The SPWM with reduced M_a for MSL is shown in Figure 7.

Whenever an OC fault occurs in any of the switches, instead of complete shutdown of the supply system, the proposed topologies are made to operate with MSL provided in Tables 5 and 6. If the OC fault occurs in switch S_{1A}, then the switching logic is designed for the healthy switches in the inverter-A and such logic is given in column-I in Table 5 for FCLBT and in Table 6 for SCBT. The switching logic for other switches when switch S_{1A} is open-circuited in

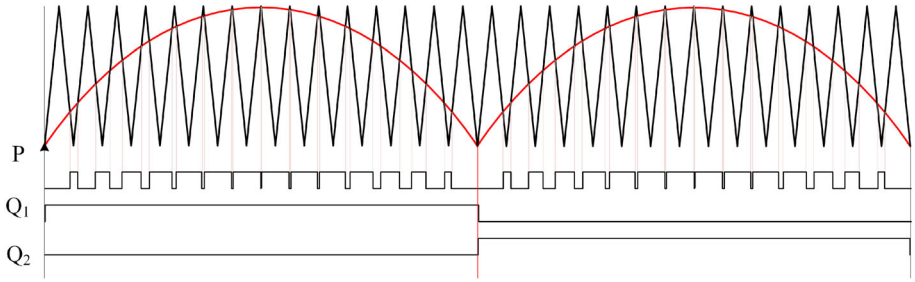


FIGURE 7 Modulation scheme with Ma = 0.5 and corresponding gate pulses

TABLE 5 Modified switching logic for FCLBT during switch OC fault conditions

Inverter-A	**Open-circuited switch**					
Switch	**I. S_{1A}**	**II. S_{4A}**	**III. S_{2A}**	**IV. S_{3A}**	**V. S_{5A} or S_{7A}**	**VI. S_{6A} or S_{8A}**
S_{1A}	0	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	$P\bar{c}^*(Q_1 + Q_2)$		P^*Q_1	
S_{2A}	$P^*(Q_1 + Q_2)$		0	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	P^*Q_2	
S_{3A}	$P\bar{c}^*(Q_1 + Q_2)$		$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	0	$P^*Q_1 + P\bar{c}^*(Q_1 + Q_2)$	
S_{4A}	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	0	$P^*(Q_1 + Q_2)$		$P^*Q_2 + P\bar{c}^*(Q_1 + Q_2)$	
S_{5A} and S_{7A}	P^*Q_1		$P^*Q_1 + P^*(Q_1 + Q_2)$		0	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$
S_{6A} and S_{8A}	$P^*Q_2 + P\bar{c}^*(Q_1 + Q_2)$		P^*Q_2		$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	0

TABLE 6 Modified switching logic for SCBT during switch OC fault conditions

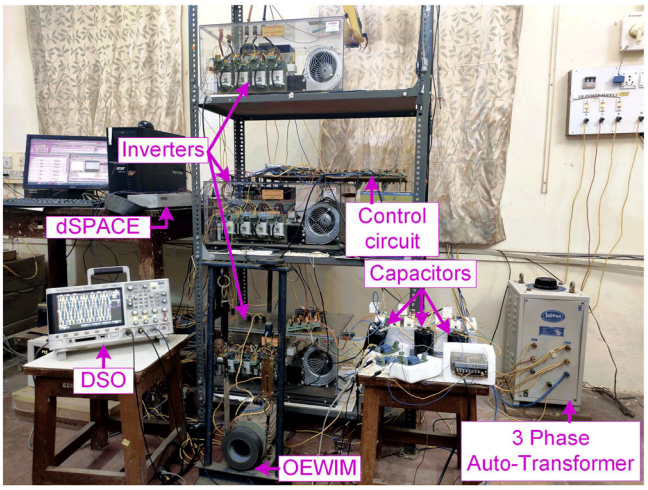
Inverter-a	**Open-circuited switch**					
Switch	**I. S_{1a}**	**II. S_{2a}**	**III. S_{3a} or S_{5a}**	**IV. S_{4a} or S_{6a}**	**V. S_{7a}**	**VI. S_{8a}**
S_{1a}	0	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	$P^*Q_2 + P\bar{c}^*(Q_1 + Q_2)$		P^*Q_2	
S_{2a}	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	0	P^*Q_1		$P^*Q_1 + P\bar{c}^*(Q_1 + Q_2)$	
S_{3a} and S_{5a}	P^*Q_1		0	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	P^*Q_1	
S_{4a} and S_{6a}	$P^*Q_2 + P\bar{c}^*(Q_1 + Q_2)$		$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	0	$P^*Q_2 + P\bar{c}^*(Q_1 + Q_2)$	
S_{7a}	$P^*(Q_1 + Q_2)$		$P^*(Q_1 + Q_2)$		0	$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$
S_{8a}	$P\bar{c}^*(Q_1 + Q_2)$		$P\bar{c}^*(Q_1 + Q_2)$		$P^*(Q_1 + Q_2) + P\bar{c}^*(Q_1 + Q_2)$	0

Note: $P\bar{c}$ is the complementary of gate pulse P.

inverter-A as presented in column-I in Table 5, the same switching logic has to be applied for all the corresponding switches in the inverter-B and inverter-C, as well to make the switching identical in all the inverters. Identical switching of inverters results in identical output voltages in all the phases.

Similarly, if the SC fault occurs in any switch, the healthy switch in such leg is completely turned-off and the gate pulses for the other switches are dispensed as given in Table 5. For example, if an SC fault occurs in switch S_{1A} then the switching logic provided in column-II for switch S_{4A} open-circuit condition is employed. This clearly shows that the switching logic for SC fault in any switch is the switching logic of the OC fault condition of its complementary switch in

FIGURE 8 Experimental set-up



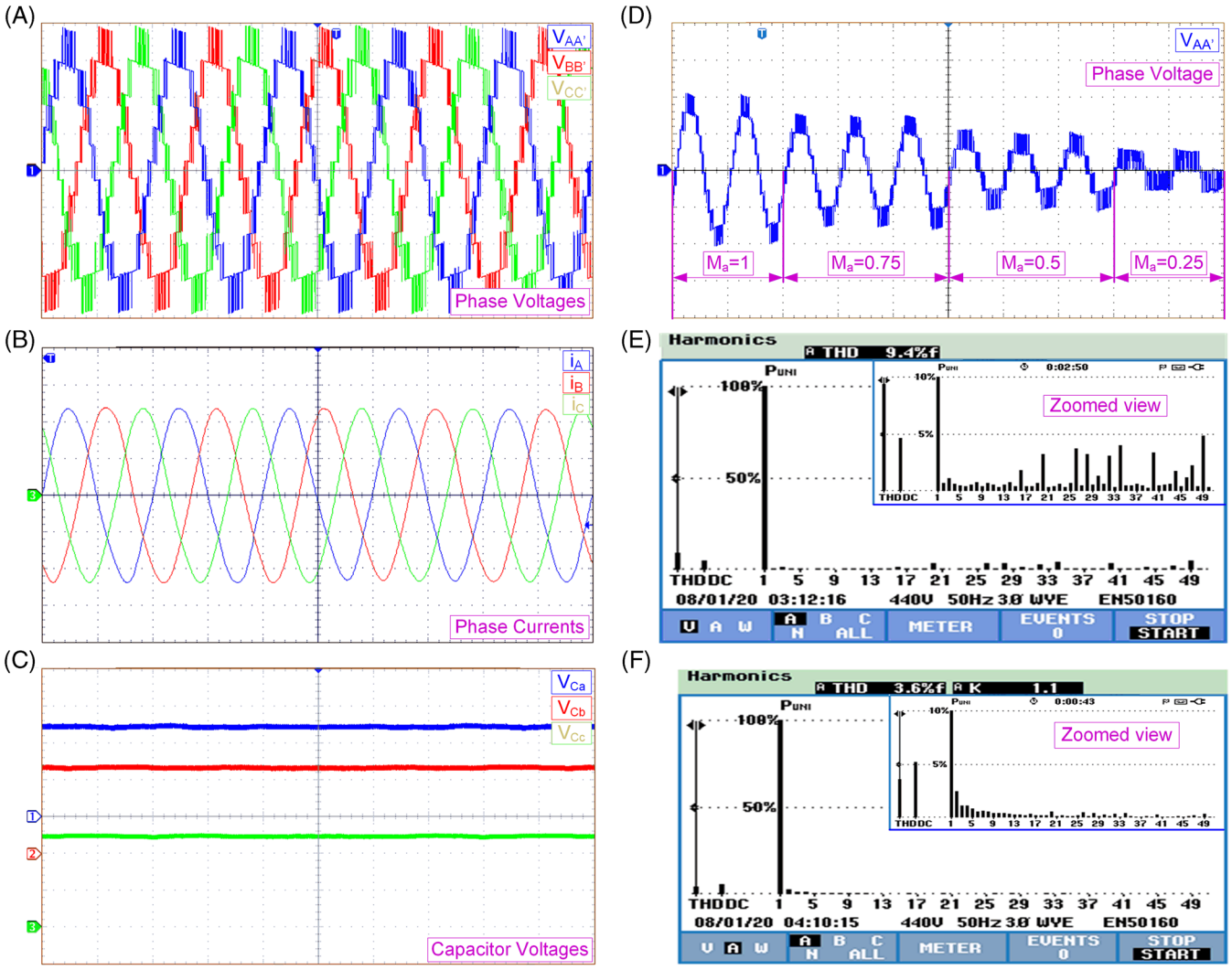


FIGURE 9 Experimental results of SCBT; A, three-phase output voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$ (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, three-phase currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, voltages across capacitor in each phase (*X*-axis: 1 s/div, *Y*-axis: 20 V/div); D, output voltage $V_{AA'}$ with variation in modulation index; E, THD for phase voltage; F, THD of phase current

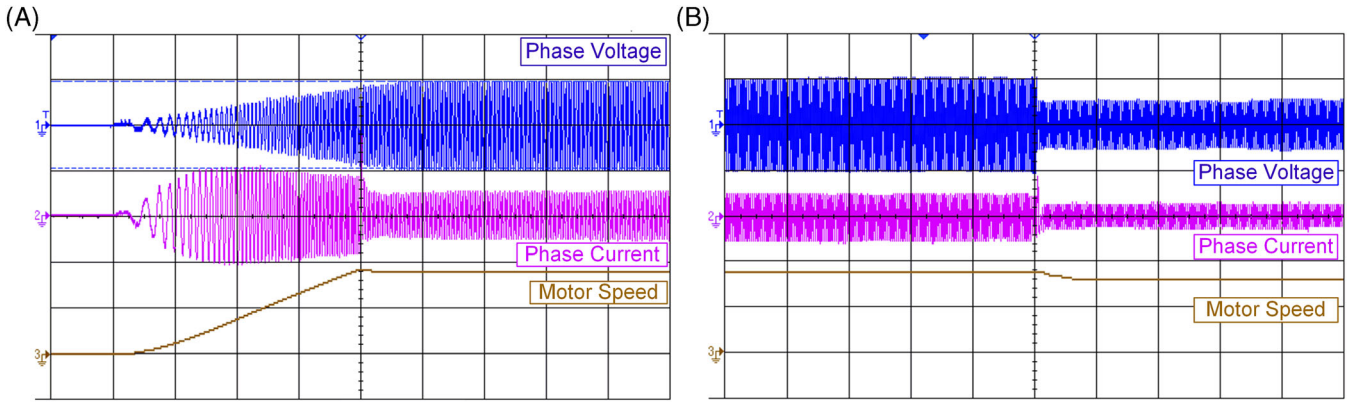


FIGURE 10 Experimental results for SCBT; A, output voltage across phase-A winding (*X*-axis: 1 s/div, *Y*-axis: 50 V/div), current through phase-A winding (*Y*-axis: 5A/div) and speed of the motor during starting (*Y*-axis: 800 rpm/div); B, output voltage across phase-A winding (*X*-axis: 2 s/div, *Y*-axis: 50 V/div), current through phase-A winding (*Y*-axis: 5A/div) and speed of the motor (*Y*-axis: 800 rpm/div) with change in modulation index from 1 to 0.5 after 5 seconds

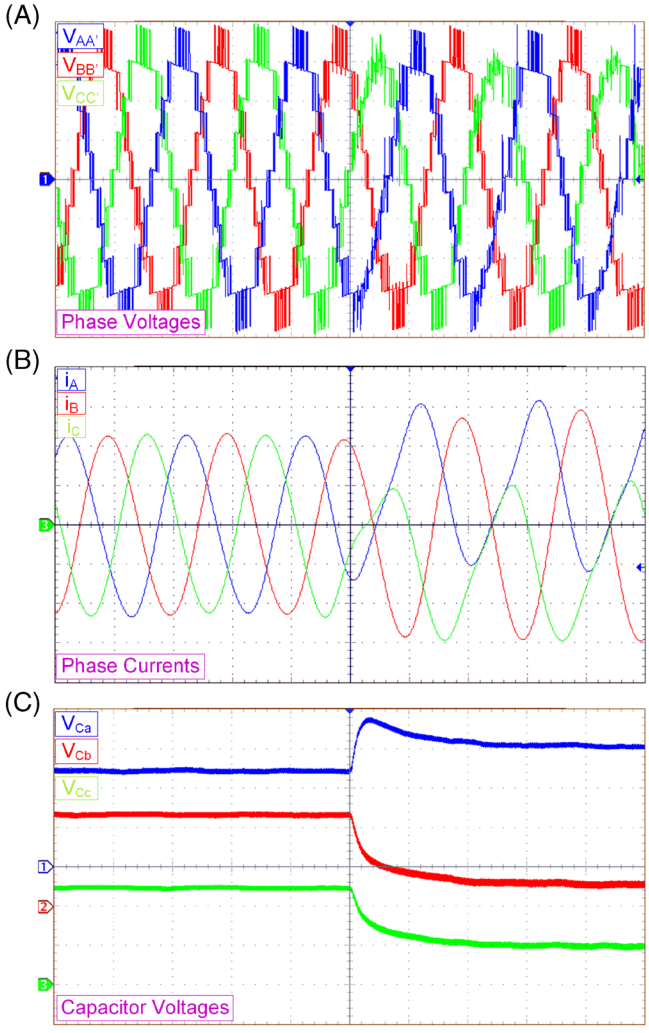


FIGURE 11 Experimental results of: A, three-phase output voltage (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, no-load currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, floating capacitor voltages (*X*-axis: 1 s/div, *Y*-axis: 20 V/div) for OC fault in switch Sa1

the same leg. The strategy applied to the OC and SC faults in any switch is the same for both the topologies. The proposed topologies are capable of operating under switch faults, hence are more reliable compared to conventional topologies.

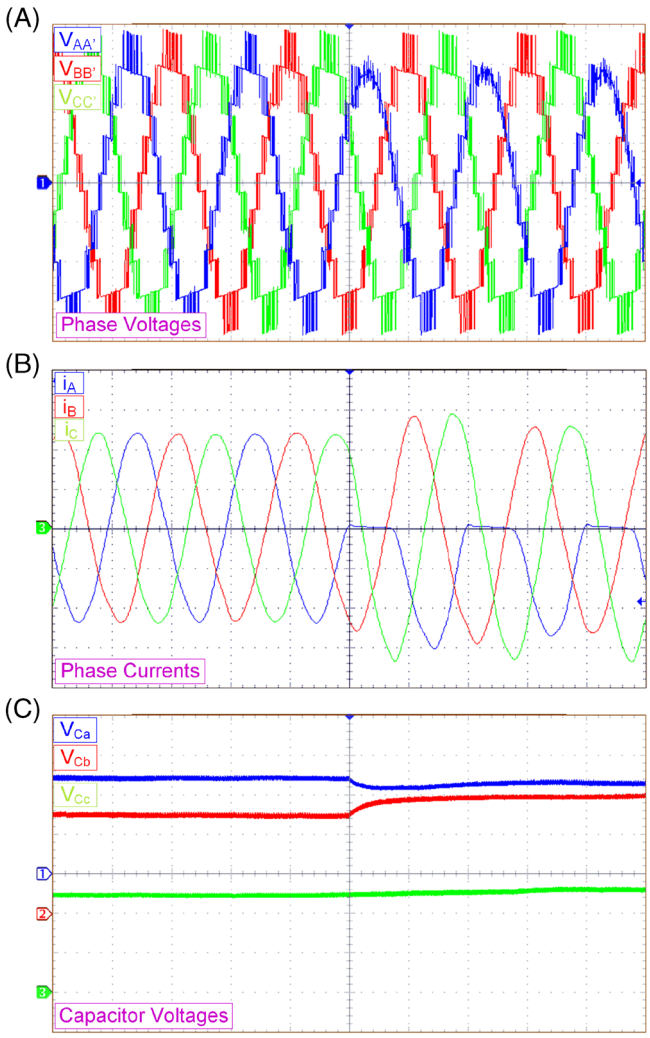


FIGURE 12 Experimental results of: A, three-phase output voltage (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, no-load currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, floating capacitor voltages (*X*-axis: 1 s/div, *Y*-axis: 20 V/div) for OC fault in switch Sa3

7 | RESULTS AND DISCUSSIONS

The proposed topologies are designed such that the switches in neutral path act as level generators, whereas the switches connected to the windings act as polarity generators. As a result, the output voltages obtained across every phase have nine levels (±2 V, ±3 V/2, ±V, ±V/2, 0) in it and the maximum output voltage is twice the source voltage (V), that is, 2 V. The proposed topologies are fed from three isolated DC sources each of 100 V to feed 1-HP OEWIM. The modified-reference PWM technique is employed to produce switching pulses for the proposed topologies and are dispensed using dSPACE 1104. A modified sinusoidal reference of the fundamental frequency is compared with the triangular carrier of frequency 1.5 kHz to generate switching pulses. The experimental set-up of the proposed topology (SCBT) feeding 1-hp OEWIM is presented in Figure 8.

7.1 | Experimental results

The three-phase output voltages, currents at no-load through three-phase windings and the voltage across the FCs in the inverters feeding the OEWIM from SCBT are illustrated in Figure 9. Figure 9A presents the phase voltages $V_{AA'}$ (blue trace), $V_{BB'}$ (red trace) and $V_{CC'}$ (green trace) across the load terminals A-A′, B-B′ and C-C′, respectively. The terminals A-A′, B-B′ and C-C′ represent phase-A, phase-B and phase-C windings of the OEWIM, respectively. Figure 9B represents three-phase currents i_A (blue trace), i_B (red trace) and i_C (green trace) drawn by the OEWIM at no-load condition. Figure 9C presents the voltages V_{Ca} (blue trace), V_{Cb} (red trace) and V_{Cc} (green trace) that represent the voltage across the FC in inverter-a, inverter-b and inverter-c, respectively. The output voltage $V_{AA'}$

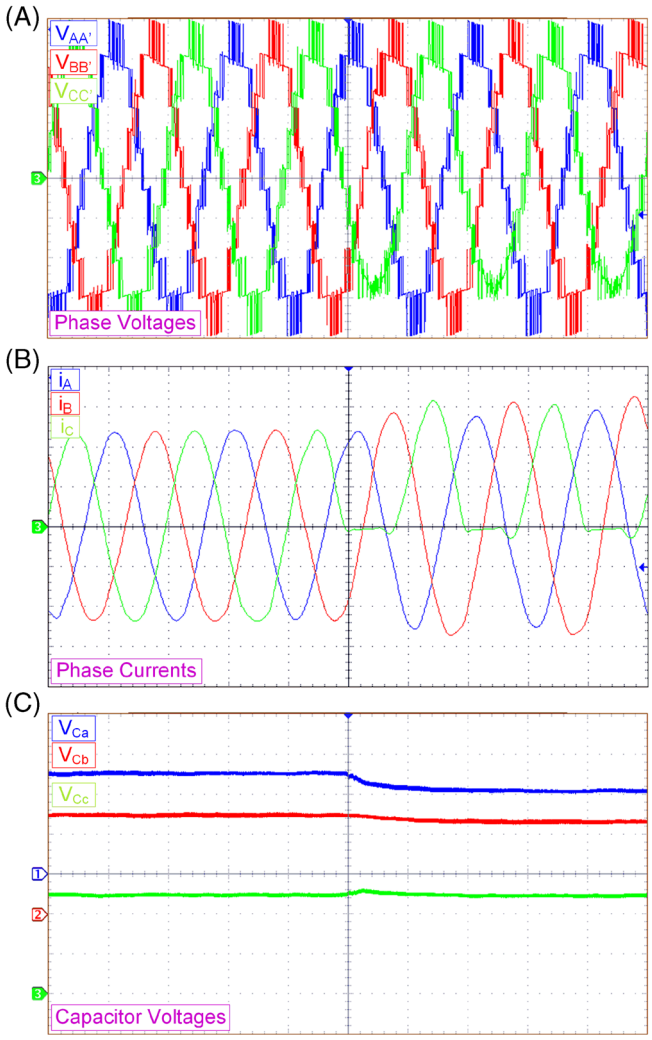


FIGURE 13 Experimental results of: A, three-phase output voltage (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, no-load currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, floating capacitor voltages (*X*-axis: 1 s/div, *Y*-axis: 20 V/div) for OC fault in switch Sa5

for various values of modulation index (Ma = 1, 0.75, 0.5, 0.25) is presented in Figure 9D. The fast Fourier transform (FFT) of THD in the output phase voltage ($V_{AA'}$) and current (i_A) in phase-A are presented in Figure 9E,F, respectively.

The behaviour of the system during starting with an increase in modulation index from 0.2 to 1 is illustrated in Figure 10A. The reference wave magnitude is determined by constant V/F ratio and speed requirement of the motor. The transition of output voltage from three levels to nine levels can be observed clearly. During starting, the current drawn by the IM is high and as the motor speed approaches the rated value, the current approaches the rated value. Figure 10B illustrates the behaviour of the system for a change in modulation index from 1 to 0.5. Decrease in modulation index will decrease the number of levels from nine to five in the output voltage, hence the output voltage magnitude reduces to half. The speed of the motor also reduces from 1440 rpm to 1270 rpm.

7.2 | Performance of SCBT during switch faults

The SCBT delivers nine-level output voltage across all the three phases under normal operating conditions. The balanced and identical output voltage across all the three phases is obtained from the inverters owing to symmetrical switching of the switching devices. However, if any of the switch fails (either OC or SC), then it leads to loss of symmetry in switching and results in unbalance in the voltage fed to the OEWIM drive. Therefore, the unbalance in the supply fed to the motor will result in unbalanced currents that lead to excessive heating of the winding.

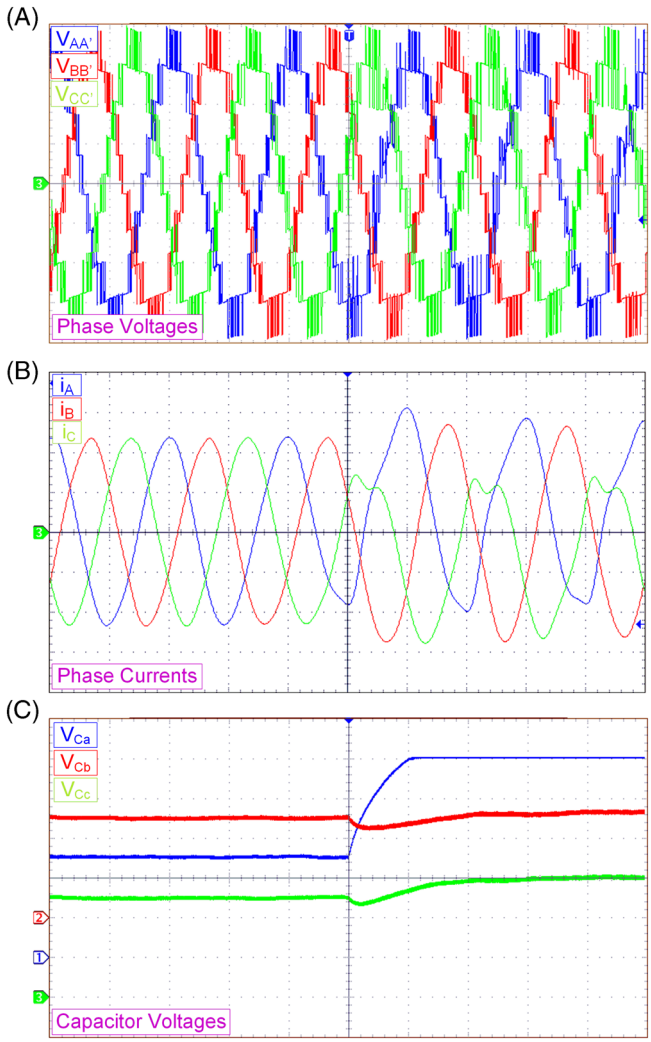


FIGURE 14 Experimental results of: A, three-phase output voltage (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, no-load currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, floating capacitor voltages (*X*-axis: 1 s/div, *Y*-axis: 20 V/div) for OC fault in switch Sa7

The effect of OC fault in switches on three-phase output voltages, no-load currents and the voltage across the FCs are to be analysed. The OC fault is created by disengaging switching pulses to the switch. Since each inverter is provided with an FC, the variation of capacitor voltages due to switch faults will be substantial depending upon the fault location. To clearly understand the variation in the FC voltages during switch faults, the scale for *X*-axis of capacitor voltages is taken as 1 s/div. The waveforms of the output voltages and currents for OC of switch S_{1a} in inverter-a are presented in Figure 11A,B. The effect of switch S_{1a} OC on FC voltages is presented in Figure 11C. Switch S_{1a} is in the neutral path of the inverter topology and is linked with phase-A and phase-C. Hence the OC of the switch S_{1a} will affect the output of two phases. The negative peak of voltage $V_{AA'}$ and the positive peak of the voltage $V_{CC'}$ are affected. The voltages across FCs also get affected with this switch fault. The voltage across FC in inverter-a increases to 60 V and the voltage across FC in inverter-b and inverter-c decreases to 10 V and 20 V, respectively.

Similarly, if OC fault occurs in switch S_{2a}, since the switch S_{2a} is operating in complementary to the switch S_{a1}, the positive peak of the voltage $V_{AA'}$ and the negative peak of the voltage $V_{CC'}$ will be affected. Consequently, the OC fault in switch S_{2a} would produce outputs as a vertical flip version of the results presented for OC of switch S_{1a}. Hence the faults in lower switches in the inverter legs that operate in complementary with upper switches are not produced. Figure 12 presents the output voltages, no-load currents and FC voltages when switch S_{3a} is open-circuited. Since the switch S_{3a} in inverter-a is connected to phase-A winding, fault in such switch will affect the phase voltage $V_{AA'}$ and limits the flow of current during positive half cycle as illustrated in Figure 12A,B. The current i_A will be a positive clamped wave with this switch fault. The FC voltage V_{Cc} is least affected with this fault, whereas the voltage V_{Ca} decreases slightly from 50 V to 46 V and the voltage V_{Cb} rises to 60 V as illustrated in Figure 12C.

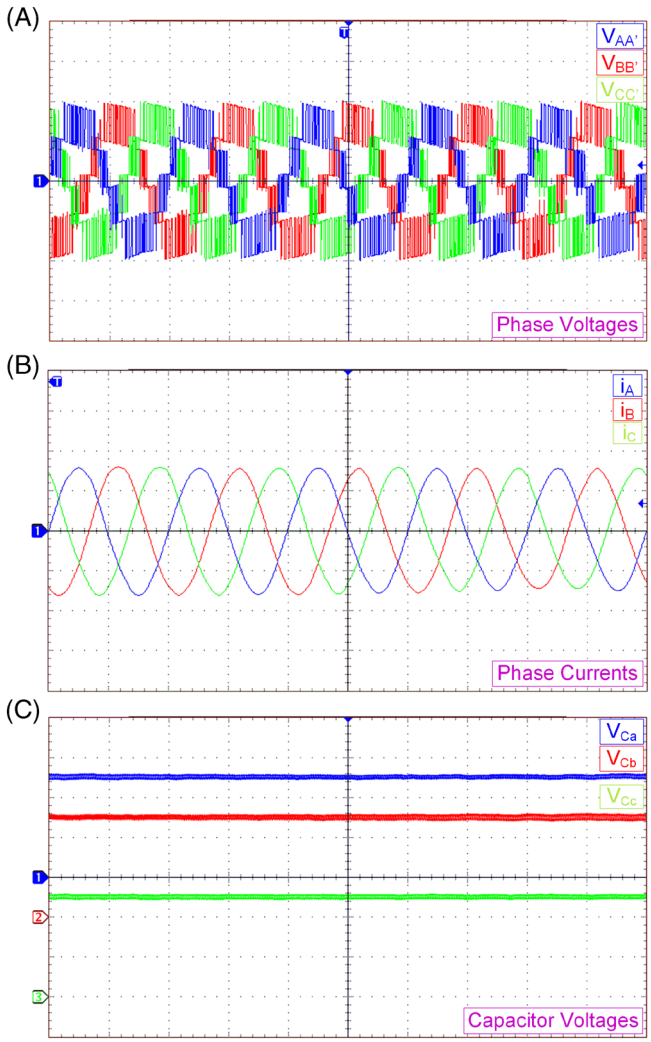


FIGURE 15 Experimental results of: A, three-phase output voltage (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, no-load currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, floating capacitor voltages (*X*-axis: 1 s/div, *Y*-axis: 20 V/div) with MSL for Sa1 OC in SCBT

Similarly, if OC fault occurs in switch S_{5a} in inverter-a, the output voltages, no-load currents and the voltage across FCs will be as illustrated in Figure 13. As the switch S_{5a} is connected to phase-C, then the OC fault in S_{5a} will affect the negative peak of voltage $V_{CC'}$ and does not allow any current in the negative cycle as illustrated in Figure 13A,B. The voltage across all the three FCs will be affected as illustrated in Figure 13C.

The output voltages, no-load currents and voltage across FCs when switch S_{7a} gets OC are presented in Figure 14. The OC fault in S_{7a} will avoid FC C_a from charging and discharging, hence the number of levels in the output voltage will gradually decrease to five levels, keeping the maximum voltage the same as that with nine levels in the output voltage as illustrated in Figure 14A,B. The voltages $V_{AA'}$ and $V_{CC'}$ will get affected with this fault and the voltage V_{Ca} will rise to source voltage $V_{DC}/2$ as the switch S_{7a} is open-circuited. The FC voltage V_{Cb} rise marginally and V_{Cc} increase from 50 V to 60 V as illustrated in Figure 14C. Hence the withstanding voltage of the FCs used for this topology should be the same as that of the source voltage ($V_{DC}/2$) such that the capacitors can withstand the voltage under such fault conditions without any damage.

7.3 | Performance of the proposed topologies with MSL

The proposed topologies are capable of operating even under switch fault conditions. Whenever OC fault occurs in any of the switches, instead of complete shutdown of the supply system, the proposed topologies are made to operate with MSL provided in Tables 5 and 6 designed considering the available switches exempting the faulty switch.

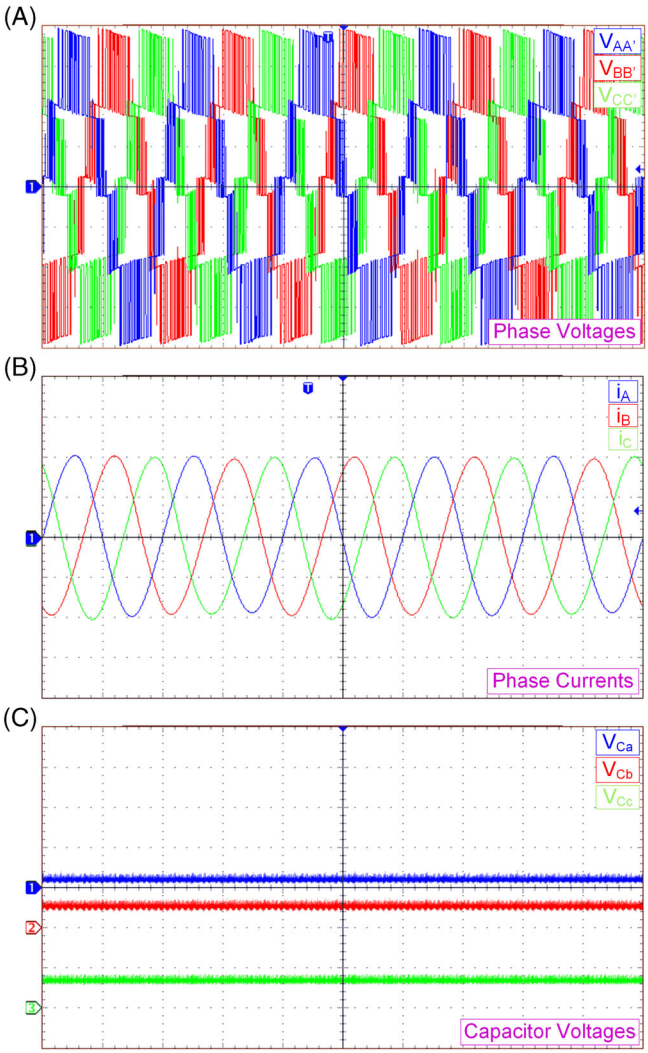


FIGURE 16 Experimental results of: A, three-phase output voltage (*X*-axis: 10 ms/div, *Y*-axis: 50 V/div); B, no-load currents (*X*-axis: 10 ms/div, *Y*-axis: 500 mA/div); C, floating capacitor voltages (*X*-axis: 1 s/div, *Y*-axis: 20 V/div) with MSL for Sa7 OC in SCBT

Lowering the value of M_a not only reduces the number of levels in the output voltage, its magnitude also reduces to half and hence the output power reduces. The FCs are charged to the same voltage level of V/2 with MSL as illustrated in Figure 15C. However, for the faults in switches S_{x7} and S_{x8} (where x ϵ a, b, c), the application of MSL will result in five-level output voltage with maximum output voltage twice the source voltage as depicted in Figure 16A. Since the FCs have no role to play in the post-fault operation, the voltages across the FCs drop near to zero as illustrated in Figure 16C. Therefore, the presented results prove that the proposed topologies work satisfactorily as five-level inverters with rated power even if the fault occurs in FC or the switches across the FC.

The proposed topologies ensure operation through normal conditions with nine-level output voltage with each step level as V/2 across each phase winding. During fault conditions, such as switch OC or SC, the proposed topologies still ensure uninterrupted operation with the decrease in levels in the output voltage as well as power. This uninterrupted operation of the proposed topologies is ensured by amending the switching pulses fed to the switches for post-fault operation. Through this study of proposed topologies over normal and abnormal conditions with pre- and post-fault analyses, it can be justified that the proposed topologies exhibit fault-tolerance property for switch faults.

Every single MLI topology possesses both advantages and shortcomings based on the area of application, and the proposed topologies are not an exemption. Compared with the conventional topologies (NPC, FC and CHB topologies), the proposed topologies have certain shortcomings such as non-modular structure and require three isolated DC sources. However, with the advantages of low source voltage requirement, simple construction and its fault-tolerance property, the proposed topologies find applications in low-voltage applications such as solar PV or fuel cell fed battery-driven electric vehicles or in industries such as steel rolling mills, paper rolling mills, etc.

8 | CONCLUSION

This paper presents FC-based fault-tolerant MLI topologies that can deliver nine-level output voltage. The proposed topologies employ a configuration that requires three three-phase inverters with an isolated DC source, FCs and additional active switches for each inverter. The FCs are charged and discharged to generate intermediate levels of the output voltage. Conventional SPWM techniques can be employed to generate switching pulses for these topologies. The proposed topologies are designed with fewer components compared to other nine-level topologies feeding OEWIM drive that are present in the literature. The magnitude of voltage sources required is also less compared to conventional topologies, hence the proposed topologies find good scope in renewable energy source applications and industry as well. The voltage rating of the FCs required is only half the source voltage rating, but to withstand the voltage during certain switch faults, the rating of the FCs should be made equal to source voltage. Both the topologies are capable of delivering power to the load during switch fault conditions. In the post-fault operation, the inverters are run with MSL and can deliver balanced three-phase output voltage with reduced number of levels, thereby ensuring continuity of supply to load even under switch fault conditions. The proposed topologies suit better for medium- and high-power traction and industrial drive applications.

PEER REVIEW

The peer review history for this article is available at https://publons.com/publon/10.1002/2050-7038.12718.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available within the article and also in appropriate references.

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