Received: 19 April 2021 | Accepted: 30 August 2021

DOI: 10.1002/2050-7038.13104

RESEARCH ARTICLE

WILEY

A space vector PWM scheme for an open-end winding induction motor drive with a reduced power loss

Patnana Hema Kumar[1] | **Debashis Mishra**[1] | **Suresh Lakhimsetty**[2] | **V. T. Somasekhar**[1]

[1]Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India

[2]Department of Electrical Engineering, Sardar Vallabhbhai National Institute of Technology Surat, Surat, India

Correspondence
Patnana Hema Kumar, Department of Electrical Engineering, National Institute of Technology, Warangal, Telangana 506004, India.
Email: hema1729@student.nitw.ac.in

Handling Editor: Dr. Zheng, Zedong

Summary

The dual-inverter fed open-end winding induction machine drive is a promising power circuit for medium-voltage, high-power industrial applications. This drive accomplishes 3-level inversion using a couple of ordinary 2-level voltage source inverters. Several PWM schemes were proposed for this drive to obtain a good harmonic performance. In this paper, an improvised space vector PWM (SVPWM) scheme is presented, which is named the *phase clamped and alternate switched* (*PCAS*) PWM strategy. This PWM scheme brings in a considerable reduction in the switching power loss in the dual-inverter system. The PCAS-SVPWM strategy switches only two phases of the switching inverter in any given sampling time period, unlike the other SVPWM schemes, wherein all the three phases of the switching inverter undergo a switching action. In addition, the proposed SVPWM achieves the waveform symmetries and reduces the common-mode voltage. Simulation results suggest that this PWM scheme results in a reduction of the overall power loss, which is in the range of 4.5% to 11% across the entire range of modulation, depending upon the rating of the machine. The effectiveness of the proposed PCAS-SVPWM scheme is assessed with simulation studies and is experimentally validated with laboratory prototype.

KEYWORDS

3-level inversion, inverter losses, open-ended winding induction machine drive (OEW-IMD), space vector pulse width modulation (SV-PWM), zero-vector placement

List of Symbols and Abbreviations: u_{xo}, u_{yo} and u_{zo}, Inverter-I pole voltages; $u_{x'o'}$, $u_{y'o'}$ and $u_{z'o'}$, Inverter-II pole voltages; $U_{dc}/2$, DC link voltage; $\boldsymbol{i_x}$, $\boldsymbol{i_y}$ and $\boldsymbol{i_z}$, Phase currents of OEWIM; 'R_s' & '$R_{r'}$', stator and the rotor phase resistances of OWIM; 'L_{ls}' & '$L_{lr'}$', stator and rotor phase leakage inductance of OWIM; 'Lm', mutual inductance; 'L_{ms}', stator magnetizing inductance; 'λ_{qs}' & 'λ_{ds}', q-axis and d-axis stator flux linkages; '$\lambda_{qr'}$' & '$\lambda_{dr'}$', q-axis and d-axis rotor flux linkages; 'i_{qs}' & 'i_{ds}', q-axis and d-axis stator currents; '$i_{qr'}$' & '$i_{dr'}$', q-axis and d-axis rotor currents; 'j', inertia of the OWIM; 'B', damping co-efficient of the OWIM; 'P', number of poles; $u_{xx'}$, $u_{yy'}$ and $u_{zz'}$, Stator phase voltages of open end winding induction motor; $u_{xx'r'}$, $u_{yy'r'}$ and $u_{zz'r'}$, Rotor phase voltages of open end winding induction motor; θ, Angle subtended by the 'q-axis' of the 'qd0' reference frame with respect to the axis of the X-phase winding of the stator; m_a, modulation index; ASHC, Alternate sub-hexagonal centre; DSAZE, Decoupled SAZE; IM, Induction Motor; NSHC, nearest sub-hexagonal centre; OWIM, Open-end Winding Induction Motor; PCAS, Phase Clamped and Alternate Switched; PWM, Pulse Width Modulation; SAZE, Sample Averaged Zero-sequence Elimination; SVPWM, Space Vector PWM; VSI, Voltage Source Inverter.

1 | INTRODUCTION

Modern industrial drive applications require regulating the output variables of electric motors against supply and loading disturbances, while complying with the requirements of the process as stipulated by controllers. Power electronic converters such as voltage source inverters (VSIs) are extensively used to accomplish this need in variable frequency drives as reflected by the authors.[1-4] Requirement to operate with high DC-link voltages while accomplishing a better spectral performance, coupled with the advances in the technology of power semiconductor switching devices, paved way to the development of multilevel converters, as evident from the work by authors.[2-4] The open-stator-based motor drives are an off-beat approach to multilevel conversion and seem to be promising in medium-voltage and medium power applications, as in both the works of authors.[1,5] A lot of technical literature has been produced in the arena of open-end winding induction motor (OWIM) drives. OWIM drives are very promising in electric vehicles owing to their superior fault-tolerant capabilities. OWIM drives display a good potential for medium voltage high power applications such as industrial pumps, fans, compressors, etc.

In a three-level OWIM drive, an open-stator induction motor is fed with a couple of two-level VSIs from either end. Each VSI is fed with a DC power supply with half of the magnitude of the voltage required in a conventional induction drive (wherein a star or a delta-connected motor is used). In other words, rated voltage is impressed across any given motor-phase winding with *two* DC power supplies (each powering one of the VSIs), each of which is capable of applying half of the rated voltage across it in a conventional (ie, star or delta connected) motor drive system.

A total of 64 switching vectors are output from this dual-inverter system. An appropriate utilization of these switching vector combinations could pave way to devise a Pulse Width Modulation (PWM) scheme, which results in a reduced switching frequency for the dual-inverter system. On the negative side, OWIM drives, which are driven with a single DC power supply, are susceptible to the problems associated with the zero-sequence currents. The unwanted effects of the zero-sequence current are well documented in the work of authors.[6-9] In short, the zero-sequence current, without contributing to the process of electromechanical energy conversion, heats up the motor and stresses the power semiconductor switching devices of the constituent VSIs of the dual-inverter system.

Several approaches are suggested in the literature to avoid the zero-sequence currents. These are: (a) use of additional bi-directional switching devices as in Reference 6 (b) use of PWM schemes given by work of authors,[7-9] and (c) use of isolated Direct Current (DC) power supplies given by work of authors.[10-13]

The power circuit with additional bi-directional switches increases the complexity of the power circuit as shown in Figure 1 as it requires either: (a) eight additional active switching devices (on the base of 12), or, (b) four active switching devices with 16 additional diodes. On the positive side, with this approach, the DC-link can be utilized to the fullest possible extent. In addition, a single DC power supply (with half the rated voltage) can be employed to impress the rated voltage across the motor phase windings. However, the additional active switching devices also require

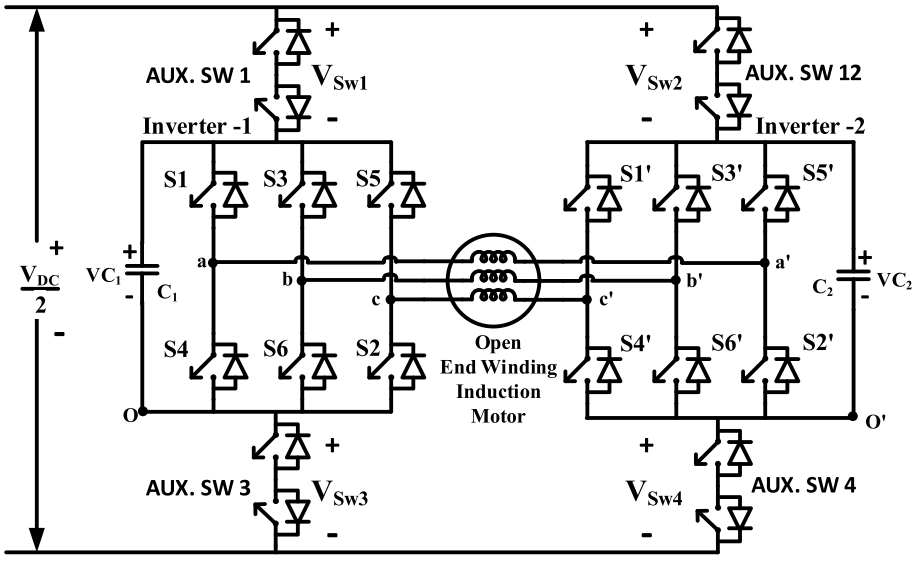

FIGURE 1 Schematic configuration of the dual-inverter fed OWIM with a single DC power supply

additional gating and protection circuitry, making the power circuit more complex and consequently less reliable, owing to the increased component count.

The zero-sequence current in the OWIM drives can also be avoided with specially devised PWM schemes. The advantage with this approach is that the OWIM drive can be realized with a single power supply as shown in Figure 2.

However, the DC-link utilization with this approach is reduced by 15% compared to the hardware approach described in the above paragraph. Two PWM schemes, called the sample averaged zero-sequence elimination (SAZE) highlighted in Reference 8 and the decoupled sample averaged zero-sequence elimination (DSAZE) highlighted in Reference 9 PWM strategies represent this genre of PWM schemes.

In the SAZE PWM scheme, one of the two VSIs (called the clamping inverter) is switched with a vector (called the clamping vector), which is situated nearest to the sample. For a given sample, the clamping vector is found at a Sub-Hexagonal Center (SHC). The second VSI (called the switching inverter) is switched around the vectored offset produced by the clamping inverter. Exploiting the freedom of choice in the placement of the active vectors to advantage, the SAZE PWM scheme suppresses the zero-sequence voltage in the average sense in each sampling time period. The advantage with this PWM scheme is that only one inverter of the two is switched in any given sampling time period. This would weigh favorably toward the SAZE PWM in terms of the reduction of the switching power losses. However, the ripple in the motor phase current is increased, partially offsetting this advantage as in the work by authors.[14]

In contrast, both inverters are made to switch in the DSAZE PWM scheme. In this PWM scheme, the reference voltage space vector of the overall dual-inverter scheme is resolved into two components, which are equal in magnitude and are anti-phased with reference to each other. Each VSI is switched with one of these two components. Though this PWM strategy results in a higher switching power loss, the *apparent* switching frequency is twice as that of the actual switching frequency. Furthermore, the overall dual-inverter system is operated with the center spaced space vector PWM scheme, unlike the SAZE PWM scheme, which is a noncentric PWM scheme.

Owing to these factors, the DSAZE PWM scheme results in a better spectral performance compared to the SAZE PWM scheme. The improved harmonic performance would translate into reduced ripple in the motor phase current. This in turn would result in a reduced torque ripple and reduced ohmic loss in the motor. Despite these advantages, the DSAZE PWM scheme suffers from two principal disadvantages, namely: (a) higher switching power loss in the dual-inverter system (as both VSIs are switched in any given sampling time period), and (b) degradation of the DC-link utilization by a factor of 15%.

The third approach to prevent the zero-sequence currents is to resort to *electrical isolation*, that is, the use of two isolated DC power supplies as shown below in Figure 3.

When two separate DC power supplies are employed to power each VSI, the zero-sequence current (constituted by the harmonic components of the triple order) will not flow due to lack of a return path. These two DC power supplies are obtained either from battery banks or by the rectification of the output of two isolation transformers connected to the grid. The latter option is particularly suited for high power drives, where electrical isolation is mandatory as in the work by authors.[10-13,15,16]

Thus, the use of isolation transformers avoids additional power semiconductor switching devices, enhancing the reliability of the drive. Furthermore, with electrical isolation, the discontinuous (phase-clamped) SVPWM switching schemes can be implemented without causing the zero-sequence current.

Several discontinuous (phase-clamped) SVPWM schemes have been described in the literature for the conventional induction motor (IM) drive. The benefits reaped by the extension of these discontinuous PWM schemes for the dual-inverter-fed three-level OWIM drives with electrical isolation are not addressed.

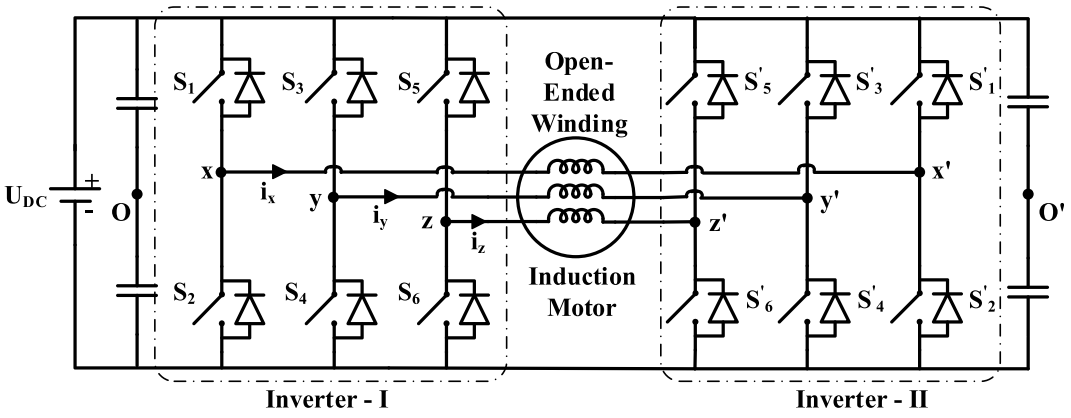

FIGURE 2 Schematic configuration of the dual-inverter fed OWIM with a single DC power supply

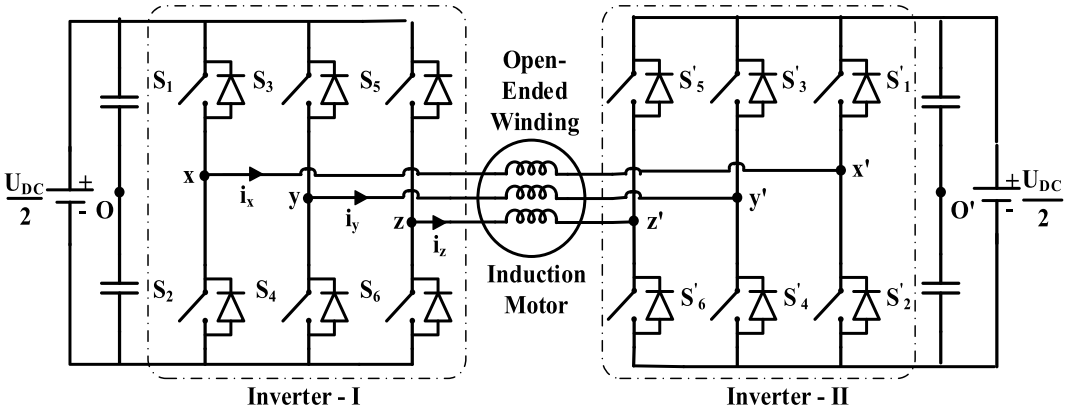

FIGURE 3 Schematic configuration of the dual-inverter fed OWIM with isolated DC power supplies

The work reported in Reference 17 proposes a space vector modulation-based technique for distributed inverter fed OWIM drive for the EV-applications, wherein each phase of the OWIM is fed by a separate DC power supply and an associated 2-level VSI.

SVPWM strategies have also been proposed in OWIM drives with higher number of voltage levels. In the research work presented in References 18,19 a decoupled-SVPWM based strategies for the OWIM configuration is proposed, in which both inverters are switched simultaneously, resulting in the shifting of the harmonic spectrum to double the switching frequency. Furthermore, these SVPWM strategies are extended to the 5-phase OWIM and the OWPMSM drive configurations as well[20,21] to achieve the objectives of avoiding the common-mode currents and reducing the ripple in the phase current.

This paper proposes a 3-level OWIM drive with two isolated DC power supplies, which employs the phase-clamped SVPWM technique. With the proposed SVPWM scheme, one inverter is clamped in any given sampling time period, while the other inverter is switched, as in the case of the NSHC PWM scheme described in Reference 5. However, the switching inverter employs the phase-clamping feature, in which switching occurs only in two of the three phases. In general, the output voltage waveform of any inverter should possess waveform symmetries viz. the quarter-wave symmetry, the half-wave symmetry and the three-phase symmetry. The phase clamping of the switching inverter leads to asymmetrical switching. The proposed SVPWM achieves the waveform symmetries, despite this asymmetry in the switching. Hence, this scheme does not only restore the advantage of improved DC-link utilization (by 15%), but also result in reduced switching (by 33.3%), which would enhance the efficiency of the OWIM drive.

Through simulation studies, this paper shows that this reduction in switching would result in a significant reduction in switching power loss. Admittedly, reduction in switching increases the duration of conduction in the switching devices. However, simulation studies indicate that the advantage of decreased switching loss outweighs the disadvantage of increased conduction loss, resulting in the reduction of overall power loss in the dual-inverter system.

To substantiate this point further and to prove the generality of the proposed PWM scheme, it is tried on two motors of different power ratings; one of the motors is a 4 kW motor and the other is a 160 kW motor. Simulation studies reveal that the overall loss of the dual-inverter system would reduce in the range of 18% to 31% with the proposed SVPWM scheme. The proposed SVPWM scheme is experimentally validated on a 4 kW motor and the experimental results have been presented along with the simulation results.

2 | MODEL OF THE DUAL-INVERTER SYSTEM AND OWIM

As stated earlier, an OWIM is fed from both ends with two 2-level inverters. The modular dual-inverter fed OWIM drive as drawn in Figure 3 comprises six poles (namely x, y, z, x′, y′, z′) and 12 switches. The pole-voltages of inverter-I are symbolized by $\boldsymbol{u_{xo}}$, $\boldsymbol{u_{yo}}$, and $\boldsymbol{u_{zo}}$, while for inverter-II they are: $\boldsymbol{u_{x'o'}}$, $\boldsymbol{u_{y'o'}}$, and $\boldsymbol{u_{z'o'}}$. Each DC link voltage is of magnitude $\boldsymbol{U_{dc}/2}$. The currents flowing in the corresponding phases of OWIM are symbolized by $\boldsymbol{i_x}$, $\boldsymbol{i_y}$, and $\boldsymbol{i_z}$.

A 2-level inverter assumes eight possible switching states, spread over seven space vector locations and six sectors. As indicated in Figure 4, these switching states are numbered from 1 to 8 (for Inverter-I) and 1′ to 8′ (for Inverter-II), respectively. Therefore, the total number of space vector combinations for the dual-inverter system is 64, that is, . (8*8).

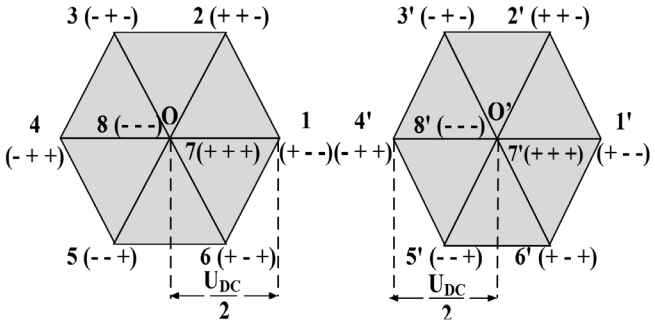

FIGURE 4 SVPWM diagrams for (A) Inverter-I (B) Inverter-II

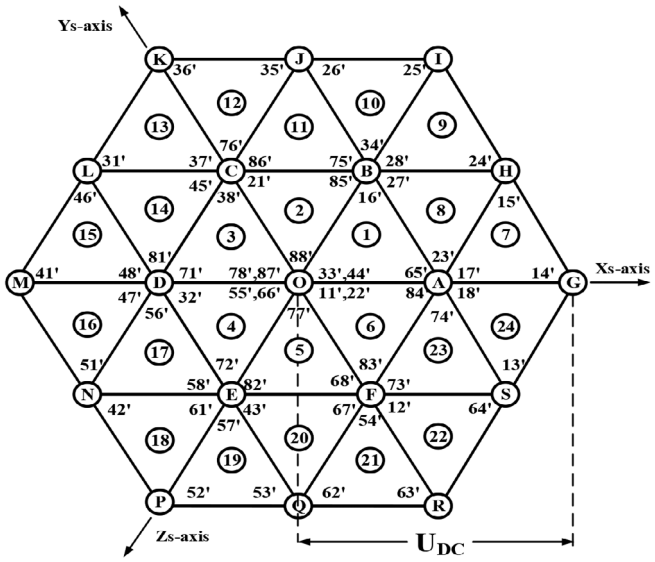

FIGURE 5 SVPWM diagram for the dual-Inverter system

These vector combinations are obtained by superposing the space-vector diagram of inverter-II upon inverter-I (Figure 4).

The resultant SVPWM diagram, pertaining to the dual-inverter system, is shown in Figure 5. It may be noted that these 64 vector combinations are spread over 19 vector locations resulting in 24 sectors.

The mathematical modeling equations of IM are given as:

$$\mathrm{I} = \mathrm{L}^{-1}\lambda \tag{1}$$

$$\dot{\lambda} = \Omega\lambda - \mathrm{R}\bar{\mathrm{I}} + \mathrm{I}_4\bar{\mathrm{U}} \tag{2}$$

$$\bar{\mathrm{I}} = \begin{bmatrix} \mathrm{i}_{qs} & \mathrm{i}_{ds} & \mathrm{i}_{qr'} & \mathrm{i}_{dr'} \end{bmatrix}^{\mathrm{T}} \tag{3}$$

$$\lambda = \begin{bmatrix} \lambda_{qs} & \lambda_{ds} & \lambda_{qr'} & \lambda_{dr'} \end{bmatrix}^{\mathrm{T}} \tag{4}$$

$$\bar{\mathrm{U}} = \begin{bmatrix} \mathrm{u}_{qs} & \mathrm{u}_{ds} & \mathrm{u}_{qr'} & \mathrm{u}_{dr'} \end{bmatrix}^{\mathrm{T}} \tag{5}$$

$\mathrm{I}_4 = 4 \times 4$ unity diagonal matrix

$$R = \begin{bmatrix} R_s & 0 & 0 & 0 \\ 0 & R_s & 0 & 0 \\ 0 & 0 & R_{r'} & 0 \\ 0 & 0 & 0 & R_{r'} \end{bmatrix} \tag{6}$$

$$\Omega = \begin{bmatrix} 0 & -\omega & 0 & 0 \\ \omega & 0 & 0 & 0 \\ 0 & 0 & 0 & -(\omega - \omega_r) \\ 0 & 0 & (\omega - \omega_r) & 0 \end{bmatrix} \tag{7}$$

$$L = \begin{bmatrix} L_{ls} + L_m & 0 & L_m & 0 \\ 0 & L_{ls} + L_m & 0 & L_m \\ L_m & 0 & L_{lr'} + L_m & 0 \\ 0 & L_m & 0 & L_{lr'} + L_m \end{bmatrix} \left(\text{Where}, L_m = \frac{3}{2} L_{ms} \right) \tag{8}$$

where, "R_s" and $\}R_{r'}\}$ are the stator and the rotor phase resistances of OWIM; $\}L_{ls}\}$ and $\}L_{lr'}\}$ are stator and rotor phase leakage inductance of OWIM; "Lm" is the mutual inductance and $\}L_{ms}\}$ is the stator magnetizing inductance; $\}\lambda_{qs}\}$ and $\}\lambda_{ds}\}$ are the q-axis and d-axis stator flux linkages; $\}\lambda_{qr'}\}$ and $\}\lambda_{dr'}\}$ are the q-axis and d-axis rotor flux linkages; $\}i_{qs}\}$ and $\}i_{ds}\}$ are the q-axis and d-axis stator currents; $\}i_{qr'}\}$ and $\}i_{dr'}\}$ are the q-axis and d-axis rotor currents.

All of these parameters are measured for the OWIM using the usual OC and the blocked-rotor tests. These parameters (enumerated in Table 1) are then used to design a Simulink model for the OWIM to assess the performance of the proposed PCAS-SVPWM algorithm.

The expression for the torque developed by the motor is given by:

$$m_d = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(i_{qs} i_{dr'} - i_{ds} i_{qr'}\right) \tag{9}$$

TABLE 1 OWIM drive parameters

Parameters	Values
DC link voltage (U_{DC})	564 V
RMS phase voltage (U_{ph})	230 V
No. of samples (n)	42
Nominal frequency (f_{nom})	50 Hz
P_{rated}	5.4 HP
Rated speed	1430 rpm
Stator phase resistance of OWIM-R_S	4.215 Ω
Rotor phase resistance of OWIM-$R_{r'}$	4.185 Ω
Stator phase leakage inductance of OWIM-L_{ls}	17.517 mH
Rotor phase leakage inductance of OWIM-$L_{lr'}$	17.517 mH
Magnetizing inductance of OWIM-L_m	516.6 mH
No. of poles	4
OWIM inertia-J	0.0131 kg-s^2
Damping co-efficient of OWIM-B	0.002985 N-m-s
Rated torque-T_m	25.5 N-m

The equation for rotor speed is obtained from following equations,

$$m_d = \frac{2}{p} J \frac{d\omega_r}{dt} + \frac{2}{p} B\omega_r + m_L \tag{10}$$

$$\omega_r = \frac{1}{J} \int (m_d - m_L - B\omega_r) dt \tag{11}$$

where, "J" indicates the inertia of the OWIM; "B" indicates the damping co-efficient of the OWIM; and "P" indicates the number of poles.

The IM d-q axis voltages are defined from the dual inverter open-end winding IM as,

$$u_{qs} = \frac{2}{3}\left(u_{xx'}\cos\theta + u_{yy'}\cos\left(\theta - \frac{2\pi}{3}\right) + u_{zz'}\cos\left(\theta + \frac{2\pi}{3}\right)\right) \tag{12}$$

$$u_{ds} = \frac{2}{3}\left(u_{xx'}\sin\theta + u_{yy'}\sin\left(\theta - \frac{2\pi}{3}\right) + u_{zz'}\sin\left(\theta + \frac{2\pi}{3}\right)\right) \tag{13}$$

$$u_{qr'} = \frac{2}{3}\left(u_{xx'r'}\cos\theta + u_{yy'r'}\cos\left(\theta - \frac{2\pi}{3}\right) + u_{zz'r'}\cos\left(\theta + \frac{2\pi}{3}\right)\right) \tag{14}$$

$$u_{dr'} = \frac{2}{3}\left(u_{xx'r'}\sin\theta + u_{yy'r'}\sin\left(\theta - \frac{2\pi}{3}\right) + u_{zz'r'}\sin\left(\theta + \frac{2\pi}{3}\right)\right) \tag{15}$$

where, $u_{xx'}, u_{yy'}, \text{and } u_{zz'}$ – Stator phase voltages of open-end winding IM; $u_{xx'r'}, u_{yy'r'}, \text{and } u_{zz'r'}$ – Rotor phase voltages of open-end winding IM; θ—angle subtended by the "q-axis" of the "qd0" reference frame with respect to the axis of the X-phase winding of the stator.

The stator phase voltages are given as,

$$u_{xx'} = u_{xo} - u_{x'o'} \tag{16}$$

$$u_{yy'} = u_{yo} - u_{y'o'} \tag{17}$$

$$u_{zz'} = u_{zo} - u_{z'o'} \tag{18}$$

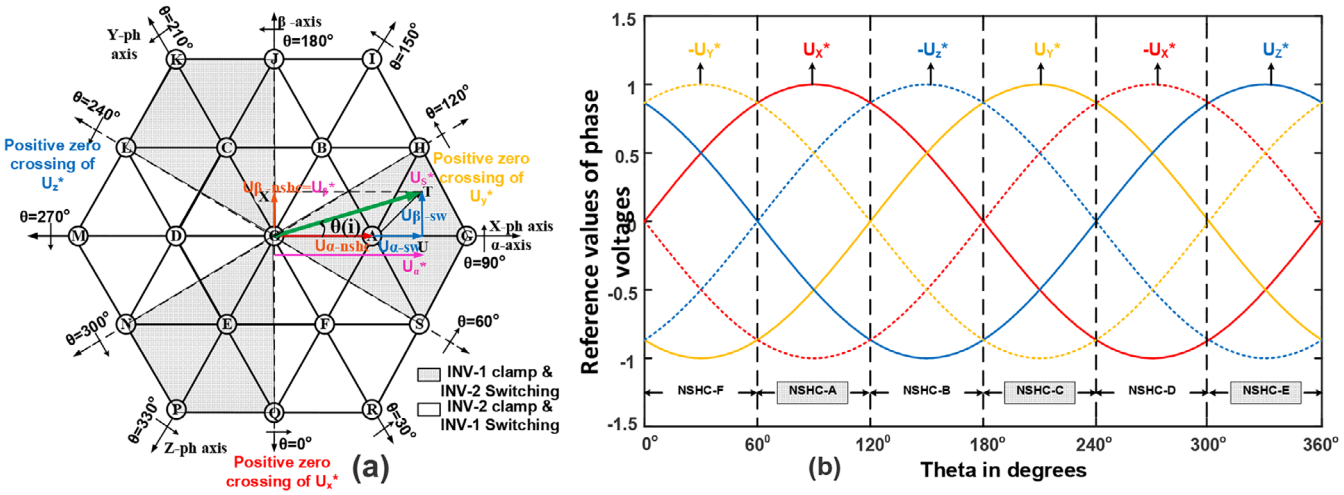

FIGURE 6 (A) Space vector diagram to analyze PCAS-SVPWM algorithm (B) Sector calculation using reference voltage waveforms

Zero sequence voltages are defined as,

$$u_{zs} = \frac{1}{3}\left[u_{xx'} + u_{yy'} + u_{zz'}\right] \tag{19}$$

The phase voltages of the open end winding IM is determined by assuming the o and o' points of dual inverter drive are shorted and their expressions are given as,

$$u_{xx'} = u_{xo} - u_{x'o'} - \frac{1}{3}u_{zs} \tag{20}$$

$$u_{xx'} = \frac{2}{3}(u_{xo} - u_{x'o'}) - \frac{1}{3}\left[\left(u_{yo} - u_{y'o'}\right) + \left(u_{zo} - u_{z'o'}\right)\right] \tag{21}$$

3 | THE PHASE-CLAMPED AND ALTERNATELY SWITCHED (PCAS) SVPWM STRATEGY

The PCAS-SVPWM scheme proposed in this paper is applicable only to an OWIM with electrical isolation (shown in Figure 3) and is an improvised version of the Alternate SHC PWM scheme proposed in the work.[12] It may be noted that the ASHC-SVPWM scheme was originally proposed to realize the OWIM drive with a single DC power supply (shown in Figure 2). A common feature of these PWM schemes is that they both require to determine the "nearest sub-hexagonal center" (NSHC), which is located nearest to the tip of the reference voltage space vector for the dual-inverter system. The ASHC-PWM scheme is briefly reviewed in the following paragraphs, which paves way to the explanation of the proposed PCAS-SVPWM scheme.

Figure 6A shows the reference voltage space vector of the dual-inverter Scheme (OT). The points *A, B, C, D, E*, and *F*, which are the centers of the sub-hexagons, such as *OBHGSF*, are known as the SHCs, which provide the clamping vectors to the dual-inverter system. The objective of the ASHC-PWM scheme is to construct the reference vector **OT** using space vector modulation (SVM).

As depicted in Figure 6A, the reference vector OT is resolved into two components, namely, **OA** and **AT**. The vector **OA** (of magnitude $\mathbf{U_{dc}/2}$) is obtained by clamping one of the two VSIs. The VSI that outputs the vector **OA** is, therefore, called as the *clamping inverter*. For the case shown in Figure 6A, there exist two such candidate clamping vectors, one from each VSI. It could either be the vector—"1" output by inverter-I (ie, $+--$, Figures 4 and 6A). It could also be the vector—"4" output by inverter-II (ie, $-++$, Figure 4). This is because; the effect of an opposite vector applied in an opposite direction would create the same effect as the original vector.

The other inverter would then produce the second component (**AT**, Figure 3) by switching around the clamping vector stipulated by the clamping inverter. For this reason, the inverter, which produces this component **AT** with the switching action, is called as the *switching inverter*. Thus, if inverter-I assumes the role of the clamping vector, then inverter-II assumes its role as the switching vector and vice versa. By switching the roles of the two inverters alternately at each SHC, it is possible to obtain an equal switching duty to these two inverters (Figure 6A).

Determination of the NSHC to the tip of the reference vector **OT** is pivotal to the implementation of the ASHC-PWM scheme. It may be noted that when the tip of the reference vector is situated in the quadrangle OHGS, the vertex 'A' becomes the NSHC. Similar observations can be made for the rest of the five quadrangles. The NSHC is deduced on the basis of the instantaneous values of the 3-phase reference voltages corresponding to the reference vector OT (Figure 6B), using the algorithm described in the work.[11] This algorithm alleviates the computational burden on the digital control platform, as cumbersome and time-consuming tasks such as sector identification and translation of active time periods into gating time periods are avoided.

In the NSHC based PWM schemes (such as the SAZE SVPWM scheme), inverter-I serves as the clamping inverter, when the NSHC is either *A*, *C*, or *E*. Hence, inverter-II serves as the switching inverter for these three NSHCs. On the other hand, if the NSHC is one among *B*, *D*, and *E*, then, the inverters are made to reverse their roles. Table 2 summarizes the roles of individual inverters, the clamping and the switching vectors employed in the ASHC-PWM. It should be noted that the symbol "θ" denotes the angle subtended by the reference voltage vector **OT** with the α-axis

TABLE 2 Determination of the NSHC

Maximum ref. voltage (Theta)	$-U_Y^*$ (0° to 60°)	U_X^* (60° to 120°)	$-U_Z^*$ (120° to 180°)	U_Y^* (180° to 240°)	$-U_X^*$ (240° to 300°)	U_Z^* (300° to 360°)
NSHC	F	A	B	C	D	E
Clamping INV (Clamping state)	INV-2 (− + −)	INV-1 (+ − −)	INV-2 (− − +)	INV-1 (− + −)	INV-2 (+− −)	INV-1 (− − +)
Switching INV	INV-1	INV-2	INV-1	INV-2	INV-1	INV-2
Uα-NSHC	$\frac{U_{DC}}{4}$	$\frac{U_{DC}}{2}$	$\frac{U_{DC}}{4}$	$\frac{-U_{DC}}{4}$	$\frac{-U_{DC}}{2}$	$\frac{-U_{DC}}{4}$
Uβ-NSHC	$\frac{-\sqrt{3}}{2}\frac{U_{DC}}{2}$	0	$\frac{\sqrt{3}}{2}\frac{U_{DC}}{2}$	$\frac{\sqrt{3}}{2}\frac{U_{DC}}{2}$	0	$\frac{-\sqrt{3}}{2}\frac{U_{DC}}{2}$

(Figure 6A). It should also be noted that the null vectors 8 (− − −) and 7 (+++) are used for inverter-II, while the null vectors 8′ (− − −) and 7′ (+++) are used for inverter-2.

The analysis for the proposed PCAS-SVPWM scheme, is presented in the following paragraphs. This analysis pertains to an instant corresponding to the one shown in Figure 6A, wherein the reference voltage space vector OT (which is constituted by the 3-phase reference voltages U_X^*, U_Y^*, and U_Z^*) has a magnitude of U_S^* and subtends an angle of $\}\theta(i)\}$ with reference to the α- axis.

The 3-phase reference voltages U_X^*, U_Y^*, and U_Z^* constitute the space vector OT (U_S^*). The component of OT along α-axis and β-axis are OT and OU (Figure 6A) denoted as U_α^* and U_β^*, respectively.

$$U_\alpha^* = U_S^* \cos\theta(i) \tag{22}$$

$$U_\beta^* = U_S^* \sin\theta(i) \tag{23}$$

where $\}i\}$ denotes the index of the sample number ($1 \le i \le 42$). Based on this angle $\theta(i)$ and the maximum value of the reference voltages $U_X^*, U_Y^*, U_Z^*, -U_X^*, -U_X^*, and -U_Z^*$ the NSHC is determined as shown in Table 2. As an example, when $60^0 \le \theta(i) \le 120^0$ (ie, when U_X^* is maximum), the NSHC is 'A'. The role of inverters and the state of the clamping inverter are presented in Table 2 for all of the six NSHCs.

The vector OT in Figure 6A can be realized using the clamping vector OA and switching vector AT. In the specific example corresponding to Figure 6A, the vector OA is realized using the clamping inverter (INV-1 with state + − −) while the vector AT is realized using the switching inverter (INV-2). The clamping vector OA is resolved into the $\alpha - \beta$ components, namely, $U_{\alpha-NSHC}$ and $U_{\beta-NSHC}$ as indicated in Table 2. Similarly, the switching vector OA is resolved into $U_{\alpha-sw}$ and $U_{\beta-sw}$ along the α-and the β-axes. The α- and β-components of the switching vector can be calculated from the Equations (24) and (25).

$$U_{\alpha-sw} = U_\alpha^* - U_{\alpha-NSHC} \tag{24}$$

$$U_{\beta-sw} = U_\beta^* - U_{\alpha-NSHC} \tag{25}$$

The 3-phase switching references U_{X-sw}^*, U_{Y-sw}^*, U_{Z-sw}^* are evaluated from 2-phase references $U_{\alpha-sw}$ and $U_{\beta-sw}$ and the clamping inverter information as given in Equation (26).

$$\begin{bmatrix} U_{X-SW}{}^* \\ U_{Y-SW}{}^* \\ U_{Z-SW}{}^* \end{bmatrix} = \text{Sign (clamp)} \begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} U_{\alpha-SW} \\ U_{\beta-SW} \end{bmatrix} \tag{26}$$

$$\begin{cases} \text{sign(clamp)} = 1 & \text{if INV} - 1 \text{ is clamping} \\ \text{sign(clamp)} = -1 & \text{if INV} - 2 \text{ is clamping} \end{cases} \quad (27)$$

In order to modulate the *switching inverter*, the algorithm presented in the work[15] is employed, which is based on the concept of the "*imaginary switching time periods"* and was proposed for a 2-level VSI, is extended to the 3-level OWIM drive. In this algorithm, a time-period known as the *effective time period* (denoted by the symbol T_{eff}), which is a fraction of the *sampling time period* (denoted by the symbol T_s) determines the RMS value of the fundamental component of the output of the VSI.

The effective time period is the sum of the switching time periods of the two active vectors pertaining to the sector in which the tip of the switching vector **AT** (Figure 6) is situated in any given sampling time period. Another time period called the offset time, denoted as T_{offset} determines the placement of the block of effective time period within a given sampling time period.

In the SVPWM technique, the block of effective time period is placed exactly at the center of any given sampling time period. Thus, this variant of SVPWM is called as the center-spaced SVPWM (CSVPWM) scheme. In the CSVPWM scheme, the effective time period is sandwiched between the two null vectors 8 ($- - -$) and 7 ($+++$). In this case, three devices are switched, pertaining to each output phase.

Instead of using two null vectors, one may use only one, which results in the switching of only two devices in any given sampling time period (T_s). In other words, it would clamp one of the phases of the switching inverter either to the negative or to the positive terminal of the DC-input rails depending on the type of the null vector used (vectors "8" and "7," respectively, Figure 4). Thus, this variant of the SVPWM scheme is called as the phase clamped (or discontinuous) SVPWM technique.

With this choice, the effective time period block is placed at one of the edges of any given sampling time period. The obvious advantage with this choice (ie, using only one null vector) is a reduction in switching by 33.3%, which would result in a reduced switching power loss. It is implemented by an appropriate choice of the offset time period, which is described in the work.[15]

Caution should be exercised while extending these PWM schemes, which are popular with the two-level VSIs to the 3-level OWIM drive, as it is required to prevent the flow of the zero-sequence current. However, as explained earlier, electrical isolation (ie, the employment of two isolated power supplies to feed individual inverters) would automatically prevent the flow of the zero-sequence current. This paper proposes the phase-clamped and alternately switched (PCAS) SVPWM scheme, which is a combination of the ASHC-SVPWM and the phase-clamped PWM techniques. It inherits the feature of clamping one of the two VSIs from the former to provide the pivot vector (**OA**, Figure 6). The switching inverter, which produces the switching vector (**AT**, Figure 6), employs the phase clamping feature, which is explained in the previous paragraphs.

Thus, for the example shown in Figure 6, where in the sample is situated in sector-7 (Figures 5 and 6), inverter-I is clamped to the state "1," that is, ($+ - -$), while inverter-II would be switched through the states: 7′, 4′, and 5′ (Figures 4-6). Hence, the space vector combinations used are: 17′-14′-15′. Alternatively, inverter-II could also be switched to follow the sequence: 8′-5′-4′. In that case, the space vector combinations deployed are: 18′-15′-14′.

Table 3 summarizes the switching sequences for all of the sectors, which fall within the jurisdiction of the SHC "A" corresponding to the quadrangle OHGS. As mentioned earlier, the SHC-A employs the clamping vector "1" ($+ - -$). It may be noted that each SHC covers two sectors fully and four sectors partially. Table 4 provides the information regarding the roles of the inverters and the clamping vectors employed by each inverter. Using Tables 3 and 4, one may deduce the switching sequences corresponding to the rest of the five hexagonal centers.

The flowchart to implement the proposed PCAS-SVPWM technique for the switching inverter is presented in Appendix A.

4 | SPEED CONTROL OF THE DUAL-INVERTER FED OWIM DRIVE WITH PCAS-SVPWM STRATEGY

With respect to the situation in Figure 6A, let it be assumed that the voltage space-vector (U_{SV}) denoted by **OT**, as situated in sector numbered (7) is generated by the dual-inverter configuration as portrayed in Figure 3.

TABLE 3 Switching sequences for NSHC—"A" with the proposed PCAS-SVPWM

Sector no.	Switching sequence-1	Clamped phase in VSI-II	Switching sequence-2	Cl amped phase in VSI-II
6 (half-covered)	17′-12′-11′	A	18′-11′-12′	C
23 (half-covered)	17′-12′-13′	B	18′-13′-12′	C
24 (fully covered)	17′-14′-13′	B	18′-13′-14′	A
7 (fully covered)	17′-14′-15′	C	18′-15′-14′	A
8 (half-covered)	17′-16′-15′	C	18′-15′-16′	B
1 (half-covered)	17′-16′-11′	A	18′-11′-16′	B

TABLE 4 Summary of the proposed PCAS-SVPWM strategy

Quadrangle containing the reference vector OT	NSHC	Fully-covered sectors	Half-covered sectors	Role of inverter-I	Role of inverter-II	Clamping vector
OHGS	A	7,24	1,6,8,23	Clamping	Switching	1 (+ − −)
OJIH	B	9,10	1,2,8,11	Switching	Clamping	5′ (− − +)
OLKJ	C	12,13	2,3,11,14	Clamping	Switching	3 (− + −)
ONML	D	15,16	3,4,14,17	Switching	Clamping	1′ (+ − −)
OQPN	E	18,19	4,5,17,20	Clamping	Switching	5 (− − +)
OSRQ	F	21,22	5,6,20,23	Switching	Clamping	3′ (− + −)

The total DC-link voltage (U_{DC}) is denoted by OU. The amplitude modulation index, denoted by the symbol m_a is defined as:

$$m_a = \frac{OT}{OU} = \frac{|U_{SV}|}{U_{DC}} \tag{28}$$

The total DC-link voltage U_{DC} is so chosen that the rated frequency and the rated voltage are produced at the edge of linear modulation, that is, $\left(\frac{\sqrt{3}}{2}\right) = 0.866$ using the SVPWM scheme by appropriate weighing of the dual-inverter system. Owing to this scaling, the fundamental frequency of this system for the modulation index m_a can be deduced as:

$$f = \frac{m_a}{\sqrt{3}/2} * 50 \tag{29}$$

As sample-based implementation is carried out with SVM, each fundamental cycle is divided into 42 samples. Thus, the sampling time period is accounted by:

$$T_s = \frac{1}{f * 42} \tag{30}$$

The imaginary switching time periods of 3-phases are calculated by using the equations given below:

$$T_{as-SW} = \frac{T_s}{(U_{DC}/2)} U_{X-SW}{}^* \tag{31}$$

$$T_{bs-SW} = \frac{T_s}{(U_{DC}/2)} U_{Y-SW}{}^* \tag{32}$$

$$T_{cs-SW} = \frac{T_s}{(U_{DC}/2)} U_{Z-SW}^{*} \tag{33}$$

The maximum and minimum values of these switching time periods are denoted as T_{max} and $T_{min,}$ respectively.

$$T_{max} = Max\{T_{as-sw}, T_{bs-sw}, T_{cs-sw}\} \tag{34}$$

$$T_{min} = Min\{T_{as-sw}, T_{bs-sw}, T_{cs-sw}\} \tag{35}$$

As mentioned before, the PCAS-SVPWM scheme is implemented by the modification of the switching algorithm described in the work[15] in terms of the offset time period. In the interest of brevity, this algorithm is not reviewed in this paper, though it is broadly outlined in the previous section. The offset time needed to place the effective time period (T_{eff}) at the left edge of a sampling time period (T_s) is given by:

$$T_{offset,left} = -T_{min} \tag{36}$$

On the other hand, the offset time needed to place the effective time period to the right edge in any sampling time interval is given by:

$$T_{offset,right} = T_S - T_{max} \tag{37}$$

TABLE 5 Switching states of the sample-based PCAS-SVPWM strategy

Sample no.	Theta (θ in degrees)	Sequence (*ON/OFF*)	Clamped INV (*Vector*)	Switched INV (*Vectors*)	PCAS switching combination
01	4.28°	*OFF*	INV I (1)	INV II (*4′-5′-8′*)	14′-15′-18′
02	12.86°	*ON*	INV I (1)	INV II (*8′-5′-4′*)	18′-15′-14′
03	21.43°	*OFF*	INV I (1)	INV II (*4′-5′-8′*)	14′-15′-18′
04	30°	*ON*	INV II (*5′*)	INV I (8-1-6)	85′-15′-65′
05	38.57°	*OFF*	INV II (*5′*)	INV I (6-1-8)	65′-15′-85′
06	47.14°	*ON*	INV II (*5′*)	INV I (8-1-2)	85′-15′-25′
07	55.71°	*OFF*	INV II (*5′*)	INV I (2-1-8)	25′-15′-85′
08	64.28°	*ON*	INV II (*5′*)	INV I (8-3-2)	85′-35′-25′
09	72.86°	*OFF*	INV II (*5′*)	INV I (2-3-8)	25′-35′-85′
10	81.43°	*ON*	INV II (*5′*)	INV I (8-3-4)	85′-35′-45′
11	90°	*OFF*	INV I (3)	INV II (*4′-5′-8′*)	34′-35′-38′

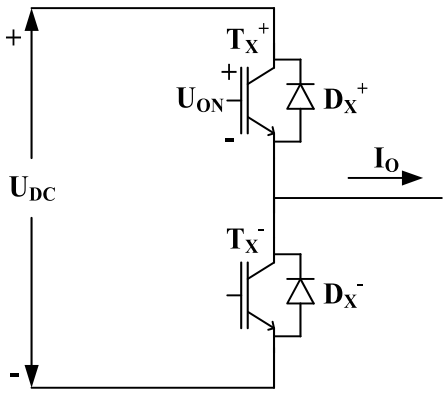

FIGURE 7 The x-phase leg of inverter-I

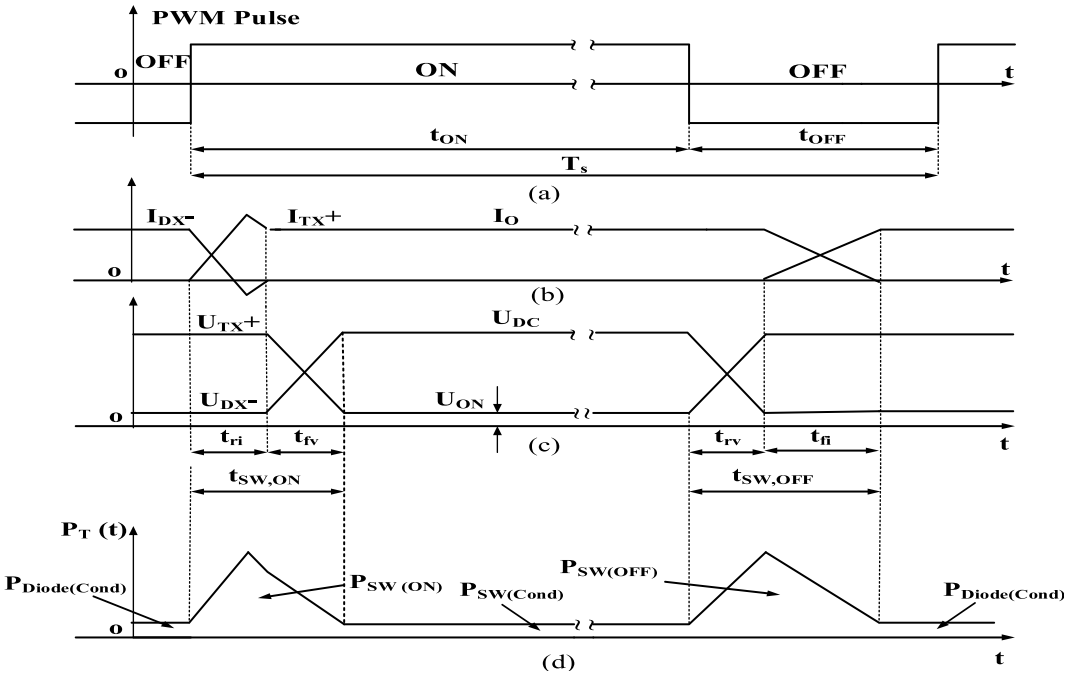

FIGURE 8 Owing to the x-phase leg of Inverter (a) PWM signal to the switch, (b) current through the devices, (c) voltage across the devices, and (d) power consumed by the devices

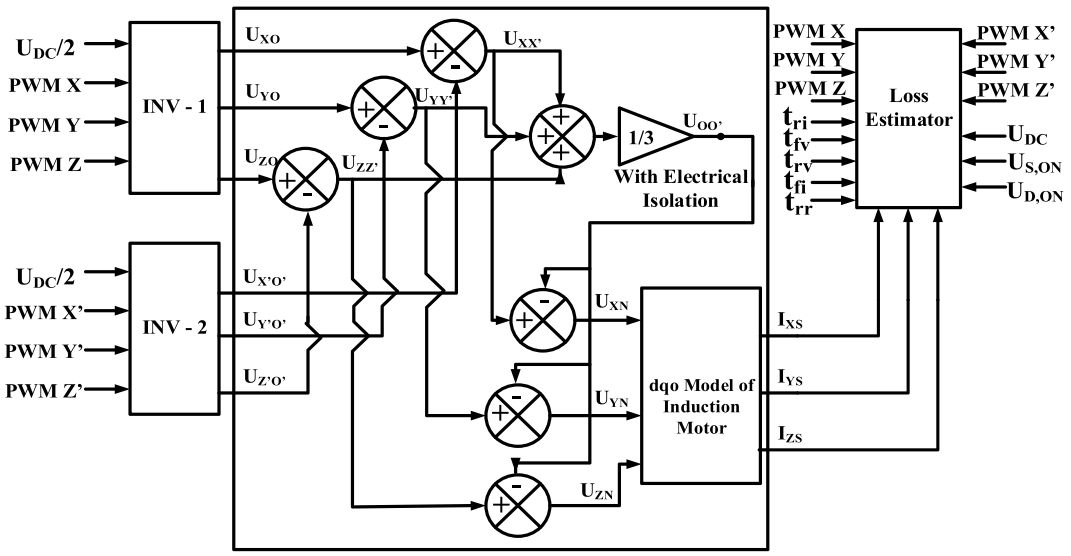

FIGURE 9 Power loss model (in dq0 reference frame) of the 3-level OWIM drive

TABLE 6 Modeling design parameters required for power loss analysis of OWIM

Parameters	Values
Voltage fall-time (t_{fv})	1 μs
Voltage rise-time (t_{rv})	2 μs
Current fall-time (t_{fi})	4 μs
Current rise-time (t_{ri})	2 μs
Diode reverse recovery time (t_{rr})	1 μs
On-state voltage drop of switch ($U_{S,ON}$)	0.76 V
On-state drop of diode ($U_{D,ON}$)	0.9468 V

The equations for the imaginary switching time periods for the over-modulation condition are given as follows:

$$T_{as-SW} = \frac{T_s}{(U_{DC}/2)} U_{X-SW}{}^{*} \frac{T_s}{T_{eff}} \tag{38}$$

$$T_{bs-SW} = \frac{T_s}{(U_{DC}/2)} U_{Y-SW}{}^{*} \frac{T_s}{T_{eff}} \tag{39}$$

$$T_{cs-SW} = \frac{T_s}{(U_{DC}/2)} U_{Z-SW}{}^{*} \frac{T_s}{T_{eff}} \tag{40}$$

$$T_{offset,left} = -T_{min} \frac{T_s}{T_{eff}} \tag{41}$$

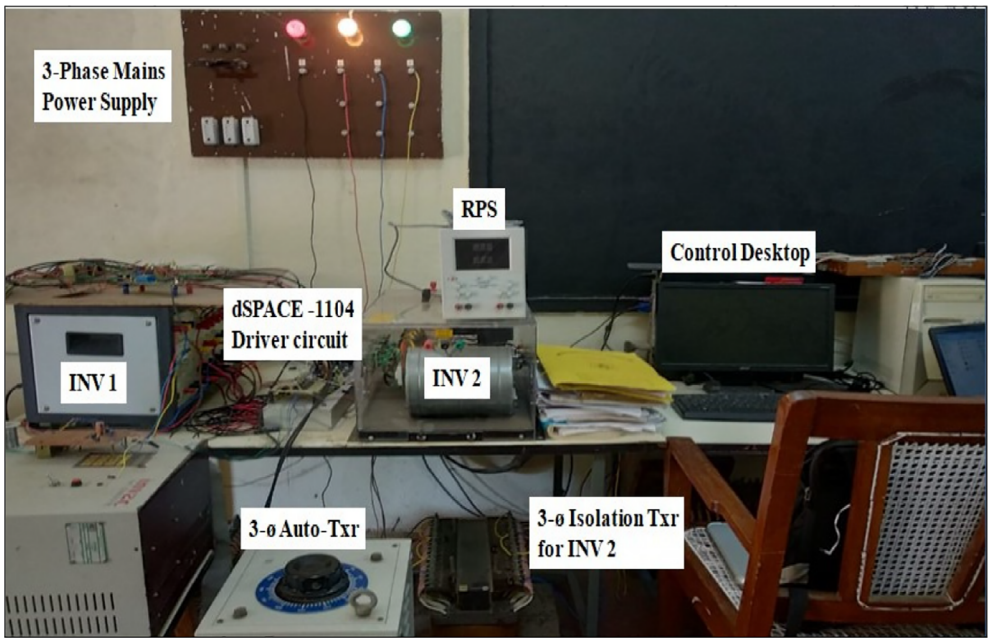

FIGURE 10 Hardware platform-I

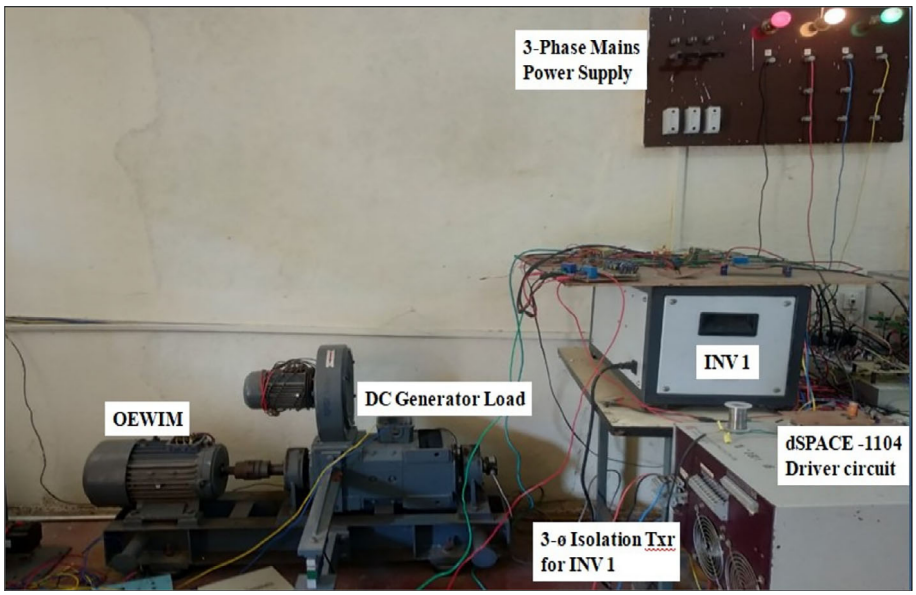

FIGURE 11 Hardware platform-II

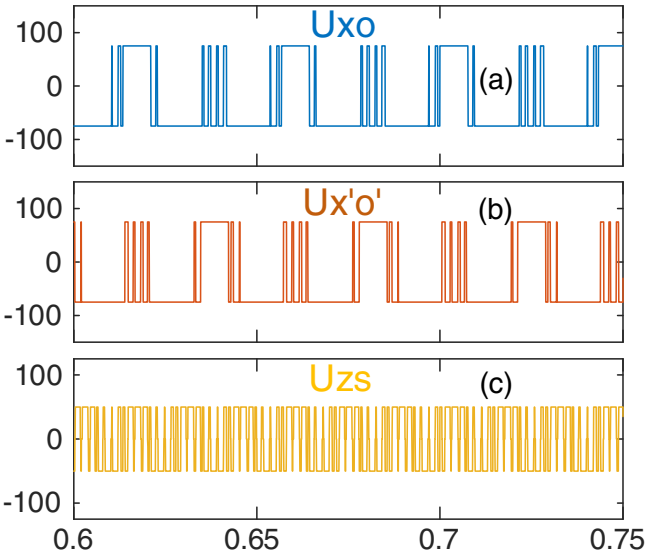

FIGURE 12 Simulated waveforms of the dual inverter pole voltages (a, b) and CMV (c) corresponding to PCAS-SVPWM at $m_a = 0.4$

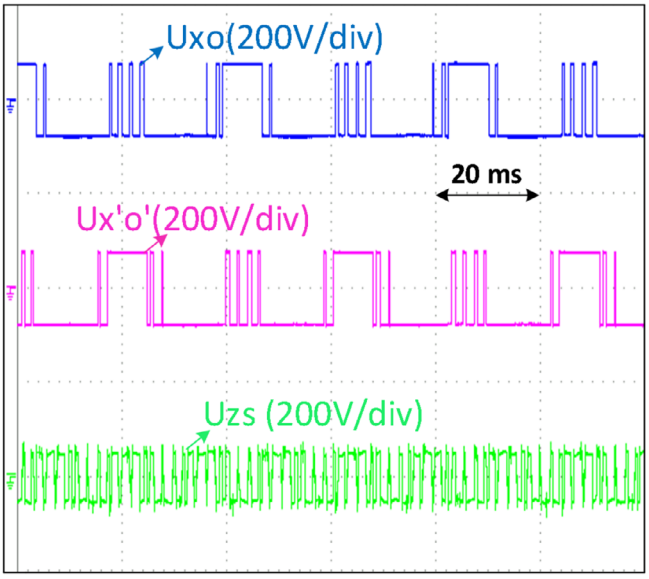

FIGURE 13 Experimental waveforms of the dual inverter pole voltages (top, middle) and CMV (bottom) corresponding to PCAS-SVPWM at $m_a = 0.4$

The on-state gating time periods for the top three devices of the switching inverter are given by:

$$T_{ga-SW} = T_{as-SW} + \left(T_{offset,left} \,(or)\, T_{offset,right}\right) \tag{42}$$

$$T_{gb-SW} = T_{bs-SW} + \left(T_{offset,left} \,(or)\, T_{offset,right}\right) \tag{43}$$

$$T_{gc-SW} = T_{cs-SW} + \left(T_{offset,left} \,(or)\, T_{offset,right}\right) \tag{44}$$

As described in the previous section, the simple choice of offset time would clamp one of the phases of the switching inverter, causing only two switching operations in the dual-inverter system. Thus, the number of switching operations is reduced by a factor of 1/3, compared to the ASHC-SVPWM scheme (in which 3 devices are switched in any given sampling time interval).

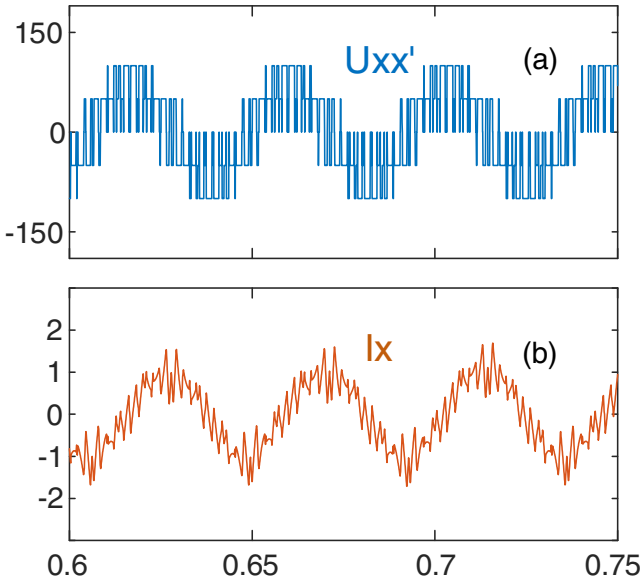

FIGURE 14 Simulated waveforms of the OWIM phase voltage (a) and phase current (b) corresponding to PCAS-SVPWM at $m_a = 0.4$

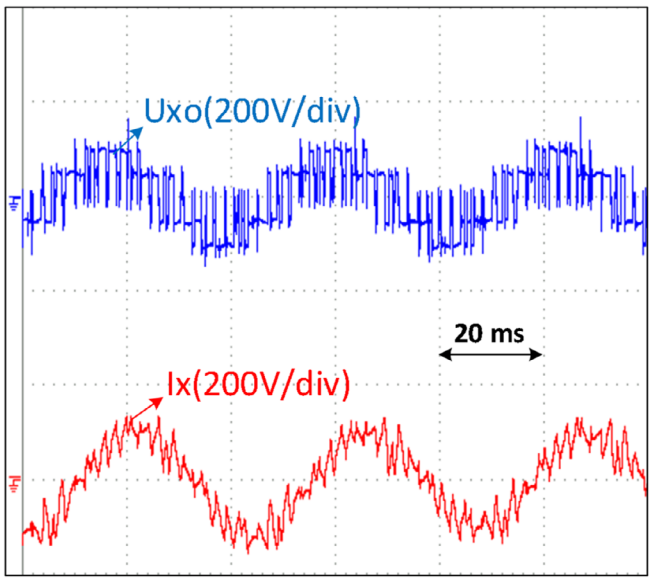

FIGURE 15 Experimental waveforms of the OWIM phase voltage (top) and phase current (bottom) corresponding to PCAS-SVPWM at $m_a = 0.4$

Table 5 furnishes the information regarding the clamping and switching inverter of the given samples, sequence (ON/OFF) of the given samples and switching states of both the inverters for the samples (1-11) out of 42 samples considered. As the samples are distributed in such a manner that the reference voltage vector obeys the quarter wave symmetry, the information of other samples (12-42) for Table 5 can be generated by the same procedure.

Admittedly, the advantage obtained by the reduction of the switching power loss is partially offset by an increased conduction power loss in the switching devices. In addition, the PCAS-SVPWM scheme would result in an inferior harmonic performance on account of the noncentric placement of the effective time period in a sampling time interval.

Hence, it is necessary to assess as to how the proposed PCAS-SVPWM scheme performs when compared to the ASHC-SVPWM scheme. The next section, with the aid of a loss estimation model, quantifies the performances of these two PWM schemes by considering performance indices such as (a) THD in voltage, (b) Weighted THD, and (c) switching power loss and the conduction power loss.

5 | EVALUATION OF POWER LOSS IN OEW-IMD SYSTEM

The salient feature of this paper is the comparative evaluation of the power losses incurred by the dual-inverter fed OEW-IMD using both the ASHC-PWM technique and the PCAS-SVPWM strategy. The loss estimation model of OWIM drive is used to carry out the loss analysis of the dual-inverter system as in the work,[16] which is based on the losses incurred in a phase leg (eg, x-phase leg of inverter-I), as shown in Figure 7.

Essentially, T_X+, T_X- represent the semiconductor switches (IGBTs) of the A-phase leg and D_X+, D_X- represent the anti-parallel diodes of these IGBTs. Figure 8 illustrates the voltage drop and the current through the top-switch (T_X^+) and the anti-parallel diode of the bottom switch (D_X^-) for $I_0 > 0$.

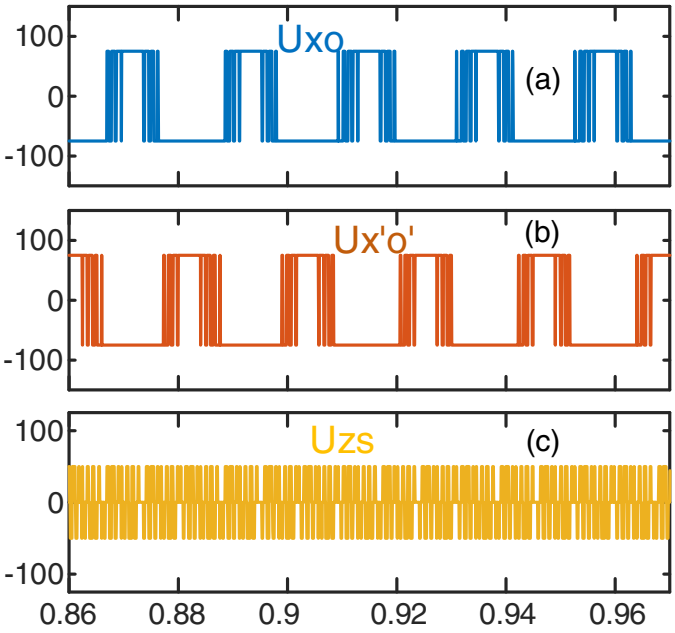

FIGURE 16 Simulated waveforms of the dual inverter pole voltages (a, b) and CMV (c) corresponding to PCAS-SVPWM at $m_a = 0.8$

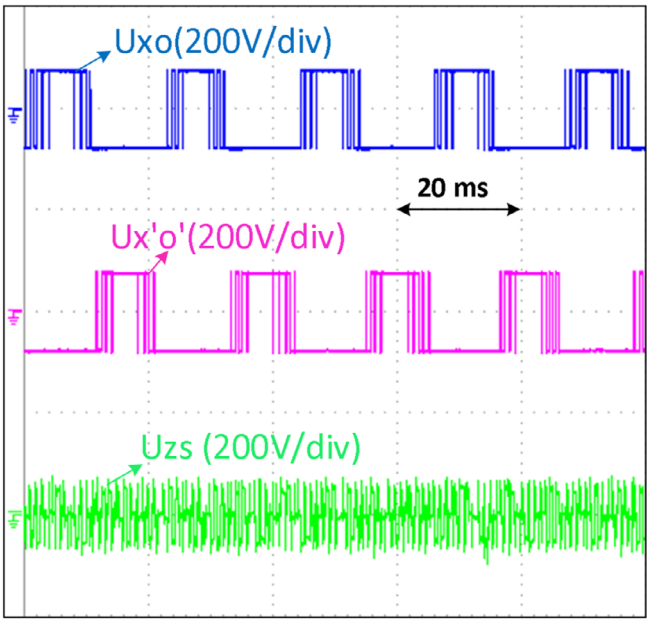

FIGURE 17 Experimental waveforms of the dual inverter pole voltages (top, middle) and CMV (bottom) corresponding to PCAS-SVPWM at $m_a = 0.8$

Based on the loss model proposed in the work,[16] the components of inverter losses are evaluated for the dual-inverter system. This loss model considers the diode reverse recovery current, conduction loss, and offerings of reverse recovery current in computing the diode losses. The switching power loss in a power semiconductor switching device is proportional to the switching frequency. The rise and fall time durations of the voltage and current through the switch (Figure 8) are principally responsible for the switching loss that takes place during both the turn-on and turn-off times. The switching power loss ($\boldsymbol{P_S}$) and conduction power loss ($\boldsymbol{P_C}$) are designated as in Reference 22:

$$P_S = [0.5 * u_S * i_S(t_{S,ON} + t_{S,OFF})] * f_s \tag{45}$$

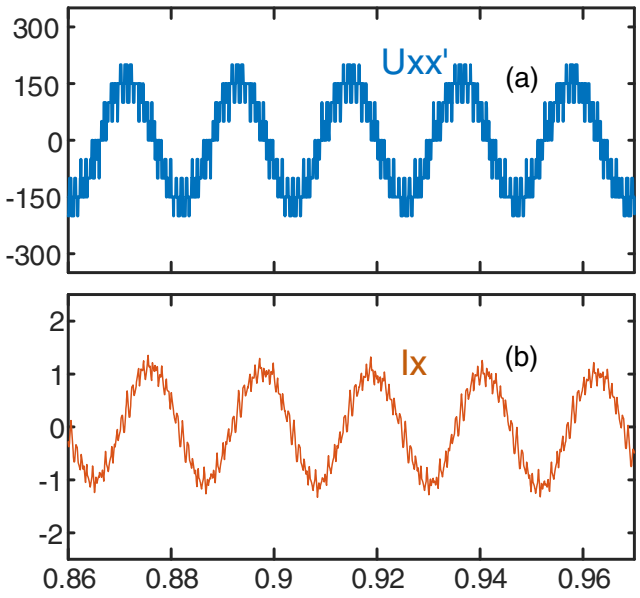

FIGURE 18 Simulated waveforms of the OWIM phase voltage (a) and phase current (b) corresponding to PCAS-SVPWM at $m_a = 0.8$

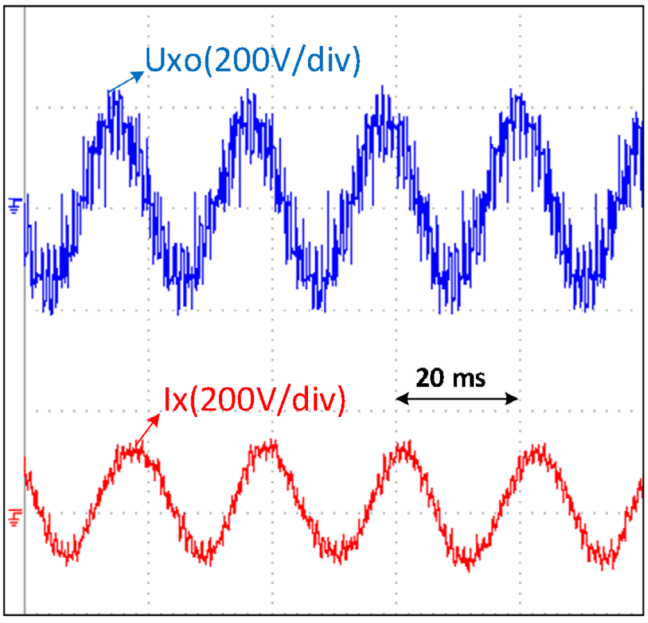

FIGURE 19 Experimental waveforms of the OWIM phase voltage (top) and phase current (bottom) corresponding to PCAS-SVPWM at $m_a = 0.8$

$$P_C = U_{S,ON} * I_{ON} * t_{ON}/T_s \tag{46}$$

It may be noted from Figure 8 that:

$$t_{S,ON} = t_{ri} + t_{fv} \text{ and } t_{S,OFF} = t_{rv} + t_{fi} \tag{47}$$

From Equations (45) and (46), it is evident that the inputs required for the estimation of losses in the dual-inverter system are: the pattern of the gating signals (ie, PWM pulses), instantaneous phase currents, the rise and fall times of the voltage across and the current through a given device ($\boldsymbol{t_{fv}}$, $\boldsymbol{t_{rv}}$, $\boldsymbol{t_{fi}}$, $\boldsymbol{t_{ri}}$), switching frequency ($\boldsymbol{f_S}$), the drop in voltage across switch in the on-state($\boldsymbol{U_{S,ON}}$), and the voltage blocked by the switch ($\boldsymbol{U_S}$).

Figure 9 depicts the MATLAB/SIMULINK implemented block diagram to estimate the losses in the dual-inverter configuration represented in Figure 3. The peak value of the reverse recovery current is assumed to be 1.2 p.u. of the

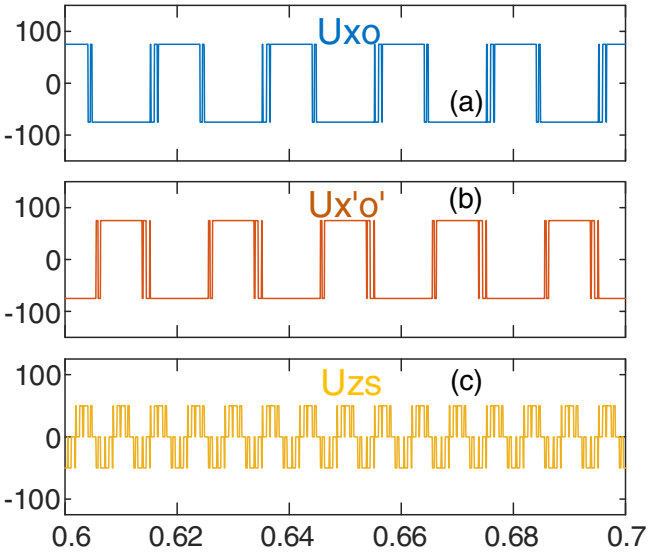

FIGURE 20 Simulated waveforms of the dual inverter pole voltages (a, b) and CMV (c) corresponding to PCAS-SVPWM at $m_a = 1$

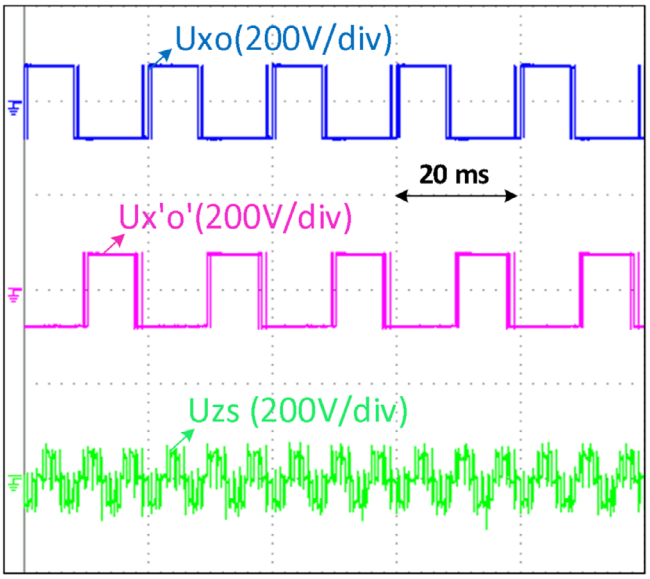

FIGURE 21 Experimental waveforms of the dual inverter pole voltages (top, middle) and CMV (bottom) corresponding to PCAS-SVPWM at $m_a = 1$

switch current, which is dependent on the load on the dual-inverter system. The parameters required for the evaluation of the power loss components for each switch/diode are presented in Table 6.

This data are kept the same for both the PWM techniques to enable a fair comparison between them. They are compared in terms of THD_V in the phase voltage of motor, WTHD (a measure of harmonic distortion in the phase current of motor under no-load condition), switching power loss and conduction loss in the dual-inverter system. In this model, the PWM signals are first translated into the pole-voltages of individual inverters. The difference of the pole voltages of individual inverters is then computed [Equations (16)-(18)]. The zero-sequence content of the difference in the pole voltages is then determined [Equation (19)]. The motor phase voltage is then computed by subtracting the zero-sequence current from the difference of pole voltages [Equations (16)-(21)]. As the zero-sequence current is automatically blocked, the *dq0* model of the conventional 3-Phase, 3-wire IM can be employed to compute the motor phase currents. The instantaneous motor phase currents are then resolved into the current components flowing in the individual switching devices using the PWM signals of the individual devices. These instantaneous device currents and switching time periods (the turn-on and

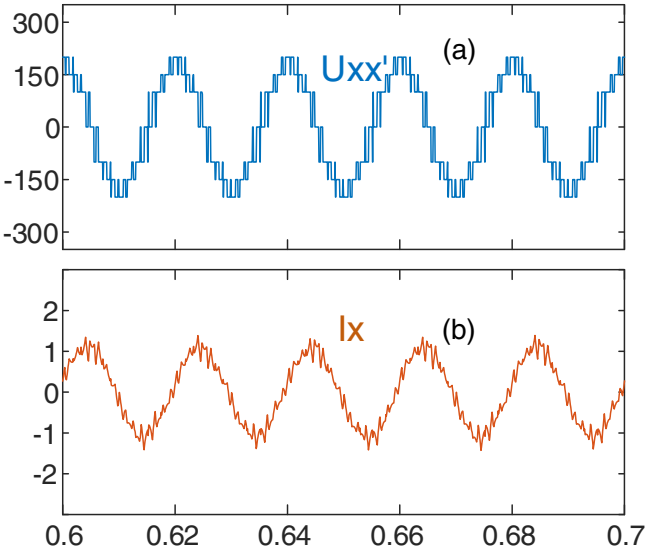

FIGURE 22 Simulated waveforms of the OWIM phase voltage (a) and phase current (b) corresponding to PCAS-SVPWM at $m_a = 1$

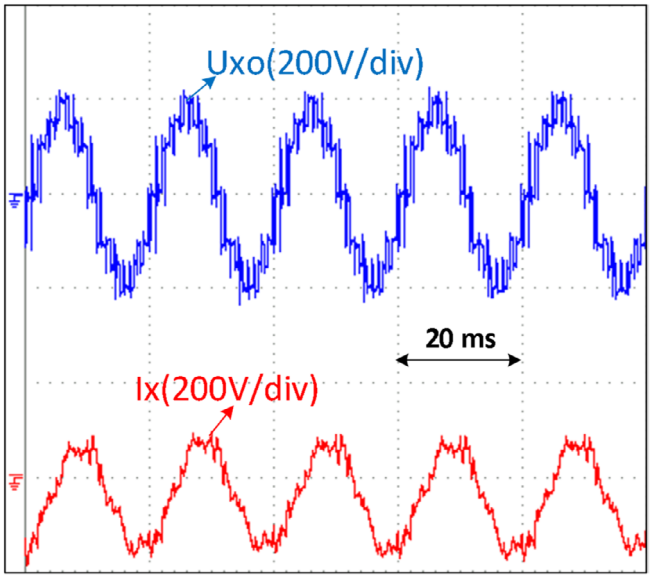

FIGURE 23 Experimental waveforms of the OWIM phase voltage (top) and phase current (bottom) corresponding to PCAS-SVPWM at $m_a = 1$

the turn-off times of the switching devices) are then passed to the loss model, which computes the switching and conduction power loss in each switch according to Equations (45) and (46). The diode losses are also estimated using the assumed values of the peak diode recovery current, reverse recovery time, and the on-state drop across the conducting diodes.

The losses estimated with the foregoing procedure are only indicative but not exact, as the model is operated with assumed data. Nevertheless, this loss model is useful to evaluate the trends, as the model parameters are common across all of the PWM schemes. However, this model assumes that all devices are perfectly matched and does not account for the production tolerances, which invariably creep into the manufacturing processes of power semiconductor switching devices.

6 | DETERMINATION OF POWER LOSSES WITH SIMULATION AND EXPERIMENTAL RESULTS

The 3-level OWIM drive, as depicted in Figure 3, is simulated with both of the PWM schemes (ASHC-SVPWM and the proposed PCAS-SVPWM schemes) using MATLAB. The open-loop *V/f* control is used to assess the performance of the drive with both of these PWM schemes (sample-based) using the control platform of *dSPACE-1104*. Both simulation and experimentation are carried on the OWIM drive having the drive parameters as shown in Table 1.

The experimental setup is presented in Figures 10 and 11. The simulation and experimental waveforms pertaining to the PCAS-SVPWM scheme are presented for three values of modulation index, that is, when m_a =0.4, 0.8, and 1. With SVPWM, until $m_a = 0.866$, the fundamental components of the output voltage and frequency vary linearly with

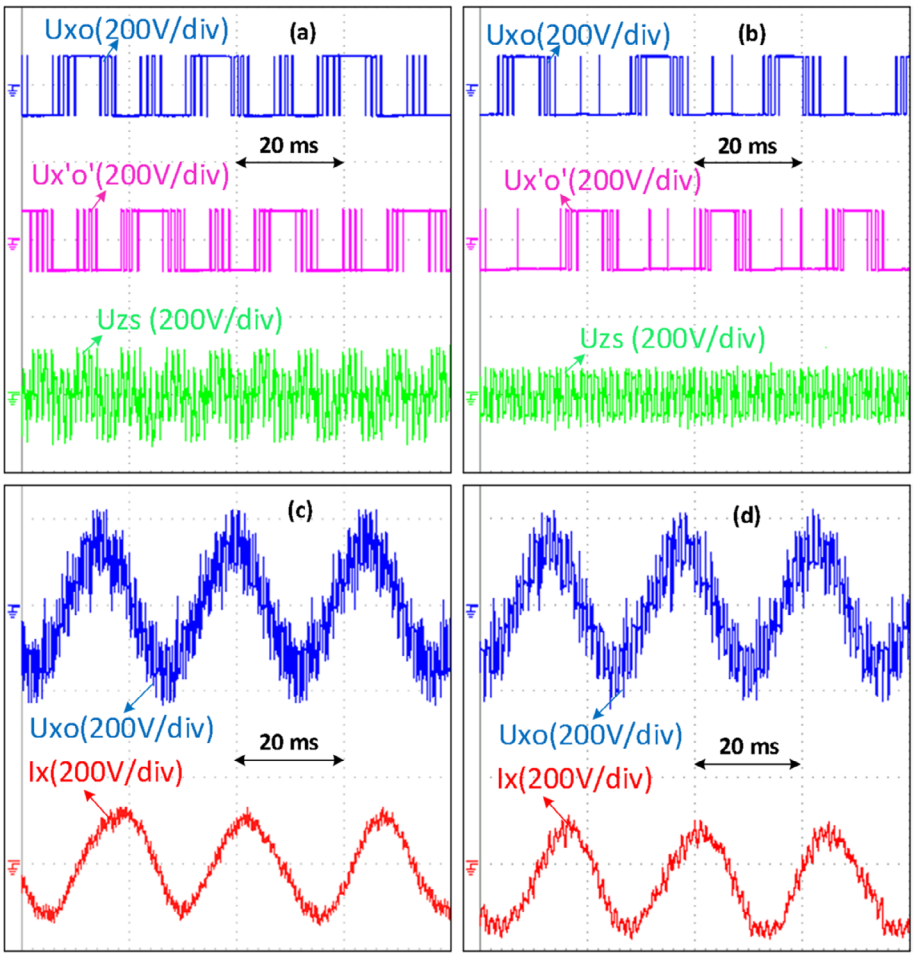

FIGURE 24 Experimental waveforms of OWIM at m = 0.7 with [(A) and (C)] ASHC-SVPWM PWM [(B) and (D)] PCAS-SVPWM techniques

m_a. Thereafter, the relation between them becomes nonlinear and the dual-inverter system is operated in the region of over-modulation.

The simulation and experimental waveforms of the pole voltages of VSI-I and VSI-II and the associated zero-sequence voltage of the dual-inverter driven OWIM drive system (appearing across the points O and O′, Figure 3) using the PCAS-SVPWM scheme for m = 0.4 are shown in Figures 12 and 13, respectively. From Figures 12 and 13, it is evident that when one VSI is clamped the other is switched and vice-versa.

The simulation and experimental waveforms of the phase voltage (Uxx′) and the phase current (Ix) of the dual-inverter driven OWIM drive system using the PCAS-SVPWM scheme for m = 0.4 are shown in Figures 14 and 15,

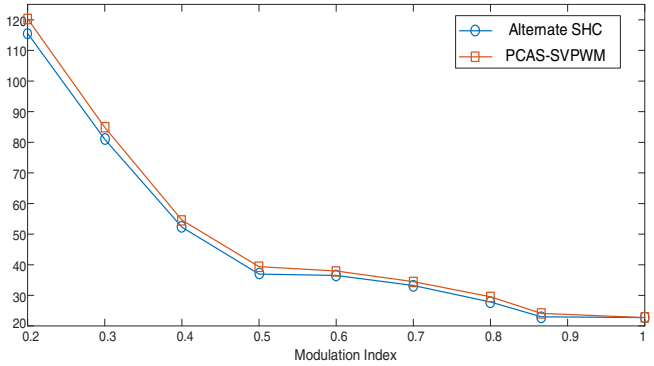

FIGURE 25 THD_V in-phase voltage (in %) v/s modulation index of the two PWM schemes

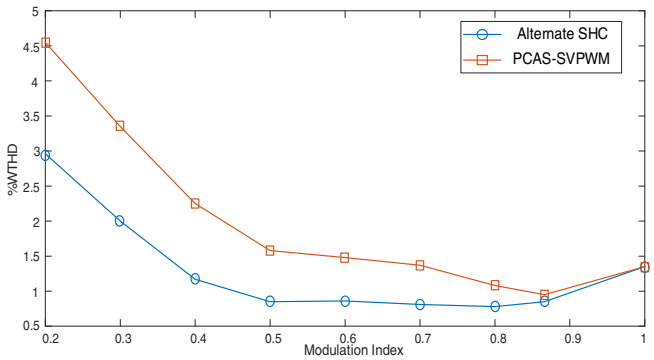

FIGURE 26 WTHD in motor current (in %) v/s modulation index of the two PWM schemes

TABLE 7 Parameters of low power (4 kW) and high power (160 kW) motors

Specifications	4 kW motor	160 kW motor
P_{rated}	5.4 HP	215 HP
Rated speed	1430 rpm	1487 rpm
R_S	4.215 Ω	0.04137 Ω
$R_{r'}$	4.185 Ω	0.023184 Ω
L_{ls}	17.517 mH	0.756 mH
$L_{lr'}$	17.517 mH	0.756 mH
L_m	516.6 mH	23.07 mH
J	0.0131 kg-s^2	2.9 kg-s^2
B	0.002985 N-m-s	0.05658 N-m-s
T_m (rated)	25.5 N-m	1018.6 N-m

respectively. The actual motor phase voltage is obtained by subtracting the zero-sequence voltage from the difference of pole voltages [Equations (16)-(21)].

Figures 16 and 17 represent the simulation waveforms of the pole voltages of VSI-I and VSI-II, the zero-sequence voltage, x-phase voltage, and the x-phase current for the dual-inverter driven OWIM drive system using the PCAS-SVPWM scheme for $m_a = 0.8$. Figures 18 and 19 show the experimental validation of these simulation results.

The simulation results for motor pole voltages, CMV, phase voltage, and phase current waveforms in the region of over modulation ($m_a = 1$) using the proposed PCAS-SVPWM technique are given in Figures 20 and 21. The corresponding experimental results are shown in Figures 22 and 23, respectively.

Figure 24 compares the experimental results of the OWIM drive obtained with the ASHC-SVPWM and the proposed PCAS-SVPWM techniques at a modulation index of m = 0.7. Figure 24A,B, respectively, present the corresponding pole-voltages and the CMV. The phase voltages and currents obtained with these PWM schemes are, respectively, presented in Figure 24C,D.

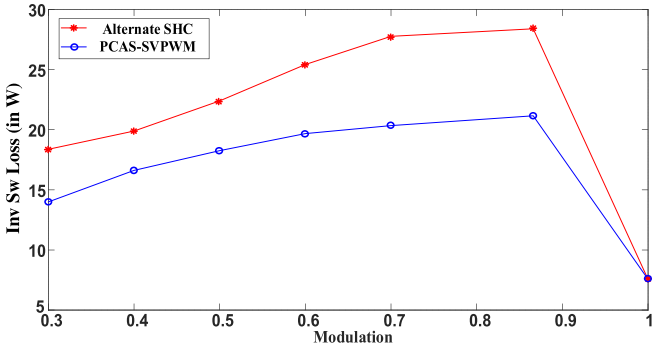

FIGURE 27 Inverter switching losses versus modulation for both PWM schemes with 4 kW motor loading

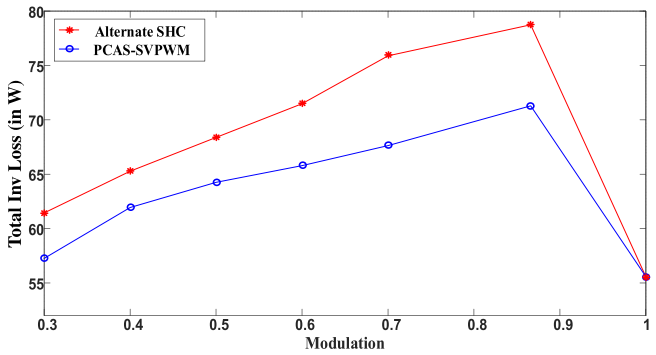

FIGURE 28 Total inverter losses versus modulation for both PWM schemes with 4 kW motor loading

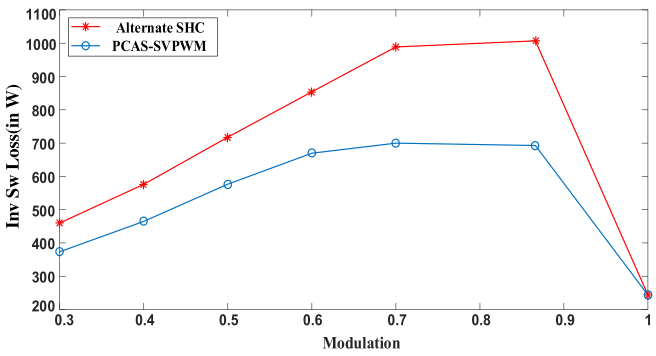

FIGURE 29 Inverter switching losses versus modulation for both PWM schemes with 160 kW motor loading

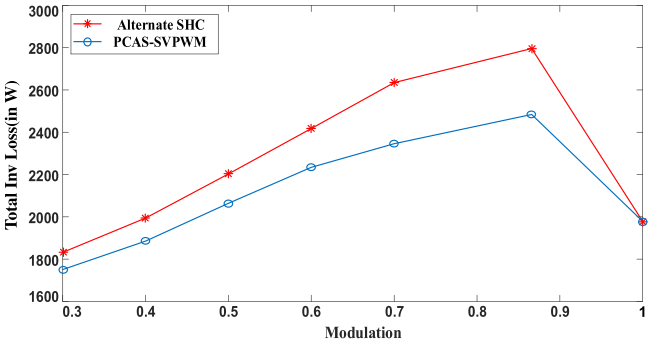

FIGURE 30 Total Inverter Losses versus modulation for both PWM schemes with 160 kW motor loading

TABLE 8 Comparison of power losses between the ASHC and the PCAS-SVPWM schemes

		4 kW motor				160 kW motor			
		ASHC-SVPWM		PCAS-SVPWM		ASHC-SVPWM		PCAS-SVPWM	
MI	Losses	INV1	INV2	INV1	INV2	INV1	INV2	INV1	INV2
0.3	Sw loss	8.91	9.46	7.17	7.84	226.9	233	177	196.6
	Cond loss	9.68	9.73	9.62	9.64	305.1	306.2	308.1	305.2
	D. cond loss	11.43	12.05	11.51	11.48	379.7	381.1	383.6	380
	Total loss	61.26		57.26		1832.1		1750.5	
0.4	Sw loss	9.67	10.21	7.72	8.54	281.6	294.4	218.5	246.3
	Cond loss	10.13	10.15	10.14	10.13	315.9	316.1	317.8	315.1
	D. cond loss	12.55	12.56	12.54	12.5	393.1	393.4	395.5	392.2
	Total loss	65.27		61.59		1994.5		1885.4	
0.5	Sw loss	10.88	11.51	8.77	9.48	349.6	367.9	367.4	309.2
	Cond loss	10.24	10.26	10.27	10.22	331.4	330.6	332.6	330.3
	D. cond loss	12.74	12.76	12.78	12.72	412.3	411.3	413.9	411
	Total loss	68.38		64.25		2203		2064	
0.6	Sw loss	12.32	13.09	9.27	10.4	415.3	438.7	316.4	352.9
	Cond loss	10.28	10.25	10.29	10.26	348.7	347.8	349.4	347.7
	D. cond loss	12.78	12.76	12.81	12.76	433.8	432.7	434.8	432.7
	Total loss	71.48		65.79		2417		2234	
0.7	Sw loss	13.61	14.14	9.89	10.45	483	505.9	341.6	358.2
	Cond loss	10.53	10.52	10.55	10.52	367.1	366.5	367.5	366.3
	D. cond loss	13.1	13.08	13.13	13.09	456.6	455.8	457.3	455.8
	Total loss	75.89		67.63		2635		2346	
0.866	Sw loss	14.35	14.03	10.53	10.47	515.9	491	351.8	341
	Cond loss	11.15	11.16	11.16	11.17	398.5	398.6	399	399.2
	D. cond loss	13.87	13.89	13.9	13.91	495.7	496.3	496.6	497
	Total loss	78.74		71.19		2796		2484	
1	Sw loss	3.37	4.22	3.37	4.22	111.7	132	111.7	132
	Cond loss	10.68	10.7	10.68	10.7	385.9	386.8	385.9	386.8
	D. cond loss	13.3	13.33	13.3	13.33	480.6	481.7	480.6	481.7
	Total loss	55.6		55.6		1978.2		1978.2	

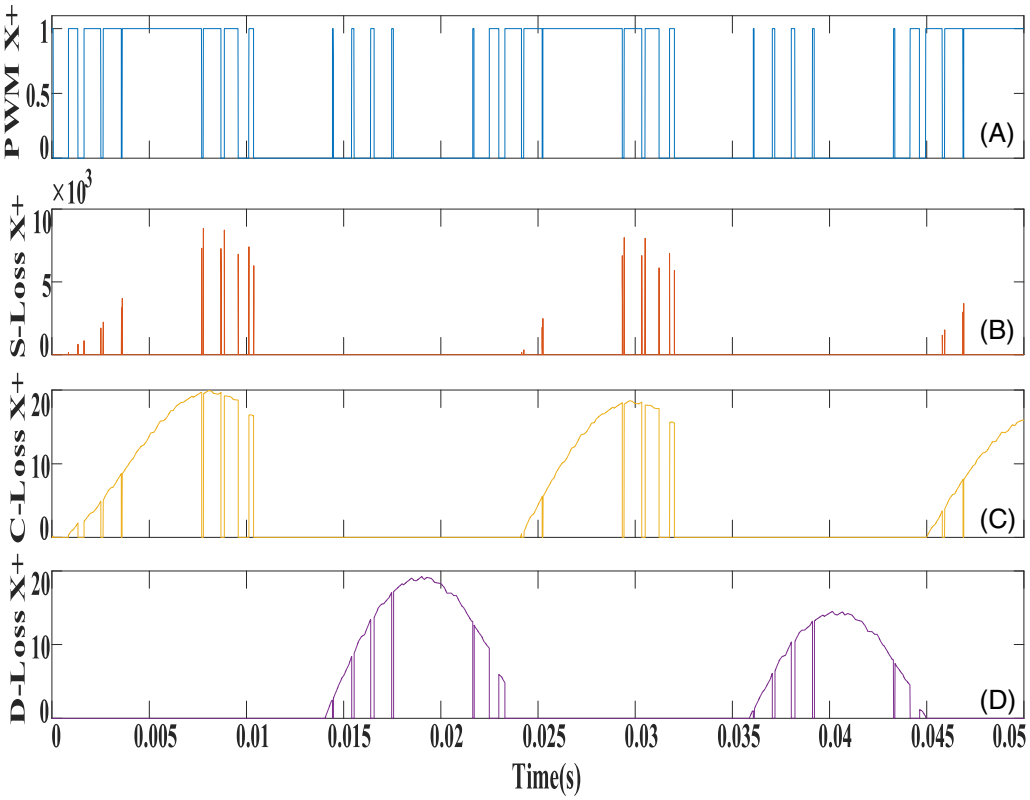

FIGURE 31 Power loss distribution for the x-leg positive DC rail devices of VSI-I with ASHC-SVPWM and loaded with 4 kW Motor at $m_a = 0.8$ (A) PWM signal to the switch, (B) switching losses, (C) switch conduction losses, and (D) diode conduction losses

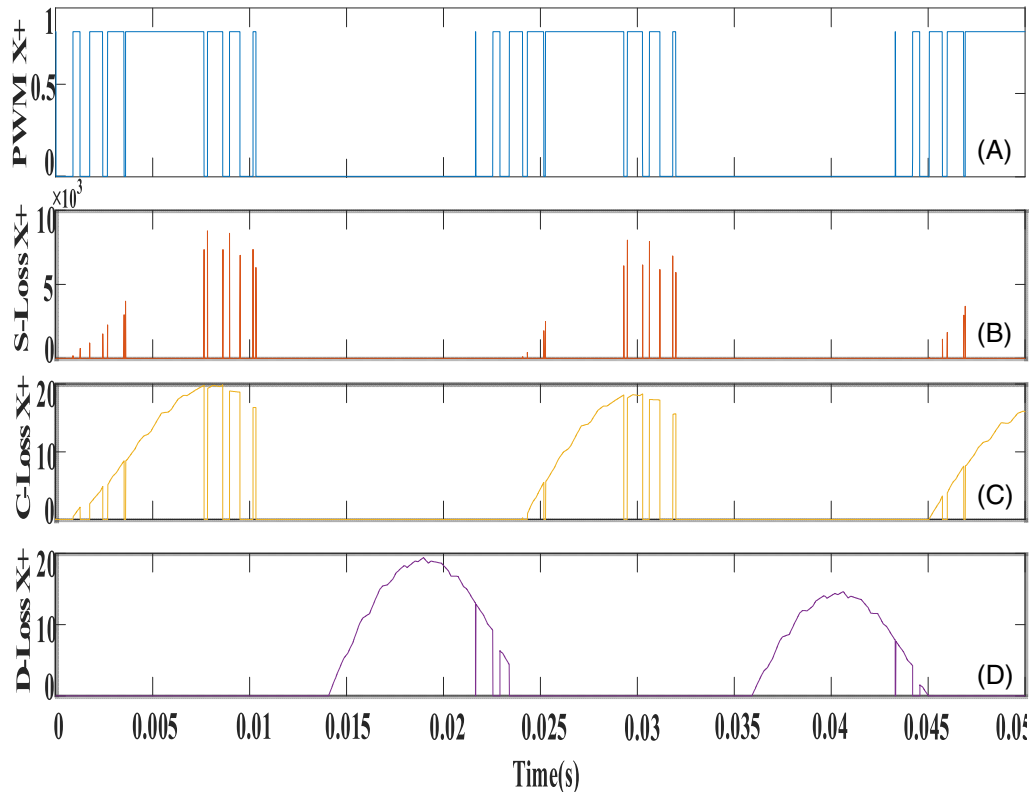

FIGURE 32 Power loss distribution for the x-leg positive DC rail devices of VSI-I with PCAS-SVPWM and loaded with 4 kW Motor at $m_a = 0.8$ (A) PWM signal to the switch, (B) switching losses, (C) switch conduction losses, and (D) diode conduction losses

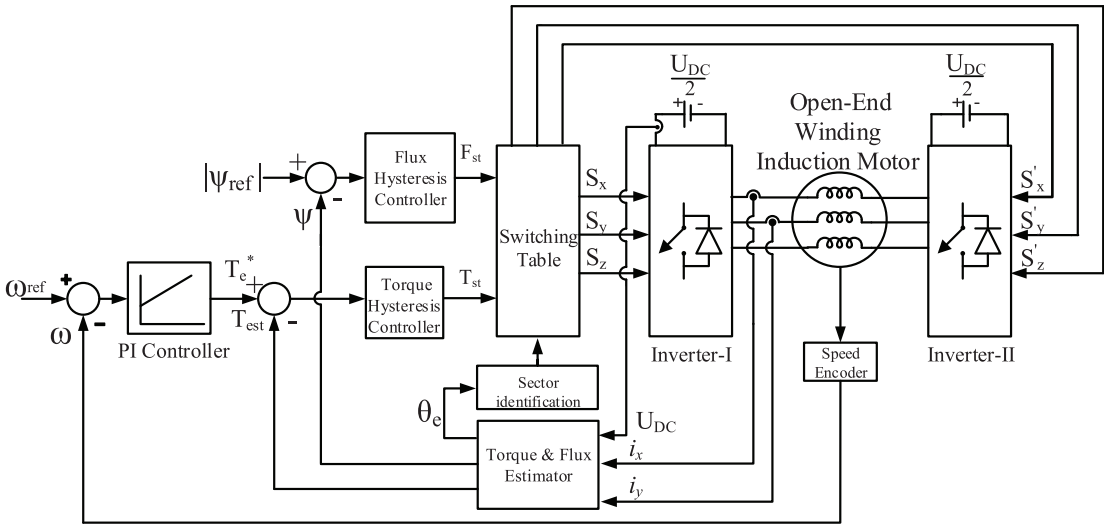

FIGURE 33 Block diagram of 3-level OEWIMD with classical DTC technique

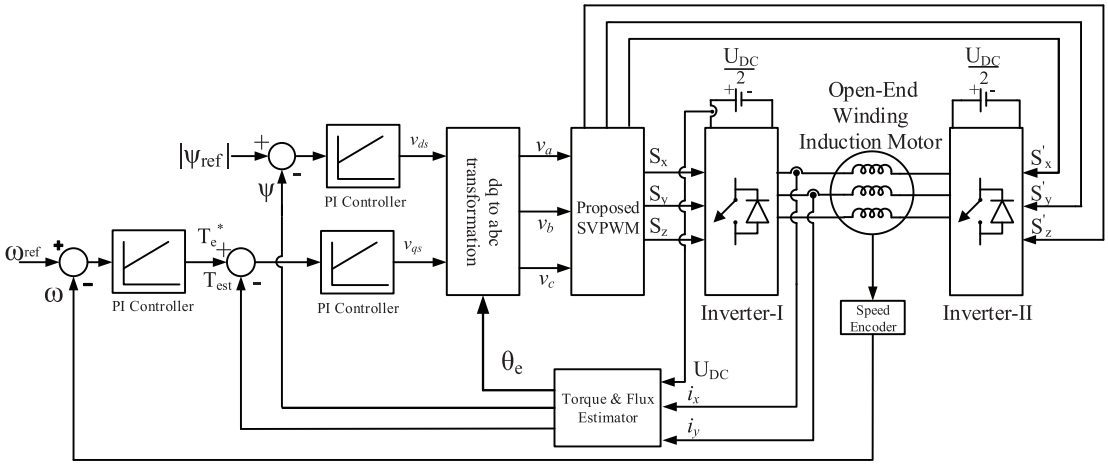

FIGURE 34 Block diagram of 3-level OEWIMD with the PCAS-SVPWM based DTC scheme

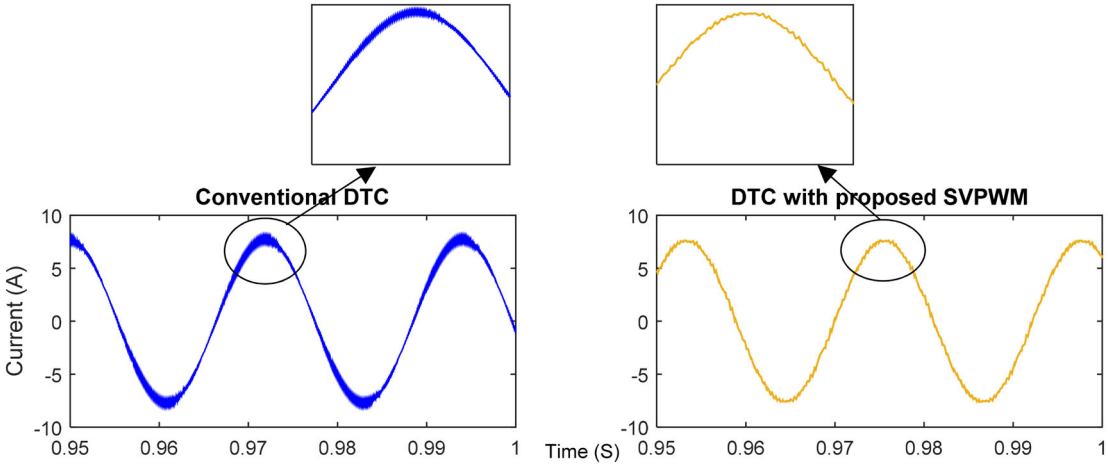

FIGURE 35 Phase current of OWIMD during the loaded condition with conventional DTC (left) and DTC with proposed SVPWM (right)

As stated earlier, the proposed PCAS-SVPWM technique switches only two phases compared to the ASHC-SVPWM technique in any given sampling time period. Thus, the proposed PWM technique results in a reduced switching (by 33% compared to the latter). This decrease in the switching frequency is clearly visible from the waveforms presented in Figure 24A,B. In other words, AHSC and the PCAS SVPWM schemes, respectively, cause 3 and 2 numbers of switching operations in each sampling time period. It may also be noted that the CMV associated with the proposed PCAS SVPWM scheme is considerably lesser than the AHSC SVPWM scheme.

One may expect that the effect of reduced switching manifests as an increased ripple in the motor phase current waveform. The experimental waveforms, presented in Figure 24C,D, comply with this expectation.

The harmonic performances of the ASHC and the PCAS-SVPWM strategies are evaluated for various modulation indices (m_a) using the FFT analysis. The total harmonic distortion in the motor phase voltage (THD_V) is shown in Figures 25 and 26 presents the weighted THD (WTHD), which is a measure of the harmonic content in the no-load current of the motor.

In simulation studies, to estimate the effectiveness of the proposed PCAS-SVPWM scheme, the power loss incurred by the dual-inverter system was analyzed by loading it with two differently rated motors. One of them is a low rating motor of 4 kW (which is previously shown and used for experimental & simulation results in the beginning of this section) and the other is a high rating motor of 160 kW rating, both rated at 400 V, 50 Hz with 4 poles. The parameters of these two motors are listed in Table 7, which are extracted from the motor parameters provided by Simulink.

The total power loss in the dual-inverter system is the sum of the power losses due to switching, conduction, and the power loss in the anti-parallel diodes of each inverter. All of these losses are estimated for the dual-inverter system using the MATLAB-SIMULINK tools, using the power loss model illustrated in Figure 7. While the THD_V and WTHD are dependent only on the switching pattern, the power losses in the dual-inverter system depends on the details of switching (PWM), the DC-link voltage, current switched through the devices (which depends on the load on the motor), the device turn-on and turn-off time, the diode reverse recovery time and the on-state voltage drops across the devices, etc. as explained in the earlier section.

While evaluating the PWM schemes, the motors (ie, both 4 and 160 kW) are loaded by 80%. Figure 27 shows the switching power loss incurred in the low power (4 kW) motor at different modulation indices from 0.3 to 1. As one might expect, the switching power loss with the PCAS-SVPWM is considerably lower than the power loss with the ASHC and decoupled-SVPWM schemes. Similarly, Figure 28 shows the total power loss incurred in the device, which is the sum of the switching and the conduction power losses. The total power loss incurred in the device is lower with the PCAS-SVPWM scheme, subject to the assumption that the voltage drop across a conducting device is constant, irrespective of the current flowing through the device.

Similar power loss estimations are presented for a higher rating machine (160 kW) in Figures 29 and 30, respectively. From these plots, it is apparent that the trends observed in the lower rating machines are carried to the high-power motors as well.

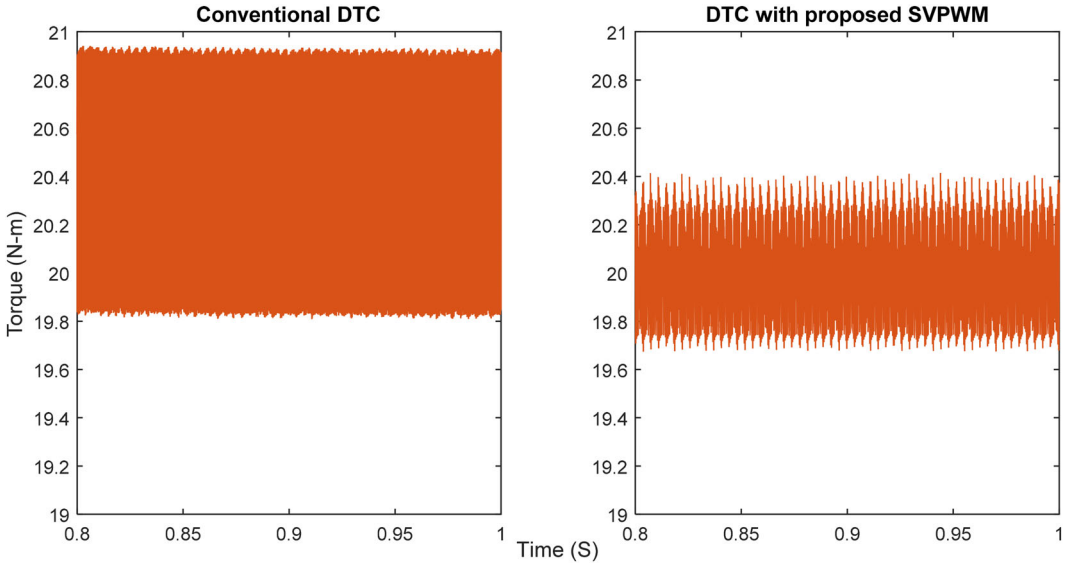

FIGURE 36 Steady-state torque wave form of OWIMD at a load torque of 20 N-m with conventional DTC (left) and DTC with proposed SVPWM (right)

Table 8 presents the numerical data corresponding to the plots presented in Figures 27-30. Figures 31 and 32, respectively, show the instantaneous power loss incurred in a typical power device connected to the positive DC rail (such as T_X^+) and an anti-parallel diode connected to the positive DC rail (such as T_D^+) belonging to the same x-phase leg for the ASHC and PCAS-SVPWM schemes, respectively. Figures 31A and 32A represents the PWM signal fed to the top power device for both the respective schemes. The plot of the instantaneous switching power loss would resemble that of the total power loss as the instantaneous value of the conduction loss is very small compared to the instantaneous value of the switching power loss.

It is clear from this data that for a 4 kW motor, the reduction in the switching varies from about 18% to 27% as the modulation index m_a varies from 0.3 to 0.866. However, all of this benefit does not percolate to the overall dual-inverter loss. The benefit reaped by the employment of the PCAS-SVPWM is reduced to the range of 6.5% to 11%, compared to the ASHC-SVPWM. Similarly, for the 160 kW motor, the switching loss is decreased by 19% to 31%. For this motor, the reduction in the overall power loss is 4.5% to 11%. This improvement may translate into a significant advantage for high power drives, where electrical isolation is generally recommended.

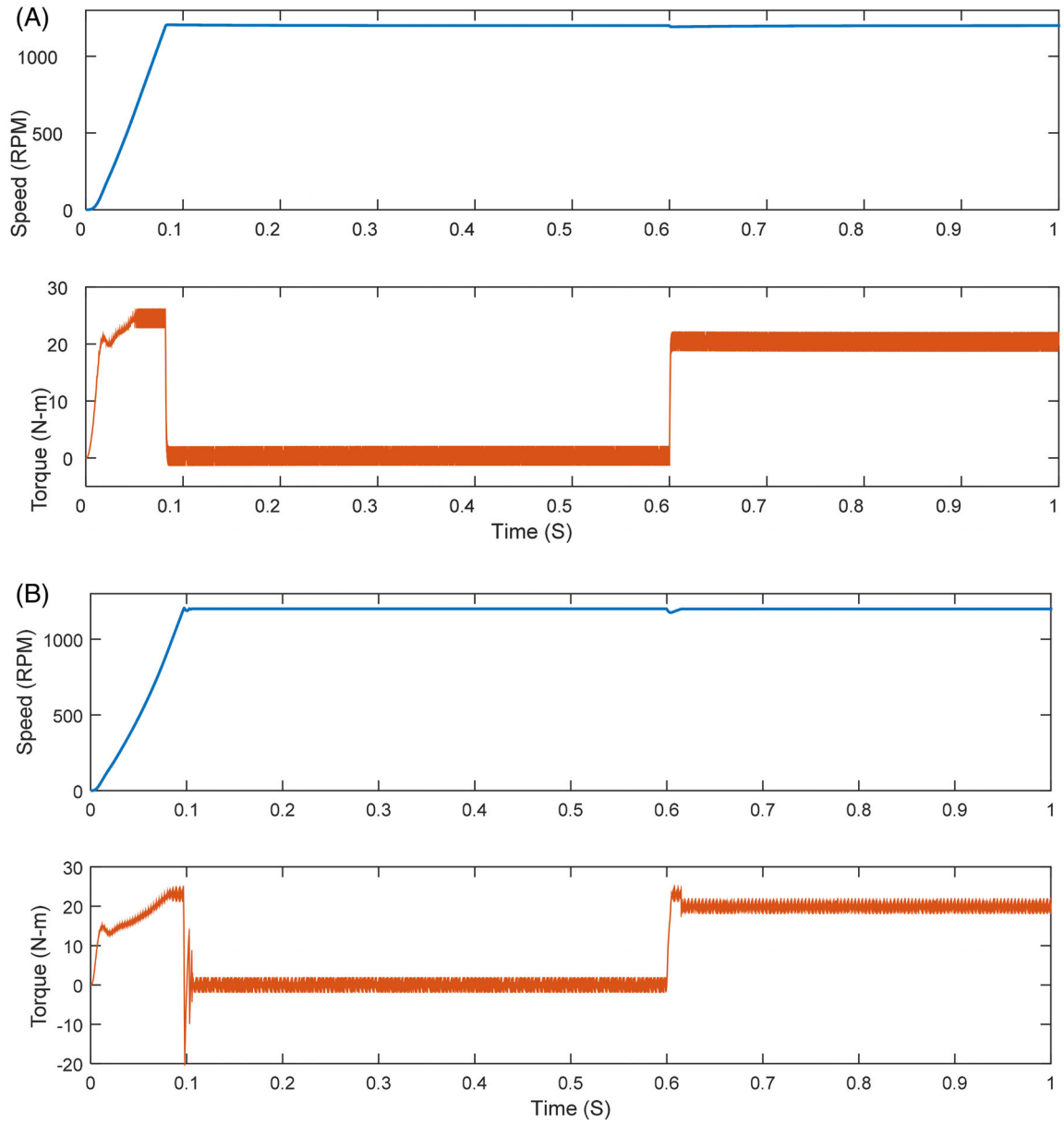

FIGURE 37 OEWIMD dynamics during staring and step change in the load (at 0.6 S) (A) conventional DTC and (B) DTC with the proposed SVPWM

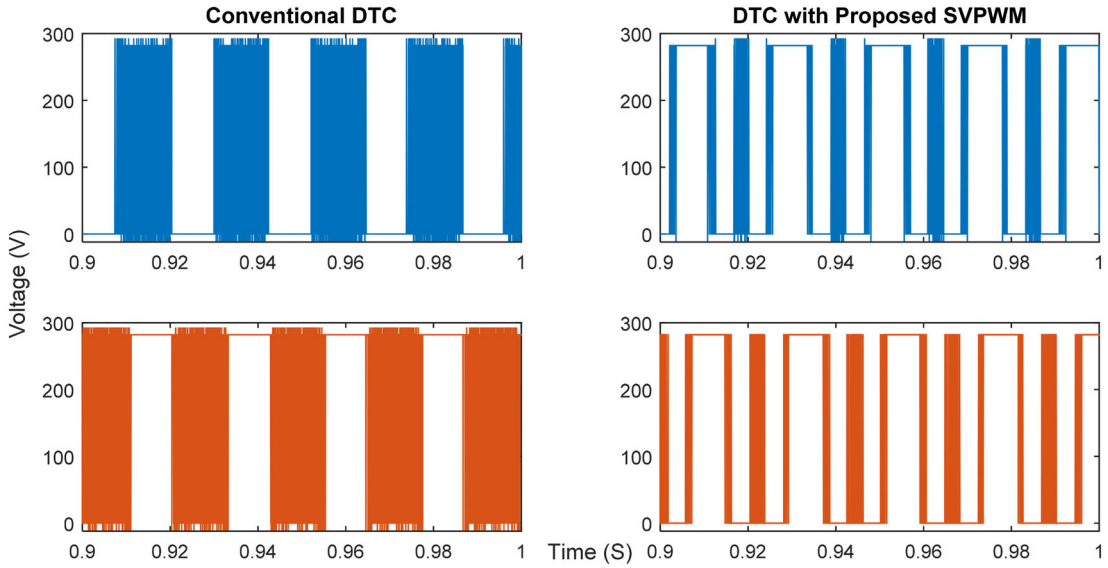

FIGURE 38 Pole voltages of inverter-I (top) and inverter-II (bottom)

Further, the applicability of the proposed PCAS-SVPWM scheme for DTC drives is assessed with simulation studies. The performance of the classical DTC drive (Figure 33) is compared with the one employing the PCAS-SVPWM scheme (Figure 34).

It may be noted that PCAS-DTC obtains the references from the PI controllers, which individually regulate the flux and the torque. The outputs of the flux and speed controllers, respectively, determine the direct and the quadrature components of the voltage references, which are then converted into the *abc*—references using the Park's transformation. The sampling frequency for the PCAS-DTC is chosen as 5 kHz. To facilitate a proper comparison, both of these drive variants are run for the same reference speed of 1200 RPM, employing an identical simulation step size of 1 μS. As is well known, the classical DTC results in a variable switching frequency and random switching based on the outputs of the flux and torque hysteresis controllers. Figure 35 shows the steady-state current drawn by the motor, when the load torque is 20 N-m. It may be noted that the proposed PCAS PWM scheme causes a reduced ripple in the stator current. This results in a reduced ripple in the steady-state torque as shown in Figure 36.

The dynamic responses with the two variants of the DTC are presented in Figure 37, when the drive starts up from rest to 1200 RPM and the subsequent handling of the increased load to 20 N-m.

The simulated pole voltages for the classical and the PCAS-DTC are, respectively, presented in Figure 38. As one might expect, the classical DTC causes more switching compared to the PCAS-DTC (owing to the variable switching frequency and random switching). Thus, it may be deduced that the PCAS-DTC could result in a considerably lesser switching power loss in the dual-inverter system compared to the classical DTC.

Thus, these simulation results reveal that the proposed PCAS-SVPWM scheme is amenable to implement high-performance drives.

7 | CONCLUSION

This paper suggests an improvisation to the existing ASHC-SVPWM strategy, which was proposed for the three-level dual-inverter fed OWIM drive. This PWM scheme is named as the PCAS SVPWM strategy. Simulation studies suggest that the proposed SVPWM scheme is particularly suitable for high power IM drives, for which electrical isolation is often recommended. The common feature of the proposed PCAS and ASHC-SVPWM schemes is that both of them operate with one of the inverters clamped, while the other is switched. Further, the PCAS-SVPWM clamps one of the phases of the switching inverter, resulting in a reduced switching by 33.3%, which reduces the switching power loss. The working principle of the drive is experimentally demonstrated with the open-loop *v/f* control.

A loss model is employed to evaluate the switching and the conduction power loss, which occur in this drive. Simulation studies, performed on two motors of different power ratings (4 and 160 kW) suggest that the advantage of

reduction in the switching power loss outweighs the disadvantage of increased conduction loss, and the benefit in terms of the reduction of overall losses is in the range of 4.5% to 11%, which could be significant in high power drives.

PEER REVIEW

The peer review history for this article is available at https://publons.com/publon/10.1002/2050-7038.13104.

DATA AVAILABILITY STATEMENT

Author elects to not share data.

ORCID

Patnana Hema Kumar https://orcid.org/0000-0002-3411-1847
Suresh Lakhimsetty https://orcid.org/0000-0001-5811-4519

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How to cite this article: Kumar PH, Mishra D, Lakhimsetty S, Somasekhar VT. A space vector PWM scheme for an open-end winding induction motor drive with a reduced power loss. *Int Trans Electr Energ Syst*. 2021;31(11):e13104. doi:10.1002/2050-7038.13104

APPENDIX A.

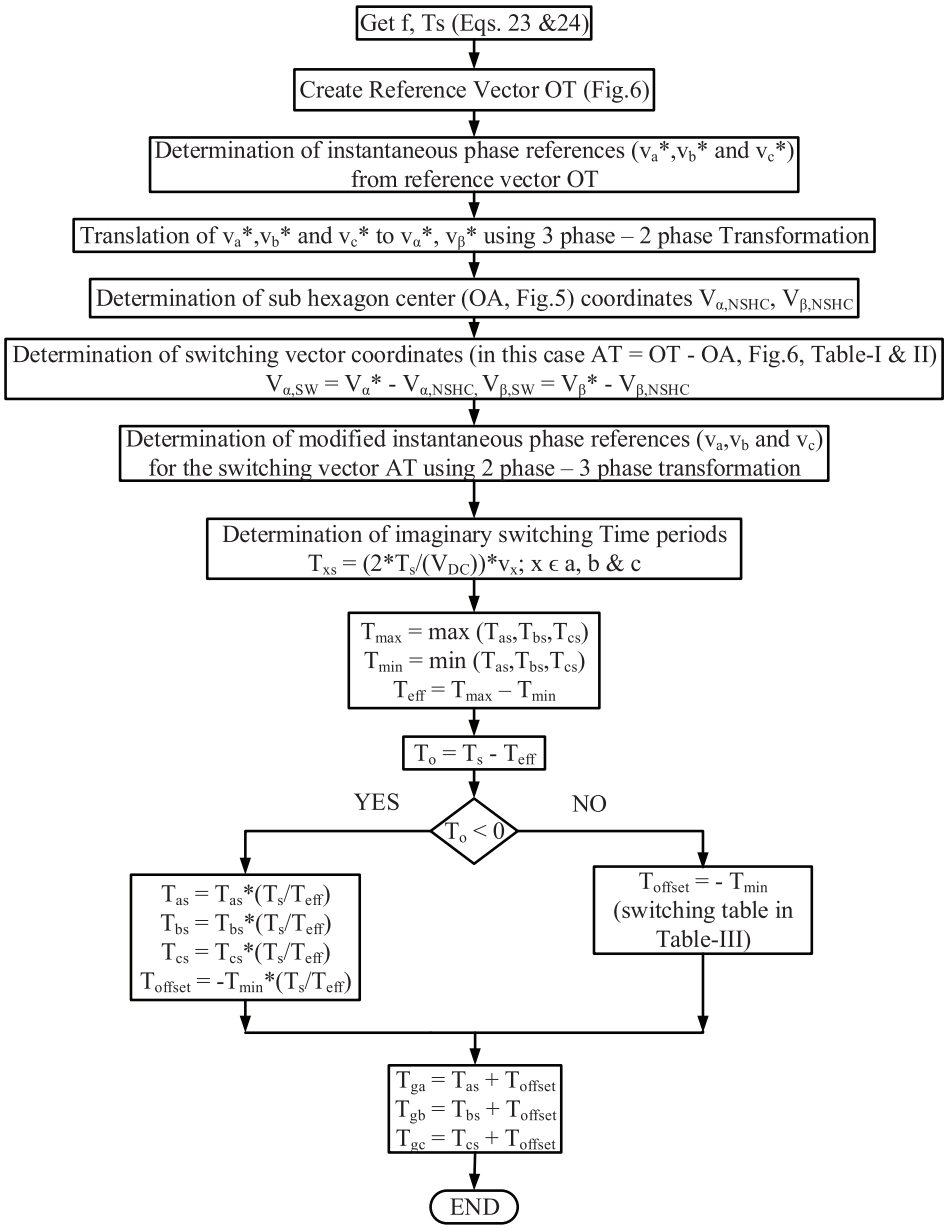

FIGURE A1 Flowchart for the implementation of the proposed PCAS-SVPWM