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RESEARCH ARTICLE

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Hybrid space-vector pulse width modulation strategies for a four-level open-end winding induction motor drive with an improvised harmonic performance and balanced DC-link capacitors

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Summary

The four-level open-end winding induction motor (4-L OEWIM) drive is constituted by two 2-level voltage source inverters (VSIs), wherein their DC-link voltages should be maintained in the ratio of 2:1. Owing to the unsymmetrical structure of the power circuit, the 4-L OEWIM drive is plagued with the drawback of capacitor voltage imbalance. The DC-link capacitor of one of the inverters, which is operated with the lower voltage level, that show the propensity of getting charged up by its higher voltage counterpart, belonging to the other inverter. In this article, two variants of space-vector pulse width modulation (SVPWM) schemes are suggested for the 4-L OEWIM drive. The suggested sample based SVPWM techniques achieve the voltage balancing of the DC-link capacitors, while improving the harmonic performance of the drive. Specifically, one of the two proposed PWM schemes manages to clamp one of the inverters in every sampling time interval. Hence this scheme results in lowering the total harmonic distortion (THD) in the no-load current in most of the operating range of the drive, resulting in lower ripple in the motor phase current, lower ohmic loss and reduced torque ripple. The performances of the proposed PWM techniques are assessed with the aid of simulation studies and are validated with the experimentation.

KEYWORDS

four-level, induction motor, open-end winding, over charging, SVPWM

1 | INTRODUCTION

Multilevel inverters (MLIs) have attained popularity in several industrial applications pertaining to the high power, medium voltage range. The advantages of MLIs over their two-level counterparts are well documented.[1-4]

List of Symbols and Abbreviations: v_{xo} ($x \in a, b, c$), pole voltages of the inverter-1; $v_{x'o'}$ ($x' \in a', b', c'$), pole voltages of the inverter-2; V_{DC}, DC-link voltage; m_a, modulation index; f_1, fundamental frequency component; T_s, Sampling time period; MLI, multilevel inverters; VSI, voltage source inverter; OEWIM, open-end winding induction motor; ZSC, zero-sequence current; SVPWM, space-vector pulse width modulation; SAZE, sample averaged zero-sequence elimination; SVC, SVPWM-small vector clamped-SVPWM; THD, total harmonic distortion.

Unlike the conventional motor-drive systems, wherein there is a clear demarcation between the power converter (MLI) and the load (motor), the open-end winding drive includes the load (motor) as an integral part of the drive system.

An induction motor with open-ended stator windings is obtained by opening the neutral point of star-connected stator windings. Alternatively, it can be obtained by the removal of end- connections for delta-connected stator windings.[5-8] The open-ends of the resulting motor are fed either with two-level voltage source inverters (VSIs) or various other types of MLIs.[9-12] The advantages of OEWIM drives are well documented.[5-12]

When compared to the conventional MLI topologies, they offer the advantages such as fault tolerance, simplified power circuit and rich redundancy of voltage space vectors. The latter property is particularly useful in devising some interesting PWM schemes.

To improve the quality of the phase voltage waveform, the DC-link voltages of the dual-inverter system are maintained in the ratio of 2:1. With this modification, four-levels are achieved in the motor phase voltages.[5] The power circuit of the resultant four-level open-end winding induction motor (4-L OEWIM) drive is shown in Figure 1A. It consists of two two-level VSIs, constituting the dual-inverter system. Each VSI is fed with an isolated DC source and their voltages are in the ratio of 2:1. The two DC-link voltages are isolated with reference to each other to avoid the circulation of the zero-sequence current (ZSC).

The space vector diagrams for the individual inverters and the nomenclature of the vectors is presented in Figure 1B. It should be noted that the dual-inverter system can raise a total of 64 space vector combinations, as each individual VSI can independently produce 8 vectors. Figure 2 depicts these 64 space vector combinations.

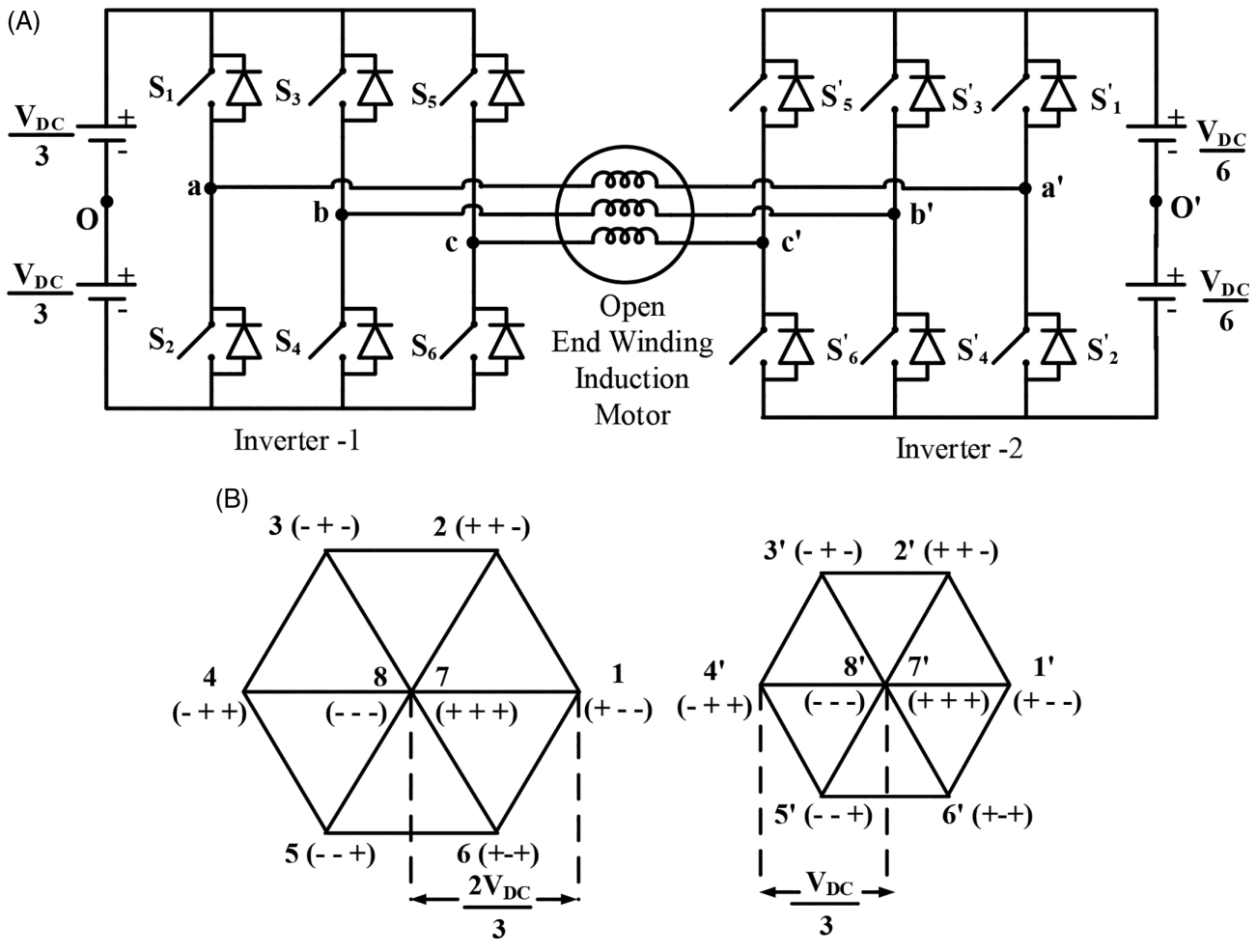

FIGURE 1 A, Circuit diagram of four-level open-end winding induction motor. B, Individual space vector diagrams of inverter-1 (left) and inverter-2 (right)

The 4-L OEWIM drive (Figure 1A), exhibits a major drawback, namely, the overcharging of the DC-link capacitor of inverter-2 (which has a lower voltage) by the DC-link capacitor of inverter-1 (which has a higher voltage).[13] As explained in Reference 13, for the 4-L OEWIM drive (Figure 1A), the switching vector combinations 11′, 22′, 33′, 44′, 55′, 66′, 12′, 16′, 23′, 34′, 45′, and 56′ cause overcharging of the lower DC-link capacitor. The corresponding switching space vector locations are: A, B, C, D, E, F, H, J, L, N, Q, and S (see Figure 2).

In the past, decoupled space-vector pulse width modulation (SVPWM) techniques have been proposed to avoid the overcharging of the lower voltage DC-link capacitor.[13] In these schemes, both of the constituent inverters are switched and controlled independently. As one might expect, these schemes incur higher switching power losses as both of the inverters are switched. In an attempt to reduce the switching power loss and to derive a better harmonic profile, phase clamped decoupled SVPWM techniques have been suggested to reduce the switching power loss.[14] These phase clamped SVPWM techniques also eliminate the overcharging of the lower DC-link voltage capacitor.

Further attempts were made to avoid the overcharging effects and to reduce the switching power loss of the dual-inverter system fed 4-L OEWIM drive.[15] Compromising on the principle of switching the nearest vector combinations, these SVPWM schemes avoid the use of the troublesome switching-vector combinations, which are responsible for the overcharging of the low-voltage DC-link capacitor. Although the SVPWM schemes proposed in Reference 15 manage to obtain the intended improvisation to a certain extent, there is still room for improvisation in terms of reducing the switching ripple in the motor currents.

Some new circuit topologies have also been suggested to avoid the overcharging phenomenon of the 4-L OEWIM drive.[16-18] However, the proposed circuit topologies possess paths for the circulation of ZSCs, causing peaky currents through the phase windings of OEWIM. To avoid the ZSC, SVPWM techniques such as the sample averaged zero-

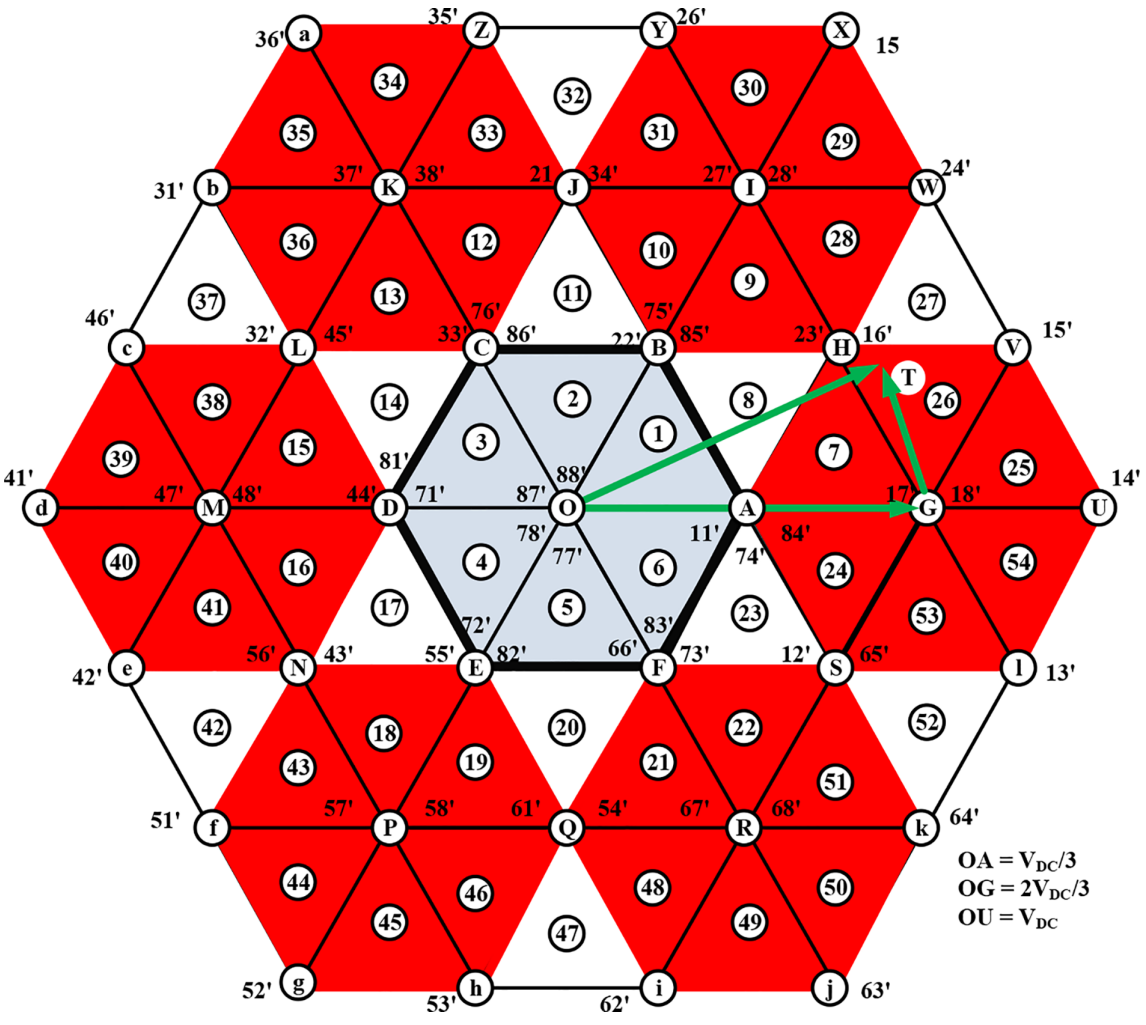

FIGURE 2 Resultant space-vector diagram of dual-inverter fed 4-L OEWIM

v_{xo}	$v_{x'o'}$	$v_{xx'}$
$V_{DC}/3$	$-V_{DC}/6$	$V_{DC}/2$
$V_{DC}/3$	$V_{DC}/6$	$V_{DC}/6$
$-V_{DC}/3$	$V_{DC}/6$	$-V_{DC}/6$
$-V_{DC}/3$	$-V_{DC}/6$	$-V_{DC}/2$

TABLE 1 Four-levels across the OEWIM phase winding

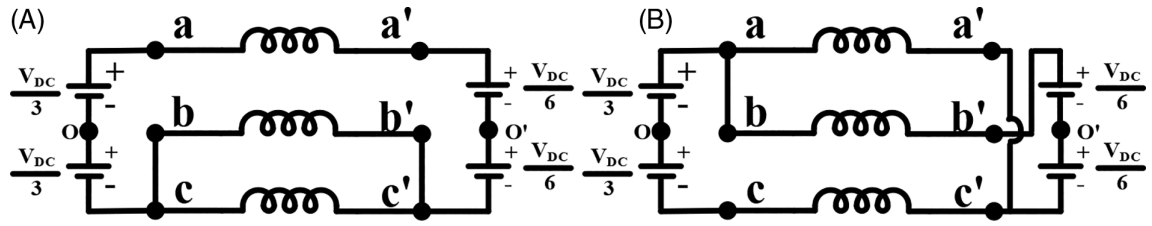

FIGURE 3 Equivalent circuit diagram of 4-L OEWIM for the switching vector combinations. A, 11′. B, 23′

sequence elimination (SAZE) SVPWM,[16] decoupled SAZE SVPWM,[17] and nested inverter clamped SAZE SVPWM[18] are proposed. The proposed techniques eliminate the ZSCs in the average sense in any given sampling time interval. However, the advantage of the improvement in the DC-bus utilization (by 15%), which is provided by the SVPWM technique is foregone with these SVPWM techniques.

Another circuit configuration has been proposed for a 4-L OEWIM drive, which uses a single DC voltage source for the main inverter (the one with higher DC-link voltage), while the second inverter is connected to a floating capacitor bank.[19] Redundant switching states are used to maintain the second DC-link voltage at half of the main inverter DC-link voltage (ie, to maintain a ratio of 2:1 between the respective DC-link voltages) and to obtain 4-level inversion.

The VSI connected to the floating capacitor is operated as the conditioning inverter to improve the waveform quality. A modified decoupled SVPWM technique is employed to control the VSIs in this work.[19] However, when the tip of the reference voltage space vector is situated in the outer hexagon, the available switching states to charge the capacitor are limited to two in each sector. Due to the lack of capacitor charging and discharging switching combinations, the modulation index is limited to 0.66 only. Thus, in this topology, the dc-link voltage utilization is reduced by 33% compared to the one shown in Figure 1A.

This survey of literature indicates that the new circuit topologies reported in References 17-19 also suffer from their own shortcomings and none of the 4-L OEWIM drives reported so far is ideal. This is the motivating factor to explore if the circuit shown Figure 1A possesses any unexplored aspects.

To achieve a better spectral performance, reduced current ripple and reduction in the switching power loss for the 4-L OEWIM drive, it is desirable to clamp the inverter with higher DC-link voltage (ie, inverter-1, Figure 1A) and switch the lower DC-link voltage (ie, inverter-2, Figure 1A) around the clamped inverter. However, the constraint of non-employability of the aforementioned forbidden switching vector combinations poses an obstacle to realize this objective.

In this article, two variants of sample based SVPWM schemes are suggested. The suggested SVPWM schemes, compared to the other works reported thus far, achieve: (a) avoidance of the overcharging of the DC-link capacitor of lower voltage by its counterpart, (b) a reduction in current ripple, and (c) reduction in the switching power loss.

The commonality in both of the two proposed SVPWM strategies is the identification of the troublesome sectors in which the deployment of optimal switching vector combinations (situated at the nearest vicinity to the reference voltage vector) is not possible. In 42 of the total 54 sectors, it is possible to clamp one of the inverters and switch the other (Figure 2). Only the other 12 belong to the category of the troublesome sectors. In these 12 sectors, a reasonable engineering compromise is made and the inverters are switched non-optimally to avoid the aforementioned problem of capacitor imbalance. In the first of the two proposed strategies, one inverter is clamped and distant vectors are switched, compromising mainly on the switching deviations. In the second strategy, both inverters are switched, compromising mainly on the switching power losses. The performances of both of the PWM schemes are first assessed with simulation studies and are then validated by experimentation.

2 | 4-L OEWIM DRIVE AND SWITCHING VECTOR COMBINATIONS EFFECT ON LOWER DC-LINK VOLTAGE CAPACITOR OVERCHARGING

2.1 | 4-L OEWIM

The inverter with higher DC-link voltage is named as inverter-1, while the inverter with lower DC-link voltage is named as inverter-2. The pole voltages of the inverter-1 and 2 are named as v_{xo} ($x \in a, b, c$) and $v_{x'o'}$ ($x' \in a', b', c'$), respectively. For the given DC-link voltage (V_{DC}), the pole voltages of inverter-1 and inverter-2, respectively, switch between the values of $\pm V_{DC}/3$ and $\pm V_{DC}/6$. The resultant four-levels across the motor phase windings ($v_{xx'} = v_{xo} - v_{x'o'}$) are shown in Table 1, while assuming the mid-points of o and o' are shorted.

As each inverter of the dual-inverter system has eight individual switching states, the resultant dual-inverter system has 64 space vector combinations, spread over 37 space vector locations in 54 sectors as shown in Figure 2.

2.2 | Switching vector combinations and their effect on the DC-link capacitors

As mentioned earlier, the switching vector combinations $11'$, $22'$, $33'$, $44'$, $55'$, $66'$, $12'$, $16'$, $23'$, $34'$, $45'$, and $56'$ cause *severe* overcharging of the lower DC-link capacitor. The equivalent circuit (see Figure 1A) for the switching combination $11'$ is shown in Figure 3A. From Figure 3A, it can be observed that, the *entire* current flowing out of the positive terminal of the DC-link capacitor of inverter-1 is constrained to flow into the positive terminal of the DC-link capacitor of inverter-2. This causes a definite overcharging of the DC-link capacitor of lower voltage. The behavior of the power circuit would be similar for the other switching vector combinations, namely, $22'$, $33'$, $44'$, $55'$, and $66'$.[13] It may be noted

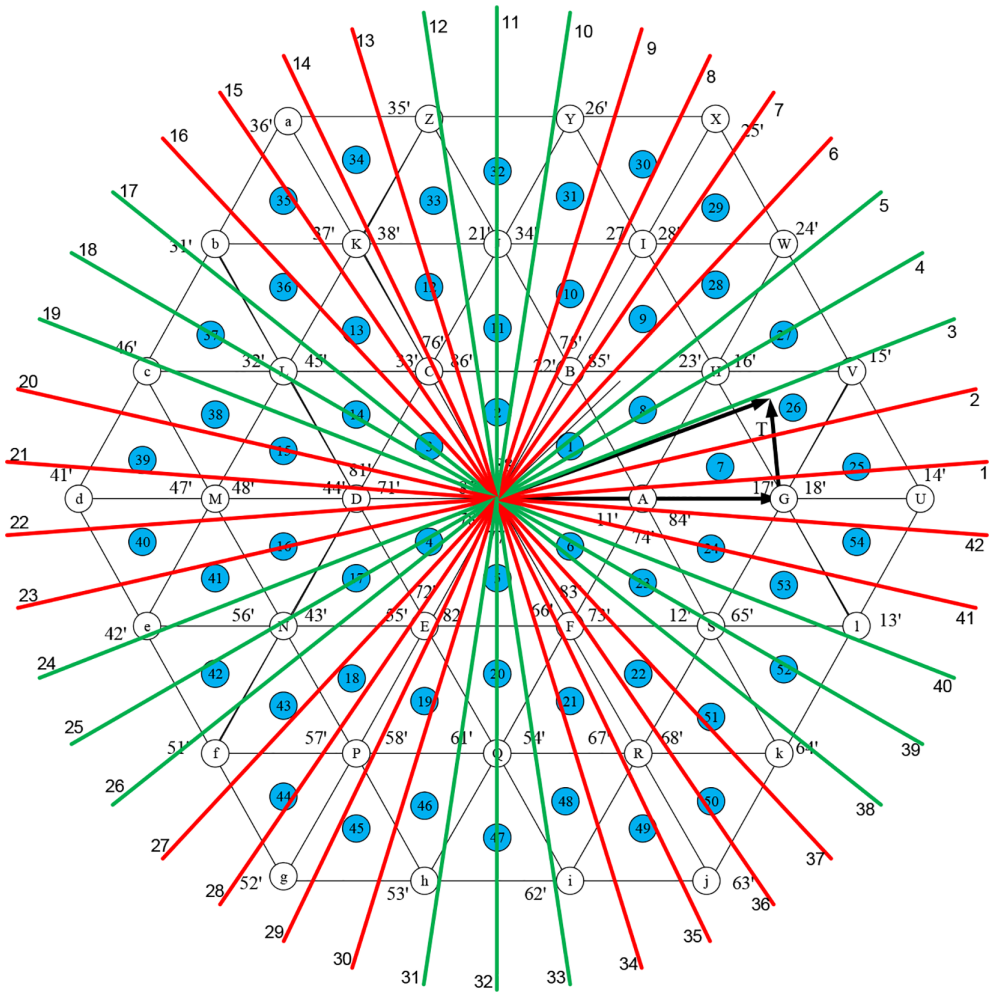

FIGURE 4 Proposed sample based SVPWM strategy for the 4-L OEWIM drive

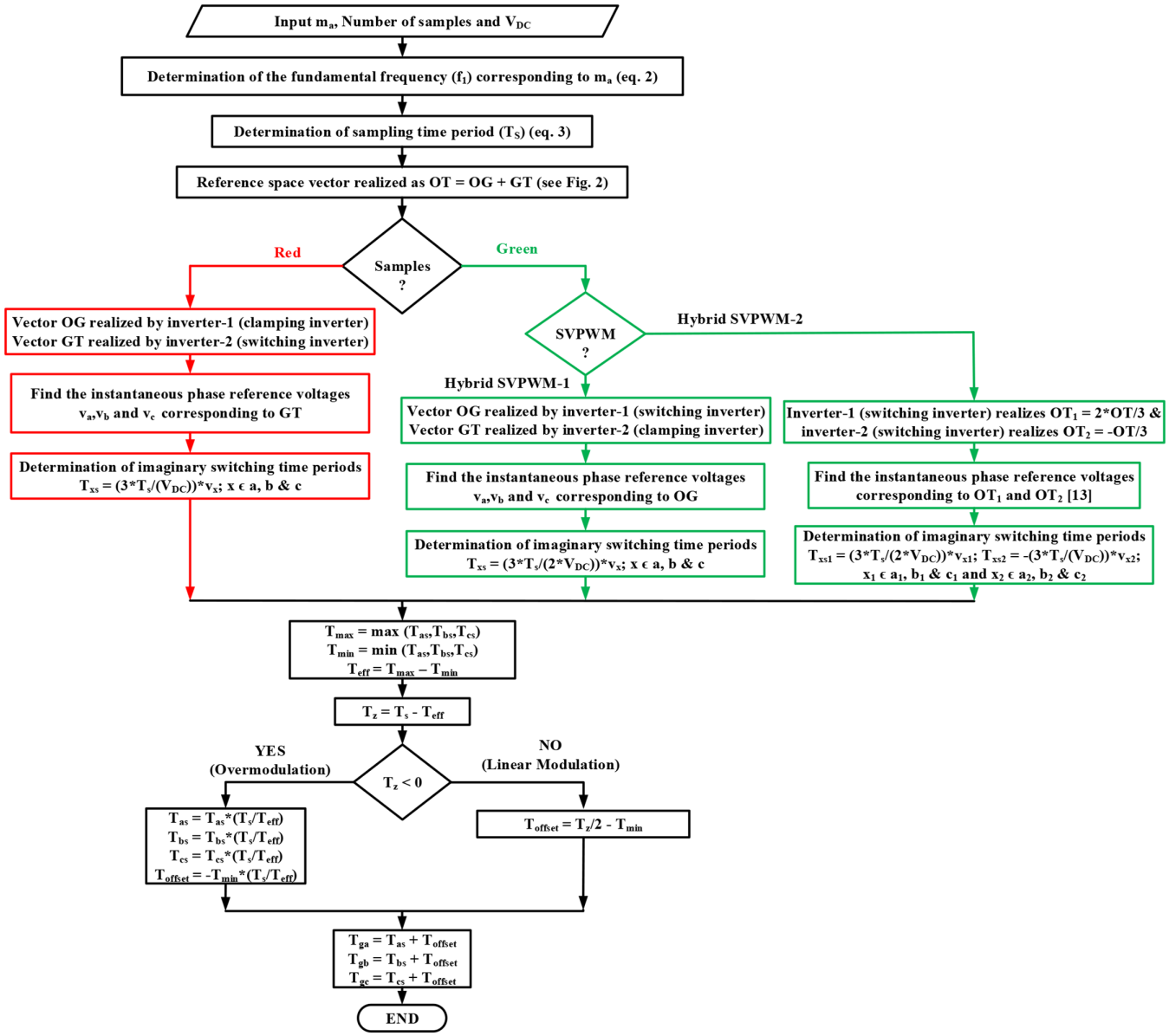

FIGURE 5 Flow chart of switching algorithm of proposed hybrid SVPWM strategies

that these *severe* charging combinations are placed at the centers of the sand-clock shaped structures, consisting of sector-pairs (8 &11), (14 & 17), and (20 & 23), which are placed at the rim of the core hexagon-*ABCDEF*. They are classified as *severe-charging* combinations, as switching of these combinations would lead to the problem of overcharging even when the motor is operated under the no-load condition. Consequently, the ratio of 2:1 in the DC-link voltages is not sustained and the motor phase voltages get severely distorted. Thus, the use of these six combinations is strictly forbidden.

Though not that severe, a similar charging effect occurs with the *mild-charging* combinations. It may be observed from Figure 2 that, these switching combinations are situated at the centers of the sand-clock shaped structures consisting of the sector-pairs (8 & 27), (11 & 32), (14 & 37), (17 & 42), (20 & 47), and (23 & 52). These structures are sandwiched between the sub-hexagons colored in red in Figure 2. A total of 12 switching combinations belong to this category. They are: 23′, 16′, 21′, 34′, 32′, 45′, 56′, 43′, 61′, 54′, 12′, and 52′.

When the combination 23′, belonging to the category of mild-charging combinations is switched (Figure 3B), only a *portion* of the DC current flowing out of the positive terminal of DC-link capacitor of inverter-1 flows into the positive terminal of DC-link capacitor of inverter-2. Thus, the severity of charging is not as much as in the previously mentioned combinations. When these combinations are switched, the lower DC-link capacitor may not charge, when the motor is

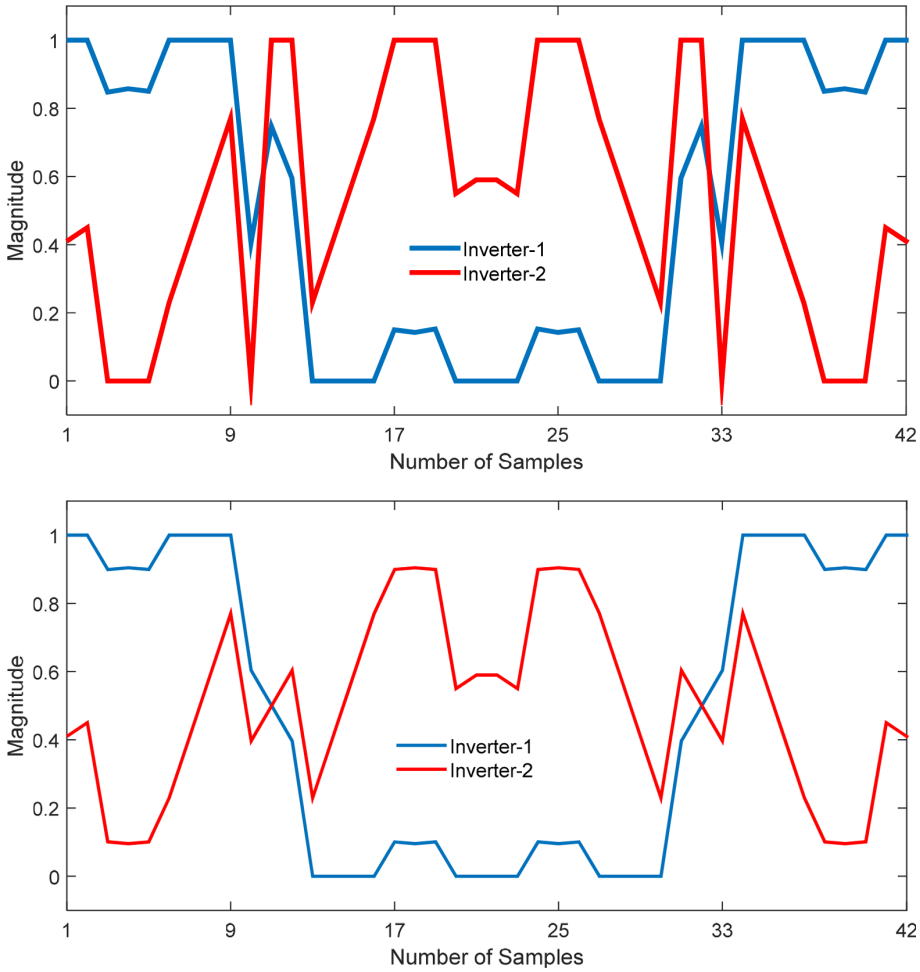

FIGURE 6 Modulating waveforms at a modulation index of 0.7 for hybrid SVPWM-1 (top) and hybrid SVPWM-2 (bottom)

operated under the no-load condition. However, when the motor is loaded and/or the tip of the reference voltage vector is closely situated to the vertex containing these mild combinations, the imbalance of lower DC-link voltage is experienced.[13] In these cases, the imbalance in the voltage of the DC-link capacitor occurs due to the larger charging current as well as the higher dwell-time associated with the switching of such combinations.

From Figure 2, it can be observed that the severe combinations can be avoided by replacing them with the redundant vector combinations (see space vector locations in A, B, C, D, E, and F in Figure 2). However, the mild charging combinations can neither be avoided nor be replaced. Thus, these combinations cause overcharging of lower DC-link voltage capacitor, when the OEWIM is loaded and/or the dwell-time at these vertices is more.

The next section explains about the principle and implementation of the proposed SVPWM techniques to avoid the overcharging of the DC-link capacitor with lower voltage.

3 | PRINCIPLE OF PROPOSED SVPWM SCHEMES

Figure 2 shows the reference voltage space vector, of magnitude $\bar{OT}$. The reference vector $\bar{OT}$ is used to generate the reference modulating waveform for the dual-inverter system. The reference voltage vector $\bar{OT}$ and the effective DC-link voltage OU of the OEWIM drive (Figure 2) are related through the modulation-index (m_a) and is given by:

$$m_a = \bar{OT}/OU \tag{1}$$

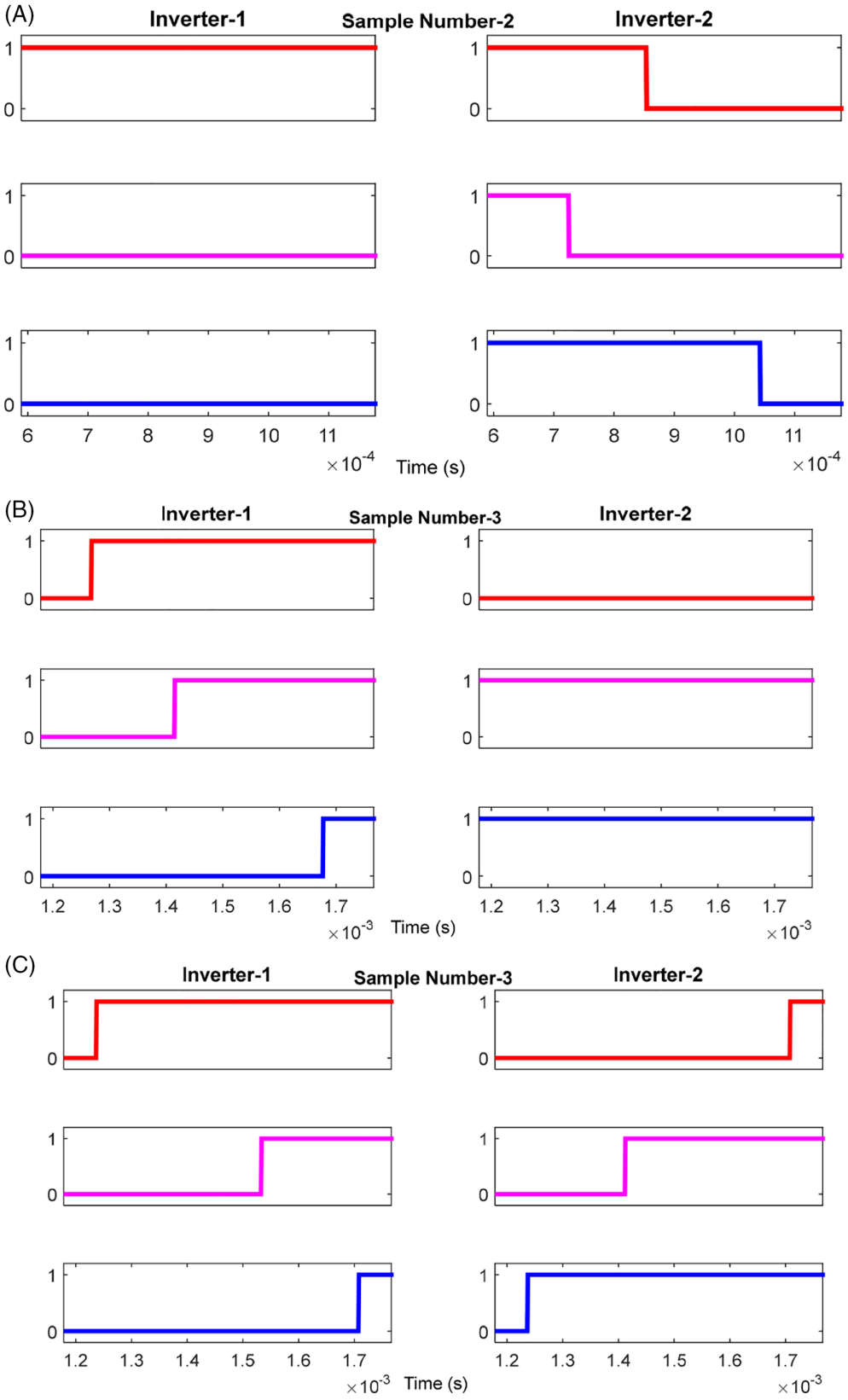

FIGURE 7 Per unit pole voltages of the inverter-1 and inverter-2 for sample number-2 (A) and 3 (B, C). A, Both SVPWMs. B, Hybrid SVPWM-1. C, Hybrid SVPWM-2

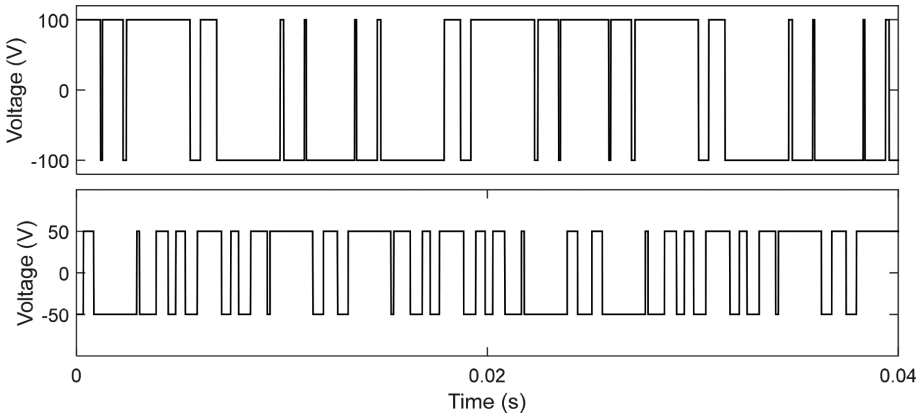

FIGURE 8 Simulated pole voltage of the inverter-1 (top), inverter-2 (bottom) at a $m_a = 0.7$ for hybrid SVPWM-1 scheme

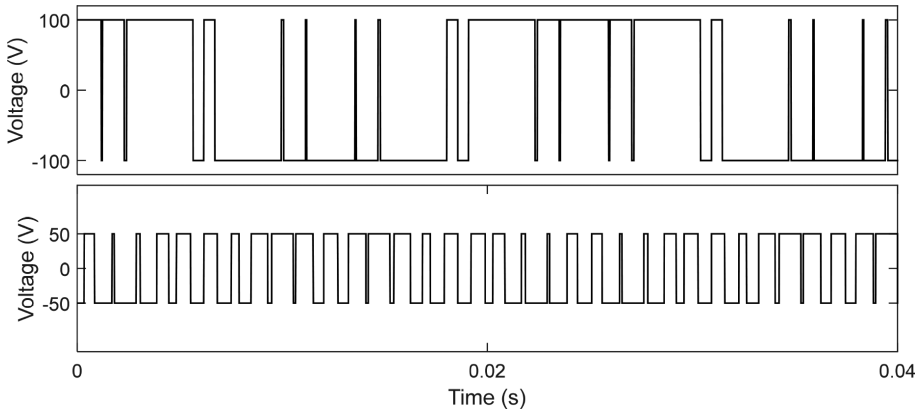

FIGURE 9 Simulated pole voltage of the inverter-1 (top), inverter-2 (bottom) at a $m_a = 0.7$ for hybrid SVPWM-2 scheme

Irrespective of the fundamental frequency, the reference space vector $\bar{OT}$ is sampled 42 times per cycle, to achieve the waveform symmetries.[13] The drive is so scaled that, the rated frequency of 50 Hz (and hence the line voltage of 400 V) is applied to the OEWIM at the edge of the linear modulation. The modulation index (m_a) corresponding to this operating point is ($\sqrt{3}/2$). Thus, the frequency of the fundamental component (f_1) and the modulation-index (m_a) are related as:

$$f_1 = \frac{m_a}{(\sqrt{3}/2)} \times 50 \tag{2}$$

The sampling time period (T_s) of the dual-inverter system is given by:

$$T_s = \frac{1}{f_1 \times 42} \tag{3}$$

From Figure 2, it can be observed that it is possible to decompose the vector $\bar{OT}$ as:

$$\bar{OT} = \bar{OG} + \bar{GT} \tag{4}$$

From Equation (4), it is evident that, to realize the reference $\bar{OT}$ with the dual-inverter system, one inverter should construct the vector $\bar{OG}$ and other inverter should realize the vector $\bar{GT}$. To achieve minimum current ripple and to reduce the switching power loss in the dual-inverter system and ohmic losses in the motor, one inverter (preferably the

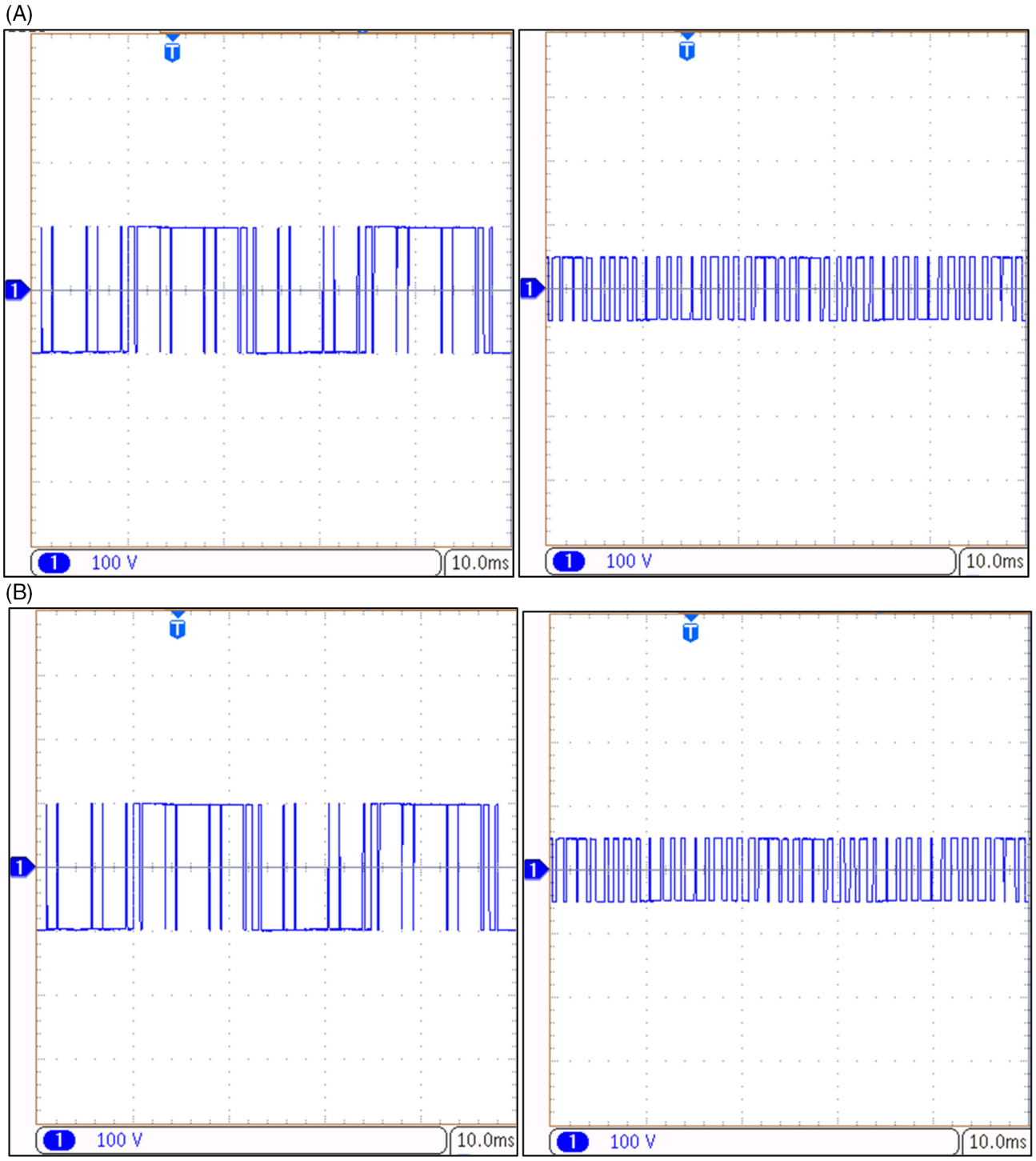

FIGURE 10 Experimentally obtained pole voltage of the inverter-1 (left), inverter-2 (right) at a $m_a = 0.7$ for, A, hybrid SVPWM-1 scheme and, B, hybrid SVPWM-2 scheme

one, which is operated with a higher DC-link voltage) of the dual-inverter system should be clamped, while the other inverter should be switched around the pivot-vector provided by the clamped inverter.

Thus, in an *ideal* switching scheme, inverter-1 and inverter-2 should, respectively, be chosen as the clamped- and switched-inverters (Figure 2). The switched vector $\overline{GT}$ is produced in the average sense using the Center-Spaced SVPWM (CSVPWM) technique. Inverter-1 is clamped to the space vector locations O, G, I, K, M, P, and R and inverter-2 is switched around these offset vectors. The switching algorithm described in Reference 20, which is based

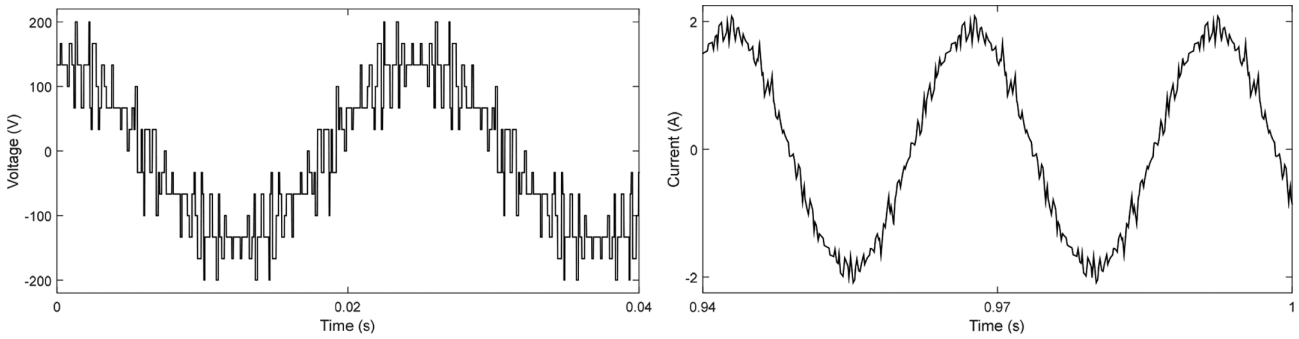

FIGURE 11 Simulated phase voltage (left) and current (right) of the 4-L OEWIM at $m_a = 0.7$ for the hybrid SVPWM-1 scheme

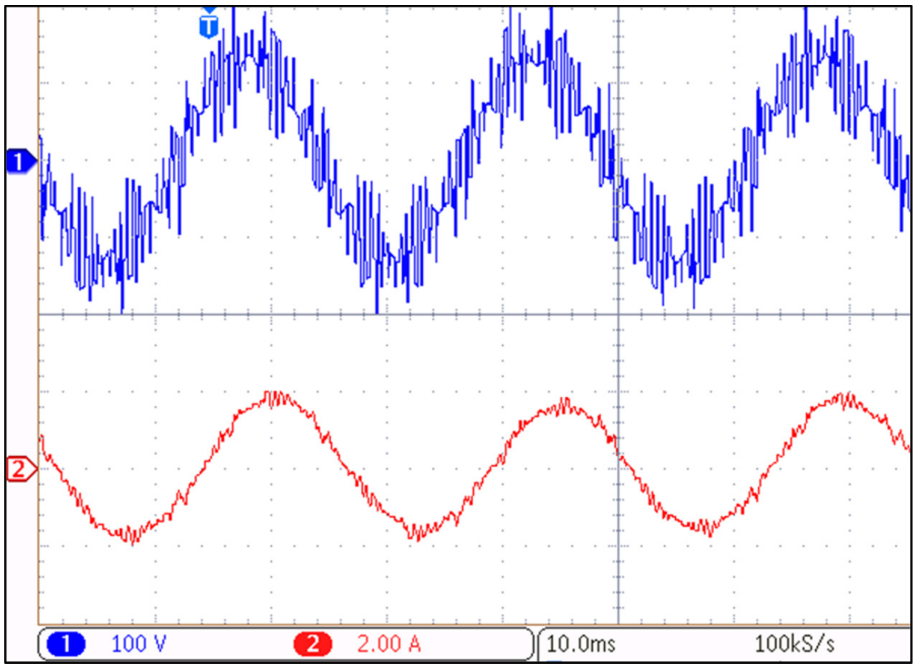

FIGURE 12 Experimentally obtained phase voltage (top) and current (bottom) of the 4-L OEWIM at $m_a = 0.7$ for the hybrid SVPWM-1 scheme

on the concept of *imaginary switching time periods*, can be used to implement the CSVPWM technique to the switched-inverter.

It is easy to observe that, when the tip of the reference vector is situated in the core-hexagon (ABCDEF, Figure 2), inverter-1 can be clamped to a null-vector and inverter-2 can be switched around the null-vertex "O" (Figure 2). When inverter-1 is clamped to a null vector (+++ or −−−), a switched neutral point is created with the terminals ***a***, ***b***, and ***c***. Thus, the OEWIM drive would revert back to the conventional two-level VSI drive, to which the CSVPWM can easily be implemented using the switching algorithm presented in.[20] On the other hand, when the tip of the reference vector is situated in any of the six red-colored sub-hexagons shown in Figure 2, inverter-1 should be clamped to provide the offset vector and inverter-2 should be switched.

However, such an *ideal* switching algorithm cannot be implemented for the proposed 4-L OEWIM drive owing to the following reasons:

1. Only 42 out of the 54 sectors are covered with this approach (shown colored in Figure 2) and 12 sectors are left uncovered (the uncolored sectors in Figure 2).
2. The 12 uncovered sectors possess both the severe- and the mild-charging vector combinations.

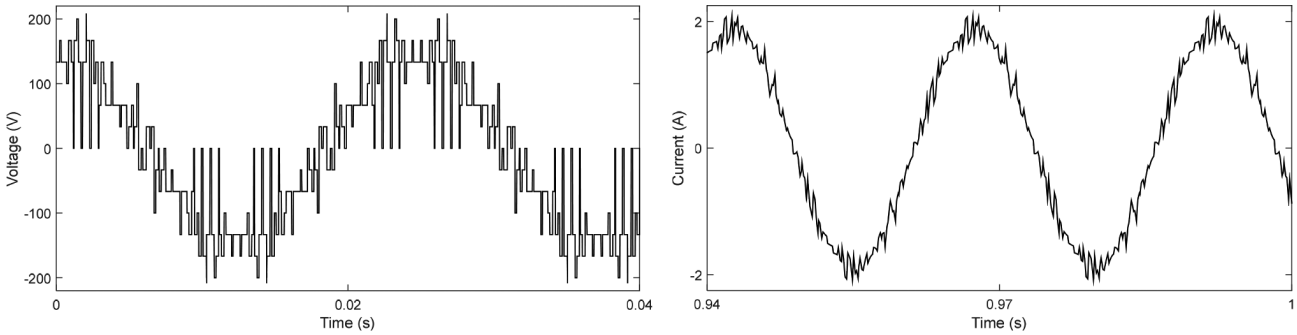

FIGURE 13 Simulated phase voltage (left) and current (right) of the 4-L OEWIM at $m_a = 0.7$ for the hybrid SVPWM-2 scheme

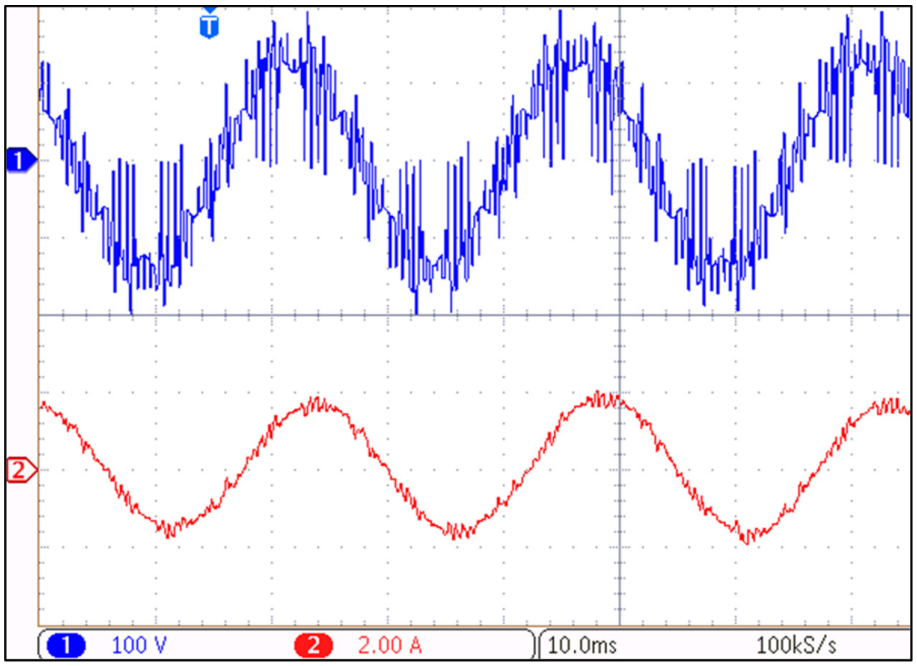

FIGURE 14 Experimentally obtained phase voltage (top) and current (bottom) of the 4-L OEWIM at $m_a = 0.7$ for the hybrid SVPWM-2 scheme

3. Even in the 42 sectors that are uncovered, there are sectors, wherein mild-charging switching combinations are present at one of their vertices. For example, in the sub-hexagon "BJYXWH" (Figure 2), there exist two mild-switching combinations at the vertex "**H**," namely, 16′ and 23′. Whenever the tip of the reference vector is closely situated to this type of vertices in a given sampling time interval, the DC-link capacitor of inverter-2 exhibits a propensity to go out of balance and overcharge above the level of " $V_{DC}/3$," under loaded conditions.

In view of the above, two SVPWM schemes have been proposed. In the work described in Reference 13, the troublesome space vectors are avoided by resolving the reference voltage space vector (*OT*, Figure 2) into two components, which are anti-phased with reference to each other. These two sub-reference vectors, which are in the ratio of 2:1, are then synthesized using the SVPWM algorithm described in Reference 20. While this scheme successfully achieves the capacitor voltage balancing, it would result in higher switching power loss, as both of the inverters are switched in every sampling time period.

A different approach is adopted in the work described in Reference 15, wherein all of the samples, situated outside the core-hexagon "ABCDEF" are realized by clamping inverter-2 and switching inverter-1. With this scheme, all of the severe- as well as the mild-charging vector combinations are avoided.[15] While this strategy successfully achieves the capacitor balancing, it would switch farther vectors, resulting in an increased ripple in the motor-phase current and an

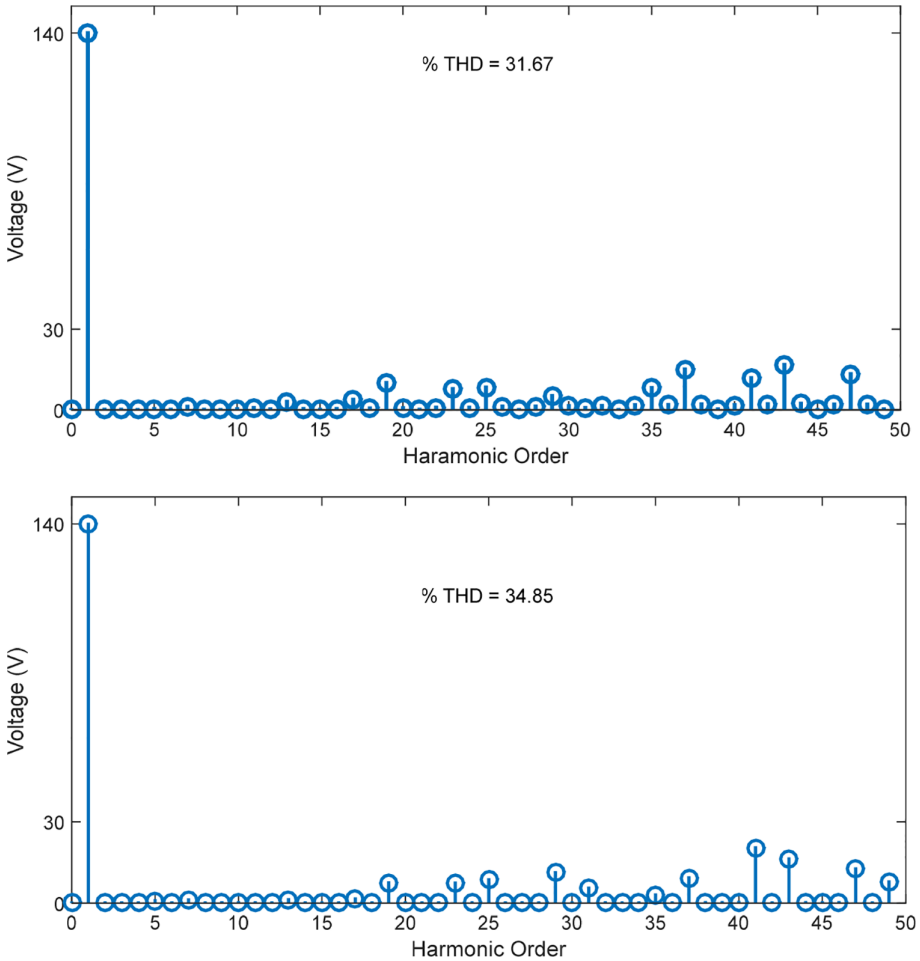

FIGURE 15 4-L OEWIM drive phase voltage FFT analysis at $m_a = 0.7$ for hybrid SVPWM-1 (top), hybrid SVPWM-2 (bottom) strategies

increased switching power loss, as the inverter with higher DC-link voltage is switched. For the rest of this article, this SVPWM scheme is named as the *small vector clamped-SVPWM (SVC-SVPWM)* scheme. This PWM scheme is used as the benchmark, with which the performances of the suggested PWM schemes (of this article) are compared.

This article suggests two improvised SVPWM methods of tackling this problem. These methods render a better harmonic performance compared to the methods suggested in the earlier literature.[13,15]

Figure 4 shows the details regarding the instants at which the reference vector (*OT*, Figure 2) is sampled. It may be noted that the instantaneous reference phase voltages, which constitute the overall reference voltage vector *OT*, are uniformly sampled in such a way that, there exist 42 samples in any given cycle, irrespective of the modulation index (and hence the frequency of the fundamental components of the phase voltages, see Equation (1)). The choice of the number of samples and their placement is decided by the considerations of waveform symmetries.[14,21]

Figure 4 also shows radial lines emanating out of the center "O" of the hexagon "UXadgj," which are colored in red and green. It may be noted that these red and green lines are interspersed. To facilitate an easy explanation, the samples situated on the red and green lines are referred as "red samples" and "green samples."

In the first of the two proposed improvisations, all the "red" samples are synthesized by clamping inverter-1, while switching inverter-2 around the pivot vector provided by it. In contrast, the "green" samples are synthesized by switching inverter-1 around the pivot vectors provided by inverter-2 (except in the core hexagon "ABCDEF," as mentioned in the previous paragraph). In other words, the roles of the two inverters are reversed for the "green" samples, when compared their "red" counterparts. It may easily be noted that, this simple maneuver would altogether avoid the deployment of the troublesome switching vector combinations. Thus, this SVPWM strategy tends to trade-off between the contrasting requirements of clamping inverter-1 in all of the 42 samples (to switch the nearest vector combinations to improve the harmonic performance) and to avoid the overcharging of the DC-link capacitor of inverter-2, which

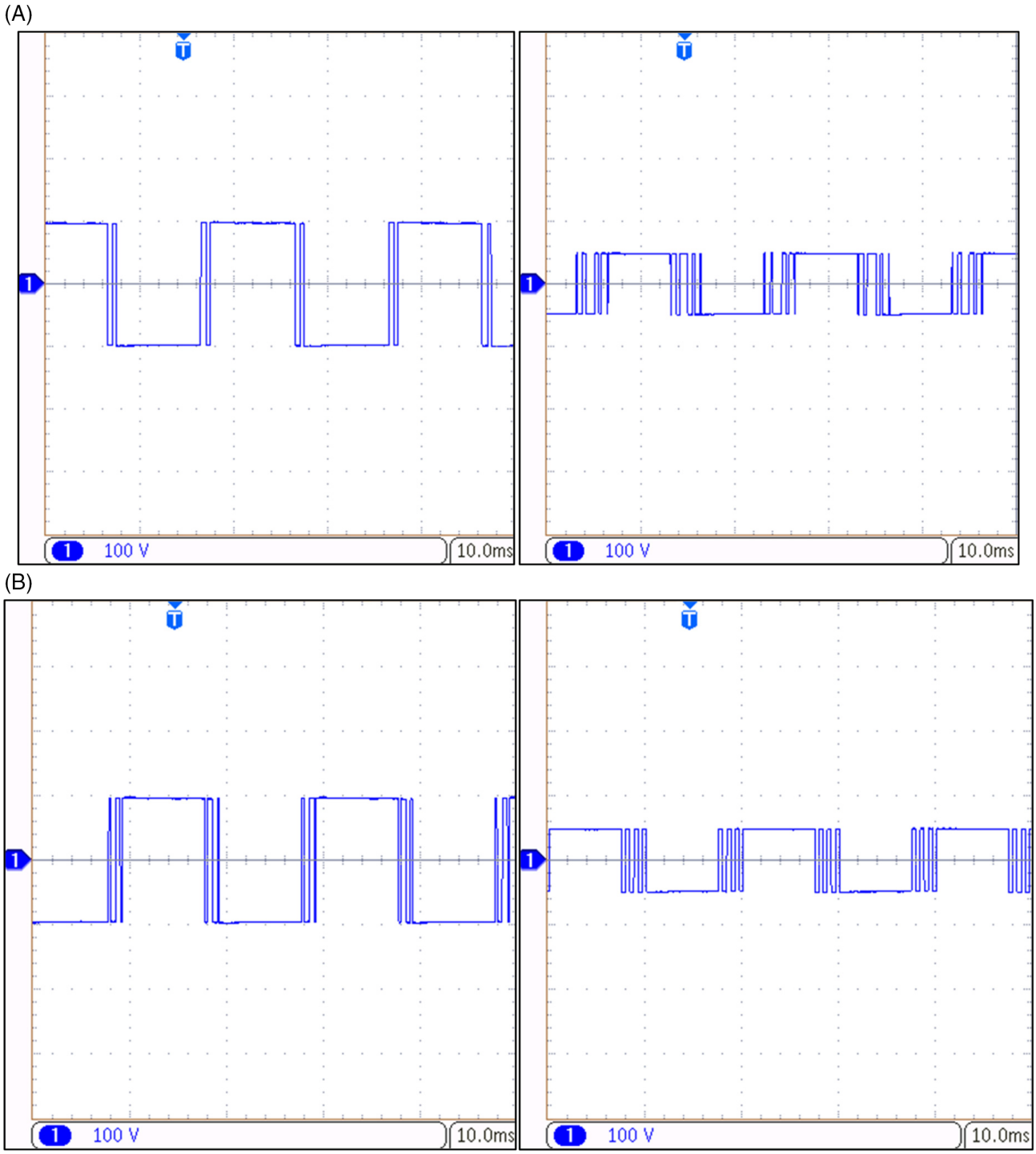

FIGURE 16 Experimentally obtained pole voltage of the inverter-1 (left), inverter-2 (right) at a $m_a = 1$ for, A, hybrid SVPWM-1 scheme and, B, hybrid SVPWM-1 scheme

would inevitably happen if such an ideal switching strategy is resorted to. For the rest of the manuscript, this PWM strategy is termed as the *Hybrid SVPWM-1*.

In the second PWM scheme, as in the previous scheme, the "red" samples are constructed by clamping inverter-1 and switching inverter-2. However, for the "green" samples, the SVPWM scheme proposed in Reference 13 is employed, which successfully obtains the required balancing of the voltage of the DC-link capacitor of inverter-2. Thus, this variant of the SVPWM is the amalgamation of aforementioned *ideal* SVPWM scheme and the Decoupled SVPWM scheme proposed in Reference 13. For the rest of this article, this SVPWM scheme is referred as the *Hybrid SVPWM-2*.

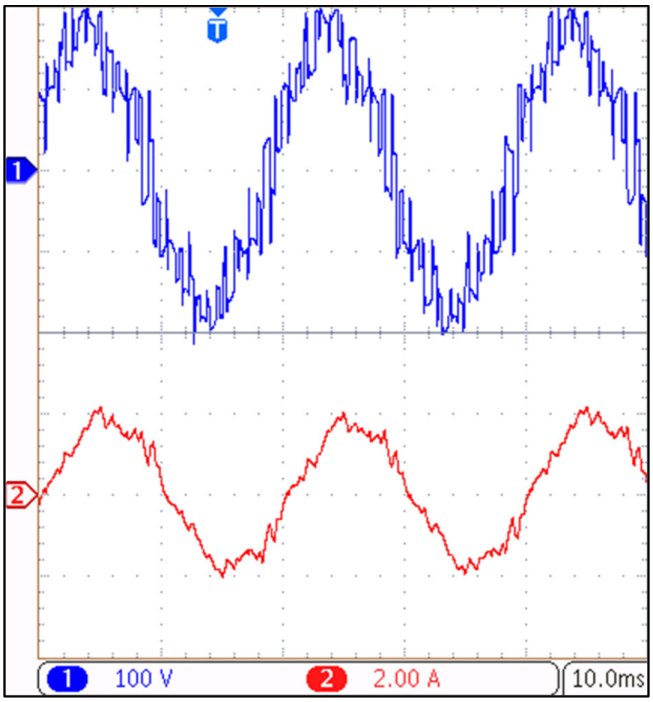

FIGURE 17 Experimentally obtained phase voltage (top) and current (bottom) of the 4-L OEWIM at $m_a = 1$ for the hybrid SVPWM-1 scheme

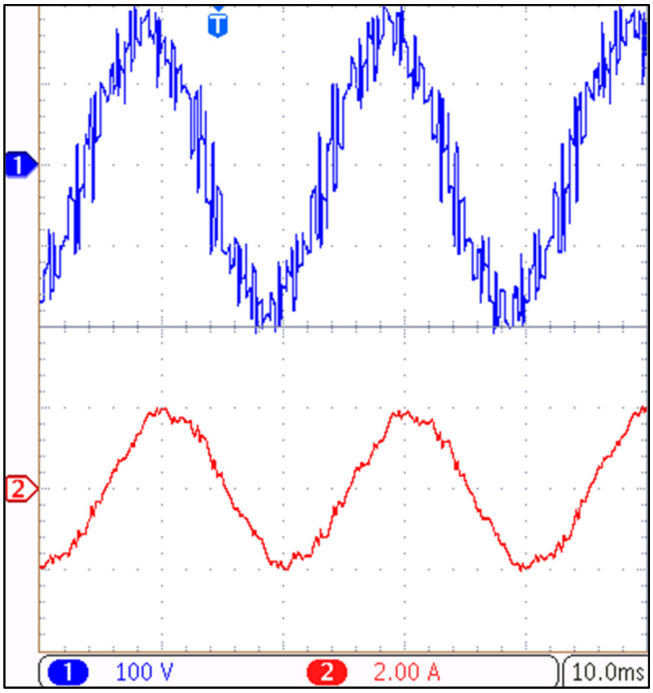

FIGURE 18 Experimentally obtained phase voltage (top) and current (bottom) of the 4-L OEWIM at $m_a = 1$ for the hybrid SVPWM-2 scheme

The flow chart of the switching algorithm is presented in Figure 5 for the proposed hybrid SVPWM strategies.

Figure 6 demonstrates the resulting modulating waveforms of the two proposed improvisations at a modulation index of 0.7. The corresponding per unit pole voltages at the sample number-2 and 3 are presented in Figure 7.

It may be noted from Figure 3 that the sample-2 is a "red" sample for both of the proposed SVPWMs. Consequently, inverter-1 acts as the clamped inverter and inverter-2 acts as the switched inverter, as is evident from Figure 7A.

At sample instant-3 for the Hybrid SVPWM-2, both inverters are switched and for the Hybrid SVPWM-1 scheme, the two inverters reverse their roles when compared with the sample instat-2 (ie, inverter-1 acts as switched inverter and inverter-2 is clamped). It may also observed from Figures 6 and 7 that, with the Hybrid SVPWM-1 at any sampling instant, either inverter-1 or inverter-2 is clamped, which results in the reduction of switching power loss.

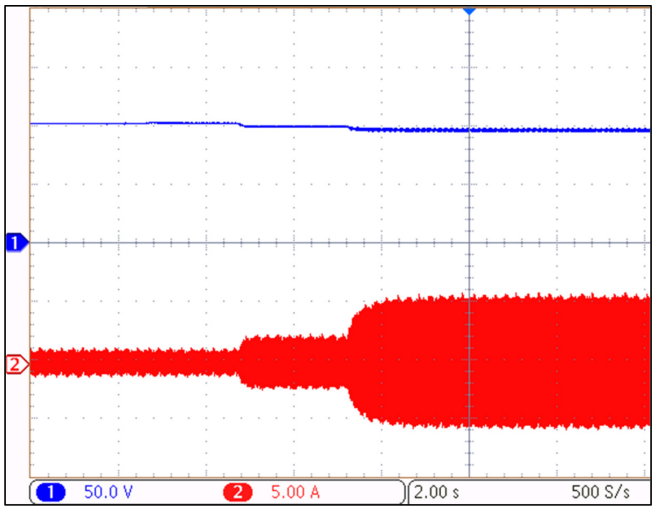

FIGURE 19 The experimentally obtained lower DC-link voltage of the inverter-2 (top), phase current (bottom) of the OEWIM drive with hybrid SVPWM-1 scheme at $m_a = 0.6$

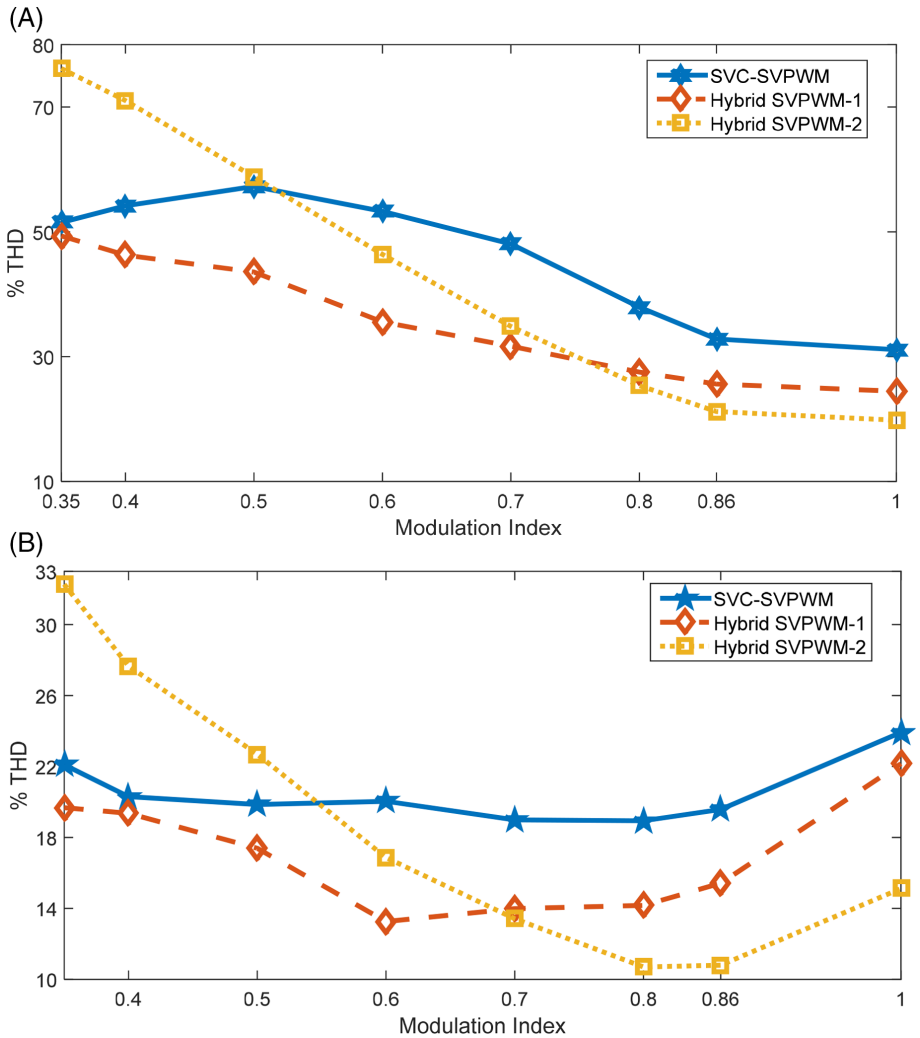

FIGURE 20 Comparative analysis of proposed SVPWMs with Reference [15]. A, % Voltage THD. B, % current THD

4 | SIMULATION AND EXPERIMENTAL RESULTS ANALYSIS

To assess the effectiveness of the proposed hybrid SVPWM schemes, simulation and experimental results are carried out on a 3-phase, 50 Hz, 4-pole, 3.7 kW, 1445 RPM OEWIM drive. The OEWIM is operated in volt/Hz control in

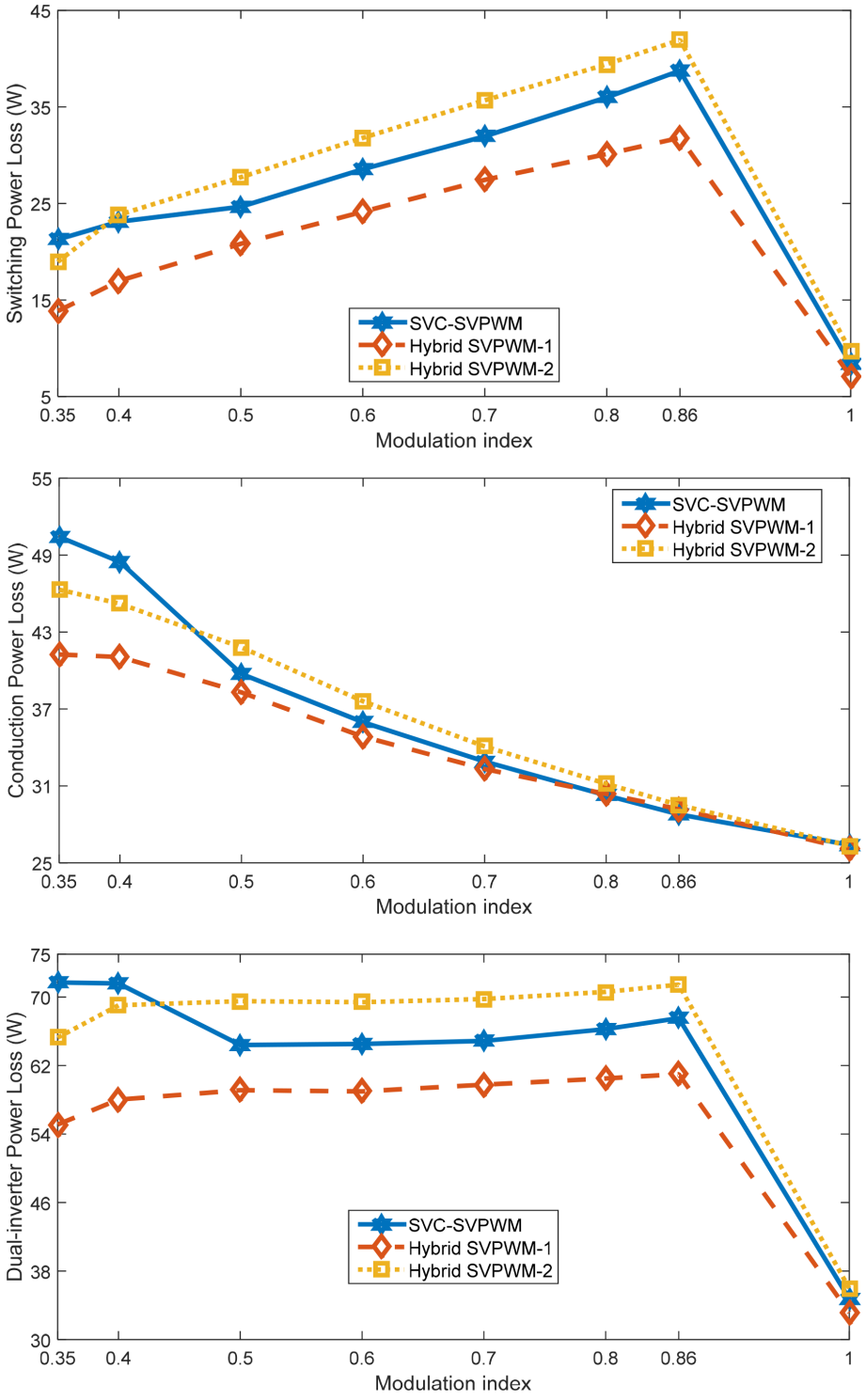

FIGURE 21 Switching power loss (top), conduction power loss (middle), and total dual-inverter power loss (bottom) of the dual-inverter system

open-loop. The OEWIM drive shown in Figure 1A is simulated in the *MATLAB/Simulink* software. The required switching pulses for the inverter-1 and inverter-2 are generated by using the *dSPACE-1104* controller.

For experimentation, the overall DC-link voltage of the dual-inverter system is chosen as 300 V (|OU| in Figure 2). To achieve 4-level operation, the overall DC-link voltage is divided in the ratio of 2:1. This leads to the respective DC-link voltages of 200 and 100 V for inverter-1 and inverter-2. The simulation parameters of the OEWIM are: $R_s = 4.215\ \Omega$; $R'_r = 4.185\ \Omega$; $x_{ls} = x'_{lr} = 5.502\ \Omega$; $X_m = 162.3\ \Omega$; $J = 0.0131\ \text{Kg} - \text{m}^2$; $B = 0.002985\ \text{N m s}$.

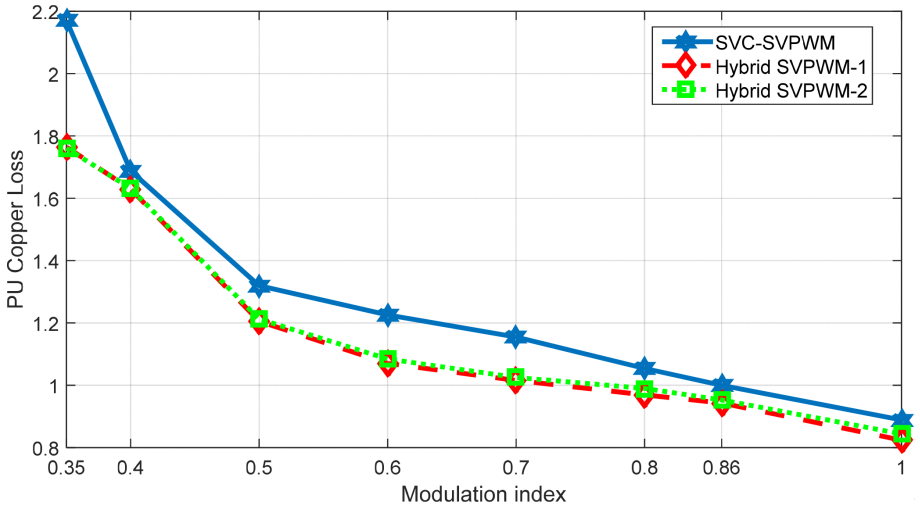

FIGURE 22 PU total copper loss of 4-L OEWIM drive

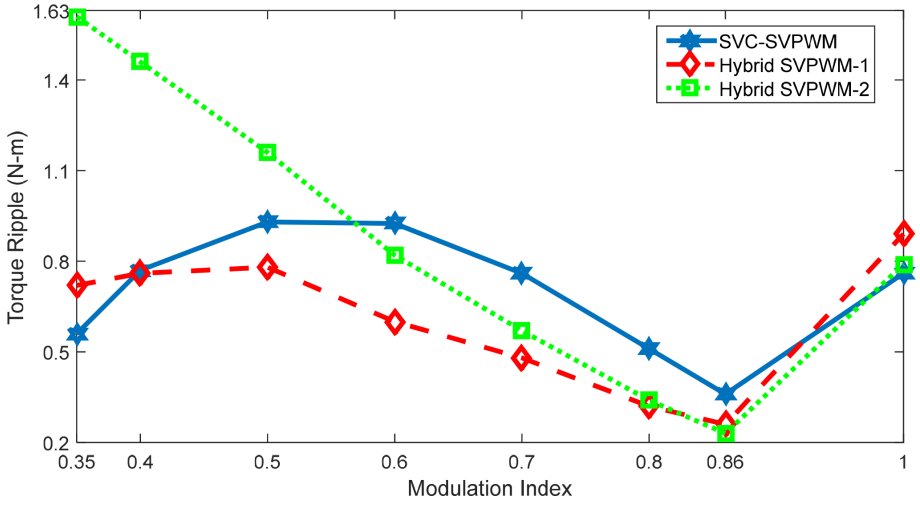

FIGURE 23 Torque ripple of 4-L OEWIM drive at no-load

4.1 | Simulation and experimental results

As mentioned in the earlier section, the modulation index varies in the range of $\left(0-\frac{\sqrt{3}}{2}\right)$ to cover the entire speed range of the OEWIM drive. As mentioned in the earlier section, when the sample lies within the core-hexagon "ABCDEF," the OEWIM drive is operated as the conventional 2-level VSI drive with a DC-link voltage of $V_{DC}/3$. This being a trivial case, experimental results corresponding to the low speed operation are not presented in this article. When the modulation index is above the value of $\sqrt{3}/2$, the drive is operated in the region of overmodulation, where the frequency of the OEWIM is fixed to rated frequency (ie, 50 Hz). In the interest of brevity, the simulation and experimental results are presented for the cases of the $m_a = 0.7$ and overmodulation.

The simulated pole voltages of the dual inverter system at a $m_a = 0.7$ are presented in the Figures 8 and 9 for the Hybrid SVPWM-1 and Hybrid SVPWM-2, respectively. The corresponding experimentally obtained pole voltages are shown in Figure 10.

From the simulated and experimentally obtained pole voltages, it can be observed that, with the hybrid SVPWM-2 scheme, switching occurs in both of the inverters, while the hybrid SVPWM-1 scheme switches only one inverter, keeping the other clamped. This would result in the reduction of switching power loss of the dual-inverter system.

The simulated and experimentally obtained OEWIM phase voltage and currents are shown in Figures 11 to 14 for both of the proposed hybrid SVPWM techniques. It may be noted that the phase voltage waveform possesses both

quarter- and half-wave symmetries.[13] One may also observe the close agreement between the simulated and the experimental waveforms.

From the phase voltage waveforms presented in Figures 12 and 14, it may be observed that, the motor windings are subjected to low dv/dt for the hybrid SVPWM-1 scheme when compared to the hybrid SVPWM-2 technique. This would be a decisive advantage with the Hybrid SVPWM-1 scheme, as the deleterious effects of higher dv/dt are well documented.[22]

Figure 15 shows the results of the FFT analysis of the phase voltage of the 4-L OEWIM drive, with the proposed hybrid SVPWMs. The FFT analysis reveals that the total harmonic distortion (THD) in the phase voltage with the hybrid SVPWM-1 scheme is lower compared to the hybrid SVPWM-2 scheme.

The pole voltages, phase voltage, and phase current waveforms for both of the proposed hybrid SVPWM techniques for over modulation (ie, $m_a = 1$) are presented in Figures 16 to 18.

4.2 | Dynamic response of the capacitor voltage with lower DC-link voltage

As mentioned in Section 2, the mild-charging switching vector combinations could result in the overcharging of the lower DC-link capacitor, when the motor is loaded. This type of overcharging may not occur at lower load currents, but may set in as the motor is loaded.[13]

The proposed sampled based SVPWM schemes switch both of the inverters in such a manner that the mild charging switching combinations are avoided, which achieves the voltage balancing of the DC-link capacitors.

To demonstrate this, the drive is run under loaded conditions at a modulation index of 0.6. At this value of m_a, the reference voltage vector (OT, Figure 2) comes very close to the locations of the mild-charging switching vector combinations (corresponding to $m_a = 0.58$). It may be noted that the DC-link capacitor of inverter-2 is highly exposed to the vulnerability of imbalance at this value of m_a, as the dwell-times of these locations would be very large (almost equal to the entire sampling time period), when the ideal SVPWM scheme is implemented. Thus, this test verifies the effectiveness of the proposed SVPWM schemes.

The result of this experiment, shown in Figure 19, concludes that both of the proposed SVPWM schemes achieve the balancing of the DC-link capacitor of lower voltage (that of inverter-2). It may be noted that this DC-link voltage is well balanced and shows the usual drop in voltage and increase in its ripple, when loaded.

The harmonic performances of both of the proposed improvisations (hybrid SVPWM-2 and hybrid SVPWM-1) are compared with the benchmark SVC-SVPWM scheme[15] by carrying out the analyses of voltage THD and current THD by operating the OEWIM at no-load. These results are presented in Figure 20.

From Figure 20, it can be observed that, when compared to the SVC-SVPWM technique,[15] the hybrid SVPWM-1 results in a lower THD in voltage throughout the range of modulation index, while the hybrid SVPWM-2 scheme performs better in the higher range. It is interesting to note that the SVC-SVPWM scheme performs better than the two proposed SVPWM schemes in the range of 0.33 to 0.42. It should also be noted that these PWM schemes should be compared only when $0.33 \leq m_a \leq 1.0$. This is due to the fact that the OEWIM drive reverts back to the conventional two-level VSI driven IM drive, as stated in the earlier section, when $m_a \leq 0.33$ (with inverter-1 clamped to a null vector).

It should also be noted that a reduced current THD results in lower ripple in the motor phase current, which in turn reduces the ohmic losses in the motor as well as the torque-ripple.

The performance of the dual-inverter system of the 4-level OEWIM drive with the proposed PWM schemes is assessed by using the loss calculation model, which was suggested in Reference 18. The switching power loss, conduction power loss and the total dual-inverter power loss (ie, sum of the switching and conduction power loss) are considered as the performance indices for the dual-inverter system. The power losses of the dual-inverter system for these SVPWMs are obtained, when the OEWIM is loaded at 20 N-m (ie, 80% of full load torque). The respective power loss plots are shown in Figure 21.

From Figure 21, it may observed that the switching power losses with all the PWM schemes are increasing monotonously with the increase in the modulation index in the range of lineal modulation (ie, up to the value of 0.866). This is due to the fact that, with the open-loop v/f control, the frequency of the fundamental component is increased as the modulation index increases. It may further be observed that, all of the power losses are lowered with the proposed hybrid SVPWM-1, when compared with the remaining two SVPWM techniques.

To assess the performance of the OEWIM drive, the total copper loss (sum of both stator and rotor) is calculated at various values of modulation indices, while the motor is loaded at 20 N-m in all of these cases. The per-unit (PU) total

copper loss is shown in Figure 22. While calculating the PU values, the copper loss incurred with the SVC-SVPWM at $m_a = 0.866$ is chosen as the base value (corresponding to the rated condition). From Figure 22, it may be observed that, the total copper loss is reduced with the proposed hybrid SVPWMs.

Figure 23 shows the torque ripple obtained with the SVC-SVPWM scheme vis-à-vis the proposed hybrid SVPWM schemes. The numerical values of the torque ripple are calculated based on the SD at no-load condition. As one might expect, the hybrid SVPWM-1 scheme performs better except in the modulation range of 0.33 to 0.42.

5 | CONCLUSION

In this article, two new SVPWM schemes are proposed for the dual-inverter fed 4-L OEWIM drive. These two PWM schemes result in a better harmonic performance in most of the operating speed range of the V/Hz controlled drive, while achieving the DC-capacitor voltage balancing.

The proposed SVPWM strategies achieve waveform symmetries and reduce the dv/dt across the motor phase windings, improving the longevity of the motor windings. One of the two SVPWM schemes (hybrid SVPWM-1) manages to clamp either inverter-1 or inverter-2 in every sampling time period. This results in the lowering of the switching power loss in the dual-inverter system. These PWM schemes also reduce the ohmic loss in the motor and the torque ripple, compared to the PWM schemes reported in earlier schemes.

DATA AVAILABILITY STATEMENT

The author elects to not share data.

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