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A cost-effective and fault-tolerant brushless direct current drive with open-stator windings for low power electric vehicles

Hema Kumar Patnana | **Somasekhar Veeramraju Tirumala**

Department of Electrical Engineering, National Institute of Technology Warangal, Warangal, India

Correspondence
Hema Kumar Patnana, Department of Electrical Engineering, National Institute of Technology, Warangal 506004, Telangana, India.
Email: hema1729@student.nitw.ac.in

Summary

Dual-inverter-driven open-end winding brushless direct current motor (OEWBLDCM) drives are amenable for the implementation of some interesting fault-tolerant features, which could find useful applications in low power electric vehicles (EVs). The power semiconductor switching devices in the dual-inverter system are vulnerable to the development of open-circuit faults (OCFs) and the short-circuit faults (SCFs). This paper investigates the possibility of imparting complete fault-tolerant capability to EVs, which employ OEWBLDC motors for propulsion. With the proposed dynamic post-fault reconfiguration of the power circuit and the reconnection of the battery banks, it is possible to deliver the rated (i.e., 100%) post-fault output power to the BLDC motor, despite the failure of a power semiconductor switching device (because of either an OCF or an SCF) in the dual-inverter system. The feasibility evaluation of the proposed fault-tolerant drive reveals that the aforementioned objectives are realizable at an affordable hike in the raw material cost of the propulsion system. Simulation studies and Experimental verification on a laboratory prototype validate the proposed fault-tolerant OEWBLDCM drive.

KEYWORDS

dynamic reconfiguration, electric vehicles, fault-tolerant, open-end winding BLDC motor

1 | INTRODUCTION

Dwindling reserves of conventional fossil fuels and their harmful impact on environment and ecosystems are the root causes for the exploration of alternative technologies for surface transportation. Apart from ruggedness, which arises from the minimum number of moving parts, electric vehicles (EVs) offer features such as quiet operation, higher efficiency, and ease of control.

Brushless direct current (BLDC) motors, which combine the advantages of both DC and alternating current (AC) motors, are poised to become the principal contenders for induction motors for EV applications in the foreseeable future. These advantages include (i) higher torque-to-volume ratio, (ii) higher efficiency, (iii) ease of control, and (iv) better dynamic response. Rapid strides made in the development of new technologies in batteries, fuel-cells, high energy capacity permanent magnets, and power semiconductor technologies also contribute to the endorsement of permanent magnet motors in the field of EVs.[1–4]

As in the case of any electrical system, fault tolerance is an important aspect in EVs. Power semiconductor switching devices are the weakest links in the propulsion systems of EVs. Statistical studies show that around 38% of the faults in the drive configurations are due to power switch failures, namely, open-circuit faults (OCFs) or short-circuit faults (SCFs).[5,6]

Ajaykumar and Patne[7] proposed a switched capacitor boost multilevel inverter configuration, which has OC fault tolerance of power switches. Similarly, Santosh Kumar et al.[8] proposed a fault tolerant multilevel inverter with modular structures, which exhibit the fault tolerant for OCF/SC faults in sources and OC fault in switches.

The research work reported by Rodriguez-Blanco et al.[9] describes a scheme to diagnose OCF/SC faults of the actuator switches based on the gate-to-emitter voltage behavior of the insulated gate bipolar transistor (IGBT) power device within 3 μs. However, this diagnostic method is applicable only for IGBT-based converters and requires auxiliary inductors.

The work reported in previous studies[10–12] presents various methods of OCF diagnosis for the traditional induction motor (IM) drives. The analyses of the pre-fault and post-fault operations for multilevel open-end winding IM drive topologies, which are capable of handling both OCF and SCF, are presented in the work.[13,14] However, in these publications,[13,14] the fault diagnosis algorithms have not been presented. The work reported in Yang et al.[15] presents the OCF diagnosis algorithm for a dual-inverter fed open-end winding IM drive. Gouichiche et al.[16] presents the fault-tolerant operation of IM drive against stator winding fault, broken bar fault and sensor failures.

However, these methods are not suitable for BLDC, owing to the trapezoidal nature of the back electromotive force (EMF). The research related to the fault-diagnosis and fault-tolerant operation of BLDC motor drives is still emerging and is gaining good attention. The available literature work is presented below:

The stator winding inter-turn fault diagnosis, based on the strategy of model current control, has been presented in the work.[17] The fault-tolerant control for the rotor-eccentricity faults in PM-BLDC motors has been suggested in the work.[18] In the research work reported in Mousmi et al.,[19] a combinational circuit has been proposed for BLDC motor drives to diagnose the faulty condition of any one of the three Hall sensors.

In the research work reported in Errabelli and Mutschler,[20] a single-switch OC (or) SC fault-tolerant drive topology for EV applications, which uses additional six TRIACs and one actuator leg, has been presented. However, this paper does not discuss the fault-diagnosis algorithms.

Open switch/phase fault-tolerant control strategies for multiphase open-end winding brushless DC motor drives (OEBLDCD), which are useful in applications such as EVs, military, manufacturing firms, and aerospace applications, are presented in the works.[21–23] These papers discuss various fault-tolerant control strategies and compensation methods for controlling the torque ripple during the open-switch/phase fault conditions.[21–23] Also, the work presented in Kim et al.[23] describes the fault-diagnosis procedure for the OCF in multiphase BLDC drive.

A fault-tolerant OEWBLDMD with a multiphase single-sided matrix converter has been proposed in Huang et al.,[24] which is capable of handling open circuited faults in the phase windings of the motor. However, in this work,[24] the pertinent fault-diagnosis algorithms are not provided. In the work,[25] an OC/SC fault-diagnosis algorithm based on pattern recognition of line-line voltages using discrete Fourier transform analysis for the in-wheel brushless DC motor used in EV applications is proposed.

In the circuit configuration presented by authors,[26] a procedure to diagnose an OCF is presented along with the fault-tolerant operation of the BLDC motor drive is given. The fault-tolerant operation is performed by connecting the faulted phase to the midpoint of the DC link using TRIAC (bidirectional) switches. However, the issues pertaining to the SCF have not been addressed in this publication.

The circuit topologies given in previous studies[27–29] employ a front-end buck converter along with the conventional two-level VSI, which feeds the BLDC motor drive for magnetically suspended control moment gyro (MSCMG) for aerospace applications. The diagnosis of OCF/SCF for the power devices constituting the inverter as well as the front-end buck converter is described in the work.[27] However, the scope of the work reported in Fang et al.[27] is confined to the process of fault diagnosis only.

A new fault-tolerant BLDC drive for MSCMG applications is presented in Li et al.[28] employs TRIACs as auxiliary switches. These TRIACs play a pivotal role in the circuit reconfiguration following the detection of either an OCF or an SCF in the power devices corresponding to the main power circuit. However, the proposed scheme of fault diagnosis by authors[28] does not address the diagnosis of faults occurring in the auxiliary switches (TRIACs).

A dual-inverter fed OEWBLDC motor drive for MSCMG applications with a single DC link is presented by the authors.[29] This drive is capable of handling both OC and SC faults, occurring in power devices. However, during post fault operation of the drive, double the rated current is made to flow through the motor windings in four modes (of a total of six modes) of operation.

Also, the fault diagnosis methods proposed by authors[27–29] are suitable only for the topology, wherein the back-end inverter (which feeds the motor) is powered by a front-end buck converter and are not suitable for the conventional two-level inverter fed BLDC drive applications.

In the work by Kumar et al.,[30] a dynamically reconfigurable dual-inverter fed OEWBLDC motor drive is proposed. The proposed drive configuration is capable of handling OCF/SC faults in any of the switching devices. However, after the occurrence of the fault and the subsequent post fault circuit reconfiguration, the power (hence speed) delivered by the motor is limited to half of its rated value. In addition, even a small disparity of terminal voltages of these two battery banks can momentarily establish an appreciable circulating current leading to stressing of the battery banks with the reconnection procedure employed.

This paper proposes a dual-inverter fed OEWBLDC drive for low power EVs, which displays an improvised fault tolerance with reasonable switch utilization and a marginal hike in the raw material cost (RMC). In this drive, open-ended stator windings of a BLDC motor are fed with two 2-level VSIs from either side. These two VSIs are powered by two individual isolated battery banks of equal voltages. It is shown that, with the aid of appropriate switchgear and the higher voltage ratings of the switching devices, it is possible to retain the full power (at rated voltage) delivering capability of the drive even under the faulty condition. This means that neither torque nor speed is compromised even in the faulted condition. Furthermore, this drive topology can handle the OCF as well as the SCF in any switching device belonging to the dual-inverter system.

This paper also presents a strategy to prevent a false positive assertion of OCF during dynamic operations of the drive.

When the dual-inverter system is healthy, each power device blocks only half of its rated voltage. This would improve the reliability of the drive, as the switching devices display a lesser propensity to fail.

The behavior of the OEWBLDC drive is first assessed with the aid of simulation studies. Experimental results, obtained with a laboratory prototype, validate the simulation results and prove the effectiveness of the proposed post-fault reconfiguration technique.

2 | PROPOSED FAULT-TOLERANT DRIVE CONFIGURATION

Figure 1A shows the proposed dual-inverter fed open-end winding brush less DC (OEWBLDC) motor drive configuration, which can tolerate the OCF/SC fault in any one of the switches in the dual inverters. This drive can provide fault tolerance for even three switching devices, so long as they all belong to either the top bank (i.e., connected to the positive terminal of the DC source) or the bottom bank (i.e., connected to the negative terminal of the DC source).

The two VSIs are fed with two respective isolated DC supplies (batteries "B1" and "B2"). Each battery is of voltage ($U_{DC}/2$), where U_{DC} denotes the rated voltage needed to power the conventional BLDC drive (wherein the motor windings are star connected). Each side of the open-ended motor is connected to its respective battery bank through DPDT relays (DPDT-1, DPDT-2, DPDT-3, and DPDT-4) and actuators as shown in Figure 1A. The nomenclature of various components and terminals of the power circuit are as follows: Terminals of motor phase windings "A, B, and C" are (a, a′, b, b′, and c,c′); Inverter-1 (shortly INV-1); Inverter-2 (INV-2); positive terminals of respective DC links of inverters: P1 (for INV-1); P2 (for INV-2); negative terminals of respective DC links of inverters: N1 (for INV-1); N2 (for INV-2); location of switching devices: upper banks of inverters (H); lower banks of inverters (L); power switch identification numbers for INV-1: (1-6); for INV-2: (1′-6′); positive and negative terminals of the DC source B1:S1 and S2; B2:S3 and S4.

The gating signals for the inverters are determined by the position of the rotor, which is sensed by the Hall-effect sensors. The back EMFs developed in the motor phases and the corresponding gating signals of dual-inverter configuration are shown in Figure 2. Similar to the conventional brushless DC motor drive, there exist six sectors of operation (represented as Sector-1 to Sector-6). From Figure 1A, it may be noted that, the two DC supplies (each of voltage $U_{DC}/2$) are connected to the dual-inverter configuration using four DPDT relays. Under normal conditions, the controlling coils of these DPDT relays are not energized; they are energized only under emergency (i.e., fault) situations. Hence, their poles are connected to the "normally closed" (NC) terminals. These relays may also be replaced with "routing" TRIACs as in the work reported in previous studies.[26,28] However, in such a scenario, these TRIACs would be prone to the OCF/SC faults for which there is no fall back.

Figure 1B shows the basic operating principle of the proposed drive configuration. Under healthy condition, both inverters are active and feed the OEWBLDC motor from either side. Whenever a fault occurs (either an OCF or an SCF), the faulty inverter, through an appropriate switching action, provides a switched neutral point at the faulty end.

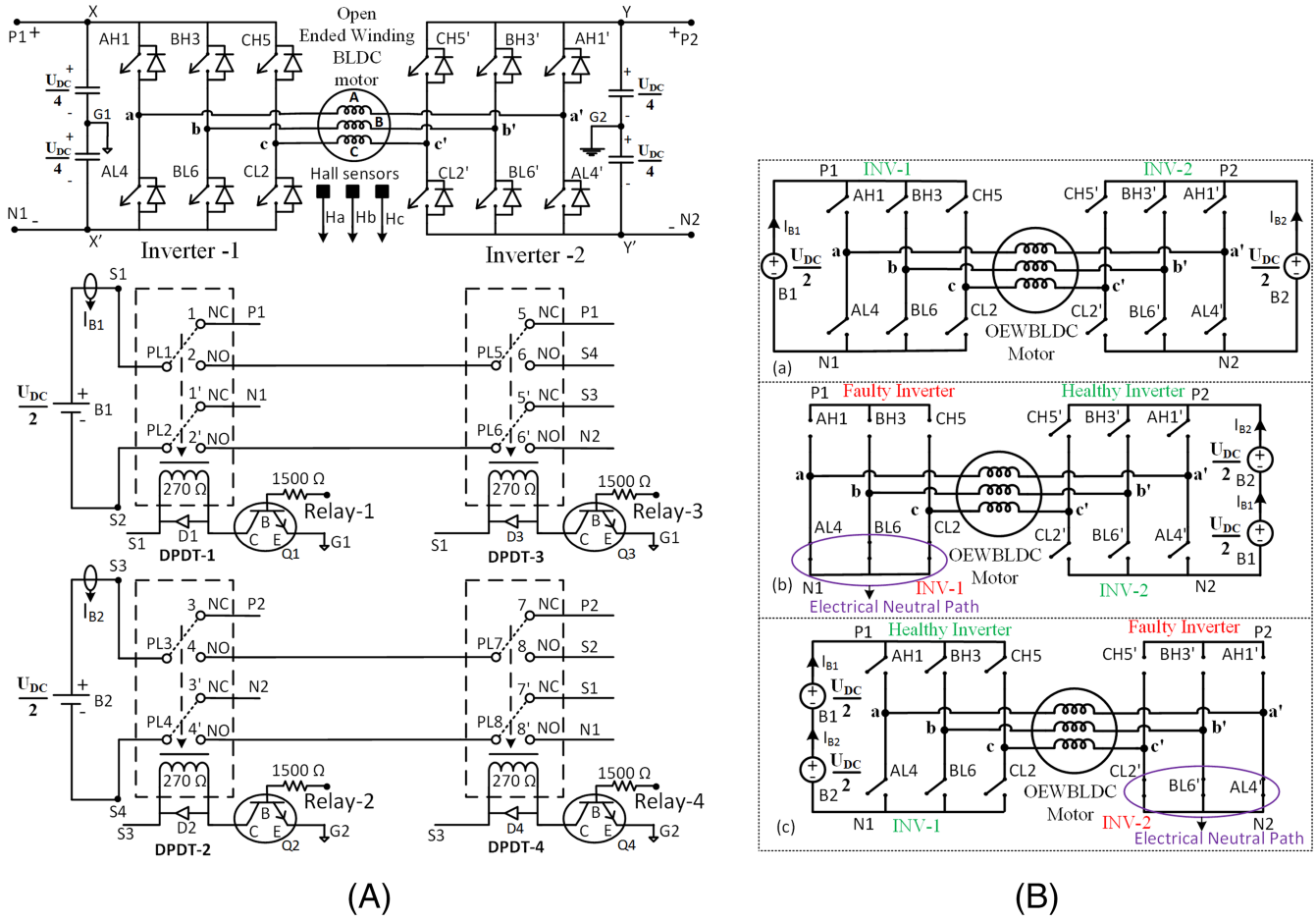
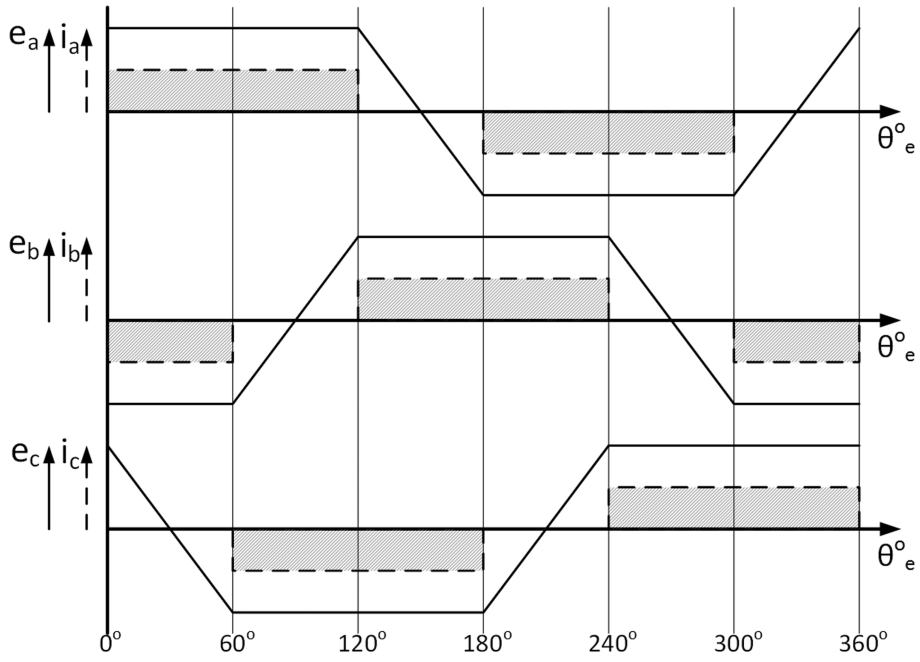


FIGURE 1 (A) Circuit topology of fault-tolerant OEWBLDC motor drive. (B) Equivalent topological configuration for (a) steady state operation, (b) OC fault in anyone of the upper switches of INV-1/SC fault in anyone of the bottom switches of INV-1, and (c) OC fault in anyone of the upper switches of INV-2/SC fault in anyone of the bottom switches of INV-2

The healthy inverter, which is now solely operative, is constrained to power the motor. Thus, to be able to supply the rated power to the motor during the post-fault operation, the following conditions must be satisfied: (i) The battery banks supplying the respective VSIs must be connected in series, so that the rated voltage can be applied to the motor, and (ii) the power semiconductor switching devices of both VSIs should be capable of blocking the total voltage (U_{DC}), which is the sum of the voltages of the battery banks B1 and B2 (i.e., twice the voltage of B1 or B2).

Figure 3A,B represents the equivalent circuit diagram of the OEWBLDC drive during Sector-1 and Sector-2 operation, when the drive is healthy. From Figure 3A,B, it is evident that the two DC supplies are connected in series and aid each other, even though they are electrically isolated and feed individual VSIs. Figures 3C,D and 3E,F present the post-fault equivalent circuit of the drive when INV-1 and INV-2 develops fault (OCF/SCF), respectively. Figure 3A–F also provides the details regarding the actual electrical connections after the process of reconfiguration. As an example, the contents within the closed parenthesis in Figure 3E (S1, PL1, 2, PL5, 5, P1) indicates the connection sequence from positive terminal of the battery bank "B1" (i.e., S1) to the positive terminal of DC link of INV-1 (i.e., P1).

After diagnosing the OCF/SCF in either INV-1/INV-2, the following reconfiguration procedure is initiated: (i) If an OCF occurs in any one of the INV-1 (INV-2) upper-bank switching devices, the three lower-bank switches of INV-1 (INV-2) are turned on continuously to create a switched-neutral through N1 (N2) (Figures 1B and 3 and Table 1). This switching action would reconfigure the OEWBLDC drive into the conventional drive, wherein the windings are connected in star and the motor is powered through INV-2 (INV-1). (ii) If an SCF occurs in one of the lower bank devices of INV-1 (INV-2), the remaining two lower bank switches of it are also turned on continuously to create a switched neutral point through N1 (N2) (Figure 1B). The motor is now driven exclusively through INV-2 (INV-1) to achieve the required fault-tolerant operation.



Sector	Sector-1	Sector-2	Sector-3	Sector-4	Sector-5	Sector-6
INV-1	AH1,BL6	AH1,CL2	BH3,CL2	BH3,AL4	CH5,AL4	CH5,BL6
INV-2	AL4',BH3'	AL4',CH5'	BL6',CH5'	BL6',AH1'	CL2',AH1'	CL2',BH3'

FIGURE 2 Switching logic for inverters along with the waveforms of motor back-EMF and phase current

However, this partial reconfiguration isolates the healthy battery bank, which is located on the side of the faulty inverter, from the rest of the system and renders it unusable. In order to make a better use of the healthy battery bank, an improvised reconnection procedure is employed in this manuscript, wherein the healthy battery bank of the faulty inverter is connected *in series* to its counterpart by turning on the appropriate DPDT relays.

Figures 3C,D and 3E,F, respectively, represent the equivalent circuits and connection sequence of the drive when OCF/SCF are diagnosed in INV-1 (INV-2) and the subsequent reconfiguration when the drive goes through the regions of Sector-1 and Sector-2. From these diagrams, it can be noticed that the two battery banks are connected in series and aid each other, while driving the motor. Thus, the drive may be operated with full rated power and torque even under the faulty condition, as rated motor voltage can be applied to the motor.

Table 1 presents the strategy of energizing the DPDT relays (Relay-1 to Relay-4, Figure 1A) during the "normal" and the "faulty" modes of operation. As an example, after the fault (OCF/SCF) diagnosis and corresponding reconfiguration procedure for the fault in INV-1, in order to utilize the healthy battery connected to the faulty inverter, the control windings of the DPDT relays Relay-1, Relay-2, and Relay-3 are energized, so that their poles are connected to the normally-open (NO) terminals. (Refer to Table 1 and Figure 1A.) It may be noted that, with this maneuver, the batteries are connected in series (aiding each other), powering the drive solely with INV-2 (Figures 1B and 3C,D). Thus, the proposed OEWBLDC drive achieves the fault-tolerant operation with the ability to deliver the rated power and the rated torque.

3 | FAULT DIAGNOSIS AND CONTROL

3.1 | Open circuit fault diagnosis algorithm and control

The work by authors[30] proposes an algorithm that is suitable to diagnose the OCF for an OEWBLDC drive. However, this algorithm shows a tendency for false positive detection during dynamic operations of the drive. This shortcoming is addressed in this manuscript and an improvised algorithm to diagnose the OCF is proposed in this paper.

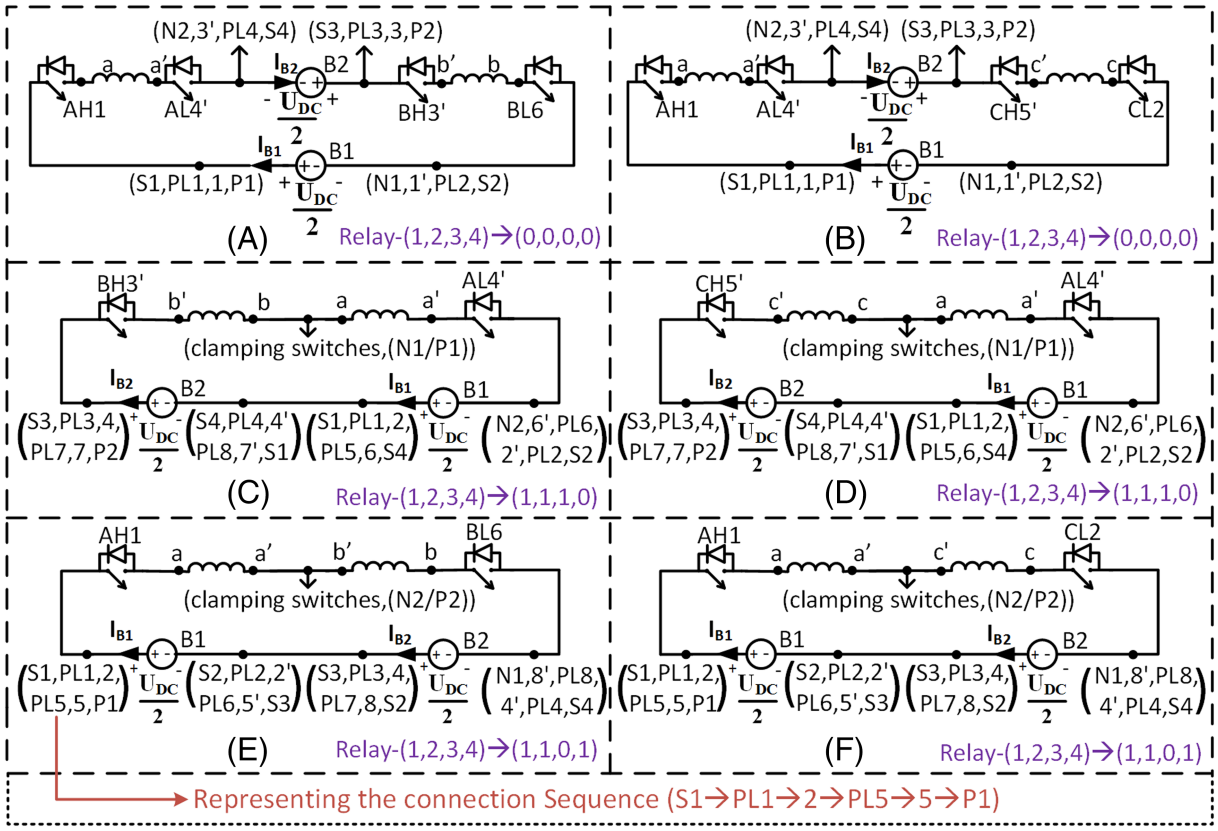


FIGURE 3 Equivalent circuit diagram of the OEWBLDC motor drive during (A) Sector-1, steady state operation; (B) Sector-2, steady operation; (C) Sector-1, INV-1 faulty condition (OCF/SCF); (D) Sector-2, INV-1 faulty condition (OCF/SCF); (E) Sector-1, INV-2 faulty condition (OCF/SCF); and (F) Sector-2, INV-2 faulty condition (OCF/SCF)

TABLE 1 Relay energizing signals, corresponding flag values, and terminal reconnections during steady and faulty operations

Drive operation	DPDT relay signals (Relay-1, Relay-2, Relay-3, and Relay-4)	Electrical neutral path, flags "INVF," and ROCFD	Battery terminals connection (S1, S2, S3, and S4)	Effective DC link voltage
Steady operation	(0, 0, 0, 0)	OEWBLDC; INVF = 0; ROCFD = 0	(P1, N1, P2, and N2)	U_{DC}
INV-1 (OCF/SCF)	(1, 1, 1, 0)	(P1 or N1); INVF = 0; ROCFD = 1	(S4, N2, P2, and S1)	U_{DC}
INV-2 (OCF/SCF)	(1, 1, 0, 1)	(P2 or N2); INVF = 1; ROCFD = 1	(P1, S3, S2, and N1)	U_{DC}

The OCF proposed in Kumar et al.[30] is briefly outlined as follows:

1. In order to detect the OCF, two Hall CTs are required to sense the respective DC link currents of the two VSIs. The algorithm is based on the observation that if any single device develops an OCF, it would miss conduction during those modes of operation, which need the conduction of the faulty device. The DC link current would therefore be discontinuous, which constitutes the main symptom of OCF.
2. Since two VSIs are in action, it will not be possible to ascertain as to which is the source of OCF in an open-winding configuration (as two devices are in series in any conducting phase). Thus, it is always assumed that the OCF occurs in INV-1 by default.
3. With that assumption, a switched neutral point is formed with the supposed healthy bank of INV-1.

4. If the discontinuity in the DC link current of the supposedly healthy inverter (i.e., INV-2) vanishes, then it means that the default assumption regarding the location of fault in INV-1 is correct and the post-fault circuit reconfiguration is retained.
5. On the other hand, if the discontinuity in the DC link current of INV-2 still persists, then it is obvious that the assumption regarding the location of the OCF (that it exists in INV-1) is wrong, and it is asserted that it has indeed occurred in INV-2.
6. This leads to the step of undoing the reconfiguration affected earlier. The dual-inverter system is again reconfigured, this time correctly, wherein the switched neutral point is formed with the devices situated on the healthy bank of INV-2.
7. The limitation of this algorithm is that the OCF diagnosis is reliable during the steady operating conditions.

In the process of diagnosing the OCF, some flags are employed to store essential information. These flags are examined by the fault diagnosing algorithms from time to time to assert the occurrence of fault. Also, these flags play a crucial role in determining inverter reconfiguration and battery re-connection. These flags are listed as follows: (a) The flag "OCFSEC" (with initial 0 value) stores the sector number at which the OCF is first affirmed; (b) the flags "$Flag_{d1}$" & "$Flag_{d2}$" (with initial 0 value) are set to unity when the OC fault is affirmed during the current sector of operation and the subsequent sector of operation respectively; (c) the flag "OCSWF" (with 0 initialization) is loaded with the switch number of the diagnosed OCF switch (which is taken as pilot fault affirmation in this algorithm); (d) the flag "INVF" set to unity (after a safe time of "Tchkinv" after the reliable OCF diagnosis)for the faulty actuator of "INV-2," otherwise it remains to its initial 0 when the initial assumption of fault in "INV-1" is true.

The simulation results carried out using MATLAB/SIMULINK platform with machine parameters given in Table 3 are used in the following sections to facilitate a clear visualization of fault diagnosis and circuit reconfiguration. Figure 4 presents the simulation results for the OCF in switch AH1 (i.e., INV-1). Figures 5–7, which are the zoomed versions of Figure 4, at Instants "t_a" and "tc," provide the finer details of the diagnostic process for the OCF. Figure 8 represents the fault diagnosis for the OC fault in switch AL4′ (i.e., INV-2).

The aforementioned diagnostic process is limited to steady operating conditions and displays a propensity to raise a false positive fault affirmation, particularly during dynamic operations of the drive. This could lead to an unnecessary post-fault circuit reconfiguration, defeating the very purpose of providing fault tolerance to the drive. In order to avoid this false fault-diagnosis, an improvised algorithm is presented in this paper. This improvisation is described in detail in the following paragraphs.

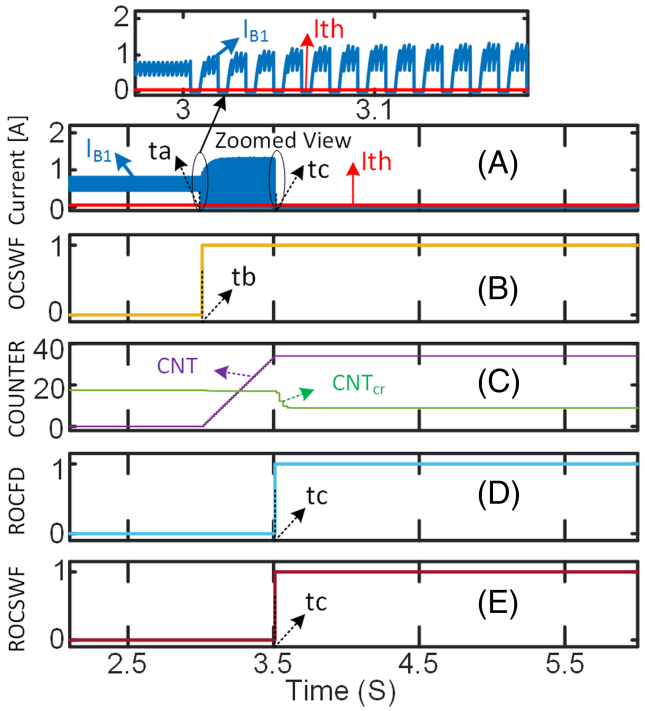


FIGURE 4 Simulation results showing OC fault in switch AH1 of INV-1: (A) I_{B1}, Ith (B) OCSWF (C) Counter, (D) ROCFD, and (E) ROCSWF

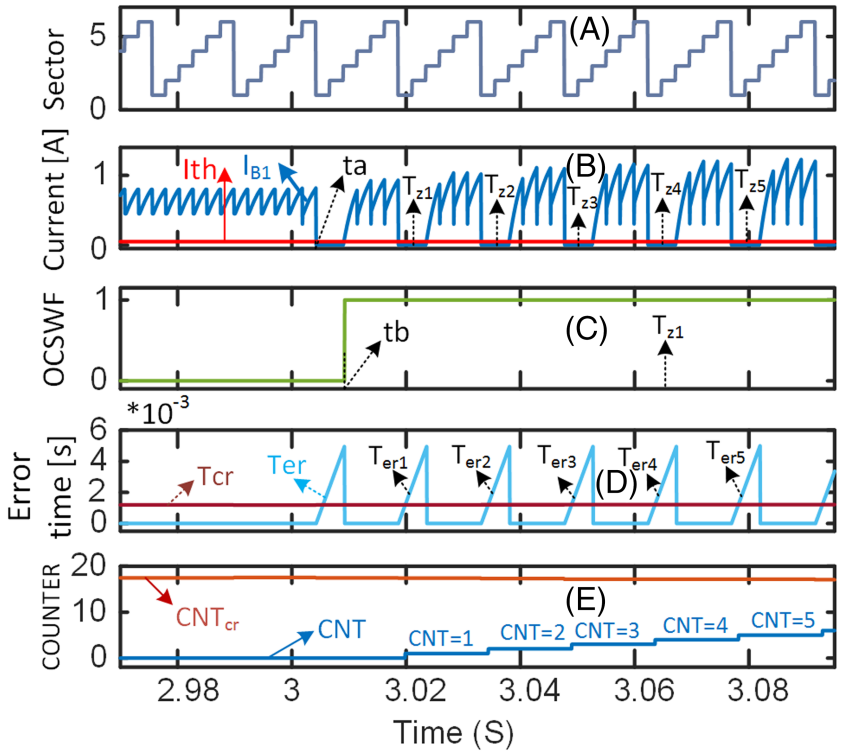


FIGURE 5 Simulation results showing OC fault in switch AH1 of INV-1 (detailed fault diagnosis at instant "ta" of Figure 4): (A) operating sector, (B) I_{B1}, I_{th}, (C) OCSWF, (D) Ter, Tcr, and (E) counter

Following a disturbance, the DC link current could show a temporary drop. Thereafter, it would quickly regain the steady state condition and shows the normal behavior, wherein all the six modes of conduction are present. However, this is not the case with OCF, wherein a failure of one switching device would lead to the presence of only four modes of conduction (out of six modes). This would lead to a periodic disruption of the DC link current (see periodic oscillations during time "tc-ta," see in Figure 4). The improvisation proposed in this paper is based on this subtle observation. The following procedure is adopted to circumvent this problem:

With the OC fault initiated in the switch "AH1" (i.e., at Instant "ta," see in Figure 4A, 5B, and 6A), the corresponding flags "OCFSEC" (i.e., at Instant "ta1," see in Figure 6D), "Flagd1" (i.e., at Instant "ta1," see in Figure 6C), and "Flagd2" (i.e., at Instant "ta2," see in Figure 6F) are loaded with the diagnostic information. Based on these flags information, the flag "OCSWF" (from Table 2) is loaded with the faulty switch number during pilot-fault affirmation stage (i.e., with "1" at Instant "tb," see in Figures 4B and 5C).

After the pilot-fault affirmation stage, in order to assert the occurrence of the OCF conclusively, the probation period of the fault is extended by a time period of "Trechk." If the occurrence of OCF is real, the DC link current drops below a threshold value "I_{th}" in "two" sectors out of total "six" sectors (see Figure 2) in every electrical cycle of operation (see zoomed portion of Figures 4A, 5B, and 7A) during this "Trechk" time ("Trechk = tc-tb"). These zero transitions of DC link current in every electrical are denoted as "T_{z1}," "T_{z2}," ... , "$T_{z(n-1)}$," "T_{zn}" (see Figures 5B and 7A). The corresponding error time periods "T_{er1}," "T_{er2}," ... , "$T_{er(n-1)}$," "T_{ern}" (see Figures 5D and 7B) for which these zero transitions (T_{z1}, T_{z2}, ... ,$T_{z(n-1)}$, T_{zn}) exist are calculated. The error time period "$T_{erx}(i)$" is an integrator, which is accumulated (see Equation 1) with the same rate at which the current is sampled. In the present work, a sampling time (T_s) of 70 μs is employed to sense the DC link currents:

$$\begin{cases} I_{B1} < I_{th}\,(T_{erx}(i) = T_{erx}(i-1) + T_s) \text{ for } T_{zx}(\mathrm{i}), \\ I_{B1} \geq I_{th} \quad \text{steady condition and } T_{erx}(i) = 0 \end{cases} \tag{1}$$

$$I_{th} = G_f * I_r \tag{2}$$

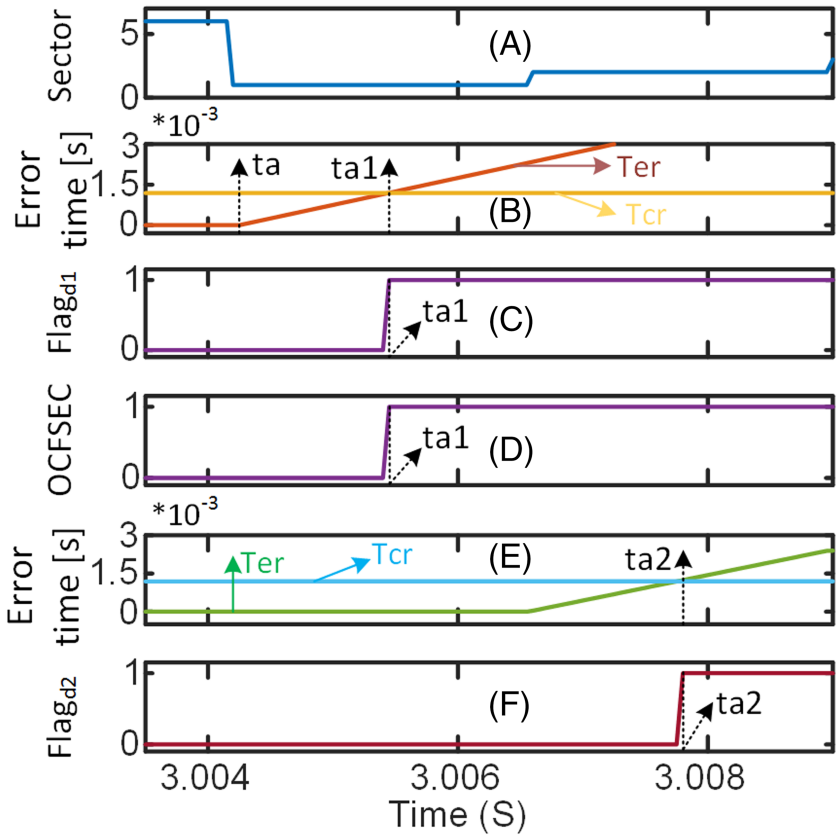


FIGURE 6 Simulation results showing flags statuses for OCF in switch AH1 of INV-1 (detailed fault diagnosis at instant "ta" of Figure 4): (A) operating sector, (B) Ter, Tcr (Sector-1), (C) Flag_{d1}, (D) OCFSEC, (E) Ter, Tcr (Sector-2), and (F) Flag_{d2}

where $x = 1, 2, \ldots, n$; "I_r" is the reference current, which is the output of current controller (Figure 10); "G_f" is the safety factor (0.5 taken in this paper); $T_{erx}(-1) = 0$.

An error-up-counter "CNT" (with an initial value of 0) is triggered at "tb," which starts counting (within the probation time period) whenever the zero transitions of DC link current "I_{B1}" ($Tz1$, $Tz2$, ... ,$Tz(n-1)$, $Tz(n)$, see Figures 5A and 7B) are identified and existed more than the critical-fault-time "Tcr." When the number of these zero transitions (stored in "CNT") are above a critical value, denoted by "CNT_{cr}" (which is determined by the speed of the motor), the OCF is conclusively affirmed.

The critical fault time (denoted as "Tcr") is determined by the dwell-time period corresponding to two sectors (i.e., 120 electrical degrees, see Figure 2). It depends on the speed of the motor and is calculated based on the set of relationships presented below:

The relation between angular velocity in mechanical radians "ω_{mech}" and angular velocity in electrical radians "ω_{elec}" is given by the following:

$$\omega_{mech} = \frac{2}{P}\omega_{elec}, \tag{3}$$

where "P" denotes the number of poles. The electrical frequency "f_{elec}" and electrical time cycle "t_{elec}" are given as follows:

$$f_{elec} = \frac{\omega_{elec}}{2 * \pi} \tag{4}$$

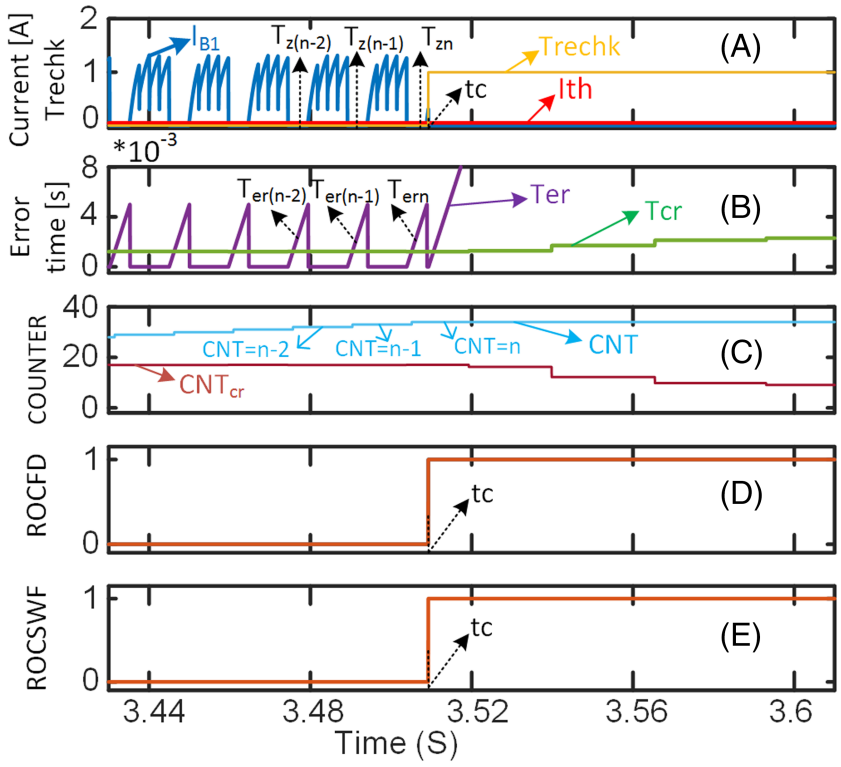


FIGURE 7 Simulation results showing OC fault in switch AH1 of INV-1 (detailed fault diagnosis at instant "tc" of Figure 4): (A) I_{B1}, I_{th}, Trechk, (B) Ter, Tcr, (C) counter, (D) ROCFD, and (E) ROCSWF

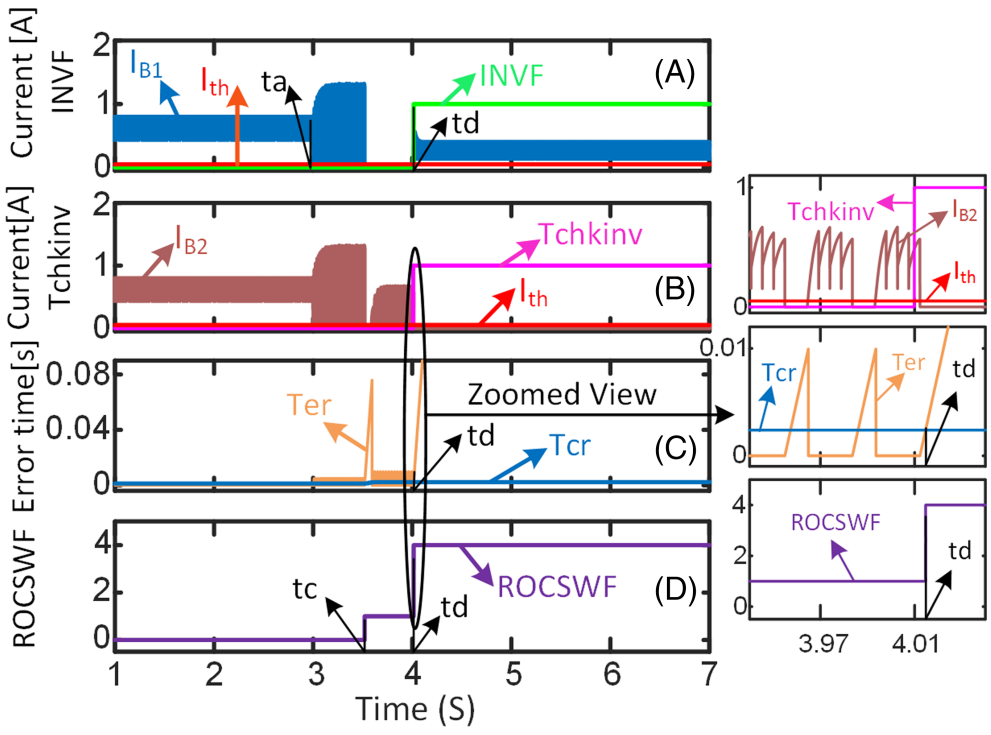


FIGURE 8 Simulation results showing OC fault in switch AL4′ of INV-2: (A) I_{B1}, I_{th}, INVF, (B) I_{B2}, I_{th}, Tchkinv, (C) Ter, Tcr, and (D) ROCSWF (left side: normal view, right side: zoomed-view of the portion encircled)

$$t_{elec} = \frac{1}{f_{elec}} \tag{5}$$

As one electric cycle is divided in to six sectors of operation, the dwell time for each sector (i.e., "Tsector") is given by the following:

$$T_{sector} = \frac{t_{elec}}{6} \tag{6}$$

Frome Equations (4)–(6),

$$T_{sector} = \frac{4 * \pi}{P * \omega_{mech} * 6}. \tag{7}$$

As two sectors are out of conduction in an electrical cycle for an OCF, the time period for two sectors in given by "2*Tsector."

The critical fault time period "Tcr" is given as follows:

$$T_{cr} = Ksf * 2 * T_{sector} \tag{8}$$

$$T_{cr} = \frac{Ksf * 8 * \pi}{P * \omega_{mech} * 6} \tag{9}$$

where "*Ksf*" denotes the factor of sensitivity ($0 < Ksf < 1$), which is a design parameter. In the present work, a value of 0.6 is chosen for "*Ksf*."

The critical count value "CNT_{cr}" depends on the electrical time cycle "t_{elec}" of the drive and the probation time period employed for re-check (i.e., "Trechk"). The electrical time cycle "t_{elec}" in turn depends on the running speed of the drive "ω_{mech}."

The number of electrical time cycles "CNT_{rechk}" within the time "Trechk" is given as follows:

$$CNT_{rechk} = \frac{T_{rechk}}{t_{elec}} = \frac{T_{rechk} * p * \omega_{mech}}{4 * \pi} \tag{10}$$

The critical count value "CNT_{cr}" is given by the following:

$$CNT_{cr} = D_{sf} * CNT_{rechk} \tag{11}$$

$$CNT_{cr} = D_{sf} * \frac{T_{rechk}}{t_{elec}} = D_{sf} * \frac{T_{rechk} * p * \omega_{mech}}{4\pi} \tag{12}$$

where "*Dsf*" denotes the factor of safety ($0 < Dsf < 1$), which is a design parameter. In this present work, a value of 0.5 is chosen for "*Dsf*."

If the value accumulated in the error-up-counter "CNT" is greater than the critical count value "CNT_{cr}" at the end of the time period "Trechk" (at Instant "tc," see Figures 4A,C and 7C), the flag "ROCFD" (re-affirmed OC fault detection) is set to a value of "1" (at Instant "tc," see Figures 4D and 7D). If the flag "ROCFD" is set to "1," it is finally admitted as a genuine fault.

$$\begin{cases} \text{ROCFD} = 1; & \text{if } (\text{CNT} > \text{CNT}_{\text{cr}}) \\ \text{ROCFD} = 0; & \text{Otherwise} \end{cases} \tag{13}$$

TABLE 2 Open-circuit-fault diagnosis information

(Flagd1,Flagd2,OCFSEC)	INVF	OCSWF	Clamping switches (ROCFD = 1)
(1,1,1) or (1,0,2)	0	AH1	AL4,BL6,CL2
	1	AL4′	AH1′,BH3′,CH5′
(1,1,3) or (1,0,4)	0	BH3	AL4,BL6,CL2
	1	BL6′	AH1′,BH3′,CH5′
(1,1,5) or (1,0,6)	0	CH5	AL4,BL6,CL2
	1	CL2′	AH1′,BH3′,CH5′
(1,1,4) or (1,0,5)	0	AL4	AH1,BH3,CH5
	1	AH1′	AL4′,BL6′,CL2′
(1,1,6) or (1,0,1)	0	BL6	AH1,BH3,CH5
	1	BH3′	AL4′,BL6′,CL2′
(1,1,2) or (1,0,3)	0	CL2	AH1,BH3,CH5
	1	CH5′	AL4′,BL6′,CL2′

At this point of time, another flag, named as re-affirmed OCF switch number flag "ROCSWF" (at Instant "tc," see Figures 4E and 7E) is made to store the product of the contents of the flags "OCSWF" and "ROCFD."

$$\mathrm{ROCSWF} = \mathrm{OCSWF} * \mathrm{ROCFD} \tag{14}$$

The information contained in "ROCSWF" would subsequently determine the process of post-fault circuit reconfiguration.

If the value accumulated in the error counter "CNT" is less than the critical count value "$\mathrm{CNT_{cr}}$" at the end of the time period "Trechk," then it is concluded that the OC fault is false diagnosed. The content of the flag "ROCFD" is verified to arrive at this conclusion. ROCFD would contain "0" after the backup test for the false diagnosis of the OC fault. Hence, all of the flags associated with the OCF (viz., "$\mathrm{Flag_{d1}}$," "$\mathrm{Flag_{d2}}$," "OCFSEC," "OCSWF," and "CNT") are reset to "0" again. This maneuver would reset the fault detecting system, which is now ready to probe a new OCF. The decision regarding the reconfiguration of the power circuit is also based on the status of this flag (ROCFD). Circuit reconfiguration is affected only when this flag is set to "1."

Figure 8 represents the diagnosis procedure for the OCF in switch AL4′ of INV-2 (i.e., at Instant "ta," see Figure 8A). With the initial assumption of OC fault in INV-1, the switch number of AH1 (which is in series with AL4′, see Figure 3A,B) is stored in the flag "ROCSWF" (at Instant "tc," see Figure 8D). As the initial assumption of fault in INV-1 is false, the periodic transitions in the current are now correctly attributed to the development of OCF in INV-2. Subsequently, the flags "INVF" is set to "1," and "ROCSWF" is loaded with the number corresponding to the actual switch (AL4′ in this case) in which the OCF has occurred (at the Instant "td," see Figure 8D) after a safe time period of "Tinvchk."

Table 2 summarizes the possible OC failure in all the switches of the dual inverter configuration and also the corresponding clamping switches information required for the reconfiguration procedure based on the flags "$\mathrm{Flag_{d1}}$," "$\mathrm{Flag_{d2}}$," "OCFSEC," "INVF," and "ROCFD."

As mentioned in Section 2, after creating a switched neutral point with the remaining healthy devices belonging to the faulty inverter, the two battery banks B_1 and B_2 are connected in series. As one may expect, the flags "INVF" and "ROCFD" play a pivotal role in energizing the required set of relays. Table 1 presents the relationship between the flags ("INVF" and "ROCFD") and the relays that are energized. To ensure safety, an appropriate time-delay ("Tdrelay") is provided between the events of creating the switched neutral point and energizing the relays. Depending upon the requirement, these relays can also be triggered manually (Figures 9 and 10).

Figure 9 represents the overall flowchart representation of diagnosis, reconfiguration, and reconnection strategies required for the fault-tolerant operation. The performance of the proposed diagnosis algorithms is experimentally verified with both open-loop and closed-loop operation of the drive. The closed-loop operation of the drive is based on the classical structure, wherein the outer speed loop specifies the reference for the inner current loop. Figure 10 presents the overall control scheme, including the generation of the gating signals needed for the switching devices of the dual-inverter scheme for both healthy and faulty conditions.

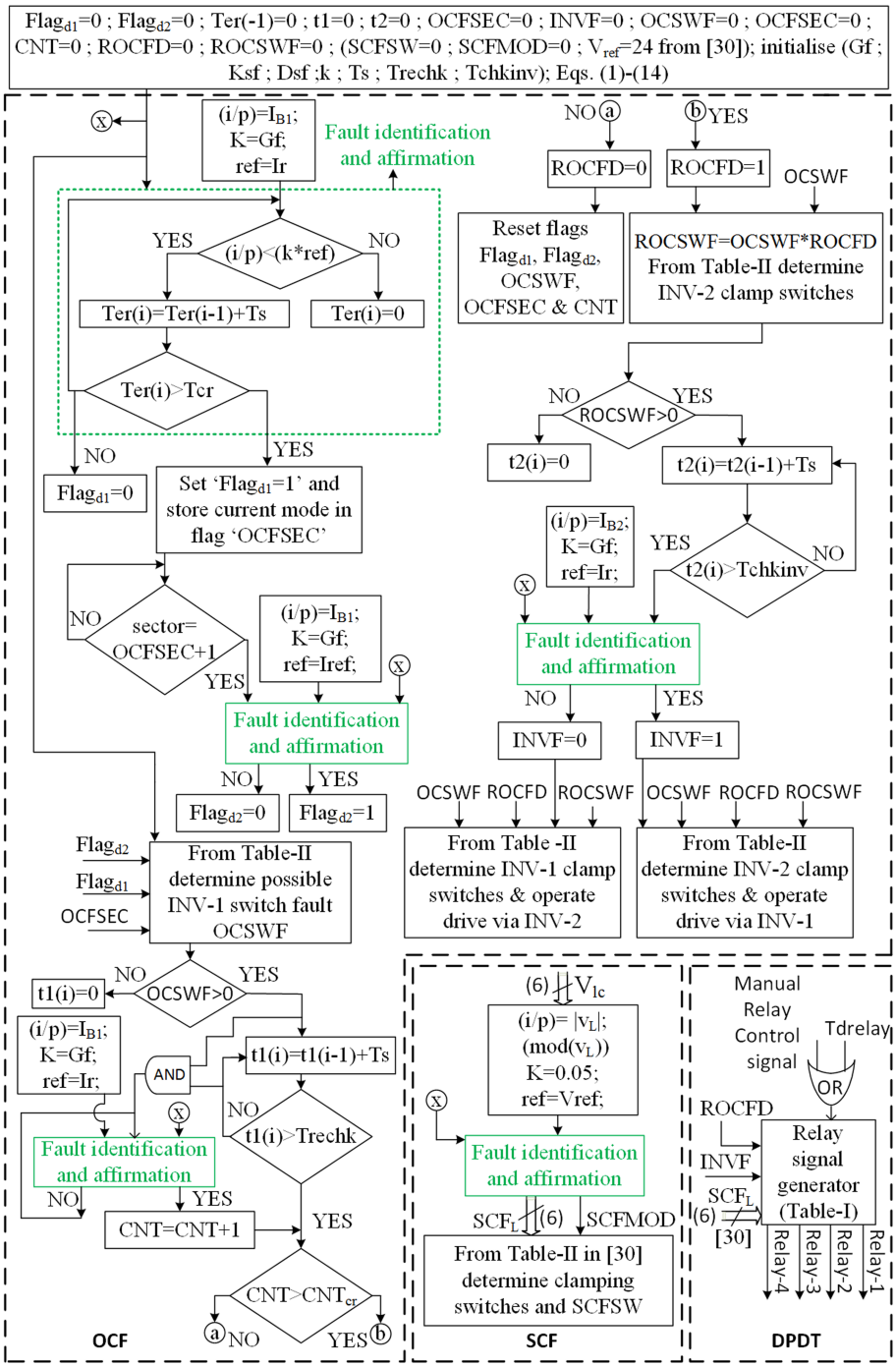


FIGURE 9 Flowchart presenting the overall fault-tolerant operation during fault conditions

3.2 | Short circuit fault diagnosis algorithm and control

In general, Hall current sensors are employed to sense currents on any electric motor drive system. However, it would be an expensive proposition to employ six Hall current sensors to sense individual currents flowing through the switching devices. To make the design cost-effective, low-cost analog voltage sensors (based on the ISO-124 device) have been employed without losing bandwidth and isolation. The technique of diagnosing the SCF is based on the periodic sensing of all of the six line-line voltages, which appear across the six terminals of an open-stator winding motor. This technique is based on the observation that, for any given phase-leg of a BLDC motor, there exists an interval of 60°

(electrical) between turning off the top switch of a given phase leg and turning on the bottom one. This technique, which is essentially anticipatory in nature, manages to prevent the over-currents associated with the shoot-through of the two devices (one of which develops the SCF) belonging to a given phase leg, before its occurrence.[30] With the proposed topology and the reconfiguration procedure (inverter reconfiguration and battery reconnection) mentioned in Section 2, the drive is capable of delivering full rated power (speed) and torque for the SCF occurrence in either of the dual-inverter configuration.

4 | RESULTS AND DISCUSSION

The prototype developed for the experimental studies for the proposed OEWBLDC motor drive is shown in Figure 11. The dSPACE-1104 control platform is used for the experimental validation. The machine parameters used for simulation and hardware prototype are presented in Table 3.

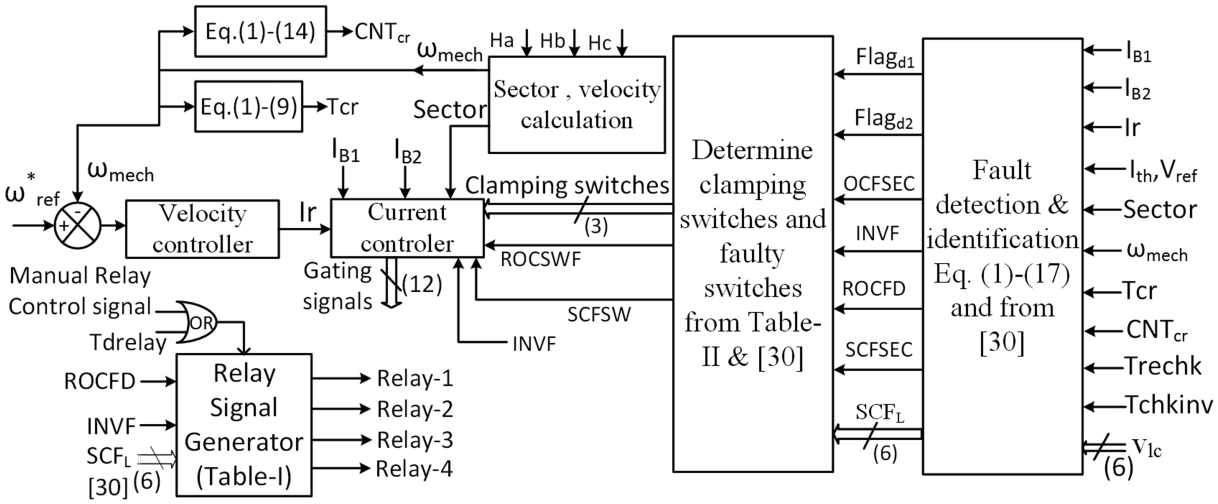


FIGURE 10 Overall control scheme under healthy and faulty operations

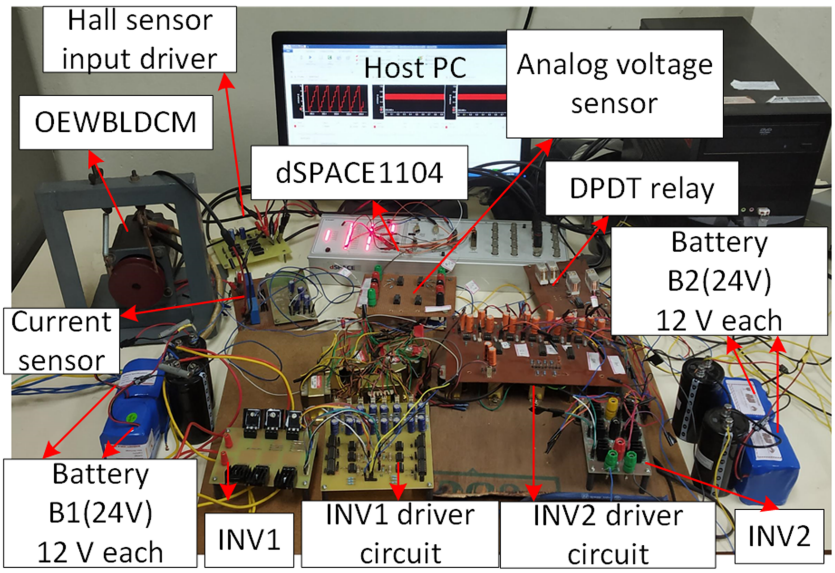


FIGURE 11 Experimental set-up of the proposed OEWBLDCM drive with fault tolerance

For experimentation, the OC fault condition is enforced by withdrawing the gate pulse of the corresponding switch continuously. Similarly, the SCF is affected by the continuous gating of the targeted device.

The diagnosis of OCF in INV-1 and INV-2 is validated by considering the switches CH5 and CL2′, respectively. The capability of the proposed fault diagnosis algorithms and the post-fault circuit reconfiguration strategy are demonstrated experimentally in terms of achieving the rated post-fault power and speed in both open-loop and closed-loop drive operation.

First, it is intended to demonstrate that the diagnostic algorithm proposed in Kumar et al.[30] displays a tendency to misjudge the occurrence of the OCF. As the present focus is only on the assessment of the merit of the fault diagnosis, the steps of post-fault circuit reconfiguration and reconnection are not carried out (for experimental results presented in Figures 12 and 13), even after the (spurious) false affirmation. The act of decreasing the speed command suddenly (at instant "tm," Figure 12) results in a sudden dip in the DC link currents of both VSIs. It may be noted that these DC link currents momentarily fall below the threshold levels (at Instant "ta," Figure 12) for a time period, greater than the critical time period "Tcr." With no further check as in Kumar et al.,[30] the algorithm raises a false affirmation of the OCF (at Instant "tb," Figure 12). In contrast, with the diagnosis algorithm presented in this paper, such a false fault diagnosis is avoided as shown in Figure 13 (as indicated by the status of the flags ROCFD, ROCSWF in Figure 13). Consequently, the drive continues to operate as an open-end winding drive. As all the relevant flags are reset to "0," the fault detecting system is now ready to probe a new OCF.

TABLE 3 Parameters of the OEWBLDC machine

Voltage (rated)	**48 V**	**B1 = 24 V** **B2 = 24 V**
Torque (rated)	0.6 N m	
Speed (rated)	3200 RPM	
Resistance (per phase)	0.295 Ω	
Back EMF constant	11.8 V/KRPM	
Power (rated)	250 W	
Number of pole pairs	4	

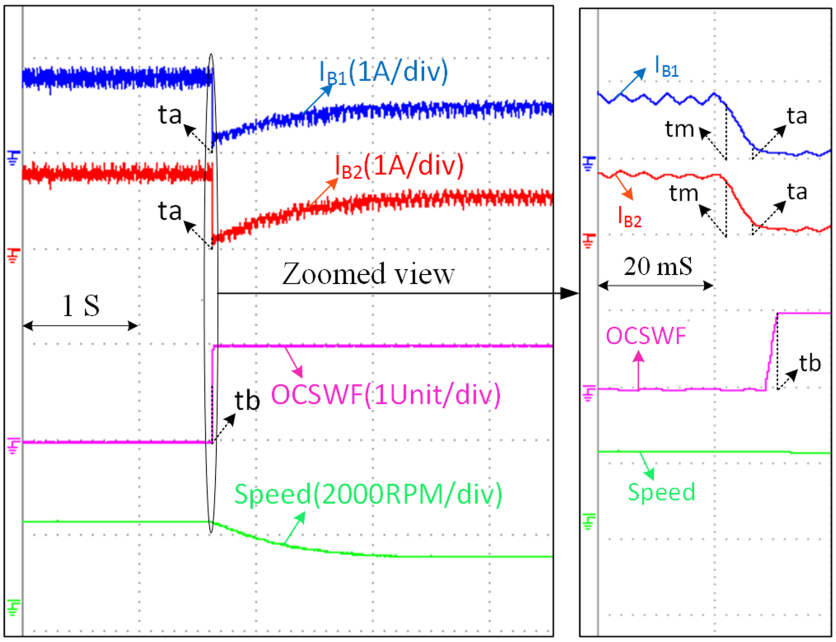


FIGURE 12 Experimental results showing false fault diagnosis of OCF during the speed dynamics for the work reported in Kumar et al.[30] (left side: normal view, right side: zoomed-view of the portion encircled)

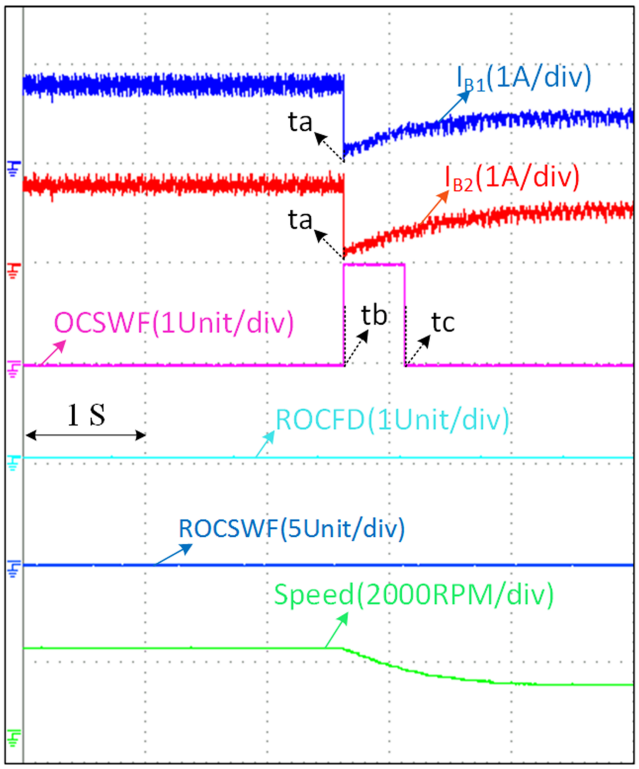


FIGURE 13 Experimental results showing reliable OC fault diagnosis during the speed dynamics with the presented diagnosis algorithm

Figure 14A,B shows the process of diagnosing the OC fault occurring in a switching device belonging to INV-1 under open-loop drive operation. Whenever an OCF occurs in the switch CH5 of INV-1 (at Instant "tf," Figure 14A), the DC link currents of both of the VSIs drop below the threshold value (at the Instant "ta," Figures 14A and 15). Subsequently, the internal flags "Flagd1," "OCFSEC," and "Flagd2" (at the Instants "ta1," "ta1," and "ta2," see Figure 14A) are loaded with values (1, 5, and 1). Depending on the values of these flags, the switch, in which the OCF has occurred, is identified, and the corresponding number is loaded into the flag "OCSWF" (i.e., OCSWF = 5 at Instant "tb," shown in Figures 14A and 15). Completion of these activities marks the end of the "pilot sensing" of the fault.

The confirmation of OCF is based on the multiple zero transitions (Figures 14A,B and 15) counted during the probationary time period "Trechk." It may be noted from Figure 15 that, when the probing counter "CNT" accumulates a higher value than the critical count "CNT_{cr}" (see CNT and CNTcr of Figure 14B), the flags "ROCFD" and "ROCSWF" (Equation 14) are, respectively, set to "1" and "5" (at the Instant "tc," Figure 15). This action confirms the occurrence of the OCF, which triggers the reconfiguration of the faulted inverter as indicated in Figures 1B and 3. Consequently, the current of the battery "B1" (i.e., "I_{B1}") drops down to 0, and the motor is now exclusively powered by the battery "B2" through INV-2, causing a decrease in the speed of the motor (Figure 15).

Figure 16 shows the fault diagnosis and the dynamic behavior of the drive (operated in open loop), when the OCF occurs in INV-2 (i.e., switch CL2′). As the algorithm for the diagnosis of OCF initially assumes that the fault occurs in INV-1, the diagnosis procedure determines the faulty switch as "CH5," belonging to INV-1. This is indicated by the fact that the flag "ROCSWF" showing a value of "5" at the Instant "tc" in Figure 16. Consequently, the reconfiguration process is initiated, and the motor is powered exclusively through INV-2. The fault diagnosis algorithm now notices that, despite this reconfiguration, the periodic discontinuity in the current I_{B2} does not vanish. It obviously means that, contrary to the initial assumption, INV-2 has developed the fault. Hence, the flag "ROCSWF" is overwritten with a value of "2" (at the Instant "td," Figure 16), indicating that the switch CL2′ (belonging to INV-2) has indeed developed the OCF. Thereafter, the switched neutral point is created with the switches AH1′, BH3′, and CH5′ belonging to INV-2, and the motor is powered exclusively through INV-1, employing the battery B1 (Figure 3E,F).

From Figures 15 and 16, it may be noted that the speed of the motor is reduced after the post-fault reconfiguration. This is due to the fact that only one battery is now operative, with a voltage of $U_{DC}/2$, and the drive is running in open loop.

The experimental results pertaining to the closed-loop operation are shown in Figures 17 and 18. In the first experiment (see Figure 17), the reference speed is set at 1500 RPM, which is less than half of the rated speed of the BLDC

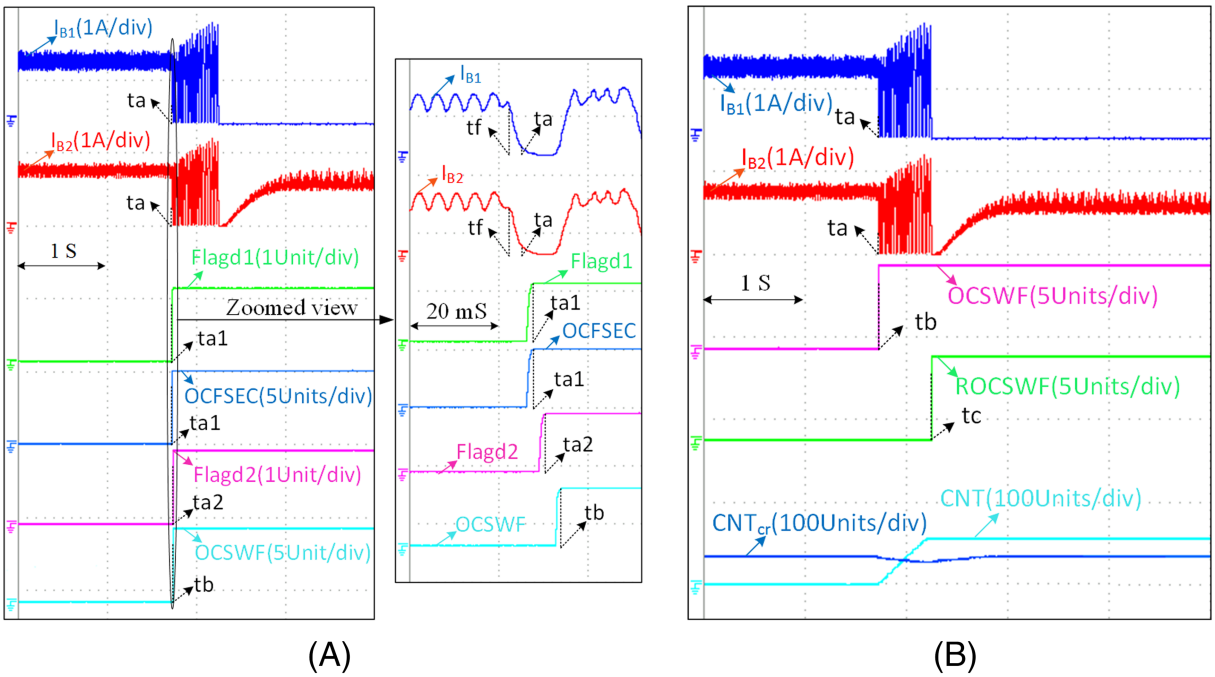
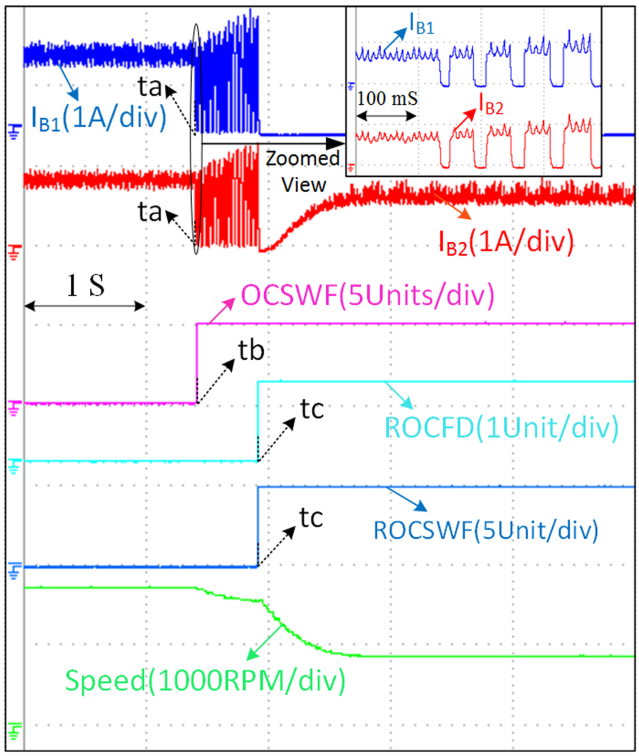


FIGURE 14 (A) Experimental results showing the flag statuses during OC fault in INV-1 (i.e., switch CH5) (left side: normal view, right side: zoomed-view of the portion encircled). (B) Experimental results showing the counter and flag statuses during OC fault in INV-1 (i.e., switch CH5)

FIGURE 15 Experimental results showing the fault diagnosis and reconfiguration for the OC fault in INV-1 (i.e., switch CH5) under open-loop operation without battery reconnection



motor. When an OCF occurs in INV-1, the motor is fed exclusively through Inverter-2. It should be noted that the speed is restored back to the reference value (see Figure 17), even without the battery ("B1") reconnection (i.e., Tdrelay = 0 in Figure 17), This is due to the fact that the regulated speed is below half of the rated value of the motor, and it can be regulated even without the aid of the battery "B1."

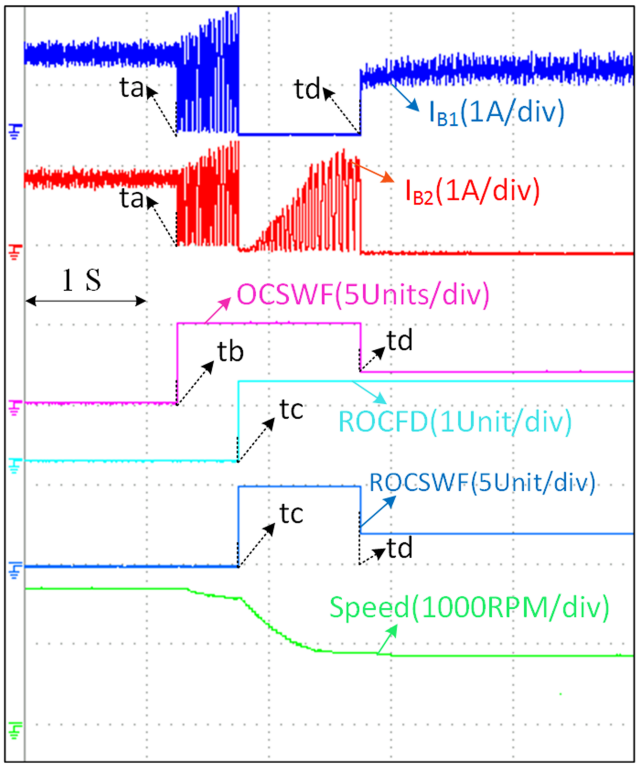


FIGURE 16 Experimental results showing the fault diagnosis and reconfiguration for the OC fault in INV-2 (i.e., switch CL2′) under open-loop operation without battery reconnection

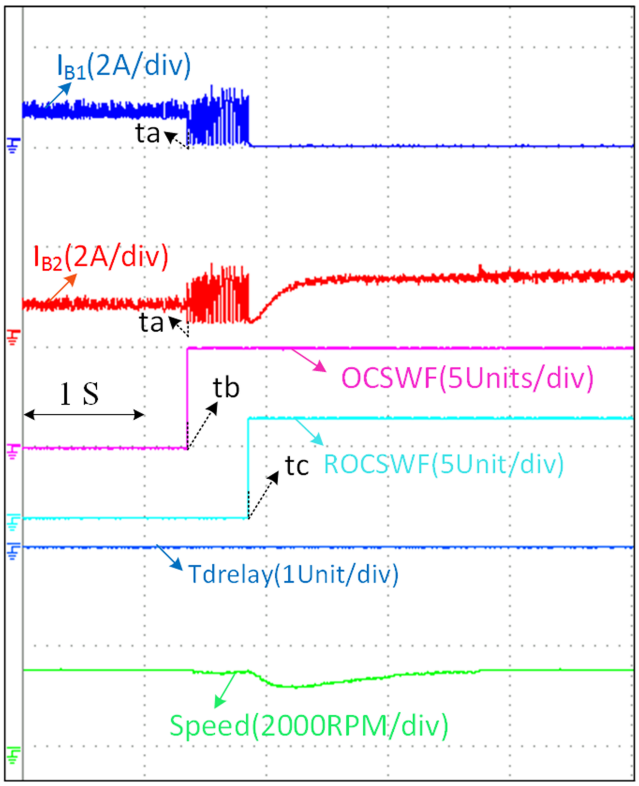


FIGURE 17 Experimental results showing the fault diagnosis and reconfiguration for the OC fault in INV-1 (i.e., switch CH5) under closed-loop drive operation (below half the rated speed) without battery reconnection

In contrast, when the reference speed is higher than half of the rated value (i.e., 2800 RPM, Figure 18), to regulate the speed, it would be mandatory to reconnect the healthy battery ("B1" in the present case) to aid the battery, which is already present in the post-fault circuit ("B2" in the present case). Hence, from the experimental result (Figure 18), it can be noted that with the inverter reconfiguration alone (without battery reconnection [i.e., Tdrelay = 0 in Figure 18]), the speed of the motor cannot reach its reference value, which is above half of the rated speed.

Figure 19 presents the effectiveness of the post-fault reconnection of the batteries (Tdrelay = 1 at Instant "tr," Figure 19) in series for the open-loop drive operation. In contrast to the results presented in Figures 15 and 16 (wherein the healthy battery corresponding to the faulty inverter is not connected), it may be noted that the speed of the motor is restored back, even after the occurrence of the OCF in INV-1 under open-loop drive operation. But if the source

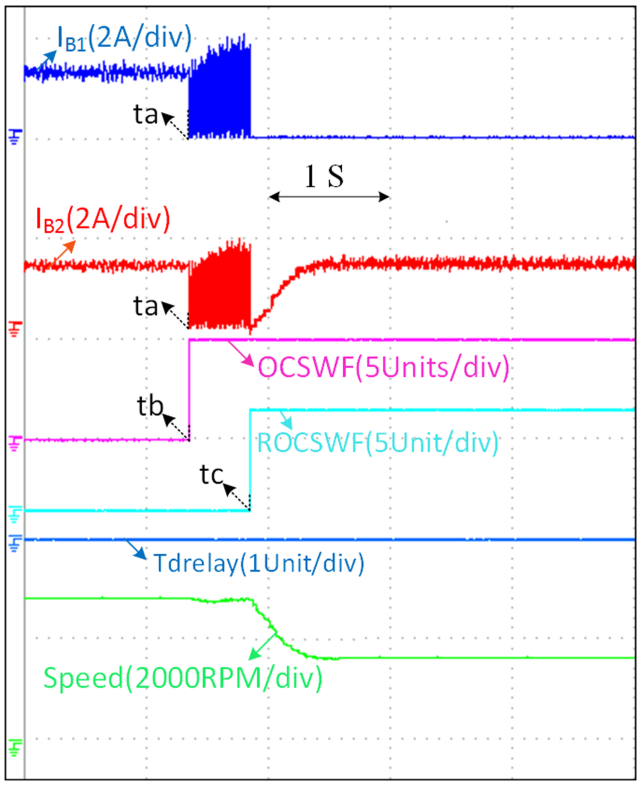


FIGURE 18 Experimental results showing the fault diagnosis and reconfiguration for the OC fault in INV-1 (i.e., switch CH5) under closed-loop drive operation (above half the rated speed) without battery reconnection

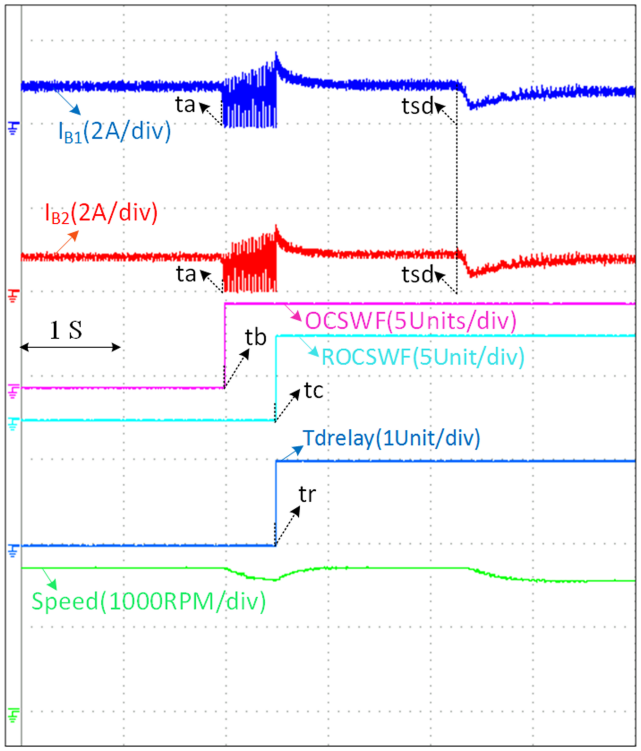


FIGURE 19 Fault tolerance (diagnosis and control) of the drive configuration for the OC fault in INV-1 (i.e., switch CH5) under open-loop drive operation

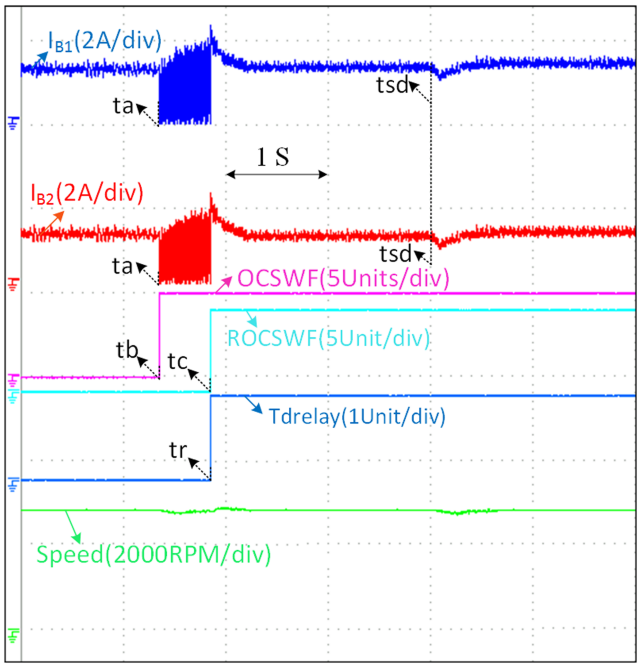


FIGURE 20 Fault tolerance (diagnosis and control) of the drive configuration for the OC fault in INV-1 (i.e., switch CH5) under closed-loop drive operation (above half the rated speed)

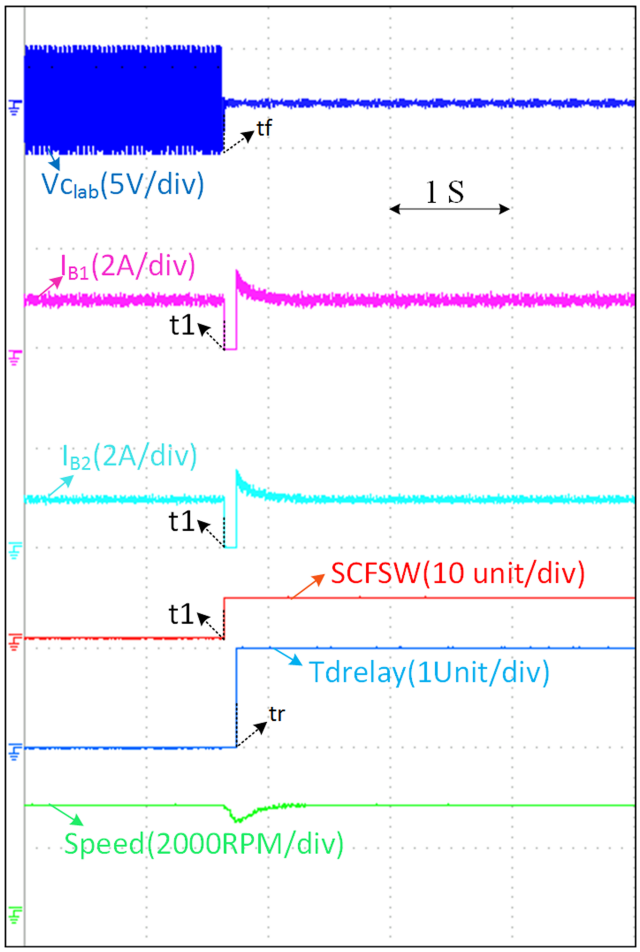


FIGURE 21 Fault tolerance of the drive configuration for the SC fault in INV-1 (i.e., switch AL4) under open-loop drive operation

TABLE 4 Comparison of the existed topologies with the topology proposed

Features of the drive topology	Kim et al.[23]	Park et al.[26]	Li et al.[28]	Feng et al.[29]	Kumar et al.[30]	Proposed topology
1. No. of switching device in inverter	Four switches/phase (multiphase H-bridge topology)	Six switches (conventional) + 3-TRIACs	Six switches (Conventional) + 6-TRIACs +1-additional leg (2-switches)	12 switches	12 switches	12 switches
2. Rating of the motor	Designed for the rated voltage and current	Designed for the rated voltage and current	Designed for the rated voltage and current	Designed for double the rated current	Designed for the rated voltage and current	Designed for the rated voltage and current
3. Auxiliary components	No	No	Buck-converter + 3-switches + 1-fault protective leg	Buck-converter + 1-SPDT switch+1-fault protective leg	Two DPDT relays	Four DPDT relays
4. Fault tolerance	(OCF and SCF)	(Only-OCF)	(OCF and SCF)	(OCF and SCF)	(OCF and SCF)	(OCF and SCF)
5. Fault diagnosis	(Only-OCF)	(Only-OCF)	(OCF and SCF)	(OCF and SCF)	(OCF and SCF)	(OCF and SCF)
6. Fault diagnosis in the inverter extra-switches	No	No	No	Yes	Yes	Yes
7. Fault mitigation time in terms of sector time periods	OCF (two sectors) SCF—not implemented	OCF (two sectors) SCF—not implemented	OCF/SCF-Inv (one sector) OCF-buck (three sectors) SCF-buck (one sector)	OCF/SCF-Inv (one sector) OCF-buck (three sectors) SCF-buck (one sector)	OCF (two sectors) SCF (one sector)	OCF (two sectors) SCF (one sector)
8.Post fault circulating current problem	No	No	No	No	Yes (causes batteries overheating)	No
9. Post fault power delivered	Depends on no. of open switch/phase faults	Rated power	Rated power	Rated power	Half the rated power	Rated power
10. Post fault speed of operation	Depends on no. of open switch/phase faults	Rated speed	Rated speed	Rated speed	Half the rated speed	Rated speed
11. Suitability of fault diagnosis for EV applications	Yes	Yes	No	No	Yes	Yes

TABLE 5 Cost analysis of the topologies in Indian (Rs.)

Equipment name		Unit cost (Rs./−)	No. of products	Total cost (Rs./−)
[a] Motor [3 KW 96 V, BLDC motor]		31,781	1	31,781
[b] Lithium-ion battery cost (12 V, 60 AH,720 WH)		13,620	8	1,08,960
[c] Inverter cost with driver [Switch safety factor for Current and voltage taken as 2]	[c_a] Inverter topology in Kumar et al.[30]	[64 + 306]	12	4440
	[c_b] Present Inverter topology	[159 + 306]	12	5580
	[c_c] Traditional Inverter Topology	[159 + 306]	6	2790
[d] Sensors	[d_a] Current sensor	1872	2	3744
	[d_b] Analog voltage sensor for SC fault,[30] [TL084CN and ISO124]	[894 + 13]	ISO 124-6 TL084CN-2	5390
[e] Auxiliary equipment's [DPDT relays]	[e_a]Topology[30]	806	2	1612
	[e_b] Present Topology	806	4	3224
Percentage of additional cost incurred for topology[30] with respect to the conventional BLDC motor drive: $= \left[\frac{d_b+e_a+[c_a-c_c]}{a+b+c_c+d_a}\right] * 100\% = \left[\frac{5390+1612+[4440-2790]}{31,781+108,960+2790+3744}\right] * 100\% = 5.87\%$				
Percentage of additional cost incurred for present topology with respect to the conventional BLDC motor drive: $= \left[\frac{d_b+e_b+[c_b-c_c]}{a+b+c_c+d_a}\right] * 100\% = \left[\frac{5390+3224+[5580-2790]}{31,781+108,960+2790+3744}\right] * 100\% = 7.74\%$				

disturbance applied at Instance "tsd," the speed falls down to a new operating value due to the open-loop operation of the motor.

The performance of the drive system with closed-loop control with the battery reconnection (Tdrelay = 1 at Instant "tr," Figure 20) is demonstrated in Figure 20. In this experiment, the drive is operated with a speed, which is more than half of the rated speed of the motor (2800 RPM). It is important to note that, in contrast to the magnitude of the motor speed shown in Figure 18 (i.e., with inverter reconfiguration alone), the pre-fault speed and power are achieved with the aid of the proposed method of reconnecting the batteries in series. Compared to the open-loop experimental result presented in Figure 19, the drive is capable of regulating the speed against the supply disturbance applied at Instant "tsd." This demonstrates the general capability of the drive for fault-tolerant operation, even though the speed control (with speed loop) is not generally required in EV applications.

The fault-tolerant performance of the proposed OEWBLDC drive is also assessed against the SCF, when it is operated in open loop (shown in Figure 21). For this purpose, an SCF is created by continuously gating the device "AL4," belonging to INV-1. With the proposed post-fault reconfiguration strategy (applied at Instant "tr," Figure 21), it is possible to retain the full power delivering capability, which is not the case for the post-fault re-configuration mentioned in Kumar et al.[30]

Thus, the proposed post-fault reconfiguration achieves 100% fault tolerance, for both OCF and SCF (i.e., without compromising on the power rating). Admittedly, this feature could be realized because of the selection of the voltage ratings of the switching devices, which are rated for a voltage of "U_{dc}," compared to the rating of "$U_{dc}/2$," employed in the work proposed in Kumar et al.[30] It would be an interesting proposition to assess as to what would be the increase in the RMC to implement this feature compared to the work presented in Kumar et al.[30] (given in Section 5).

5 | FEASIBILITY ANALYSIS OF THE PROPOSED ELECTRIC DRIVE TOPOLOGY

Table 4 presents the comparison of the proposed fault tolerant topology and the corresponding fault diagnosis algorithm vis-à-vis the fault tolerant topologies and fault diagnosis algorithms, which have been reported in earlier literature. The comparative analysis reveals that the presented fault tolerant topology along with the corresponding fault diagnosis algorithms are capable of (i) handling both OCF and SCF in any of the inverter switches and (ii) delivering rated power (hence rated speed) and rated torque even after the occurrence of the fault, which are essential for an EV.

It is shown in Kumar et al.[30] that the fault-tolerant OEWBLDC drive proposed in Kumar et al.[30] requires about 6% more RMC compared to the conventional BLDC drive, considering only the propulsion system of the EV. A similar assessment is undertaken in this section, while evaluating the economic viability of the proposed OEWBLDC drive vis-à-vis the one proposed in Kumar et al.[30] In this evaluation, summarized in Table 5, the cost of automobile body, chassis, supervisory controllers, and additional accessories, which are common to the traditional and the fault-tolerant drive topologies, is not included.

It may be noted from Table 5 that the hike in the RMC to achieve 100% post-fault output power (against OCF as well as SCF) is a meagre 2%, compared to the drive proposed in Kumar et al.[30] Considering that the fault-tolerant drive proposed in Kumar et al.[30] delivers only 50% of the rated power in the post-fault conditions, it appears that the OEWBLDC motor drive proposed in this work appears to be financially viable. Furthermore, the percentage increase in the RMC would be further swamped when the additional costs due to the chassis, body, accessories, and aesthetics are considered.

6 | CONCLUSION

This paper proposes a dual-inverter fed dynamically reconfigurable OEWBLDCM drive. The post-fault reconfiguration depends on the type of the fault developed in any given semi-conductor switching device present in the dual-inverter system. The post-fault reconfiguration of the power circuit and the reconnection of the batteries in series ensure that the BLDC motor is supplied with its rated power even after the development of either an OCF or an SCF in the dual-inverter system. Even though such an agreeable situation arises due to the doubling of the voltage rating of the switching devices by a factor of "2," it would be still be an affordable proposition for low power EVs, as the total increase in the RMC (of only the propulsion system) is only about 8% compared to the conventional BLDC drive, which does not offer the feature of fault tolerance. Compared to the previously proposed OEWBLDC drive, which achieves only 50% post-fault power delivery to the motor, the hike in the RMC is only 2% with the proposed power circuit configuration, considering the costs of individual components on the basis of bulk purchase. Besides this, the process of affirming the OCF, which is susceptible to false diagnosis, is further improvised in this manuscript.

DATA AVAILABILITY STATEMENT

The data that supports the findings of this study are available within the article and also in appropriate references.

ORCID

Hema Kumar Patnana https://orcid.org/0000-0002-3411-1847

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