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An improved quasi Z-source based H5 inverter with low leakage current for photovoltaic applications

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Abstract

Grid-connected Single-Stage Boost Inverters (SSBI) are extensively being researched in the area of photovoltaic energy conversion systems. Owing to their single-stage boosting capability, this class of power converters results in higher efficiency and reliability. This power circuit configuration is constituted by two mutually dependent sub-converters, in that a front-end quasi-Z-source (qZS) part is integrated to a back-end multilevel inverter (MLI). The MLI provides the shoot-through state to the qZS, while the qZS provides the pulsating DC input to the MLI. In general, solar photovoltaic inverters suffer from the disadvantage of leakage current that flows from solar panels to the grid/load. This paper introduces a dual quasi-Z-source based multilevel inverter, which achieves the following benefits: (a) five-level output voltage, (b) reactive power capability, (c) shoot-through immunity, (d) continuous input current, and (e) reduced leakage current based on VDE 0126-1-1 standards. In this paper, a modified modulation scheme, which is based on the employment of phase-disposed and level-shifted carrier signals, has been used to reduce the leakage current. To reduce the leakage current further, a passive filter is employed to eliminate high frequency variations across the parasitic capacitance. The working principle of the proposed power converter and the effectiveness of the modulation scheme have been validated with simulation studies in both standalone and the grid-connected mode. Finally, the simulation studies are verified through an experimental prototype of 500 W rating.

KEYWORDS

common mode voltage, leakage current, multilevel inverter, quasi Z-source, shoot-though

LIST OF SYMBOLS AND ABBREVIATIONS: V_{IN}, input voltage; V_{DC}, boosted DC link voltage; V_O, output voltage; D_S, shoot through duty cycle; m, modulation index; V_{C1}, voltage across capacitor 1; V_{C2}, voltage across capacitor 2; V_{CMV}, common mode voltage; V_{CPAR}, voltage across parasitic capacitance; i_{LEAK}, leakage current; B, boost factor; i_{L1}, current through inductor 1; P_O, output power; k_{C1}, ripple across capacitor 1; k_{C2}, ripple across capacitor 2; k_L, ripple through inductor current; $\hat{V}_{DC}$, peak DC link voltage; L, inductor; C, capacitor; C_f, filter capacitor; L_f, filter inductor; CMV, common mode voltage; DPGS, distributed power generation systems; HFT, high frequency transformer; LST, lower shoot through; MLI, Multilevel inverter; MPPT, maximum power point tracking; PV, Photovoltaic; qZS, Quasi Z source; qZS-MLI, quasi-Z source based multilevel inverters; RES, renewable energy sources; SSBI, single-stage boost inverter; TBV, total blocking voltage; UST, upper shoot through; ZS, Z-source.

1 | INTRODUCTION

Environmental degradation, which is caused by an extensive use of fossil fuels, continues to motivate researchers to pursue methods of producing clean electric power. Of the available renewable energy sources (RES), solar photovoltaic (PV) systems are deemed suitable for both large-scale as well as distributed power generation systems (DPGS).[1] PV systems can be operated either in the standalone mode or in the grid-connected mode based on the requirements of DPGS. In either case, they require a power conditioning circuit to process the power based on the load/ utility grid adhering to proper standards.[2]

Solar PV systems, which are integrated into the grid with isolation transformers have lower leakage currents and the absence of dc current injection. The transformer that interconnects the grid and the source can be placed either on the ac-side or on the dc-side. Placing an isolation transformer on the ac-side would invite disadvantages such as: increased cost, increased volume, and reduced efficiency. This shortcoming may be addressed by designing a system, which places a high frequency transformer (HFT) on the dc-side. Even though PV systems with dc-side HFTs achieve lower volumes, they still demand improvements in the aspects of efficiency and cost.[3]

Thus, this situation encourages pushing research towards the development of a transformerless PV system, which aims to reduce the size, cost, and leakage current while improving efficiency.

In a transformerless PV power converter, the leakage current (which is also called as the common-mode current) is produced due to the time-varying nature of the common-mode voltage (CMV). Fluctuations in CMV cause a corresponding variation in the voltage across the parasitic PV capacitance (which is denoted by the symbol "u") and the value of the resulting common-mode current (or leakage current) is directly proportional to the rate of change of voltage across this parasitic capacitor. The leakage current flows in the resonant path formed by the interaction of various circuit components such as the decoupling capacitors, grid filters, and parasitic capacitances of PV panels.

Thus, it is evident that the leakage current can be suppressed by clamping the CMV and avoiding high du/dt across the parasitic capacitance. The other benefits obtained by the suppression of leakage current are: (a) improved efficiency, (b) increased life expectancy of PV panels, (c) high operational security, and (d) high grid current quality.[4]

Considerable research work has been carried out in the area of transformerless PV systems for single-phase systems. Several new circuit topologies and modulation schemes have been explored to suppress leakage current.[5-7] Most attractive amongst the power converter topologies are: H5,[8] H6,[9] HERIC[10] and their improved versions, which reduce the leakage current by isolating the source and the grid.[11] These inverters require an intermediate dc-dc power conversion stage, which serves two purposes: (a) boosting the input voltage to the required level and (b) to implement maximum power point tracking (MPPT). However, such a two-stage system results in lower efficiency and increased cost, as the boosting stage requires additional power devices, control, and drive circuitry. This motivates researchers to explore the possibilities to design a *single-stage system*, which is capable of: (a) boosting the input PV voltage to the desired level (b) achieve MPPT, and (c) inverting dc power into ac power.[11]

A Z-source inverter[12] acts as a Single-stage Boost Inverter (SSBI) that performs boosting and inverting in a single stage. A Z-source (ZS) is an impedance network, which is constituted by the combination of inductors and capacitors. The conventional Z-sources are not suitable for PV applications, as they suffer from the problem of discontinuous input current. A quasi-Z source network[13] is an improved version of the Z-source network, which provides an inductor after the input source, resulting in continuous input current. Hence, quasi-Z source-based multilevel inverters (qZS-MLI) are suitable for PV applications.[14,15]

For PV applications, qZS based transformerless SSBI systems have not fully been explored. The literature available on the topic of leakage current mainly pertains to the modulation schemes as in Reference 16–18.

The research work reported in Reference 16 utilizes a half-bridge with an active power filter to eliminate the ripple corresponding to the second harmonic component. Also, the CMV is reduced by replacing the zero states in the modified modulation technique. A new qZS based transformerless inverter topology (consisting of two additional IGBTs and diodes) along with a modified PWM scheme for grid-current control are proposed in Reference 17. The power converter configuration described in Reference 18 uses two additional switches on the grid-side to isolate the source and load to minimize the leakage current. Despite this research effort, there is a scope for improvement in the area of leakage current reduction for 1-Ph SSBI systems with 5-level output.

The organization of this paper is as follows: Section 2 explains the working principle of the power converter. Section 3 describes the operating modes of the proposed power converter and suggests a modification to an existing modulation scheme, which aims to suppress the leakage current. This section also describes the closed-loop control strategy, which is required to regulate the output in the standalone mode operation. Furthermore, a comparative study is presented, wherein the proposed power converter is compared with the previously reported five-level topologies.[19-22] Section 4 presents the steady-state and the dynamic performance of the system, which are assessed with simulation

studies. Finally, the working principle and the performance of the proposed power converter are experimentally validated with a low-power laboratory prototype. Section 5 concludes the manuscript by summarizing the work carried out and the contribution made in the area of single-phase, 5-level SSBI.

2 | DUAL QUASI Z SOURCE BASED IMPROVED H5 INVERTER

The proposed qZS based transformerless 5-level inverter is presented in Figure 1, which consists of 3 parts. The first part is the dual quasi-Z source, which is constituted by four inductors (L_1-L_4), four capacitors (C_1-C_4), and two diodes (D_1, D_2). The dual quasi-Z source network is formed by connecting two conventional quasi-Z sources. The junction of the inner capacitors of these two quasi Z-sources forms the neutral point of the dc-link, as shown in Figure 1. The quasi-Z source impedance network has an advantage over the traditional Z source inverter in that it results in a continuous input current and a reduced capacitor rating, making it suitable for PV systems. The second part consists of the 5-level inverter, which is capable of the following features: (a) single stage boosting, (b) reactive power control, (c) isolation of the source and grid sides, (d) clamping of neutral point voltage to load and (e) provision of freewheeling paths for various loads. The 5-level inverter itself is obtained by integrating an H-bridge (S_1-S_4), an additional switch connected to positive rail (S_5), and a bidirectional switch (S_6 and S_7). There are two purposes of the bidirectional switch. First, it helps in producing an extra voltage level by connecting the point- A to the midpoint of the dual qZS structure (point O, Figure 1). Second, it helps in clamping the midpoint voltage to the load/ grid in order to avoid variations in CMV during the zero periods. Finally, Part 3 consists of a notch filter, which consists of 4 filter inductors and 2 capacitors where the midpoint of the connection is clamped to the negative rail of the source. This type of connection does not only filter the stepped output voltage of the 5-level inverter; it also filters the high frequency variations in the voltage across the parasitic PV capacitor, which in turn reduces the leakage current.

This basic topology can easily be extended to realize cascaded operation. The basic unit and a cascaded structure are shown in Figure 2A,B respectively. The details of the operation and various working modes are explained in the following section.

3 | OPERATING MODES AND MODIFIED MODULATION SCHEME

As mentioned in the earlier section, a modification is proposed to an existing switching scheme[19,23] for the proposed power converter to realize its advantages. Four level-shifted and phase disposed carrier signals along with one modulating signal are used to generate the switching signals that determine the level of operation for the proposed 5-level inverter (Figure 3).

The working modes of the proposed power converter are divided into three categories, namely, the active, the shoot-through, and the free-wheeling modes. While the active states produce the required voltage levels, the shoot-through and the free-wheeling modes are used for boosting the input voltage and supporting the non-unity PF loads.

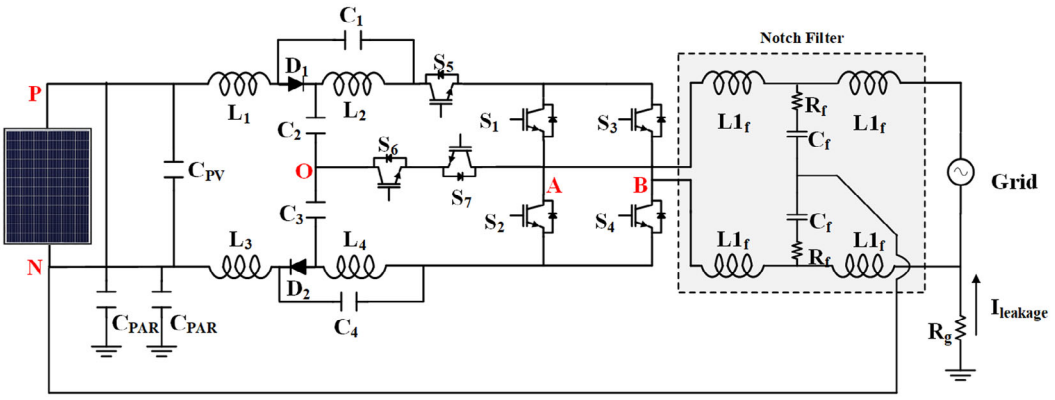

FIGURE 1 Proposed dual qZS based improved H5 inverter

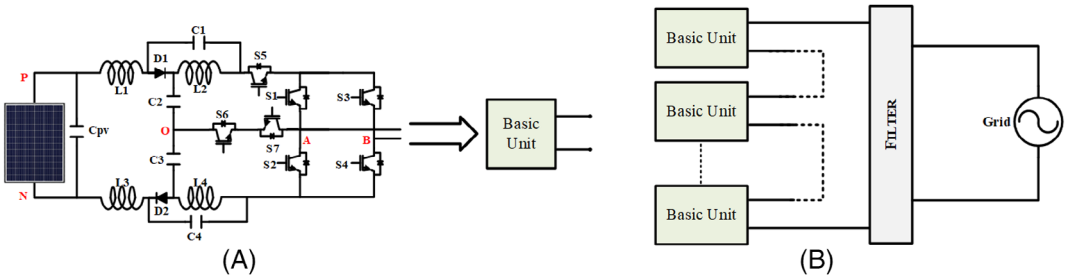

FIGURE 2 (A) Basic unit; (B) Generalized structure for N-level inverter

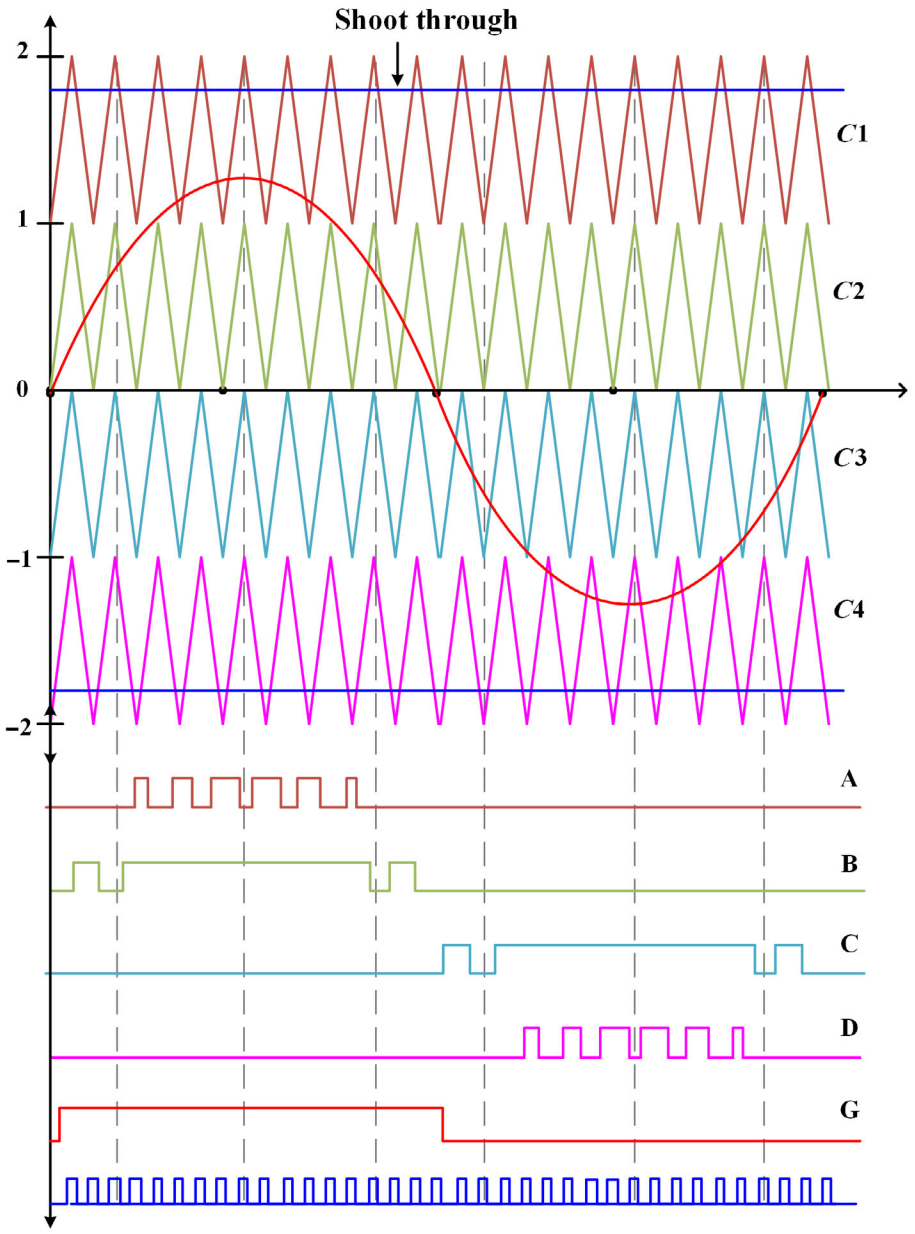

FIGURE 3 Level shift pulse width modulation scheme

The active states are divided into 4 parts, which produce four voltage levels, namely, $\pm V_{dc}/2$ and $\pm V_{dc}$. The method of generating the voltage level of $+V_{dc}/2$ is shown in Figure 4A. In this mode, the switches S_4, S_6, and S_7 belonging to the lower qZS network are turned on to produce the required voltage level. Similarly, the switches S_1, S_4, and S_5 are

turned on to generate the voltage level of $+V_{dc}$ as shown in Figure 4B. On the negative side, the voltage level of $-V_{dc}/2$ is obtained by turning on the switches S_3, S_5, S_6, and S_7 (Figure 4C). In order to generate the voltage level of $-V_{dc}$, the devices S_2, S_3, and S_5 are turned on, as shown in Figure 4D.

The shoot-through states, which render the feature of voltage boosting, are categorized into two types; the Upper Shoot Through (UST) and the Lower Shoot Though (LST) states. The UST (Figure 4F) and LST (Figure 4) are applied to the converter during the positive and the negative values of the voltage levels respectively. The modified implementation of the shoot-through mode avoids the problem of switching the voltage level of zero, while switching between the levels of $+V_{dc}/2$ and $+V_{dc}$.

Analysis of the working modes presented in Figure 4 and Table 1 paves way to devise an improved switching scheme.

It may be noted from Figure 1 that the branch, constituted by S_6 and S_7, can conduct bidirectionally in a controlled manner. When allowed to conduct, this branch connects point A (Figure 1) to the midpoint of the two capacitors

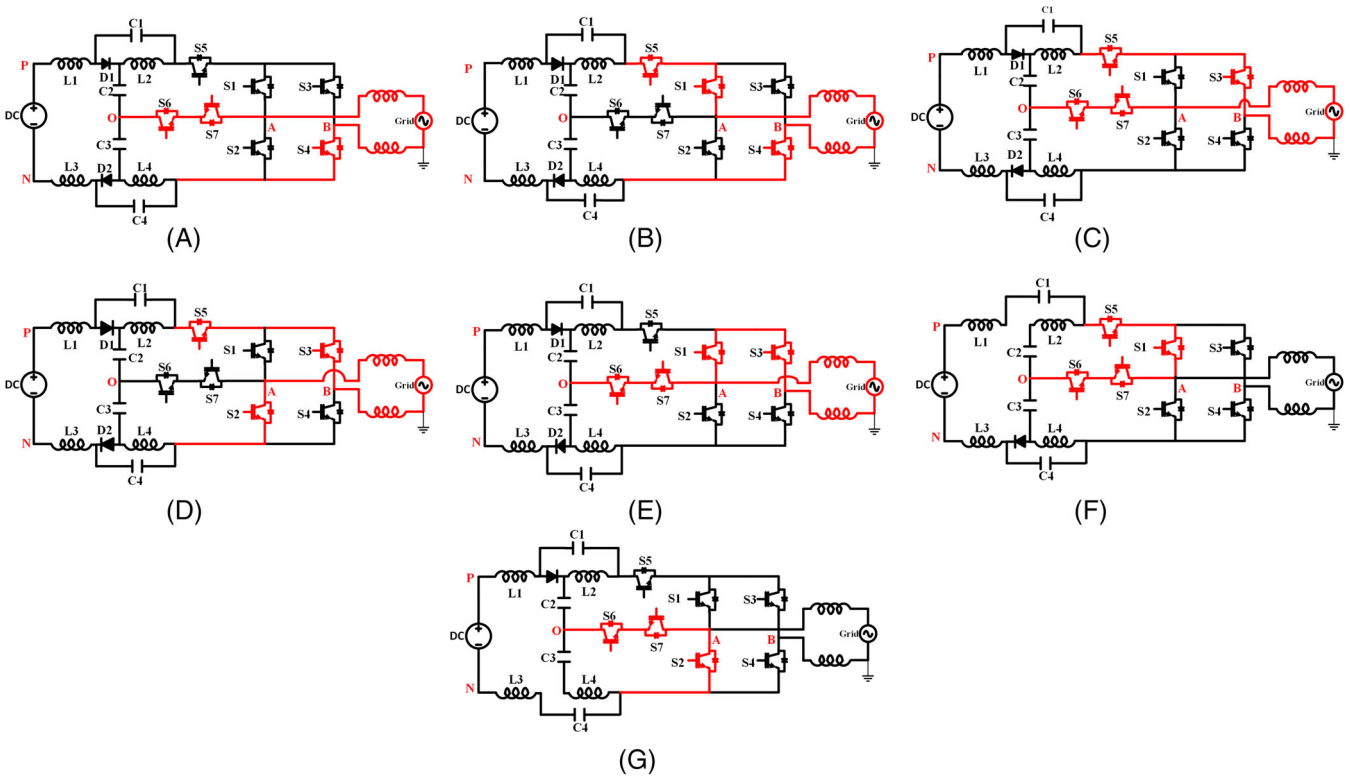

FIGURE 4 Working modes of the proposed inverter: (A) Active switches for generating $+V_{dc}/2$; (B) Active switches for generating $+V_{dc}$; (C), Active switches for generating $-V_{dc}/2$; (D) Active switches for generating $+V_{dc}$; (E) Active switches for generating zero state; (F) Active switches for generating upper shoot though; (G) Active switches for generating lower shoot through

TABLE 1 Switching table for proposed converter

S1	S2	S3	S4	S5	S6	S7	Output voltage	Switching state
0	0	1	0	0	1	1	0.5 V_{DC}	Active
1	0	1	0	1	0	0	V_{DC}	Active
0	0	0	1	1	1	1	−0.5 V_{DC}	Active
0	1	0	1	1	0	0	$-V_{DC}$	Active
1	0	0	1	0	1	1	0	Zero
1	0	0	0	1	1	1	0	UST
0	1	0	0	0	1	1	0	LST

(C_2 and C_3), facilitating the generation of the voltage levels ($\pm V_{dc}/2$). Also, this branch clamps the neutral point voltage to the load in the free-wheeling period to keep the CMV as low as possible (Figure 4F). During the free-wheeling period, the switches S_1 and S_3 are turned ON and switch S_5 is turned OFF to isolate the grid side from the source side. This method of isolation helps in reducing the leakage current in inverter. The free-wheeling state facilitates reactive power compensation for both leading and lagging loads. Whenever the output voltage and the output current do not have the same zero-crossing instants, the switches S_1 and S_3 conduct, providing a path for the freewheeling current during the time-gap between the two zero-crossing events. At appropriate intervals, the shoot-through is inserted using the switches S_1, S_2, and S_5 to obtain the required voltage boosting. The five basic PWM signals A, B, C, D, and G (Figure 3) are logically manipulated to derive the gating signals for individual switching devices of the proposed converter.

The switching logic to derive the gating signals of all switching devices is provided in (1).

$$\begin{aligned} S_1 &= B + \overline{A}G + \overline{CG} + \mathrm{UST}, S_2 = D + \mathrm{LST}, S_3 = A, S_4 = C + \overline{A}G + \overline{CG}, S_5 = B + C + \mathrm{UST}, S_6 = S_7 \\ &= (A \oplus B) + (C \oplus D) + \overline{A}G + \overline{CG}. \end{aligned} \tag{1}$$

The condition to apply the shoot-through state is given by:

$$D_s + m \leq 1 \tag{2}$$

where D_s and m respectively denote the values of the shoot-through duty cycle and the peak modulation index. Assuming symmetrical values of passive components ($L_1 = L_2 = L_3 = L_4$ and $C_1 = C_2 = C_3 = C_4$) the peak dc-link value is given by:

$$\widehat{V}_{\mathrm{DC}} = V_{C1} + V_{C2} + V_{C3} + V_{C4}, \tag{3}$$

where, $V_{C1}, V_{C2}, V_{C3}, V_{C4}$ represent the average capacitor voltages of the qZS capacitors. The capacitor voltages and the boost factor can be determined using the voltage balance equations for inductors over one switching period. The voltages across the capacitors and the boost factors are obtained as follows:

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{(2 - 4D_S)}, \tag{4}$$

$$V_{C2} = V_{C3} = \frac{(1 - D_S) V_{IN}}{(2 - 4D_S)}, \tag{5}$$

$$B = \frac{V_{DC}}{V_{IN}} = \frac{1}{1 - 2D_S}, \tag{6}$$

where B is the boost factor of the proposed converter, which is the same as the one obtained for the conventional qZS structure. The symbols V_{IN} and V_{DC} respectively denote the voltage input to converter and the peak dc-link voltage.

3.1 | Passive components selection

The values of the inductors and the capacitors of the qZS network are estimated based on the switching frequency and the allowable ripple content for them. The average input current can be estimated using the power balance equation:

$$P_{\mathrm{IN}} = P_{\mathrm{OUT}}. \tag{7}$$

Insertion of the shoot-through time period causes high frequency ripple in the inductor current. The inductor current increases during the shoot-through period and decreases during the active period. The estimated rise in current in this time interval is as follows:

$$\Delta I_{L1} = \int_0^{TD_s} \frac{dI_{L1}}{dt} dt = \frac{V_{IN} + V_{C1} + V_{C4}}{2L} TD_S. \tag{8}$$

From the above equation, the minimum value of inductor can be estimated as:

$$L = \frac{4V_O^2(1-2D_S)TD_S}{(1-D_S)K_L P_{\text{OUT}}}, \tag{9}$$

where, V_O is the output voltage, K_L is the allowable ripple though inductor current. A similar expression can be used to estimate the values of the capacitors.

$$C_1 = C_4 = \frac{TP_{\text{OUT}}(1-D_S)^2}{4k_{C1}V_O^2(1-2D_S)}, \tag{10}$$

$$C_2 = C_3 = \frac{TP_O(1-D_S)D_S}{4k_{C2}V_O^2(1-2D_S)}, \tag{11}$$

where, K_{C1} and K_{C2} represent the allowable ripple voltage across the capacitor. From these equations it is evident that the shoot-through duty and the values of the passive components can be estimated[23,24] based on the required boost factor and the output power.

3.2 | Analysis of the common-mode voltage

In a solar inverter, the parasitic/stray capacitance is formed between PV terminals and the ground (Figure 5A), which provides the path for the common mode current (popularly called as the leakage current). This leakage current flowing from PV terminals can be measured establishing a RC circuit between point N and load negative. The common mode voltage is defined as the average voltage between inverter terminals to the negative rail of the source. The CMV of the system can be defined as:

$$V_{\text{CMV}} = \frac{V_{\text{AN}} + V_{\text{BN}}}{2}, \tag{12}$$

where, V_{AN} and V_{BN} are inverter terminal voltages with respect to point N (Figure 1). The common-mode equivalent circuit for the proposed inverter is shown in Figure 5. The current flowing through this circuit represents the leakage current, which primarily depends on the ground resistance and the value of the parasitic capacitances (Figure 5B). The exact equivalent circuit of the whole system where VCMV acts as a source presented in Figure 5C. Figure 6 shows the variation of the leakage current (RMS value) with respect to the aforementioned circuit parameters for a CMV of 50. From this figure, it may be noted that the RMS value of the leakage current is directly proportional to the parasitic

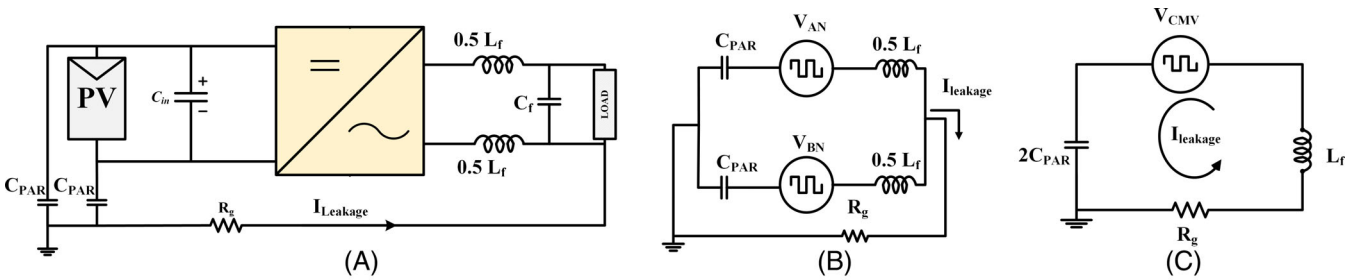

FIGURE 5 (A) Total circuit for leakage current flow; (B) Equivalent circuit form source to load side; (C) Equivalent circuit form source to load side

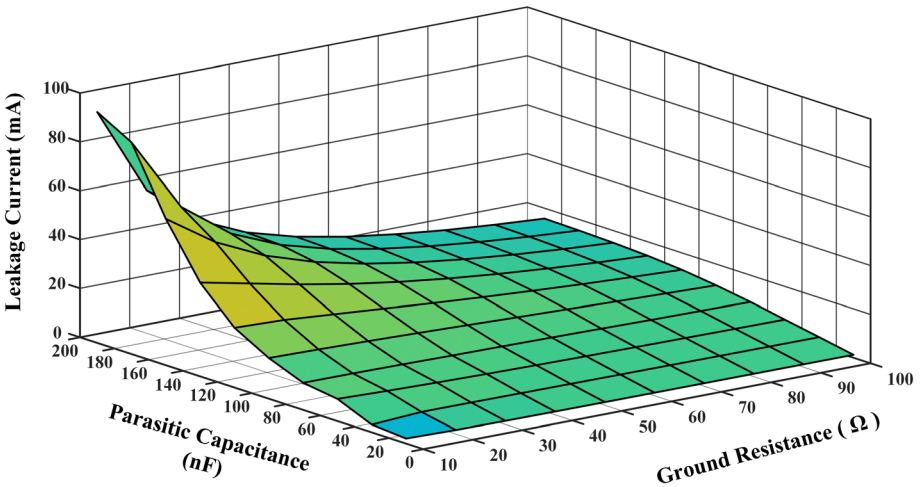

FIGURE 6 Variation of leakage current with respect to ground resistance and parasitic capacitance (CMV = 50 V)

capacitance but is inversely proportional to the ground impedance. Hence an increased ground resistance results in a decrease of the leakage current.

Also, the leakage current that flows through the ground is directly proportional to the rate change of the voltage across the parasitic capacitance. Therefore, the leakage current can be reduced by reducing the variation of voltage across the stray capacitance. The proposed modulation scheme ensures that the mid-point voltage of the inverter is clamped to the load terminals during the freewheeling period clamping the CMV to zero, reducing the voltage variation across the parasitic capacitor.

The shoot-through mode in the qZS networks, which is inserted to obtain the required voltage boosting, results in the presence of the CMV as well as its high frequency variation across the stray capacitance paving way to the circulation of the leakage current. However, the notch filter, which is an LCL filter kept at the output, reduces both the magnitude of CMV and its high-frequency variation. In this LCL filter, the inductors and the capacitor are split as shown in Figure 1. The midpoint of the split capacitor is connected to the negative rail of the source (point N, Figure 1). This connection reduces the leakage current by making the high frequency voltage waveform assume a trapezoidal shape (which is impressed across the parasitic capacitance).

3.3 | Comparison

A detailed comparison of the proposed converter with existing literature is provided in table 2. Amongst the existing PV based inverters, shown in Reference 25-30, the proposed inverter has the lowest switch count to provide five-level output except the one described in Reference 26, which has same switch count. However, it suffers from the shoot-through problem associated with single stage boosting. The topologies DMSC5L-TL[27] and 5L-CGBT-ANPC[28] possess the ability to suppress the leakage current due to the common ground feature. DMSC5L-TL[27] requires a higher number of active devices to produce the same number of voltage levels. Furthermore, it requires an additional boosting stage to obtain variable boosting feature. The single-stage topology, denoted as 5L-CGBT-ANPC[28], displays an identical device count and exhibits the feature of variable voltage boosting similar to that of the proposed power converter. However, in this topology, at any given instance of time, a higher number of semiconductor devices conduct to produce the same voltage level compared to the proposed power converter. Furthermore, the power circuit configurations enumerated in ref[25-30] need capacitors of higher voltage rating compared to the one proposed in this manuscript.

The Total Blocking Voltage (TBV), which is the sum of the voltages blocked by individual devices of a given power converter, is also lower for the proposed converter compared to all other topologies except the qZS-CMI[20] and the one described in ref[29]. However, the proposed topology requires only oneinput dc power source, compared to two in the case of the qZS-CMI[20] topology; this advantage out weighs the disadvantage associated with the TBV. The reliability of the power converter proposed in ref[29] is lower to the one proposed in this manuscript owing to the requirement of higher number of diodes and the shoot though problem associated with it Reference 29. The presence of clamping

TABLE 2 Complete comparison of proposed topology with existing topologies

Features	qZS-IH5	qZS NPC	qZS-CMI	MqZS	qZS-HBI	25	26	27	28	29	30	31
Levels	5	5	5	5	5	3	5	5	5	3	3	3
No. of switches (Bidirectional Switch)	6(1)	8(0)	8(0)	8(0)	8(0)	6(1)	6(1)	7(2)	7(0)	5(0)	5(1)	4(0)
No. of inductors	4	4	4	2	4	0	0	0	1	4	1	3
No. of capacitors	4	4	4	4	4	2	2	3	2	2	1	1
No. of diodes — qZS diodes	2	2	2	3	2	0	0	0	0	0	0	0
No. of diodes — Power Diodes	0	4	0	0	0	1	1	1	0	5	2	2
Total blocking voltage	5.5 * V_{DC}	6 * V_{DC}	4 * V_{DC}	6 * V_{DC}	6 * V_{DC}	10*V_{DC}	10*V_{DC}	10*V_{DC}	12*V_{DC}	5*V_{DC}	6*V_{DC}	4*V_{DC}
Type of PWM Scheme	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar	Unipolar
Boosting	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Fixed	Yes, Fixed	Yes, Fixed	Yes, Variable	Yes, Variable	Yes, Variable	Yes, Variable
No. of sources	1	1	2	1	2	1	1	1	1	1	1	1
Reactive power capability	Yes	No	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Issue of leakage current	Addressed	Not addressed	Not addressed	Not addressed	Not addressed	Zero	Zero	Zero	Zero	Zero	Zero	Zero
Maximum No. of switch conducting at a time	3	4	4	4	3	3	3	4	4	3	3	2
Voltage across each capacitor	$V_{C1}=V_{C4}=\frac{D_sV_{DC}}{2}$, $V_{C2}=V_{C3}=\frac{(1-D_s)V_{DC}}{2}$	$V_{C1}=V_{C4}=\frac{D_sV_{DC}}{2}$, $V_{C2}=V_{C3}=\frac{(1-D_s)V_{DC}}{2}$	$V_{C1}=V_{C4}=D_SV_{DC}$, $V_{C2}=V_{C3}=(1-D_s)V_{DC}$	$V_{C1}=V_{C4}=\frac{D_sV_{DC}}{2}$, $V_{C2}=V_{C3}=\frac{(1-D_s)V_{DC}}{2}$	$V_{C1}=V_{C4}=D_SV_{DC}$, $V_{C2}=V_{C3}=(1-D_s)V_{DC}$	$V_{C1}=V_{DC}$, $V_{C2}=2V_{DC}$	$V_{C1}=V_{DC}$, $V_{C2}=2V_{DC}$	$V_{C1}=V_{DC}$, $V_{C2}=2V_{DC}$	$V_{C1}=2V_{DC}$, $V_{C2}=V_{DC}$	$V_{C1}=V_{DC}$	$V_{C1}=V_{DC}$	$V_{C1}=V_{DC}$	$V_{C1}=V_{DC}$
								$V_{C1}=V_{C4}=\frac{D_sV_{DC}}{2}$, $V_{C2}=V_{C3}=\frac{(1-D_s)V_{DC}}{2}$					$V_{C1}=V_{DC}$
Shoot through risk	No	No	No	No	No	Yes	Yes	Yes	No	No	Yes	No

diodes in qZS-NPC[19] make it susceptible to failure and excessive power losses. Hence, it can be inferred that the proposed topology could be more efficient than the other topologies belonging to this genre. However, unlike the proposed power converter, the MqZS[21] doesn't addresses the issues of reactive power handling capability and leakage current. Furthermore, owing to the absence of an inductor at the input, the input current is discontinuous in MqZS[21]. Hence, it is not suitable for PV applications.

To summarize, the proposed converter displays features such as the lowest switch count, single stage boosting, absence of risk associated with the shoot though, low total blocking voltage, reactive power capability, low capacitor rating and capability to reduce the leakage current. Thus, this power converter configuration appears to be a promising proposition for PV applications.

3.4 | Control scheme

Figure 7 shows the closed-loop controller, which regulates the dc-link (and hence the output voltage) of the proposed power converter against source and load disturbances. This control scheme consists of a two-loop structure. In this scheme, the outer loop regulates the dc-link voltage. The inner loop, which is appreciably faster than the outer loop, regulates the output current of the PV source.

First, the peak dc-link voltage is obtained by summing the physically measured voltages, which appear across the capacitors C_1 and C_2 (Figure 1) and multiplying this value by a factor of 2. Generally, the reference peak dc-link voltage is determined by the MPPT controller, though it can also be set manually. The voltage error is processed through a proportional integral (PI) controller, which generates the reference value for the PV output current (which flows through the inductor i_{L1}). The actual inductor current (i_{L1}) is then measured and compared with this reference value and the error is then compensated with a proportional controller, which generates the signal to obtain the shoot-through duty cycle. In this work, this controller is implemented digitally using the Xilinx -Spartan 6 FPGA board.

4 | RESULTS AND DISCUSSION

The performance of the proposed converter has been verified using simulation studies using MATLAB/Simulink tools and the experimental validation has been carried out with a scaled down laboratory prototype. Both simulation and experimental studies have been performed at a power level of 500 W with similar parameters as enumerated in Table 3.

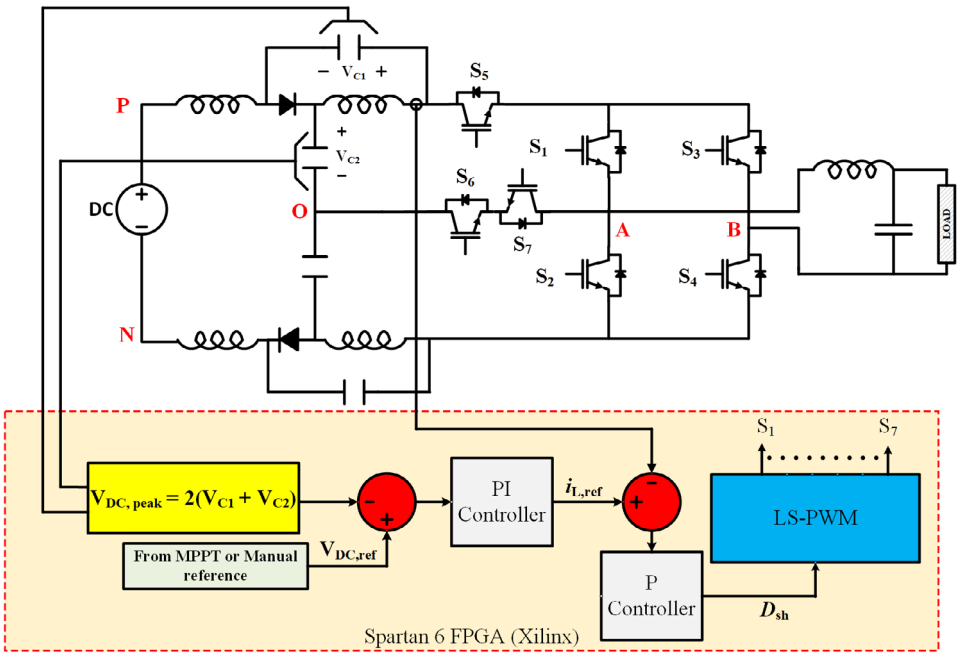

FIGURE 7 Closed-loop scheme

TABLE 3 Simulation and Experimental Parameters

Parameters		Values
Output power		500 W
Input voltage		100 V
Output voltage (RMS)		110 V
Inductors	L_1-L_4	1 mH
	L_f	4 mH
Capacitors	C_1-C_4	1000 μF
	C_f	4 μF
Switches (S_1-S_7)		IRFP460
Diodes (D_1, D_2)		MURS1560

4.1 | Simulation results

Figure 8 shows the simulated steady-state performance of the proposed converter. The formula for the boost factor obtained with this converter is given by (Table 2):

$$B = \frac{1}{1 - 2D_S}.$$

The above equation suggests that a boost factor of 2.2 is obtained with a shoot-through duty $D_S = 0.27$.

As shown in Figure 8A, an input voltage of 100 V and a shoot-through duty cycle of $D_S = 0.27$ result in a boosted dc-link of 220 V (with a 10 V ripple). This complies with the above expression, as a boost factor of 2.2 is obtained. The modified modulation scheme and the shoot though insertion technique avoid the dc-link value to fall to zero every time. The steady-state waveforms of the output voltage of the 5-level inverter, the load voltage, and current waveforms (with a multiplication factor of 10) are shown in Figure 8B,C respectively. Figure 8D presents the current through the inductor L_1, which increases during the shoot-through mode of the qZS network. Owing to the symmetry of the qZS network and identical values of inductances, all other inductor currents show identical waveforms.

Due to the symmetry of the qZS network, $C_1 = C_4$ and $C_2 = C_3$. Figure 8E,F present the voltages across the capacitors C_1 and C_2. The average values of these capacitor voltages comply with Equations (4) and (5).

The common mode characteristics of the proposed power converter is presented in Figure 9. The CMV (V_{CMV}) is calculated using V_{AN} and V_{BN} (Equation 12). The steady-state waveforms of these three voltages (V_{AN}, V_{BN}, and V_{CMV}) are presented in Figure 9A. The shoot-through mode inserted in every switching cycle manifests as the high-frequency content in these waveforms.

The top waveform of Figure 9B shows the voltage across the stray capacitance, wherein the high-frequency content is absent. This shows the effectiveness of the proposed modulation scheme and the filter arrangement. The second waveform in Figure 9B is the leakage current that flows from the source to the load. Due to the trapezoidal nature of the voltage across stray capacitor the peak value of leakage current is restricted to 20 mA which is well below the German standard VDE 0126-1-1 (which specifies that the leakage current be within ≤300 mA).

As explained in the earlier section, the modulation scheme, besides suppressing the leakage current in the proposed converter, provides it the capability to support reactive power. The proposed converter achieves this feature by providing a path for the free-wheeling current for lagging or leading loads. Figure 10 demonstrates the reactive power capability of the converter, wherein the load is changed from UPF to 0.9 lagging power factor. This capability is achieved by turning on the switches S_1 and S_3 during the zero-period as shown in Figure 4E. During this period, the CMV is clamped to a value of zero, which is achieved by turning on the devices S_6, S_7 (connecting the point "A" to the midpoint of the NPC structure, that is, . "O") and turning off the device S_5 (which isolates the source-side and the load-side) as shown in Figure 4E.

The dynamic performance of the proposed converter under the load disturbance is demonstrated in Figure 12. The control scheme, shown in Figure 7, aims to maintain a constant dc-link voltage by regulating the shoot-through duty cycle. In the simulation result shown in Figure 12A, the load on the converter is removed at t = 2 seconds and is again applied at t = 4 seconds. Zoomed views of all quantities, namely the output voltage, the output current, the peak dc-

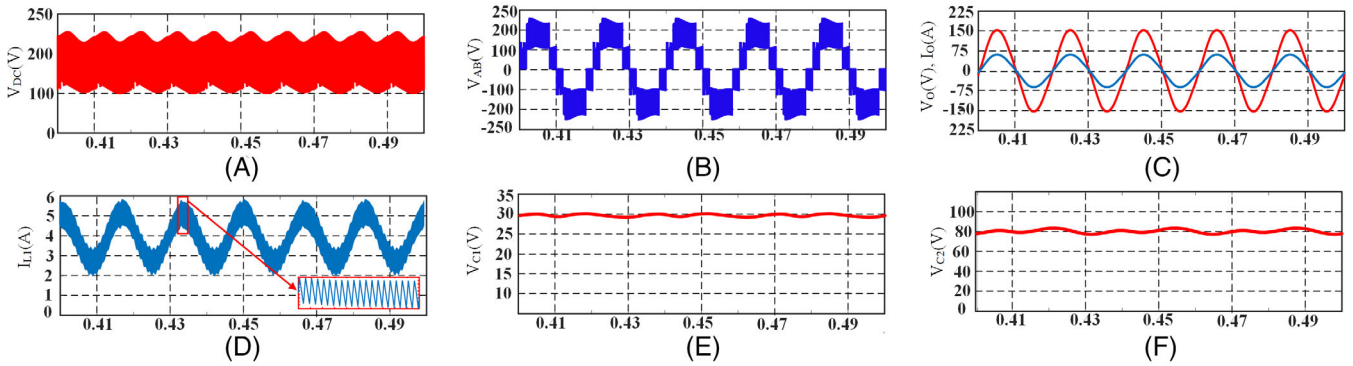

FIGURE 8 (A) Boosted DC link voltage; (B) Inverter terminal level voltage; (C) Output voltage and current; (D) Inductor current for L_1; (E) V_{C1}; (F) V_{C2}

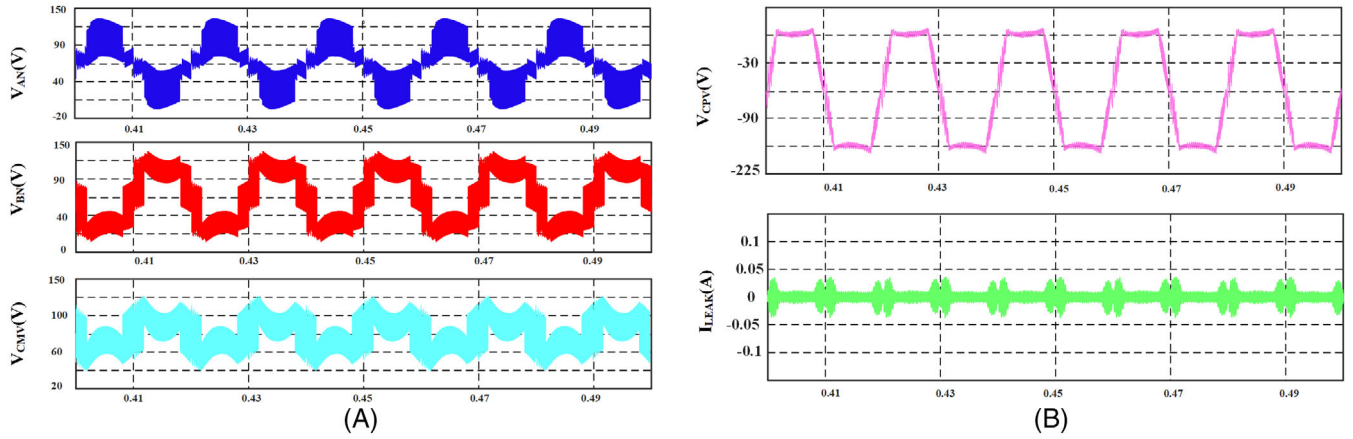

FIGURE 9 (A) Common mode characteristics V_{AN}, V_{BN} and V_{CMV} respectively; (B) Voltage across parasitic capacitor and leakage current

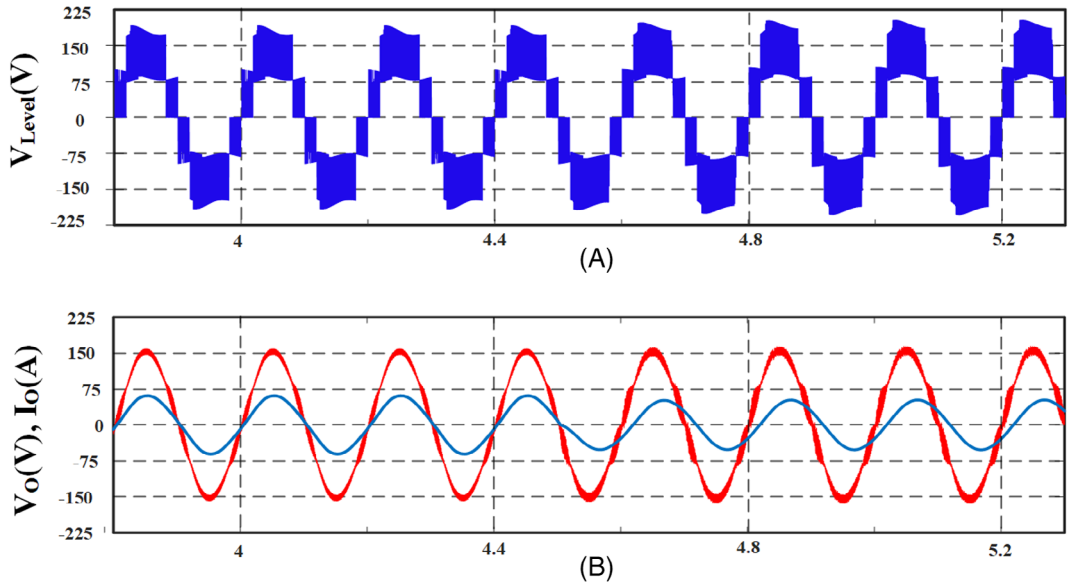

FIGURE 10 Reactive power capability of the converter (A) Inverter terminal voltage during load change from UPF to 0.9 Lag PF; (B) Output voltage and current

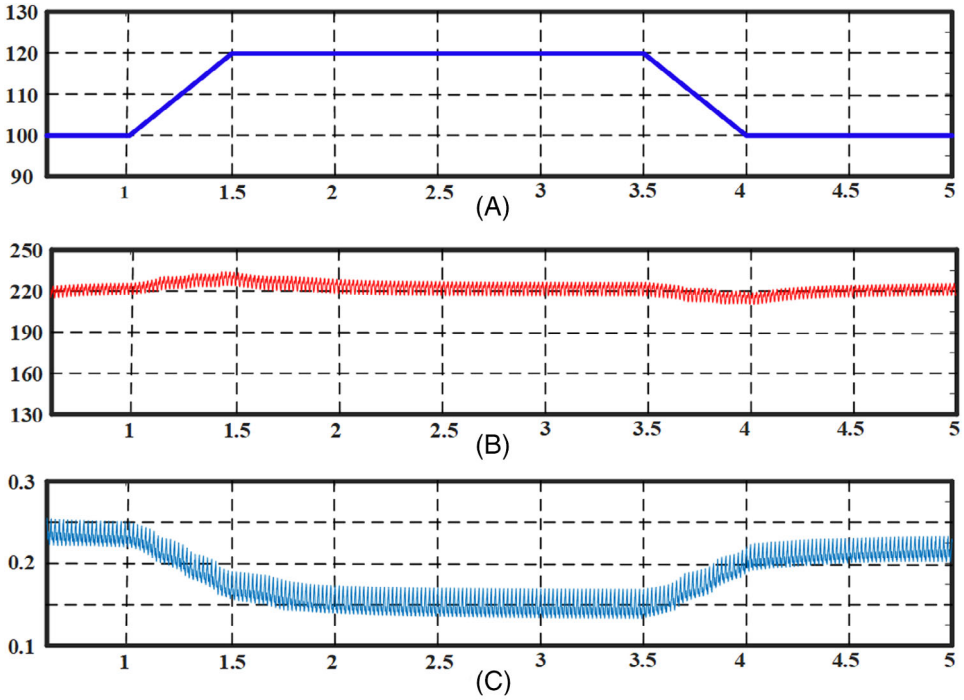

FIGURE 11 Simulation results for closed-loop control during change in input voltage: (A) Ramp change in input voltage from 100 to 120 V at t = 1 second and 120 to 100 V at t = 3.5 seconds; (B) Regulated DC link voltage; (C) Change in shoot-through duty cycle

link voltage, and the shoot-through duty cycle are shown in Figure 12B-D. It can be observed that the shoot-through duty cycle is automatically adjusted by the controller to maintain the peak dc-link value at its reference value.

Figure 11 shows the dynamic response of the proposed converter against the source disturbance. In this simulation study, the input voltage is ramped up from 80 to 100 V, starting at t = 1 second. The input voltage is then ramped down to 80 V at $t = 3.5$ seconds. Both of these changes are affected gradually (ie, as a ramp) to simulate the real-world condition (Top trace, Figure 11). The middle and bottom traces of Figure 11 present the responses of the peak dc-link voltage and the shoot-through duty respectively. It can be observed that the peak dc-link voltage changes due to the change in the input voltage. The controller then springs into action and adjusts the shoot-through duty cycle to regulate the peak dc-link voltage at its reference value.

4.2 | Experimental results

In order to validate the simulation results presented in the above section, an experimental prototype is developed, which is rated for a power rating of 500 W (Figure 13). The parasitic elements that trigger the leakage current is emulated by connecting a resistance (R_g) and a capacitance (C_{PAR}) in series, which is connected between the negative terminal of the source output and load as shown in Figure 1. The inductors and capacitors of the qZS, which are calculated using (9)-(11), are used for the realization of the physical prototype (the same component values are used in simulation studies too). IRFP460 power-MOSFETs and MURS1560 diodes (for qZS) have been employed to construct the power converter. The PWM scheme and the controller have been implemented with the Spartan 6 series FPGA.

The steady-state performance of the converter is presented in Figure 14. The dc-link voltage and the terminal voltage of the 5-level inverter are presented in Figure 14A. Figure 14B presents the inverter terminal voltage, the output voltage (after filtering) and the load current. The current flowing through the inductor L_1 and the voltages across the two capacitors C_1 and C_2 are presented Figure 14C. The FFT of the inverter terminal voltage, output voltage and output current is presented in Figure 14D-F. The THD of output voltage and current have a value of 2.98% and 2.05% which are well within IEEE standard.

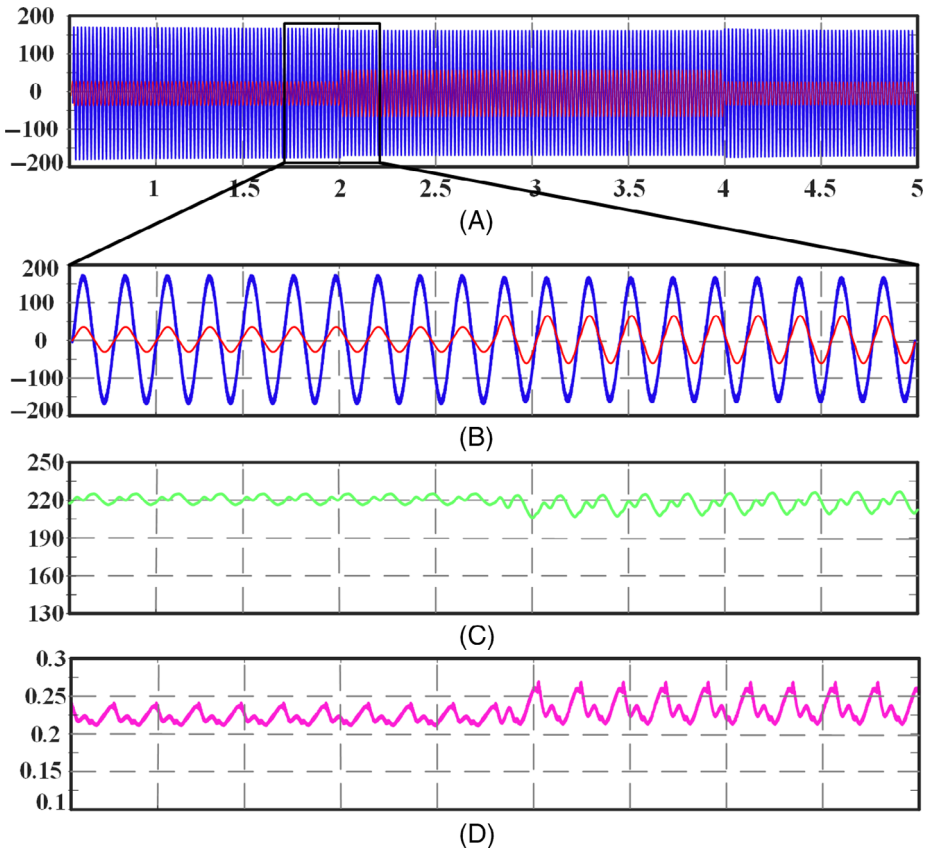

FIGURE 12 Simulation results for closed-loop control during change in load: (A) Complete simulation results with output voltage and current; (B) Zommed version of load voltage and current during release of load at t = 2 seconds; (C) Peak DC link voltage; (D) Shoot-through duty cycle

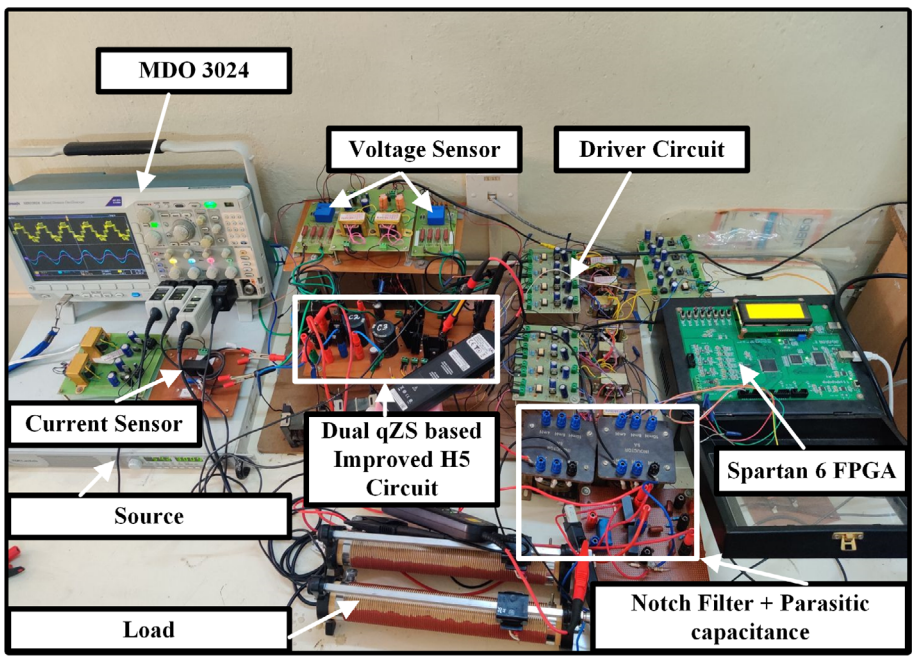

FIGURE 13 Hardware setup of proposed inverter

Figure 15 describes the common mode characteristics of the proposed inverter. The inverter terminal voltages (V_{AN}, V_{BN}) and the CMV (V_{CMV}) are shown in Figure 15A. Figure 15B presents the voltage across the parasitic capacitance and the leakage current. It is evident from Figure 15B that the proposed PWM scheme and the notch filter succeed in

suppressing the leakage current. It may be noted that the resulting leakage current is 20 mA (RMS), which is well within the value stipulated by the German VDE 0126-1-1 standard (≤ 300 mA).

The experimental result presented in Figure 16 validates the reactive power capability of the converter. It may be noted that, despite the change in the nature of the load (UPF to 0.9 lag), the terminal voltage of the inverter remains undistorted. As explained earlier, this reactive power handling capability is attributed to the availability of the free-wheeling paths for the inverter current during the time-gap between the positive zero-crossing instants of the output voltage and the output current.

Figure 17 shows the dynamic performance of the proposed converter against the source disturbance. It may be observed that despite a gradual change in input voltage (90-105 V and then 105-80 V), the dc-link voltage is regulated at the reference value by the controller in both the condition. The dynamic response of the system against the load disturbance is presented in Figure 18. It is evident that the control system (Figure 7) can also tackle the load disturbance. Figure 18 reveals that the dc-link voltage of the converter is regulated by the controller effectively as the load is changed from 5 to 4A and vice-versa.

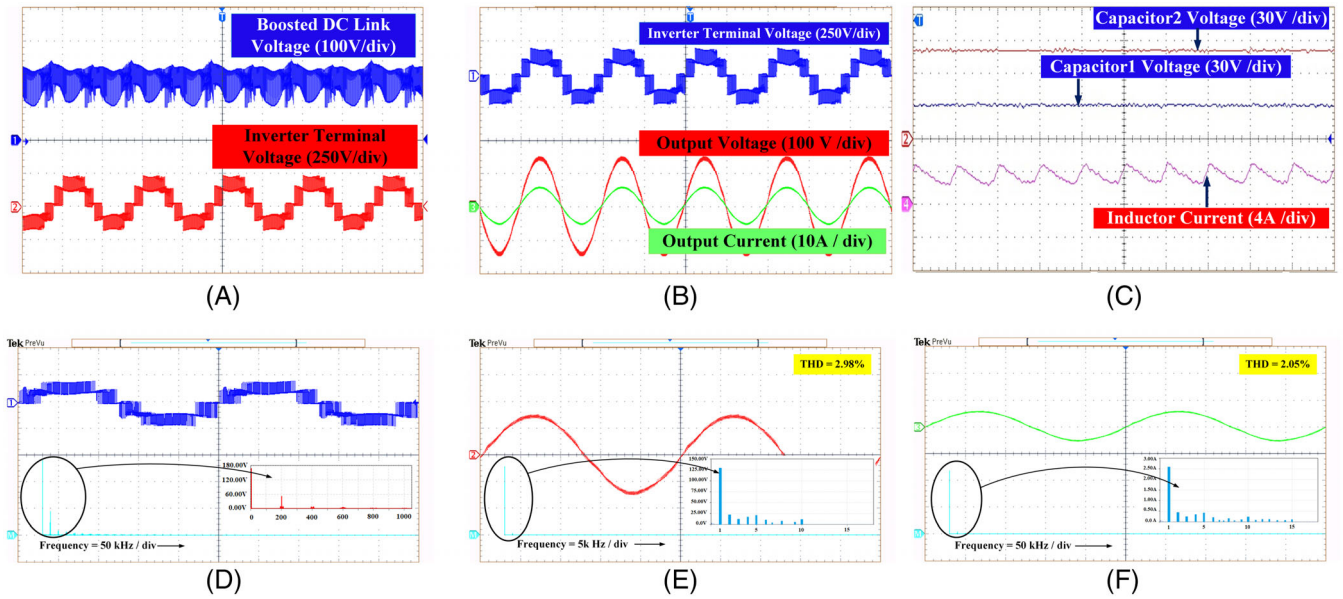

FIGURE 14 Steady state performance of the proposed converter: (A) Boosted dc link voltage, Inverter terminal voltage; (B) Inverter terminal voltage, output voltage and current; (C) i_{L1}, v_{C1} and $v_{C2;}$ (D) FFT of inverter terminal voltage; (E) FFT of inverter output voltage; (F) FFT of inverter output current

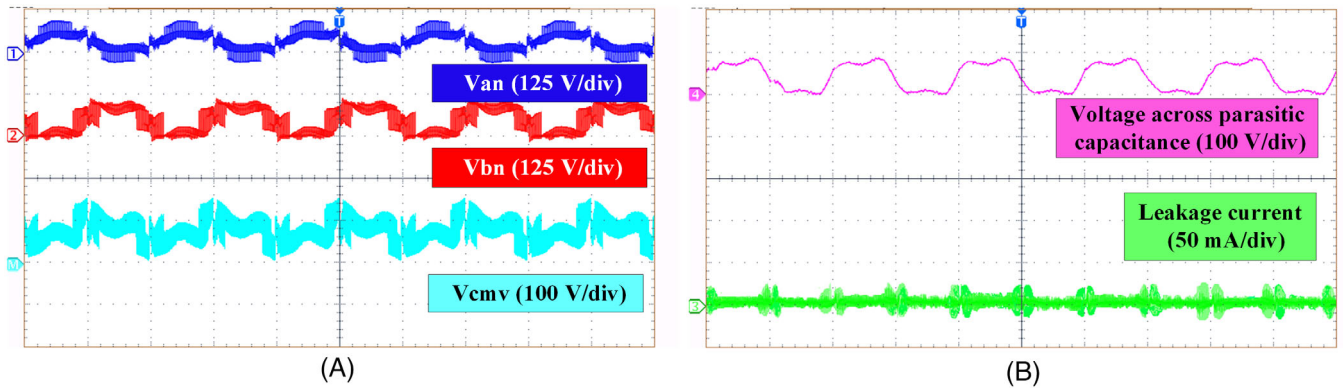

FIGURE 15 Common mode characteristics of inverter: (A) V_{AN}, V_{BN} and V_{CMV}; (B) Voltage across parasitic capacitance and leakage current

4.3 | Efficiency

The section presents a comparative study of the efficiencies displayed by various single-phase five-level inverter topologies.[18-22] Efficiencies of these inverters are estimated using the thermal models of the switching devices available with the PSIM software.[32] While performing these efficiency calculations, identical parametric values are used across all of the converters ($V_{IN} = 100$ V, $D_S = 0.27$, $m = 0.7$).

Figure 19A presents the efficiencies of existing qZS based five-level topologies. It is evident that the proposed converter exhibits a higher efficiency compared to the other converters (described in Table 2) throughout the operating range of the converter. It may also be noted from Figure 19A that the proposed converter achieves a maximum efficiency of 92% around 250 W. Higher efficiency of the proposed power converter is attributed to the employment of lesser number of switching devices and a suitable modulating technique. The loss distributions in various active and passive devices are shown in Figure 19B. It can be observed that copper losses take top most position followed by the losses in switch S_5 and diode (D_1 and D_2). Among the switches S_5 incurs the highest amount of loss due remaining in conduction state for most of time in whole cycle. However, based on the formulas provided in Reference 16,17,20 the losses are calculated and compared with the simulated losses as seen in Figure 19C. It can be verified that simulated loss (red bar) and calculated losses (blue bar) are almost have same values which proves the effectiveness of efficiency

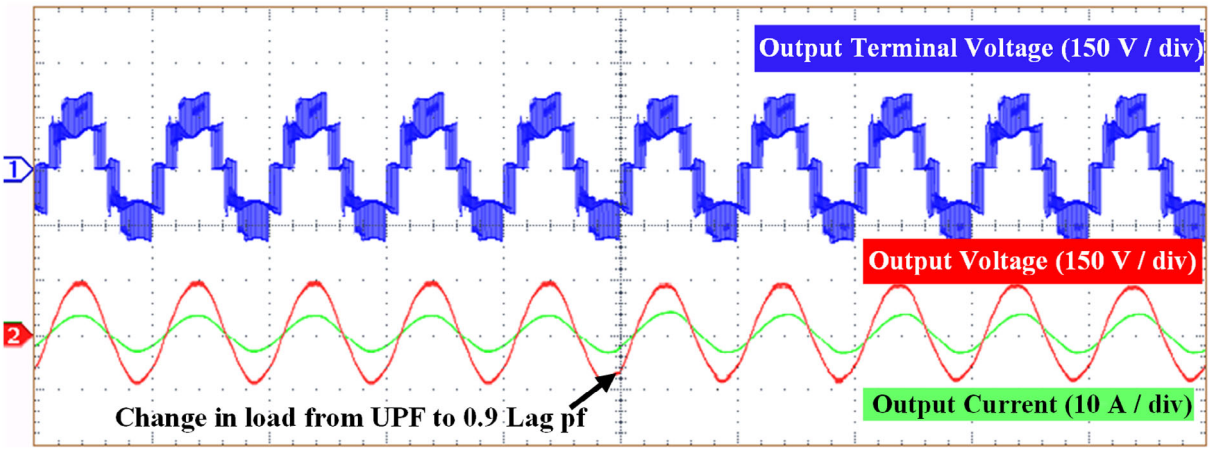

FIGURE 16 Reactive power capability of converter

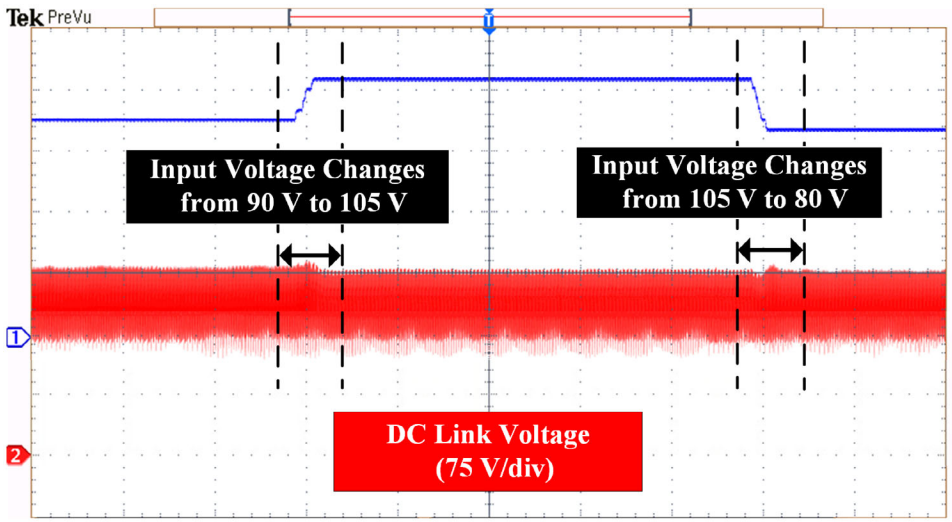

FIGURE 17 Closed-loop results for change in input voltage

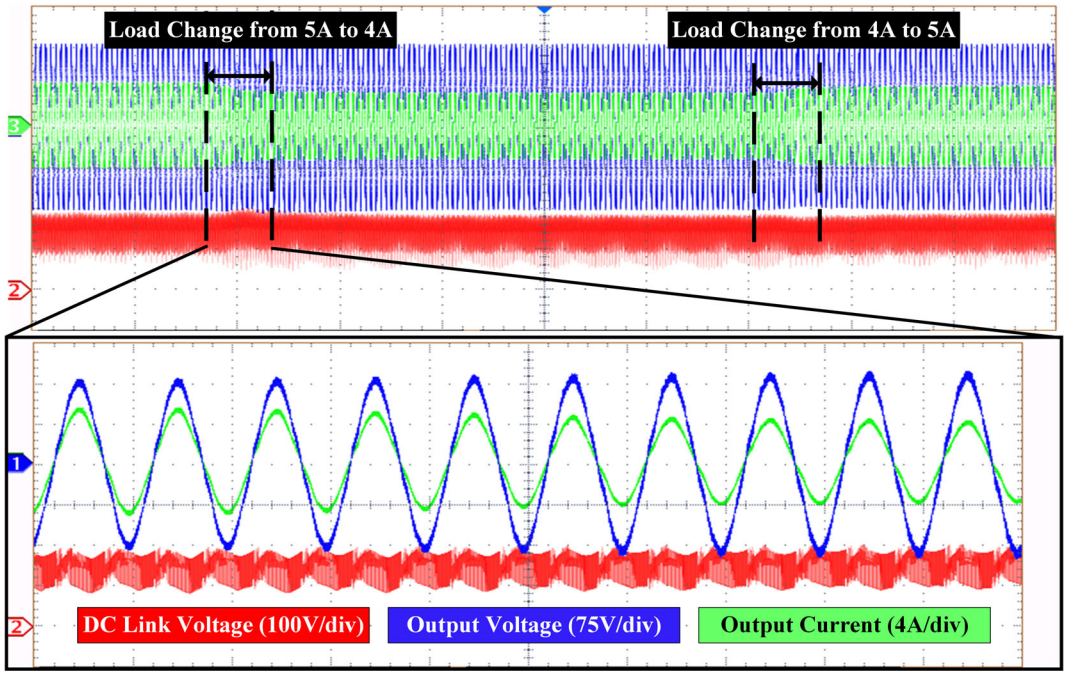

FIGURE 18 Closed-loop results for change in load

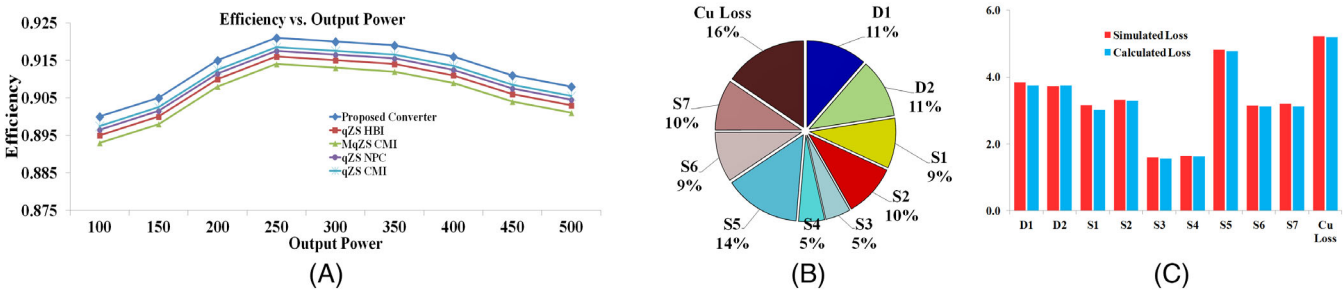

FIGURE 19 Efficiency comparison; (A) Efficiency vs. Output power curve for various qZS based converters; (B) Loss distribution among various components; (C) Comparison of simulated and calculated loss for various components

curves. Efficiency of the converter can still be improved by replacing the conventional silicon devices with their SiC or GAn counterparts.

5 | CONCLUSION

This paper proposes a new power circuit configuration for single-phase, single-stage PV systems. The proposed power converter is constituted by fusing a qZS network with a 5-level voltage source inverter. The 5-level inverter is synthesized by augmenting an *H5-inverter* with a bi-directional clamping branch. This bi-directional clamping branch, besides obtaining the clamping of the mid-point voltage, produces an additional level in the output voltage waveform.

The qZS network is formed by connecting two symmetrical quasi Z-sources in a back-to-back manner. Such a network results in a neutral point clamped structure with single-stage boosting. The modulation technique used for this power converter aims to achieve: (a) five voltage levels (b) reactive power handling capability, and (c) suppression of the leakage current to be well within the standards of VDE 0126-1-1.

The effectiveness of the adopted modulation strategy and the control scheme are assessed with simulation studies. These simulation studies reveal that both steady-state and dynamic performances of the proposed converter are

satisfactory. Simulations studies clearly show that the controller regulates the peak value of the dc-link voltage against the source and load disturbances by adjusting the shoot-through duty cycle.

These simulations are then experimentally validated on a 500 W laboratory prototype using the Spartan 6 FPGA control platform. Experimental results, which agree with the simulation results validate the working principle of the proposed converter and the adopted modulation scheme.

A comparative study of the proposed power converter with other comparable topologies reported in literature so far reveals that proposed converter yields a better performance in aspects such as switch count, reliability, efficiency, leakage current, and reactive power handling capability. Based on these advantages, it appears that this power converter is a viable proposition for PV applications and merits further exploration.

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PEER REVIEW

The peer review history for this article is available at https://publons.com/publon/10.1002/2050-7038.13187.

DATA AVAILABILITY STATEMENT

The Data that support the findings of this study are available within the article and also in properly cited references.

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