

Single-Phase Five-level Transformerless Inverter for Multi-String Photovoltaic Applications

K. Sateesh Kumar, *Member IEEE*
 Dep. of Electrical and Electronics
 Engineering
 SRM Institute of Science and
 Technology, Kattankulathur
 Chennai, India
sateeshkuncham@gmail.com

S. Raghavendran, *Member IEEE*
 Dep. of Electrical and Electronics
 Engineering
 SRM Institute of Science and
 Technology, Kattankulathur
 Chennai, India
raghavagi@gmail.com

A. Kirubakaran
Senior Member IEEE
 Dep. of Electrical Engineering
 National Institute of Technology
 Warangal
 Warangal, India
a_kiruba81@rediffmail.com

Umashankar Subramaniam,
Senior Member IEEE
 Dep. of Communications and
 networks
 Prince Sulthan University
 Saudi Arabia
shankarums@gmail.com

Abstract — In this paper a novel single-phase two-stage five-level asymmetrical filter inductor based transformerless inverter is proposed for the multi-string photovoltaic (PV) applications. The multi-output boost converter is developed with resonant soft-switching circuit to obtain either zero current switching (ZCS) or zero voltage switching (ZVS) during turn-on and turn-off of the both main and auxiliary switches. The six switch asymmetrical filter inductor based five-level inverter eliminates the high-frequency oscillations in the common mode voltage (CMV). Consequently, the flow of leakage current magnitude from the grid to PV panels is reduced significantly without the use of an isolation transformer. Moreover, the improved modulation scheme enhances the inverter operation in all the operating power factor conditions of the grid. Further, the integration of the soft-switched multi-output boost converter and five-level inverter at reduced power losses increases the overall efficiency and reliability of the multi-string PV systems. Simulation studies are carried-out in the PSIM and MATLAB platforms to validate operation of the proposed concept.

Keywords — *Distributed power generation systems, two-stage configuration, soft-switched DC-DC converter, multilevel transformerless inverter, leakage current, common mode voltage.*

I. INTRODUCTION

As the cost of PV panels is declining day by day due to the technology development in the manufacturing, the share of the PV power in the electricity market is increasing. Inverter is an important power electronic circuit in the PV power generation system and it is used to convert direct current from PV module to the alternating current and further fed into the utility grid. The summary of various grid-tied PV inverters is given in ref [1]. This paper proposes a multi-string five-level PV inverter as per the structure given in the Fig. 1, where several PV panels are connected in series to form a string and then it is connected with an individual boost converter for forming a high-voltage DC bus. Each string is controlled independently and can be easily extend the power rating by adding a new string along with DC converter. Moreover, the front-end DC-DC converter can perform the functions of maximum power tracking (MPT) and voltage boosting. The inverter regulates the DC voltage and grid current injection. Thus, the maximum energy extraction and flexible operation is achieved in comparison with the central inverters [2].

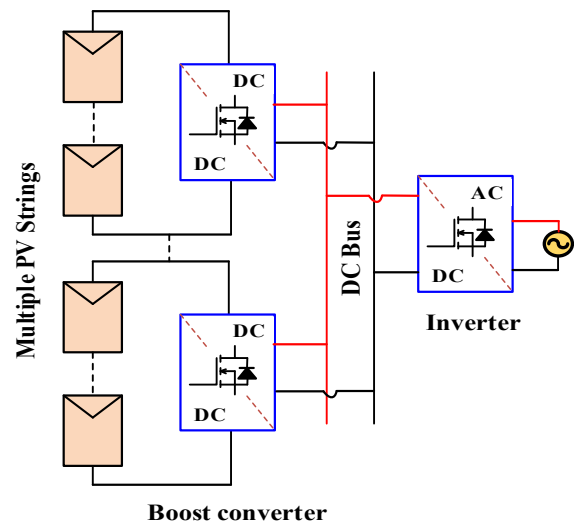


Fig. 1. Multi-string PV power generation system

In this context different multi-string inverter topologies have been introduced in the literature for PV systems. The inverters employed for string applications can also be used for the multi-string applications by adding an additional DC-DC converter stage in between the PV panels and the inverter. SMA solar inverter company introduced the first two-level multi-string inverter with the conventional boost converter [3]. Some of the other inverter topologies are also proposed by replacing the two-level inverter with three-level inverters such as neutral point clamping (NPC), and T-type for improving the total harmonic distortion (THD) and also to reduce the electromagnetic interference (EMI) [4]. However, the DC bus voltage requirement and power semiconductor device rating is double than the grid peak value. To overcome these drawbacks a full-bridge four switch inverter is developed with Bipolar and Unipolar pulse width modulation (PWM) schemes. Unfortunately, the issues like THD, EMI and leakage current are not completely eliminated to use them directly in the grid-connected PV systems [5]. Thus, to overcome the aforesaid issues different modifications and patented solutions were developed to the full-bridge inverter configuration, named as H5, Heric, H6 and its derived topologies [6]. Even though an isolation transformer is not used in the above-said full-bridge inverter topologies, the leakage current is reduced significantly by preserving constant common mode voltage (CMV).

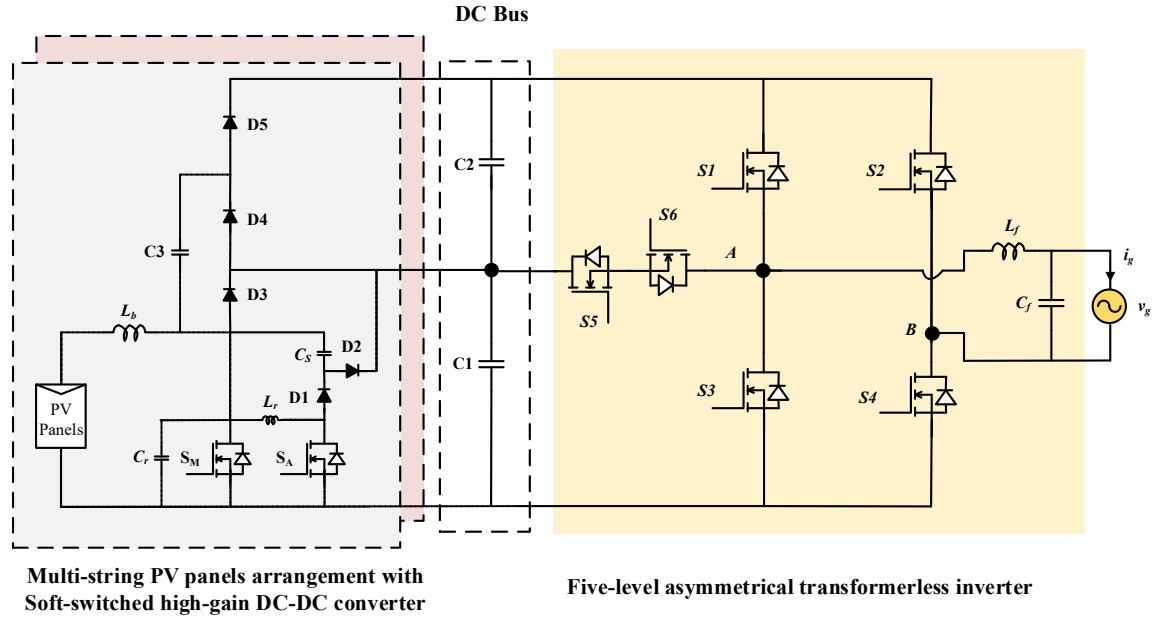


Fig. 2. Proposed five-level asymmetrical inductor based transformerless inverter topology for multi-string PV application.

Consequently, these inverters attain high power density, lower cost, high efficiency and reliability. Contemporarily, the multilevel inverters are getting more popular in the high voltage and medium power applications for improving the output waveform quality, reduce the dv/dt stress across the switching devices and also to reduce the output filter size [7].

As a result, different multilevel inverters are developed in the recent years for PV applications. A multi-string five-level inverter with novel PWM scheme is proposed in ref [8], where a traditional boost converter is used to integrate PV power into the grid. Due to the limited voltage gain of the traditional boost converter the number of PV panels required in series are more and it results in the issues of voltage mismatches and partial shading. In [9], a nine-level multi-string inverter is proposed with a multi-level boost converter. The gain of the front-end converter is improved and also more number of output levels are possible by adding an additional circuitry. However, the boost switch experiencing more switching losses due to higher blocking voltage. Another, simplified five-level multi-string PV inverter is proposed in [10], with a coupled inductor based high-gain converter. Unfortunately, all the above-said multi-string multilevel inverters require an additional isolation transformer or an EMI filter to reduce the leakage current. Consequently, the overall system became less reliable, low efficient, and reduced power density. Further, the inverter topologies and their PWM schemes were only explored to operate under real power transfer. But, as per the revised grid standards the newly designed inverter should also be operate under the negative power transfer (i.e., reactive power control) as the conventional power plant does [3].

To overcome the above-said drawbacks, in this paper an asymmetrical inductor based five-level transformerless inverter is proposed with a soft-switched multi-level boost

converter. The following are the merits obtained with the proposed system:

- 1) The front-end converter balances the DC capacitor voltages naturally by utilizing the clamping diodes and also boost the low PV voltage to high DC-link voltage.
- 2) Moreover, the resonant circuit employed in the converter creates ZVS and ZCS during the operation of both main and auxiliary switches which further reduces the switching losses.
- 3) Inverter utilizes less number of components to realize the five-level output and also provides bi-directional current path to support the reactive power.
- 4) The improved SPWM scheme achieves grid frequency variations in the total common mode voltage (CMV). Consequently, the magnitude of leakage current is reduced significantly without the use any additional isolation transformer.

Thus, due to the reduction in switching and conduction losses of the two power conversion stages the overall efficiency increases.

II. PROPOSED MULTI-STRING INVERTER

Fig. 2 illustrates the proposed multi-string PV system. It comprises of a soft-switched multi-output boost converter and a five-level transformerless inverter.

A. Soft-Switched Multi-output Boost Converter

The detailed operation of the traditional multi-output boost converter is clearly explained in the ref. [11]. The main switch in the converter operating at switching frequency and also experiencing high voltage stress (i.e., equal to the DC-link voltage), which results in higher switching losses. In this paper, an additional resonant circuit is employed to reduce

the switching loss of the main switch. The main switch ' S_M ' turn on and off under zero voltage condition. First, the auxiliary switch turn on under ZCS because of the resonant inductor. Then resonance happens between the inductor ' L_r ' and the capacitor ' C_r '. The anti-parallel diode of the main switch clamps the voltage across ' C_r ' to zero. The main switch turned on under zero voltage condition. At this time, the auxiliary switch is turned off which makes the ZVS condition as the energy stored in the resonant inductor is now transferred to the snubber capacitor ' C_s '. Then the energy stored in the snubber capacitor is transferred to the load. When the main switch is turned off, the voltage across the resonant capacitor ' C_r ' raises slowly, which makes the ZVS of main switch. The resonant components are selected such that the actual operation of the converter is unaffected, and the auxiliary switch is turned on for a short time.

B. Asymmetrical Inductor based Five-level Transformerless Inverter

The proposed asymmetrical inductor based five-level transformerless inverter is illustrates in Fig. 2. The operation of the inverter is explained in six modes based on the output voltage level and it is shown in Table. I. Mode I and II corresponds to V_{dc} and $V_{dc}/2$, Mode III & IV corresponds to zero level, Mode V and VI corresponds to $-V_{dc}/2$ and $-V_{dc}$. In every mode both positive and negative current directions are provided by the switches and diodes to realize the inverter operation in both the real and reactive power regions respectively.

- 1) **Mode I:** The terminal voltage of the inverter $V_{AB} = V_{dc}$, switches S1, S4 & S5 are ON. The current flows from the source to the grid and vice-versa. In this mode the two DC-link capacitors are connected in series and they are in parallel with the grid.
- 2) **Mode II:** The terminal voltage of the inverter $V_{AB} = 0.5*V_{dc}$, the switches S4, S5 & S6 are ON. The current flows from the source to the grid and vice-versa. In this mode the capacitor C1 is connected in parallel with the grid.
- 3) **Mode III:** The terminal voltage of the inverter $V_{AB} = 0$ and $i_g > 0$, the switches S3 and S4 are ON. The current freewheels through any one of the switch and body diode based on the current direction.
- 4) **Mode IV:** The terminal voltage of the inverter $V_{AB} = 0$ and $i_g < 0$, the switches S1 and S2 are ON. The current freewheels through any one of the switch and body diode based on the current direction.
- 5) **Mode V:** The terminal voltage of the inverter $V_{AB} = -0.5*V_{dc}$, the switches S2, S5 & S6 are ON. The current flows from source to grid and vice-versa. In this mode the capacitor C2 is connected in parallel with the grid.
- 6) **Mode VI:** The terminal voltage of the inverter $V_{AB} = -V_{dc}$, switches S2, S3 & S6 are ON. The current flows from the source to the grid and vice-versa. In this mode the two DC-link capacitors are connected in series and they are in parallel with the grid.

TABLE I. SWITCHING OF THE FIVE-LEVEL INVERTER

Modes of operation		Switching states					
		S1	S2	S3	S4	S5	S6
Positive	V_{dc}	1	0	0	1	1	0
	$0.5V_{dc}$	0	0	0	1	1	1
Zero	$i_g > 0$	0	0	1	1	0	0
	$i_g < 0$	1	1	0	0	0	0
Negative	$-0.5V_{dc}$	0	1	0	0	1	1
	$-V_{dc}$	0	1	1	0	0	1

Thus, the proposed inverter is able to produce five-level output and also provides the bi-directional current path in each mode which enhances the inverter operation in both positive and negative power regions without disturbing output level voltage. The SPWM scheme is employed for the generation of gate pulses to the inverter switches. The switches S5 and S6 are operating with the grid frequency and the remaining switches are operating other than the grid frequency as shown in Fig. 3. Moreover, the switch S5 is turned on in both $0.5V_{dc}$ and V_{dc} levels to make ready the switch for the next instant. Similarly, the switch S6 is turned on in both $-0.5V_{dc}$ and $-V_{dc}$ levels during negative half-cycle. Further to provide bi-directional current path irrespective of the voltage polarity these (S5 and S6) are ON during $\pm 0.5V_{dc}$ levels. The dead-time issues in the proposed inverter is not present because of the absence of complementary switching action within the same leg.

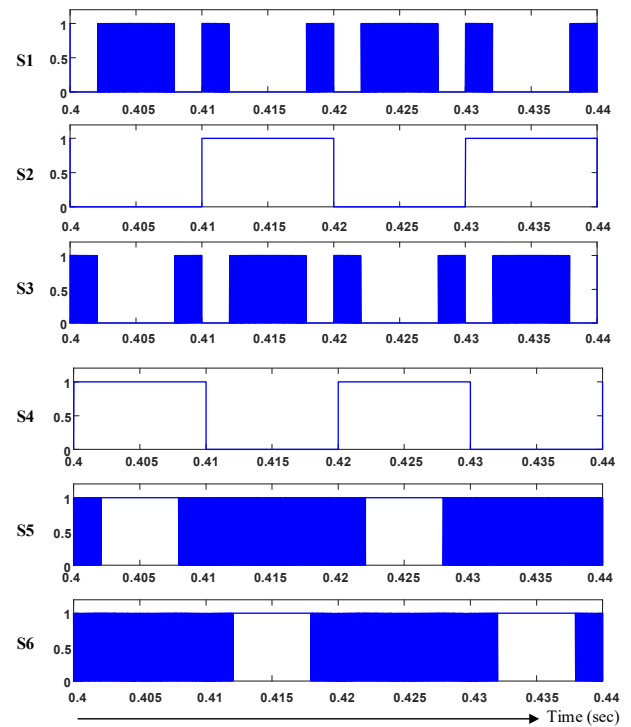


Fig. 3. Gate pulses for the five-level inverter.

III. CMV ANALYSIS

From the analysis given in the reference [12], the total CMV (V_{tcmv}) and the asymmetrical voltage (V_{S1}) are as shown in Eqs. 1 and 2 respectively. Where, V_{CM} and V_{DM} are the common mode and differential mode voltages respectively. V_{CM} and V_{DM} in terms of inverter terminal voltages (V_{AN} and V_{BN}) are shown in the Eqs. 3 and 4. The calculated values of all the voltages are given in Table. II and it is noted that the V_{tcmv} has only the grid frequency (50Hz) variations.

$$V_{tcmv} = V_{CM} + V_{S1} \quad (1)$$

$$V_{S1} = -V_{DM} / 2 \quad (2)$$

$$V_{CM} = 0.5(V_{AN} + V_{BN}) \quad (3)$$

$$V_{DM} = V_{AN} - V_{BN} \quad (4)$$

$$i_{leakage} = C_{PV} \frac{dV_{tcmv}}{dt} \quad (5)$$

TABLE II. TOTAL COMMON MODE VOLTAGE CALCULATION

Level	V_{AN}	V_{BN}	V_{dm}	V_{cm}	V_{S1}	V_{tcmv}
V_{dc}	V_{dc}	0	V_{dc}	$0.5 V_{dc}$	$-0.5 V_{dc}$	0
$0.5V_{dc}$	$0.5V_{dc}$	0	$0.5 V_{dc}$	$0.25 V_{dc}$	$-0.25 V_{dc}$	0
0	0	0	0	0	0	0
0	V_{dc}	V_{dc}	0	V_{dc}	0	V_{dc}
$-0.5V_{dc}$	$0.5V_{dc}$	V_{dc}	$-0.5 V_{dc}$	$0.75 V_{dc}$	$0.25 V_{dc}$	V_{dc}
$-V_{dc}$	0	V_{dc}	$-V_{dc}$	$0.5 V_{dc}$	$0.5 V_{dc}$	V_{dc}

From Eq. 5, it is identified that the leakage current ($i_{leakage}$) magnitude is directly proportional to the rate of change of total common mode voltage and the magnitude of PV parasitic capacitance (C_{PV}). In general, the magnitude C_{PV} is in the range of several pico farads to few micro farads and it depends on the environmental conditions [13]. Hence, it is obvious that the reduction of leakage current is only possible by limiting the high-frequency variations in the V_{tcmv} . Since, the proposed five-level inverter and its modulation scheme eliminates the high-frequency oscillations in the V_{tcmv} , the magnitude of leakage current is negligible.

IV. SIMULATION RESULTS

To evaluate the performance of the single-phase multi-string PV inverter, simulation studies are carried by using PSIM and MATLAB tools. Two equally rated PV strings are emulated as dc sources. The soft-switched multi-output boost converter is integrated with each dc source to boost the voltage to grid peak level. Further it is connected to the proposed five-level inverter. Moreover, the inverter operation is verified under unity, lagging and leading power factor conditions of the grid; along with that V_{tcmv} and $i_{leakage}$ are also illustrated to validate the reduction of the leakage current under different power factor conditions of the grid. Different ratings selected for the proposed inverter are shown in Table. III.

TABLE III. SYSTEM PARAMETERS

S.No	Parameter	Range
1	Power	500W
2	PV voltage	100V each string
3	Grid voltage	230V, 50Hz
4	Switching Frequency f_s	20000 KHz
5	Capacitors $C1$, $C2$ and $C3$	100 μ F
6	Capacitors C_r , C_s and C_{PV}	10 nF, 100 nF, 10 pF
7	Inductors L_b and L_r	1 mH, 10 μ H
8	Filter elements L_f and C_f	8 mH, 2 μ F

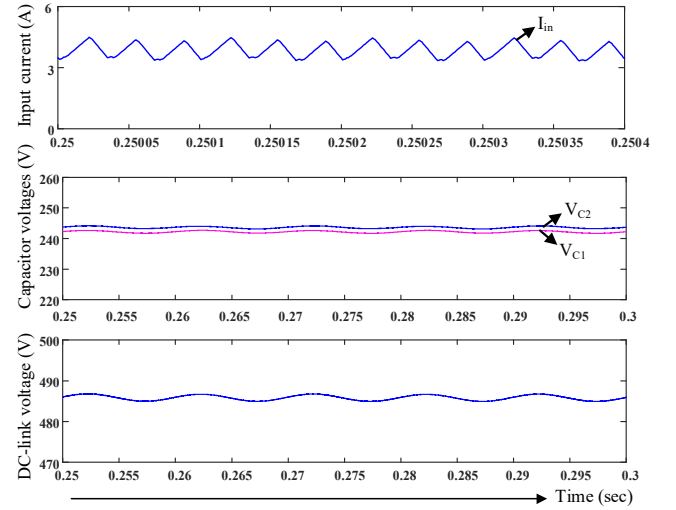


Fig. 4. Waveforms for the multi-output boost converter: (a) Inductor current, (b) DC-link capacitor voltages of the two strings, (c) DC-link voltage.

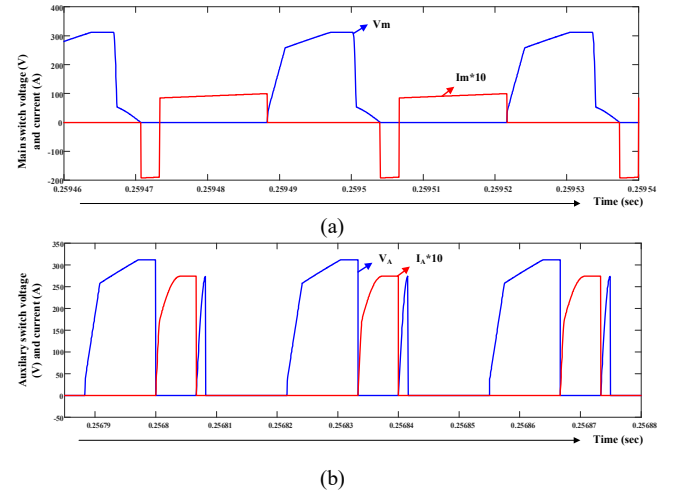


Fig. 5. Soft-switching waveforms for the multi-output boost converter: (a) Voltage and current waveforms of the main switch, (b) Voltage and current waveforms of the auxiliary switch.

Fig. 4 illustrates the inductor current, voltages across $C1$ & $C2$ and total DC-link voltage waveforms of the multi-output boost converter. The voltage and current waveforms of the main and auxiliary switches are illustrated in Fig. 5,

which confirms that the additional resonant circuit effectively eliminates the switching losses of the multi-output boost converter. Further, the output waveforms of the inverter under different power factor operations of the grid are illustrated in Figs. 6 and 7. The bi-directional current path provided by the inverter and modified SPWM scheme enhances the operation of the proposed inverter during non-unity power factor conditions of the grid without increasing the THD. Also, the high-frequency variations are eliminated in the V_{icmv} results in the leakage current of less than 30 mA. However, small spikes are present in the leakage current due to sudden transitions in the V_{icmv} from V_{dc} to zero and vice-versa.

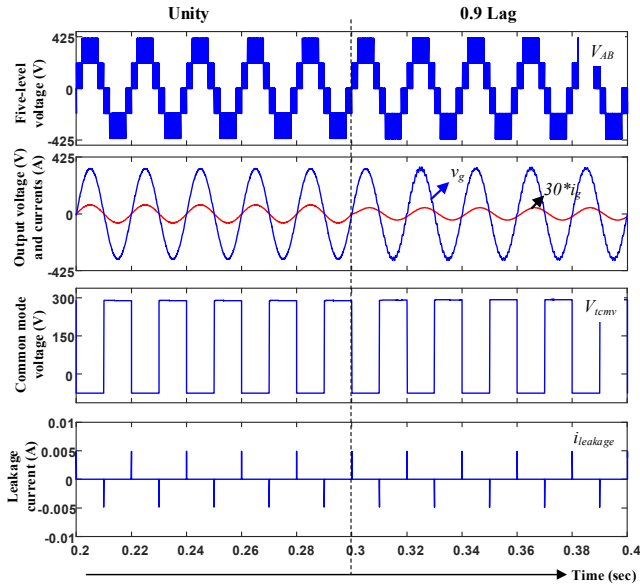


Fig. 6. Voltage and current waveforms of the inverter during power factor changes from unity to lagging.

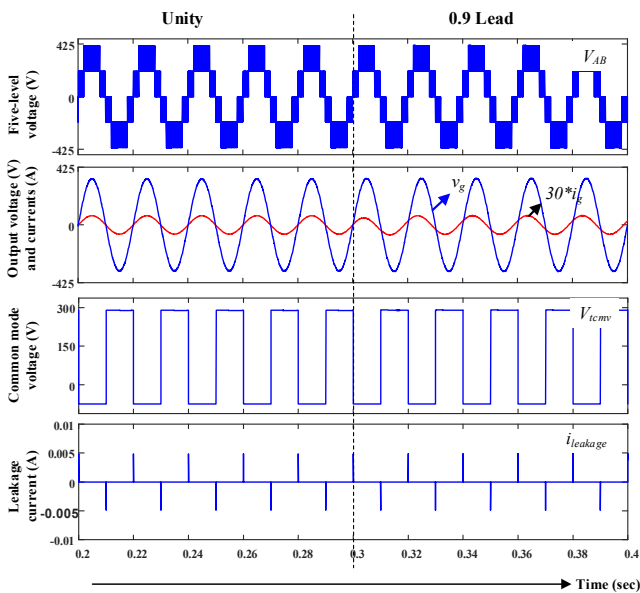


Fig. 7. Voltage and current waveforms of the inverter during power factor changes from unity to leading.

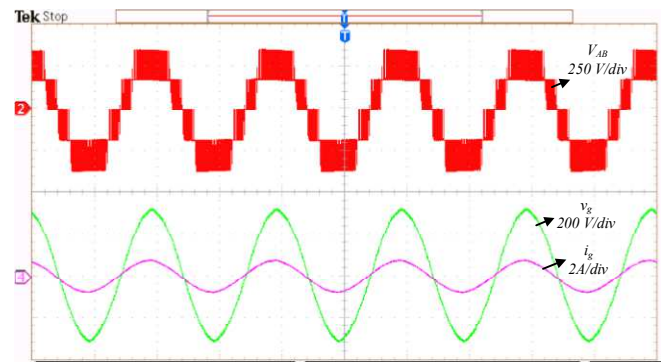


Fig. 8. Experimental result of the inverter under unity power factor (V_{AB} , v_g and i_g).

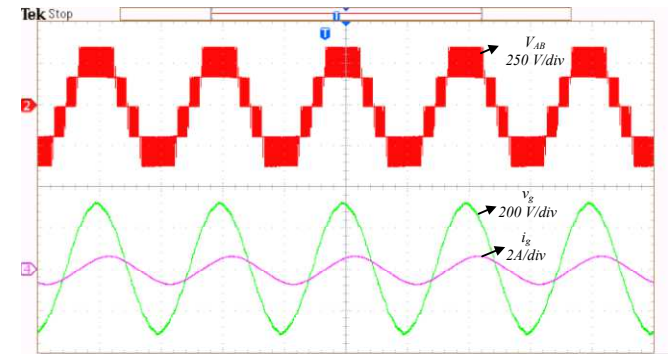


Fig. 9. Experimental result of the inverter under 0.9 lagging power factor (V_{AB} , v_g and i_g).

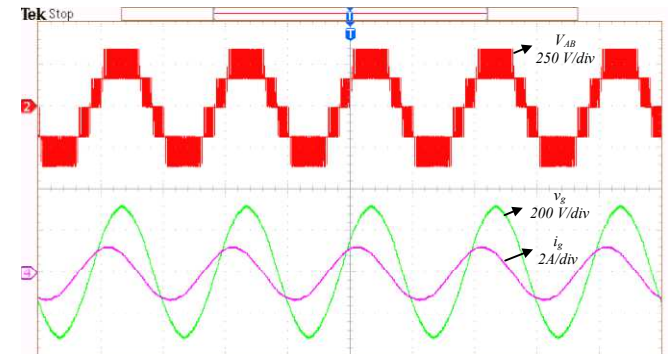


Fig. 10. Experimental result of the inverter under 0.9 leading power factor (V_{AB} , v_g and i_g).

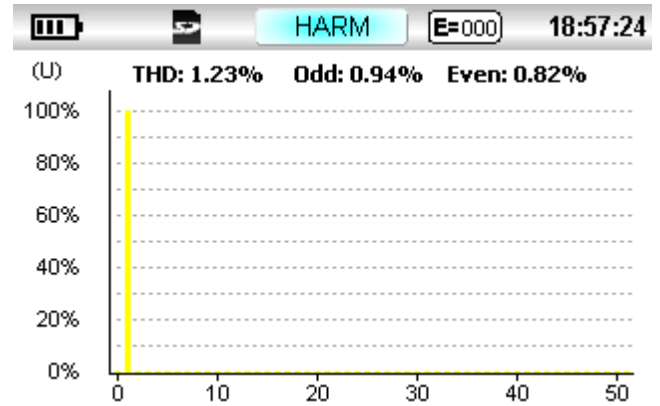


Fig. 11. FFT spectrum of the output voltage.

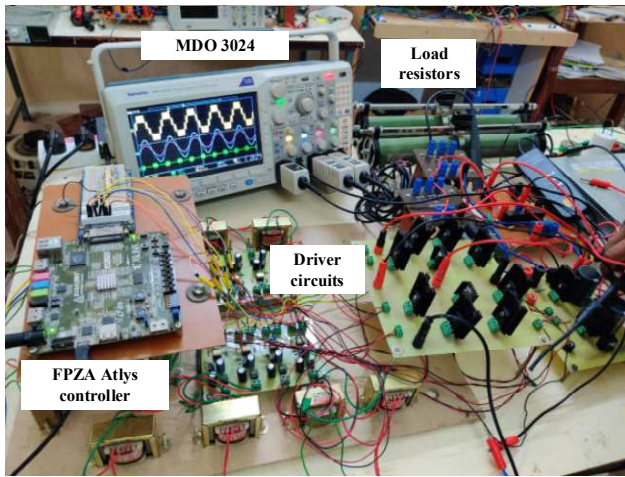


Fig. 12. Experimental setup.

Further the experimental results of the proposed multi-string inverter under unity, lagging and leading power factor conditions are illustrated in Figs. 8 to 10 respectively. As per the revised grid standards, the reactive power capability for the grid-connected inverters is one of the important requisite [14] and it is well proved with the proposed inverter. Also, the FFT spectrum of the output voltage under unity power factor is shown fig. 11, which is well below the grid standards. From the simulation and experimental results it is concluded that the proposed five-level inverter and modified SPWM scheme enhances the inverter operation under different power conditions of the grid.

V. CONCLUSION

In this paper, a single-phase asymmetrical inductor based five-level transformerless inverter is proposed for the multi-string PV applications. A soft-switched multi-output boost converter with enhanced efficiency is integrated to the five-level inverter for obtaining the improved overall performance of the PV system. The inverter produces five-level output voltage without any distortions during the non-unity operating conditions of the grid. Moreover, the magnitude of the leakage current is reduced by eliminating the high frequency oscillations in the CMV. Further the inverter utilizes only two switches in any mode of operation to realize the five-level output which results in lower switching and conduction losses. Finally, the simulation and experimental results are presented to validate the performance of the proposed inverter. The detailed loss analysis and grid-integration with multi-string PV systems will be investigated in the extended version of the manuscript.

REFERENCES

- [1] O.P. Mahela and A.G. Shaik, "Comprehensive overview of grid interfaced solar photovoltaic systems", *Renewable and Sustainable Energy Reviews*, vol. 68, pp.316-332, Feb. 2017.
- [2] B. Mirafzal and A. Adib, "On grid-interactive smart inverters: Features and advancements", *IEEE Access*, 8, pp.160526-160536, Sep. 2020.

- [3] S. Kouro, JI Leon, D Vinnikov and LG Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology", *IEEE Industrial Electronics Magazine*, vol. 9(1), pp. 47-61, Mar 2015.
- [4] S.B. Kjaer, J.K. Pedersen and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules", *IEEE transactions on industry applications*, vol. 41(5), pp.1292-1306, Sep. 2005.
- [5] V. Sonti, S. Jain, V. Agarwal and S. Bhattacharya, "Terminal voltage analysis for the transformerless PV inverter topologies in a single-phase system", *IET Renewable Power Generation*, vol. 13(15), pp.2723-2739, Aug. 2019.
- [6] Z. Ahmad and S.N. Singh, "Comparative analysis of single phase transformerless inverter topologies for grid connected PV system", *Solar Energy*, vol. 149, pp.245-271, Jun. 2017.
- [7] X. Zhang, T. Zhao, W. Mao, D. Tan and L. Chang, "Multilevel inverters for grid-connected photovoltaic applications: Examining emerging trends", *IEEE Power Electronics Magazine*, vol. 5(4), pp.32-41, Dec. 2018.
- [8] N.A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application", *IEEE transactions on industrial electronics*, vol. 57(6), pp.2111-2123, Oct. 2010.
- [9] A.I. Ali, E.E. Mohamed, M.A. Sayed and M.S. Saeed, "Novel single-phase nine-level PWM inverter for grid connected solar PV farms", *In proceedings of International Conference on Innovative Trends in Computer Engineering (ITCE)*, pp. 345-440, Feb. 2018.
- [10] Y.H. Liao and C.M. Lai, "Newly-constructed simplified single-phase multistring multilevel inverter topology for distributed energy resources", *IEEE Transactions on Power Electronics*, vol. 26(9), pp.2386-2392, May. 2011.
- [11] S. Raghavendran and B. Chitti babu, "Performance Improvement of Soft Switching DC-DC Boost Converter for Photovoltaic (PV) Applications", *Journal of Low Power Electronics*, vol. 10(1), pp.58-64, Mar. 2014.
- [12] K. Sateesh Kumar, A. Kirubakaran and N. Subrahmanyam, "Bidirectional Clamping-Based H5, HERIC, and H6 Transformerless Inverter Topologies With Reactive Power Capability", *IEEE Transactions on Industry Applications*, vol. 56(5), pp.5119-5128, Jun. 2020.
- [13] W. Chen, X. Yang, W. Zhang and X. Song, "Leakage current calculation for PV inverter system based on a parasitic capacitor model", *IEEE Transactions on Power Electronics*, vol. 31(12), pp.8205-8217, Jan. 2016.
- [14] H. Zhao, N. Wu, S. Fan, Y. Gao, L. Liu, Z. Zaho and X. Liu, "Research on low voltage ride through control of PV grid-connected inverter under unbalance fault", In Chinese Automation congress, pp. 3991-3996, Oct. 2017.