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A Novel SVPWM algorithm for five level flying capacitor configuration

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***Abstract*—A novel SVPWM algorithm for 5 level flying capacitor multilevel inverter topology has been presented in this paper. The algorithm is based on vector mapping technique which can easily determine the location of reference vector, calculate ON-times, select the switching sequence and can be extended to n-levels. This PWM scheme employs a single carrier wave and multiple modulating waves. The proposed algorithm is simulated using MATLAB/ Simulink environment and and the results are presented.**

Keywords—Space vector modulation, flying capacitor, multilevel operation, THD analysis, ma.

I. INTRODUCTION

Several multilevel inverter topologies have achieved widespread interests amongst researchers because they have the qualities of reaching high voltage with low voltage rating components. David Prince published an article in the GE Review titled "The Inverter"[1] around 1925. It was visualized to be a device that functions like a rectifier but operated in an inverted mode, hence the name inverter. But the conventional inverters have the disadvantage of lower output voltage and higher harmonic distortion. To overcome these drawbacks, research was carried out to improve PWM techniques themselves. In 1981, Akira Nabae introduced the concept of multilevel inverters. Use of multilevel inverters can eliminate the requirement of step up transformer and decrease the harmonics in the output. Multilevel inverter was initially introduced for decreasing the harmonics in the output waveform. It was also observed by Nabae [2] that in a multilevel inverter the DC bus voltage could be enhanced above the voltage rating of an single power device by the usage of a voltage clamping network containing diodes. The advantages of a multilevel inverter with more than three levels, with respect to harmonic reduction was presented by Bhagwat [7]. Neutral point clamped topology has the drawback of unbalanced DC link voltage, indirect clamping of inner devices, multiple blocking voltages of clamping diodes and complexity in controlling real power flow for individual converter etc[3],[4]. The enhancement of the inverter KVA rating above the limits of an individual device was further analyzed by Carpita [10] where the idea of using clamping diodes was extended to higher number of levels. Meynard [5] proposed a multilevel inverter topology where voltage clamping was obtained by using clamping capacitors instead of clamping diodes. The use of capacitors permits several switching combinations for a particular voltage level generation, which may be used for preferential charging and discharging of capacitors.

The usage of the transformer-less multilevel inverter has lead to the development of various pulse width modulation (PWM) schemes to control the switching of the active devices. Since Bhagwat and Stefanovic [7] introduced the idea of the multilevel PWM converter, various modulation strategies have been developed and studied in detail [7]–[9]. Among these schemes, space-vector modulation (SVM) is highly efficient because it offers flexibility in optimizing switching waveforms [11]–[13] and can be easily implemented on a digital platform. This paper proposes a new SVPWM algorithm for 5 level flying capacitor multilevel inverter topology.

II. FLYING CAPACITOR TOPOLOGY

This topology uses capacitor to divide the input DC voltage thereby limiting the voltage across the switches. Thus the blocking capacity required for the switches decreases resulting in lower rating of switches and reduced power loss. The output waveform is improved decreasing the filter requirements.

For a 5-level flying capacitor multilevel inverter, number of switches per leg are 8, number of balancing capacitors are 6, number of DC link capacitors are 4.The below figure shows a five level flying capacitor multilevel inverter.

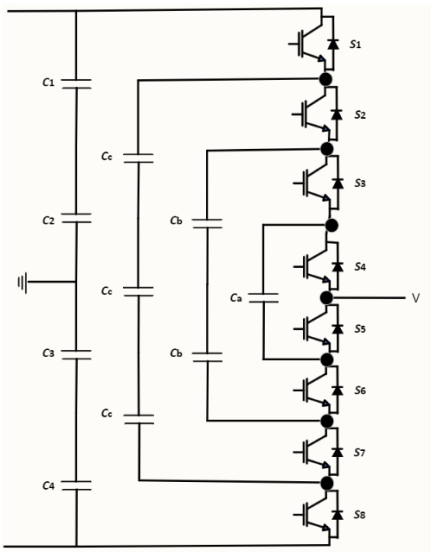

Fig. 1. Single leg diagram for 5 level FCMLI

The below table shows the switching states for a 5-level flying capacitor clamped multilevel inverter.

TABLE I. SWITCHING STATES AND THEIR RELATIONS FOR 5-LEVEL

STATE	OUTPUT VOLTAGE	S1	S2	S3	S4
4	E	ON	ON	ON	ON
3	E/2	ON	ON	ON	OFF
2	0	ON	ON	OFF	OFF
1	-E/2	ON	OFF	OFF	OFF
0	-E	OFF	OFF	OFF	OFF

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III. ALGORITHM

The main idea for this algorithm comes from the fact that the shapes of 6 regions are identically same and symmetric about many axes [14]. Therefore there exists some relation between their switching sequences and on times allocations. By careful mathematical analysis, if these relations are deduced, on times for the switches can be calculated in certain pre-determined region (say region 1) irrespective of region in which the instantaneous reference space vector is located. And then map them back into its original region of location. The relations are explained clearly in further sections.

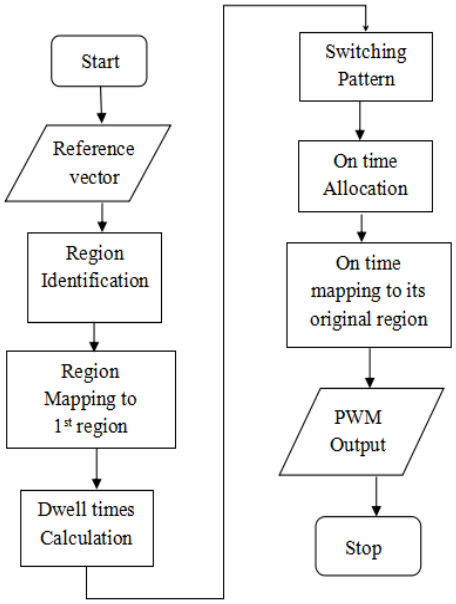

Fig. 2. Flow chart for proposed SVPWM algorithm

A. SPACE VECTOR

A 5 level inverter single leg has 8 switches and has 5 switching states namely 0, 1, 2, 3, 4 as shown in TABLE I. So on the whole, there exist 125 switching states in three-phase five-level converter, out of which 120 are active states and 5 are zero states. Each of these combinations is represented by a space vector.

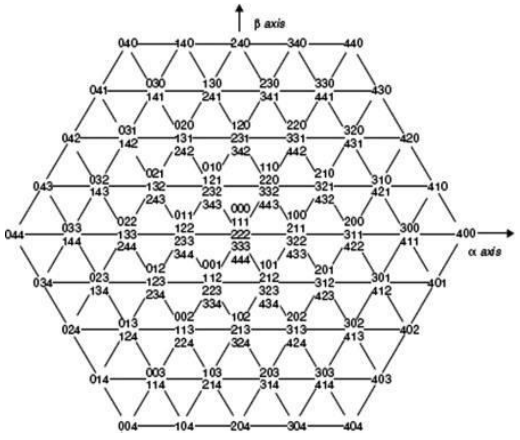

Fig. 3. Space vector diagram for 5 level

The space vector diagram of 5 level for region 1 is shown in the below figure.

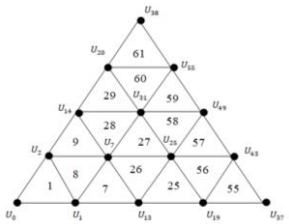

Fig . 4. Sectors in region 1

Then the instantaneous reference space vector is mapped to region 1 and the sector is identified using the below procedure.

Consider a reference vector r in region 1. It is projected onto 2 axes, 60 degrees apart. Let the vector along a phase axis be p and along negated c phase axis be q. Therefore p and q vectors are obtained as follows.

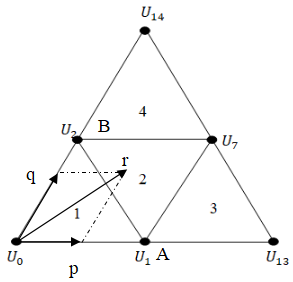

Fig. 5. Reference vector in region 1

$$m_a = \frac{V_{ref}}{\frac{2}{3}V_{dc}} \qquad (1)$$

$$p = \frac{2}{\sqrt{3}} * r * \sin\left(\frac{\pi}{3} - \phi\right) \qquad (2)$$

$$q = \frac{2}{\sqrt{3}} * r * \sin(\phi) \qquad (3)$$

From the above figure, it is observed that the locus of line AB is p+q=0.5.

TABLE II SUB-REGION IDENTIFICATION

Sub-region	p	q	p+ q
1	≤0.5	≤0.5	≤0.5
3	>0.5	-	-
2	≤0.5	≤0.5	>0.5
4	-	>0.5	-

After deciding the sub-region, two new variables namely, p1and q1 are defined to identify the sector in the sub-region.

a) For sub-region 1, p1=p and q1=q.

TABLE III SECTOR IDENTIFICATION IN SUB-REGION 1

Sector	p1	q1	p1+ q1
1	≤0.25	≤0.25	≤0.25
7	>0.25	-	-
8	≤0.25	≤0.25	>0.25
9	-	>0.25	-

b) For sub-region 2, p1=p-0.5 and q1=q-0.5.

TABLE IV SECTOR IDENTIFICATION IN SUB-REGION 2

Sector	p1	q1	p1+ q1
58	≥-0.25	≥-0.25	≥-0.25
26	-	≤-0.25	-

27	≥-0.25	≥-0.25	<-0.25
28	≤-0.25	-	-

c) For sub-region 3, p1=p-0.5 and q1=q.

TABLE V SECTOR IDENTIFICATION IN SUB-REGION 3

Sector	p1	q1	p1+ q1
25	≤0.25	≤0.25	≤0.25
55	>0.25	-	-
56	≤0.25	≤0.25	>0.25
57	-	>0.25	-

d) For sub-region 4, p1=p and q1=q-0.5.

TABLE VI SECTOR IDENTIFICATION IN SUB-REGION 4

Sector	p1	q1	p1+ q1
29	≤0.25	≤0.25	≤0.25
59	>0.25	-	-
60	≤0.25	≤0.25	>0.25
61	-	>0.25	-

B. DWELL TIME CALCULATION

The dwell times are calculated using volt-second balance equation as below,

$$V_{REF}T_S = V_0T_A + V_1T_B + V_2T_C$$
$$T_S = T_A + T_B + T_C$$

On solving the above equations, we get

$$T_A = T_S - \frac{8}{\sqrt{3}} * r * T_S * sin\left(\frac{\pi}{3} - \phi\right) \quad (4)$$

$$T_B = \frac{8}{\sqrt{3}} * r * T_S cos\left(\frac{\pi}{6} - \phi\right) \quad (5)$$

$$T_C = \frac{8}{\sqrt{3}} * r * T_S * sin(\phi) \quad (6)$$

Using the same procedure, the dwell times for other sectors of region1 are calculated.

C. SWITCHING SEQUENCE ARRANGEMENT

If the dwell times are calculated out, the switching sequence has to be determined. Based on the conditions explained before, the switching sequences for 5 level can be obtained as below,

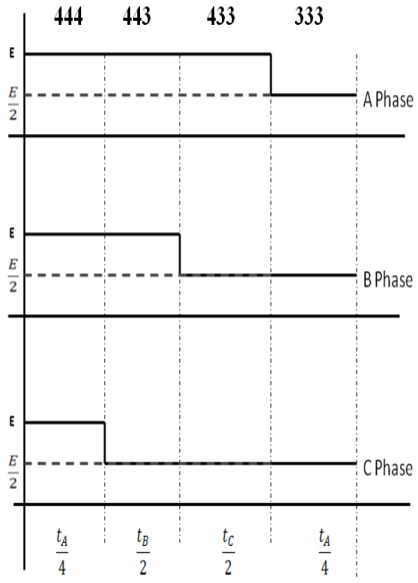

Fig. 6. SWITCHING SEQUENCE FOR SECTOR 1

The switching sequences in the sectors of region 1 are arranged as follows

TABLE VII SWITCHING SEQUENCES OF REGION-1

SECTOR	SWITCHING SEQUENCE
1	444-443-433-333
8	433-432-332-322
7	433-432-422-322
26	422-421-321-311
25	422-421-411-311
56	411-410-310-300
55	411-410-400-300
9	443-442-432-332
28	432-431-331-321
27	432-431-421-321
58	421-420-320-310
57	421-420-410-310
29	442-441-431-331
60	431-430-330-320
59	431-430-420-320
61	441-440-430-330

After designing the optimum switching sequence, the on times of the switches are calculated from Fig 6.

TABLE VIII ON TIMES OF SWITCHES FOR SECTOR 1

Phase A		Phase B		Phase C	
1A	$T_S/2$	1B	$T_S/2$	1C	$T_S/2$
2A	$T_S/2$	2B	$T_S/2$	2C	$T_S/2$
3A	$T_S/2$	3B	$T_S/2$	3C	$T_S/2$
4A	$T_S/2-T_A/4$	4B	$T_C/2+T_A/4$	4C	$T_A/4$

D. ON TIME MAPPING

Once the on times of switches corresponding to region1 are calculated out, they are mapped back into their original region of location using voltage shifting and reversal.

TABLE IX RELATIONSHIPS BETWEEN PHASE VOLTAGES OF REFERENCE VECTOR CORRESPONDING TO ALL REGIONS

REGION	PHASE VOLTAGE A	PHASE VOLTAGE B	PHASE VOLTAGE C
A	Vao	Vbo	Vco
B	-Vbo	-Vco	-Vao
C	Vco	Vao	Vbo
D	-Vao	-Vbo	-Vco
E	Vbo	Vco	Vao
F	-Vco	-Vao	Vbo

The voltage shifting can be easily done by replacing the present

PWM signals with the new shifted phase voltage PWM signals.The voltage reversal can be done by mirroring the PWM signals of corresponding switches, as shown in the below table

TABLE X MIRRORING OF PWM SIGNALS

V_O	ON TIMES			
	S1	S2	S3	S4
U	PWM_S1	PWM_S2	PWM_S3	PWM_S4
-U	$\frac{T_S}{2}$ – PWM_S4	$\frac{T_S}{2}$ – PWM_S3	$\frac{T_S}{2}$ – PWM_S2	$\frac{T_S}{2}$ – PWM_S1

IV.MULTI LAYER OPERATION

The numbers of levels in the output voltage of a three phase 5-level FCMLI with SVPWM control strategy depends upon the amplitude modulation index (ma) keeping frequency modulation index (mf) constant. The table below shows the variation of levels with ma,

TABLE XI VARIATION OF OUTPUT LEVELS WITH ma

Number of output levels	**ma range**
2	$0<m_a<0.25$
3	$0.25<m_a<0.5$
4	$0.5<m_a<0.75$
5	$m_a>0.75$

V. SIMULATION RESULTS

The general block diagram of n-level SVPWM control circuit is shown below.

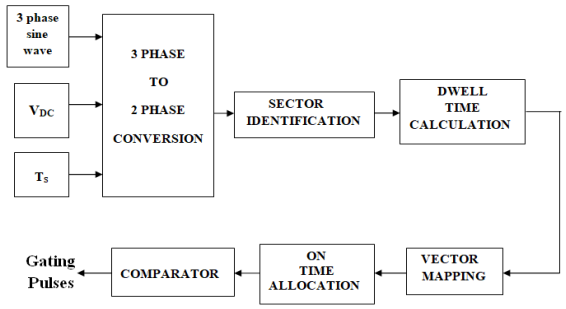

Fig. 7. Control Circuit Block Diagram

SIMULATION PARAMETERS

Amplitude modulation index m_a=0.8
Frequency modulation index m_f=10
DC link voltage V_{dc}=400
3 phase RLC load R= 5Ω; L=50mH ;C=10000μf

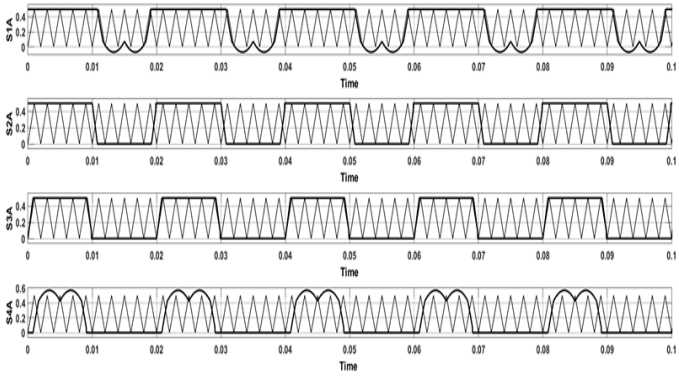

Fig. 8. Modulating and carrier(triangular)waveforms of switches S1A(first trace), S2A(second trace), S3A(third trace) and S4A(fourth trace)

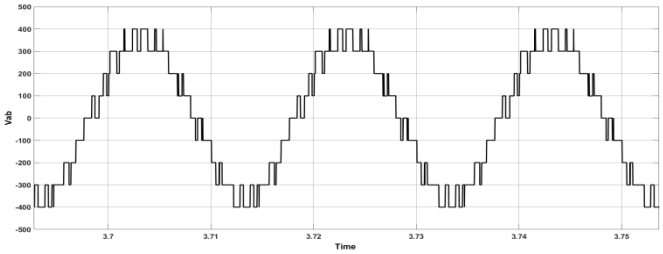

Fig. 9. Line voltage

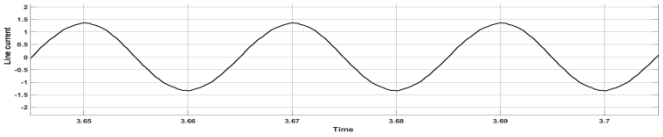

Fig. 10. Line current

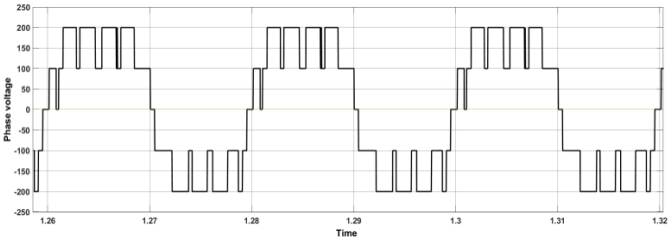

Fig. 11. Phase voltage

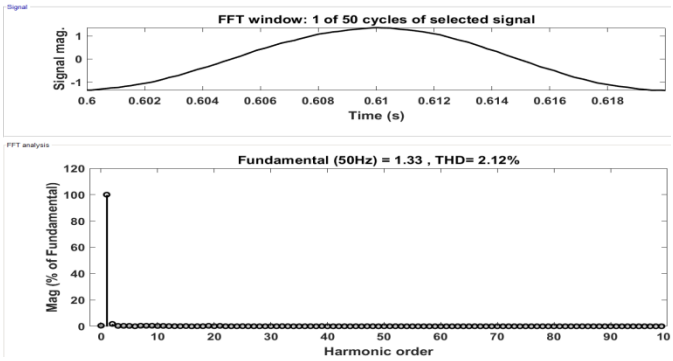

Fig. 12. Line current THD analysis

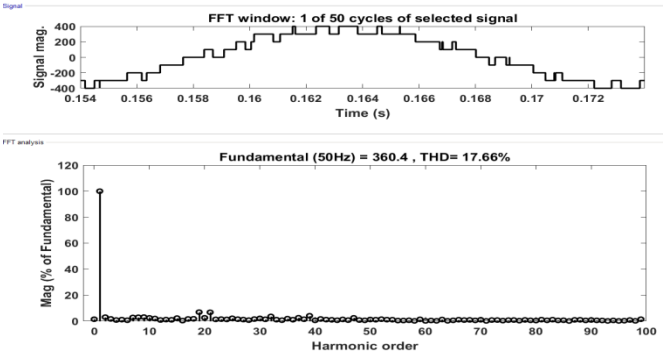

Fig. 13. Line voltage THD

analysis MULTI LAYER OPERATION

A. TWO LEVEL OPERATION

m_a range, $0<m_a<0.25$

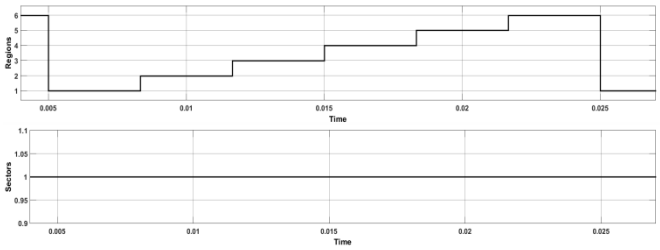

Fig 14 Regions and sector traced by tip of Vref for 2 level operation

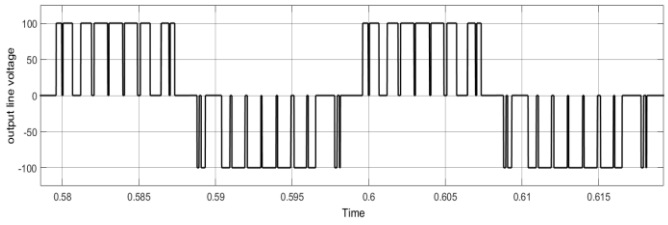

Fig. 15. Line voltage for ma

B. =0.2 THREE LEVEL OPERATION

m_a range, $0.25<m_a<0.5$

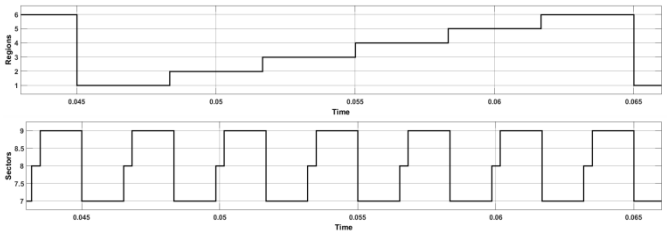

Fig. 16. Regions and sector traced by tip of V_{ref} for 3 level operation

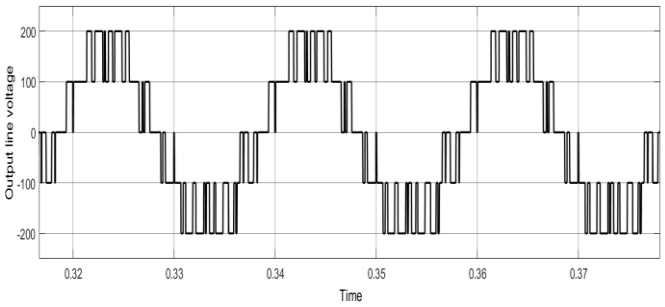

Fig. 17. Line voltage for ma =0.4

C. FOUR LEVEL OPERATION

ma range, 0.5< ma <0.75

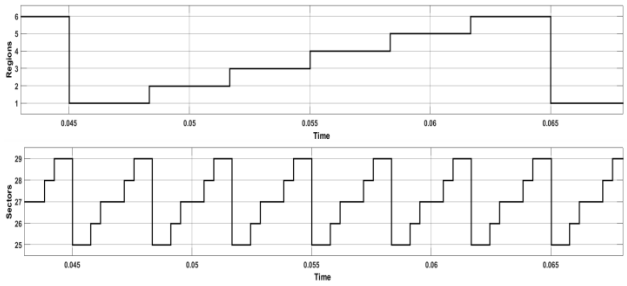

Fig. 18. Regions and sector traced by tip of Vref for 4 level operation

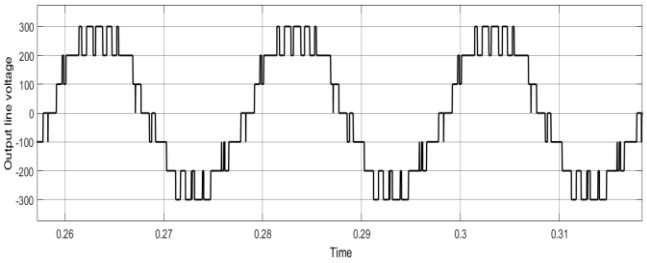

Fig. 19. Line voltage for ma

D. =0.6 FIVE LEVEL OPERATION

m_a range,m_a>0.75

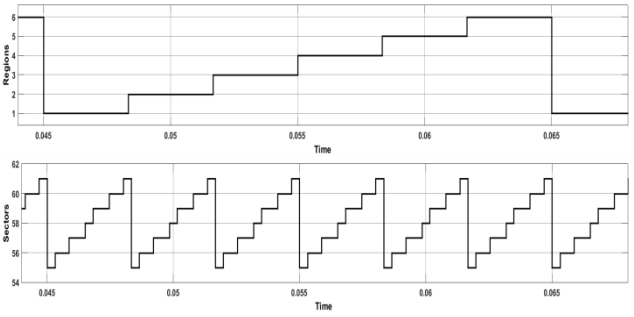

Fig. 20. Regions and sector traced by tip of Vref for 5 level operation

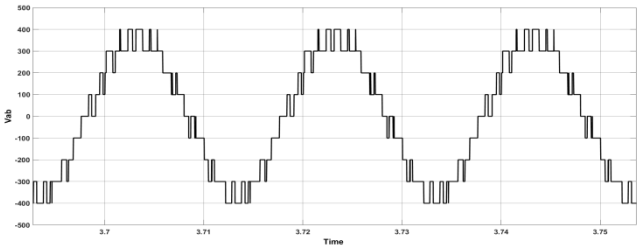

Fig. 21. Line voltage for ma=0.8

E. OVERMODULATION

m_a range,m_a>1

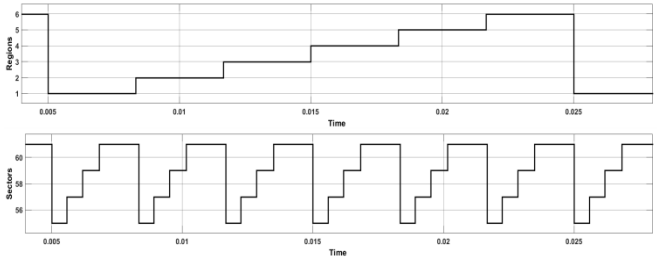

Fig. 22. Regions and sector traced by tip of Vref for over modulation

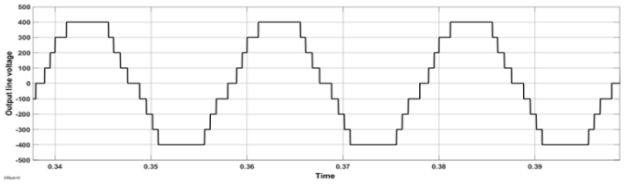

Fig. 23. Line voltage for ma=1.2

VI.CONCLUSIONS

In this paper, the simulation of 5 level FCMLI based on SVPWM technique is presented and analyzed in detail. It can be concluded that, as the number of levels increased, the output waveform is nearer to sinusoidal and this resulted in lower output THD and improved fundamental voltage.

TABLE XII COMPARISION OF VARIOUS MULTI LEVEL OPERATION

ma	Number of output levels	Fundamental voltage(volts)	Line voltage THD (%)
0.2	2	92.4	61.72
0.4	3	175.7	37.30
0.6	4	279.8	20.8
0.8	5	360.4	17.66
1.2	5	429	11.75

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