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DC-Link Current Ripple Reduction in Switched Reluctance Machine Drives

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***Abstract*—Because the dc-link current is created during phase commutation in low-frequency harmonics, switched reluctance machine (SRM) drives necessitate a significant dc-link capacitor. Putting in a large the cost of the drive is greatly influenced by the capacitor bank in the drive and total volumetric power density. The purpose of this section is to analyze SRM's dc-link current ripple and present a control technique to minimize dc-link current ripple while maintaining machine operating performance. The suggested approach uses a high-pass filter to extract the ripple components of the dc-link current. The controller makes certain that ripple power circulates between phases, lowering the dc supply's pulsating energy demand. The dc-link ripple is reduced over a broad speed range allows for efficient and dependable drive operation without the addition of any additional hardware system. The proposed control technique's effectiveness for both steady-state and transient conditions using simulation outcomes.**

***Index Terms*—Control algorithm, ripple in dc-link current, switched reluctance machine (SRM), ripple in torque.**

I. INTRODUCTION

SWITCHED reluctance machines (SRMs) are becoming increasingly popular in the automotive industry such as electric vehicle (EV) and hybrid EV (HEV)applications because of numerous benefits such as minimal cost, high starting torque, ease of manufacture, torque–inertia ratio that is quite high, toughness, and Having the capacity to operate at various speeds when in comparison in comparison to other forms of electric machinery [1–3].In addition, SRMs' fault-tolerant characteristics allow for efficient and reliable operation in tough areas such as automotive and aerospace.

Despite their many advantages, SRMs are slow behind Because of their very nonlinear and asymmetric torque generation method, on torque ripple requirements [4]. Furthermore, SRMs have increased vibration and acoustic noise, as well as large dc-link current ripple at the inverter input. The significant dc-link current ripple necessitates the use a big dc-link capacitor, this raises the drive's size and cost while decreasing density of volumetric power. As a result, SRM applications are still restricted to applications requiring a high-power density per unit of volume.

In the literature, various techniques for reducing Current ripple on a dc-link for motor drive applications are investigated. [5] reduces dc current ripple by modifying the voltage on the dc bus proportionally to speed. To reduce the requirement for capacitance, the authors of [6] implemented a control technique that involves a change in input voltage to stabilize the dc-link voltage. The majority of common methods incorporating an additional power conversion stage (i.e., dc–dc converter) inductors or a boost converter can be used between the battery and inverter to adjust the input voltages and currents [7–9]. In [10], the authors describe a technique for power decoupling in which they use a parallel the dc-link capacitor serves as an active filtering step. [11], [12] proposed using complicated switching control algorithms analytical model for a dc-link current. The dc-link current ripple and the torque ripple are related issues discussed in [13].Lowering the dc-bus capacitor, the authors of [14] suggest a method of active filtering based on electronic switches and inductors. However, the met and more volume to incorporate the inductor, as well as increased switching loss when operating at high frequencies.

The creators of [15] discussed a method that combines PI and continuous control to decrease the ripple of dc input current in an SRM drive system with an integrated multiport power converter. The ripple current in the battery is reduced in [16] by inserting and operating a direct current–direct current intermediate stage between the battery and the inverter. [17] Proposes an SRM rotor arrangement based on reluctance profile that suppresses both the input current and the torque ripple. However, due to phase current distortion, the proposed system sacrifices the efficiency for high-speed operation. [18] Proposed a way of controlling that use less capacitance on the dc-link than conventional inverters. To reduce current harmonics, the phases' switching states are commutated causing the dc-link voltage to vary. In [19-20], described a fixed switching frequency predictive current control for SRM applications described with torque ripple and dc-link current ripple are both low. However, in order to attain decent results, this approach necessitates the use of high-bandwidth current and position sensors, which makes implementation difficult.

[21] Proposes a carrier-based PWM modulation approach grid applications to reduce ripple in a PWM inverter's dc-link. By modifying the carrier waveform, the technique can reduce ripple by approximately 20%. The dc-link current ripple is minimized in the literature by either adding more hardware configurations or optimizing the machine architecture. The first method is rigid in terms of volumetric power density, whereas the second way is machine-specific. This paper proposes an SRM drive closed-loop dc-link current ripple minimization technique that requires no additional hardware or software reconfiguration. The proposed method only senses the input dc-link current, and the phase currents are shaped to reduce dc-link current fluctuations and ripple elements. The proposed control minimizes the capacitor demand, which reduces the size of the inverter and enhances the system's total volumetric power density. Furthermore, the machine's performance is unaffected while the system is running.

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The remainder of the article is structured as follows: Section II goes over the SRM drive system. Section III explains the cause of ripple in dc-link current. Section IV also describes control algorithm presented. The SRM modeling machine is described in Section V. Section VI describes the current controller's design. The simulation results are displayed in Section VII. Section VIII describes the conclusions of this work.

II. SRM DRIVE SYSTEM

It is shown in Fig.1 that a typical four-phase SRM drive setup is depicted. Using an asymmetric half bridge inverter, phase currents can be supplied to particular machine phases. Controlling the SRM's operation can be accomplished in a number of methods, including torque, power, and speed control. In order to maintain the predetermined speed, the speed controller establishes the reference current. An instantaneous reading of the rotor position is obtained by connecting a resolver to the machine shaft and a decoder to the resolution. For each phase, a commutation time interval is calculated using the angle of turn-on and angle of turn-off, and the reference current and speed are provided as inputs. Based on the measured phase currents and the reference current, a current control block generates the desired gate signals.

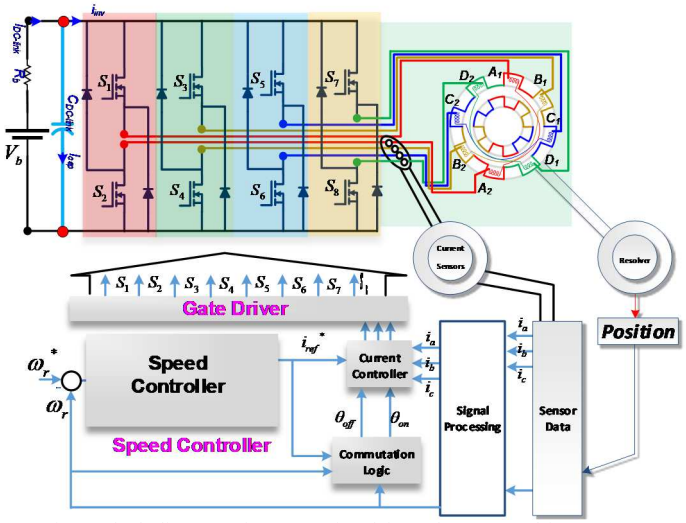

Fig.1. Block diagram of a conventional four-phase SRM drive system.

DC-link capacitors are installed between the inverter and the battery to absorb or provide the inverter's instantaneous ripple energy requirement during operation. Capacitor life depends on ripple current absorption; hence the dc-link capacitor's ripple current capability must be large. A greater capacitance value is required for increased ripple current capabilities. The capacitor bank's size can be reduced by reducing the ripple current. The majority of the system volume in high-power systems is taken up by dc-link capacitors. The DC-link ripple attenuation and suppression must be addressed in order to achieve an efficient and high volumetric power density design.

III.ORIGIN OF RIPPLE CURRENT IN SRM DRIVE

This section describes how the dc-link ripple current is calculated and analyzed, as well as how it refers to machine phase currents. By applying Kirchhoff's current law to the circuit depicted in Fig.1, the dc-link nodal current relation is given as follows.

$$i_{dc-link}(\mathrm{t}) = C_{dc-link}\frac{dv_c(\mathrm{t})}{dt} + i_{inverter}(t) \qquad (1)$$

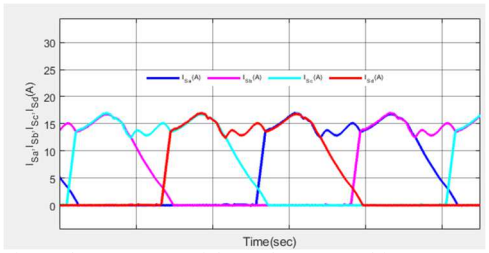

Fig.2. Phase currents of three-phase SRM drive systems.

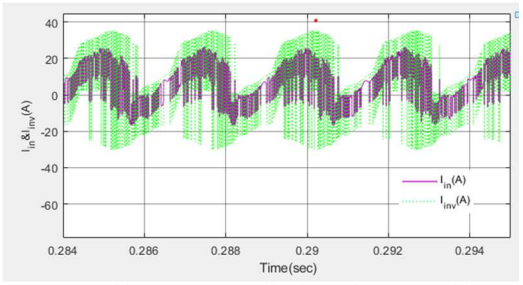

Fig.3. Inverter and battery current of a three-phase SRM drive system.

There is an inverter input current of $i_{inverter}(t)$ and an output battery current of $i_{dclink}(t)$ in this equation, and the capacitor node voltage is given by the expression $V_c(t)$. Fig.2 depicts machine phase current waveforms at machine base speed, In Fig.3, the battery and converter currents are displayed for comparison. An ideal voltage source and a series resistance can be used to represent dc-link current, which can be expressed in terms of battery and capacitor voltages.

$$i_{dc-link}(\mathrm{t}) = \frac{v_b(t)-v_c(t)}{R_b} \qquad (2)$$

A battery's voltage ($V_b(t)$) and resistance (R_b) are shown in this equation: one can use the differential equation generated by adding the fundamental voltage and current on the battery side to figure out how to link the inverter and battery currents together.

$$i_{dc-link}(\mathrm{t}) + R_b\, C_{dc-link}\frac{di_{dc-link}(\mathrm{t})}{dt} = i_{inverter}(t) \qquad (3)$$

As shown in Fig.2, the Fourier series given in Equation (4) [27] can be used to represent the phase current profiles. The m[th] order harmonics' magnitudes and phases are given by $c_m(T_{ref})$ and $\emptyset_{cm}(T_{ref})$, the reference torque level, and max (highest order harmonics incorporated into the model), respectively, while taking saturation effects into consideration,

$$i_k(\theta_a, T_{ref}) = c_0(T_{ref}) + \sum_{m=1}^{m_{max}} c_m(T_{ref})\sin\{m\,N_{rp}\theta_a + \emptyset_{cm}(T_{ref})\} \qquad (4)$$

The instantaneous switching function $s_k(t)$ and the phase currents i_k can be used to derive $i_{inverter}(t)$.

$$i_{inverter}(t) = \sum_{k=1}^{N_p} s_k(t) i_k\left(\theta_a, T_{ref}\right) \qquad (5)$$

where k represents the phase number and

$$S_k(\theta_a) = \begin{Bmatrix} 1, uring\ magnetization\ state \\ 0, during\ freewheeling\ state \\ -1, during\ demagnetization\ state \end{Bmatrix}$$

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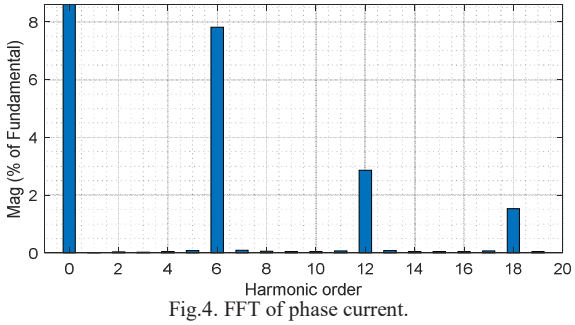

Fig.4. FFT of phase current.

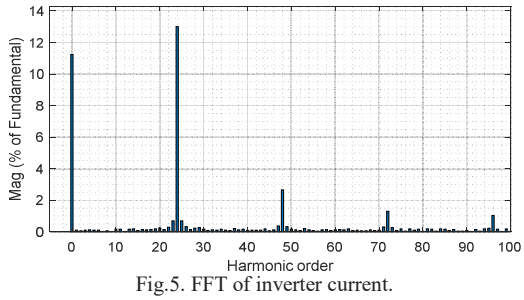

Fig.5. FFT of inverter current.

By combining (4) and (5), we can represent the inverter current in terms of its Fourier expansion as

$$i_{inverter}(t) = a_0(T_{ref}) + \sum_{n=1}^{\infty} a_n(T_{ref}) \sin\{nN_p N_{rp}\theta_a + \emptyset_{an}(T_{ref})\} \quad (6)$$

Because the $i_{inverter}(t)$ additionally includes switching harmonics, rather than only phase currents, the harmonic number n differs from m in this situation. For the number of rotor poles (N_{rp}) as well as for the number of phases (N_p) an FFT analysis is shown in Figs. 4 and 5, respectively. The dc-link current is obtained by solving the differential equation (3) with regard to inverter current harmonics (7)

$$i_{dc-link}(t) = a_0(T_{ref}) + \sum_{n=1}^{\infty} \frac{a_n}{\sqrt{1+n^2N_p^2N_{rp}^2\,\omega_a^2R_b^2C_{dc-link}^2}} \sin\{\emptyset\} \quad (7)$$

Where

$$\emptyset = nN_pN_{rp}\theta_a + \emptyset_{an}(\tau_{ref}) + tan^{-1}n\omega_nN_pN_{rp}R_bC_{dc-link}.$$

For both dc-link and inverter currents, there is no average current in the capacitor, which means that the dc component is the same in both cases. It gets a significant quantity when switching frequencies are high, i.e., $n^2N_p^2N_{rp}^2\,\omega_a^2R_b^2C_{dc-link}^2 \gg 1$, When switching frequencies are increased, harmonic content decreases. This can be achieved by using wide band gap devices that can handle greater switching frequencies. Consequently, harmonic content is insignificant at switching frequency, as shown by the following approximation:

$$\frac{a_n}{\sqrt{1+n^2N_p^2N_{\mathrm{rp}}^2\omega_a^2R_b^2C_{\mathrm{dc-link}}^2}} \approx \frac{a_n}{nN_pN_{\mathrm{rp}}\omega_aR_bC_{dc-link}} \propto \frac{a_n}{n\omega_a} \approx 0. \quad (8)$$

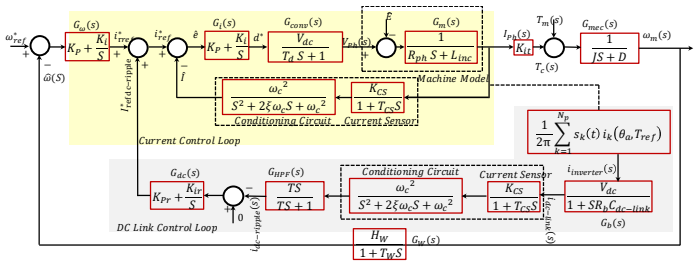

Fig.6. Overall control diagram including the proposed control loop.

Analysis performed in (4) through (8) demonstrates that the harmonic order of the dc-link current is primarily made up of the dc component and the multiple of N_pN_{rp}. When operating at low speeds, to provide and suppress the appropriate harmonic contents, a significant amount of dc-link capacitance is required. $n^2N_p^2N_{rp}^2\,\omega_a^2R_b^2C_{dc-link}^2 \ll 1$ and the inverter's dc-link current will reflect that harmonic content. Thus, (8) might be reworded as (9)

$$\frac{a_n}{\sqrt{1+n^2N_p^2N_{\mathrm{rp}}^2\omega_a^2R_b^2C_{\mathrm{dc-link}}^2}} \approx a_n \quad (9)$$

IV. DC-LINK RIPPLE MINIMIZATION ALGORITHM

Significant dc-link capacitance is required to prevent low-frequency dc link ripple current, which is an expensive and hefty solution. It is proposed in this work that a closed-loop control technique can be utilized to minimize low-frequency harmonics without affecting the torque density of the SRM. The updated SRM control technique for decreasing dc-link current ripple is shown in Fig.6. There is a smaller bandwidth and a lower average value generated by the outer speed control. To obtain dc-link ripple components, additional control loops are added to the standard speed control loop. There are three components to the control loop for the DC-link: A dc current sensor, a noise filtering circuit, and a post high-pass filter are all included. If there is an issue in the dc link current ripple, a PI controller is used to correct it. In order to generate a dynamic reference i_{ref}^*, the output signal from the speed controller block is added to the reference, Controllers for the dc-link and the dc-current link's ripple work in tandem.

$$i_{ref}^*(\theta, \omega_{\mathrm{ref}}) = \left[I_{Tref}^*(\omega_{\mathrm{actual}}, \theta) + I_{ref_{dc-ripple}}^*\right] \quad (10)$$

For example, I_{Tref}^* and $I_{dc-ripple}^*$ are the outputs of the PI controllers from the speed and DC-link current ripple blocks, respectively, for the speed and dc-link current ripple. A first-order high-pass filter's cutoff frequency is referred to as $\omega_{cHPF}\left(=\frac{1}{\mathrm{T}}\right)$, which is the transfer function.

$$G_{\mathrm{HPF}}(s) = \frac{Ts}{1+Ts} = \frac{s}{s+\omega_{c_{\mathrm{HPF}}}} \quad (11)$$

T is the first-order high-pass filter's time constant to reduce harmonic content, the cutoff frequency ω_{cHPF} must be chosen so that it contains the lowest harmonic order (N_pN_{rp}) of the dc-link current. A band pass filter with a restricted bandwidth of N_pN_{rp} to the present sensor cutoff frequency $\omega_{Ccs}\left(=\frac{1}{\mathrm{T_{cs}}}\right)$ can be used to model the overall harmonic extraction mechanism. Consequently, the minimal high pass filter's time constant can be expressed as

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$$\frac{1}{\omega_{c_{\mathrm{HPF}}}} = T_{min} = \frac{30}{\pi n_{\mathrm{rpm}} N_p N_{rp}} \quad (12)$$

The suggested algorithm's highest harmonic index desired (n_{CBW}) can be connected to the existing controller bandwidth (f_{CBW}) as follows:

$$f_{\mathrm{CBW}} \approx n_{\mathrm{CBW}} \left(\frac{n_{\mathrm{rpm-base}} N_p N_{\mathrm{rp}}}{60} \right) \quad (13)$$

Higher order harmonics must be suppressed by the dc-link capacitance (i. e. , $n_{\mathrm{CBW}} N_p N_{rp}$). The attenuation ($\gamma$) and available f_{CBW}may be used to calculate the smallest dc link capacitor.

$$\frac{a_{n_{n_{\mathrm{CBW}}+1}}}{\sqrt{1+(n_{\mathrm{CBW}}+1)^2 N_p^2 N_{\mathrm{rp}}^2 \omega_{a-base}^2 R_b^2 C_{\mathrm{dc-link}_{min}}^2}} = \gamma a_{n_{\mathrm{CBW}}+1} \quad (14)$$

This means the minimum capacitance value can be expressed as follows:

$$C_{dc-link_{min}} = \frac{\frac{30}{\pi}\sqrt{\left(\frac{1}{\gamma}\right)^2 - 1}}{(n_{\mathrm{CBW}}+1) N_p N_{\mathrm{rp}} n_{\mathrm{rpm-base}} R_b} \quad (15)$$

An attenuator has been selected for the capacitance that will give 50% ($\gamma = 0.5$) attenuation of the third harmonic content with this controller's base speed set to the second harmonic ($n_{\mathrm{CBW}} = 2$). For example, $C_{dc-link_{min}}$ is the computed minimum capacitance. A 1mF capacitor is selected for the dc-link capacitor $C_{dc-link}$.

Lower-order harmonics are eliminated by the controller, while higher-order harmonics are eliminated by the dc-link capacitor near the switching frequency range. Furthermore, wide band gap devices can be used to implement the converter, which results in a large reduction in the dc-link capacitance need

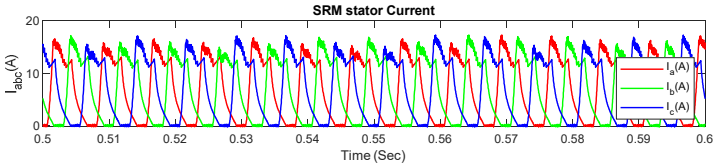

Fig.7. Illustration of the phase current profiling after implementing the proposed algorithm.

Figure 7 depicts the phase current profiling after implementing the proposed control. Other phases are regarded as disturbances affecting the operating phase while one phase is in operation. For example, during phase-A demagnetization (blue region), both switches of phase A are turned off, and phase A discharges excess energy toward the battery via the diodes. During this time, phase B attempts to magnetize, build the current, and reject the phase A disturbance. On the other hand, it requires excess energy from the dc supply during the magnetization of phase C (red region). During this time, phase B attempts to discharge some of the energy in order to reduce the excess energy demand from the dc supply and thus reject the disturbance from phase C. As a result, the proposed algorithm ensures ripple energy circulation between phases while reducing the pulsating energy demand from the dc supply.

V. DYNAMIC MODELING OF SRM

SRM's voltage balance equation is as follows:

$$\begin{aligned} V_{\mathrm{ph}} &= i_{\mathrm{ph}} R_{\mathrm{ph}} + \frac{d\lambda(i_{ph},\theta)}{dt} \\ &= i_{\mathrm{ph}} R_{\mathrm{ph}} + \frac{\partial \lambda}{\partial i}\frac{di_{\mathrm{ph}}}{dt} + \frac{\partial \lambda}{\partial \theta}\frac{d\theta}{dt} \\ &= i_{\mathrm{ph}} R_{\mathrm{ph}} + L_{\mathrm{inc}}\frac{di_{ph}}{dt} + \frac{\partial \lambda}{\partial \theta}\omega \end{aligned} \quad (16)$$

An external disturbance is represented by the speed-dependent term $\hat{E} = \frac{\partial \lambda}{\partial \theta}\omega$ in the machine model, which may be stated as follows:

$$G_m(s) = \frac{I_{\mathrm{ph}}(s)}{V_{\mathrm{ph}}(s)} = \frac{1}{R_{\mathrm{ph}} + sL_{\mathrm{inc}}} \quad (17)$$

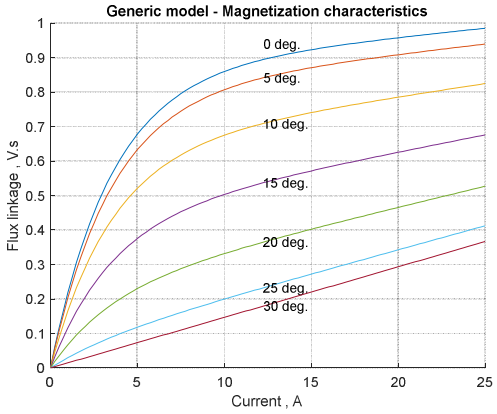

Fig.8. Incremental inductance profile at different currents of SRM from finite element analysis.

This shows that the incremental inductance $L_{INC}(i_{ph},\theta)$has an effect on the machine transfer function. Aligned inductance drops as current increases, while unaligned inductance does not. The flux saturation effect is considered while importing the inductance profiles from FEA software. The saturation effect is seen in Fig.8 by the diminishing aligned inductance curve with increased current.

VI.CURRENT CONTROLLER DESIGN

The current controller's closed-loop transfer function can be stated using the model depicted in Fig.6.

$$G_{cc}(s) = \frac{I_{ph}(s)}{I_{ref}^*(s)} = \frac{G_c(s)G_{conv}(s)G_m(s)}{1+G_c(s)G_{conv}(s)G_m(s)H_c(s)} \quad (18)$$

$G_c(s)$ and $G_{conv}(s)$are the transfer functions for compensators and converters, respectively, from (19) and (20).$K_{\mathrm{ic}}$and$K_{\mathrm{pc}}$are the present controller's integral and proportional gains. $H_c(s)$denotes the measurement dynamics, Current sensor data is processed through a Sallen–Key low-pass filter with an extremely high cutoff frequency that removes only high-frequency noise from this data.

$$G_c(s) = K_{pe} + \frac{K_{ic}}{s} \quad (19)$$

$$G_{conv}(s) = \frac{V_{dc}}{1+sT_d} \quad (20)$$

$$H_c(s) = \left(\frac{K_{cs}}{1+sT_{cs}}\right)\left(\frac{\omega_c^2}{s^2+2\zeta_c\omega_c s+\omega_c^2}\right) \quad (21)$$

With the PWM generation and current sensors, the dynamic response is significantly faster than with the SRM. As a result, it is possible to disregard them. A typical second-order transfer function can be used to approximate the controller's overall transfer function [17]. (22),

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where, $\omega_n{}^2 = \frac{V_{dc}K_{cs}K_{pc}}{L_{INC}}$ and $2\zeta\omega_n = \frac{V_{dc}K_{cs}K_{pc}}{L_{INC}}$

$$G_{cc}(s) \approx \frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (22)$$

[19] shows that classical control analysis can be used to express ω_n, K_{pc} and K_{ic} as a function of the needed control bandwidth ((f_{CBW}).

$$\omega_n = \frac{2\pi f_{CBW}}{\sqrt{(1+2\zeta^2)+\sqrt{(1+2\zeta^2)^2+1}}} \quad (23)$$

$$K_{pc} = \frac{2\pi f_{CBW}}{V_{dc}K_{cs}\sqrt{(1+2\zeta^2)+\sqrt{(1+2\zeta^2)^2+1}}} \quad (24)$$

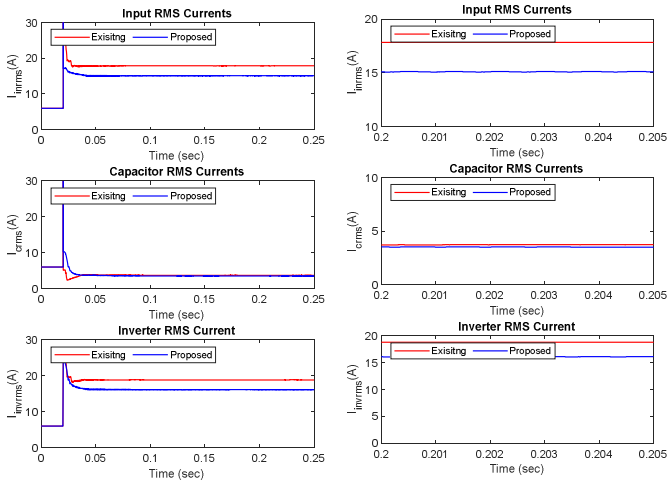
$$K_{ic} = \frac{4\pi^2 f_{CBW}^2}{V_{dc}K_{cs}\left((1+2\zeta^2)+\sqrt{(1+2\zeta^2)^2+1}\right)} \quad (25)$$

TABLE I: SRM DRIVE SPECIFICATIONS

DC Bus Voltage	230 V
Estimated Source Resistance, R_b	110 mΩ
No. of Phases, N_p	4
No. of Stator Poles, N_{sp}	8
No. of Rotor Poles, N_{rp}	6
Base Speed, $n_{rpm-base}$	3000 rpm
Phase Resistance, R_{ph}	0.65 Ω
Incremental Inductance, L_{inc}	Shown in Fih.9

VII. SIMULATION RESULTS

The suggested algorithmic control is validated by simulating the SRM drive in MATLAB/Simulink. Modeling and designing an SRM with 8 slots and 6 poles in FEA software is done. A magnetostatics study determines inductance, flux linkage, and torque profiles. Constant current is applied in increments from zero to maximum to the one phase that is rotated at one degree per second for each electric cycle. This data is then entered into an SRM MATLAB/Simulink model to find the best ON and OFF angles that will result in a higher torque while drawing less RMS current. Traditional current control is employed in a wide range of applications. This is followed by an implementation of the proposed dc-link ripple control technique.



(i) transient response (ii) steady state response

Fig.9. SRM Drive RMS (a) Input (b) DC-Link Capacitor (c) Inverter currents

The effectiveness of the suggested control is demonstrated by simulations at 3000 rev/min and 7 N.m. operating conditions. RMS currents of input, dc-link capacitor and inverter switching network are depicted in Fig.9 for comparison. Results from the conventional method are depicted in red, while those from the suggested method are depicted in blue. According to Fig.9 (a), there is difference of 2.75A, 0.25A and 2.7A of input, dc link capacitor and inverter RMS currents reduction in the proposed method when compared with traditional control. From Fig.9, it can be observed that, input, dc link capacitor and inverter RMS currents are 15.1A, 3.5A, and 16.1A respectively in the proposed method whereas those parameters are 17.85A, 3.75A and 18.8A in the conventional method. Hence, there is an improvement of 15.41%, 6.67% and 14.36% in input, dc link capacitor and inverter RMS currents reduction in the proposed method. The proposed control, on the other hand, requires less input currents by a factor of 18.21and 16.77 percent respectively as shown in Figs. 9 (a) and (c). From these analysis, it can be understood that, the suggested method decreases both input and inverter current by effective utilization (recirculation) of energy stored in the other phases, without effecting the capacitor currents. At the same, to investigate the performance of overall drive various other parameters such as speed in rpm, flux linkages, phase currents and load torque and electromagnetic torques also are illustrated in Fig.10 while applying speed control. Fig.10 (a) shows that SRM drive speed and reference speed, and demonstrates that SRM drive with proposed control techniques perfectly tracking the speed. To track the speed flux linkages produced inside the machined and stator currents are shown in Fig.10 (b) and (c) respectively. Fig.10 (d) illustrates the load torque and the electromagnetic torque.

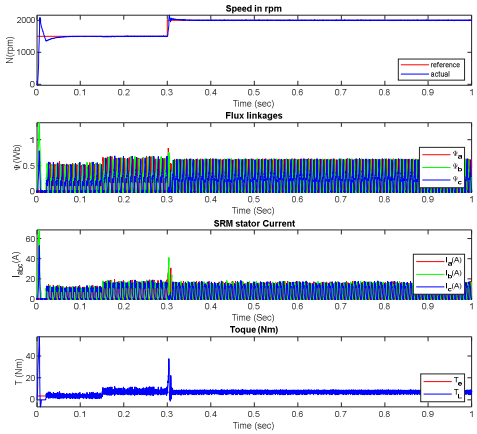


Fig.10. (a) Speed in rpm, (b) flux linkages (c) phase currents, and (d) instantaneous torque (IT) of SRM drive with proposed control algorithm

The dc-link control loop proportional and integral gains K_{pr} and K_{ir} have an impact on the overall performance of the suggested control method. Fig.9 depicts the maximum input current, DC-link ripple, and inverter current for a variety of controller gain levels. A constant 7N.m of torque on average is maintained during a period of 3000 revolutions per minute during testing duration. Increase K_{pr} and K_{ir} to decrease when increasing peak current demand, dc-link ripple current, as shown in Figs. 11(a) and (b). K_{pr}, on the other hand, has a far greater impact on phase current peak values and dc link current ripple than does K_{ir}. There is an ideal K_{ir} with the minimum peak phase current for each K_{pr}. As long as the user's priority is to accomplish target dc-link ripple

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while preserving desirable peak phase current and torque ripple, gain values can be selected.

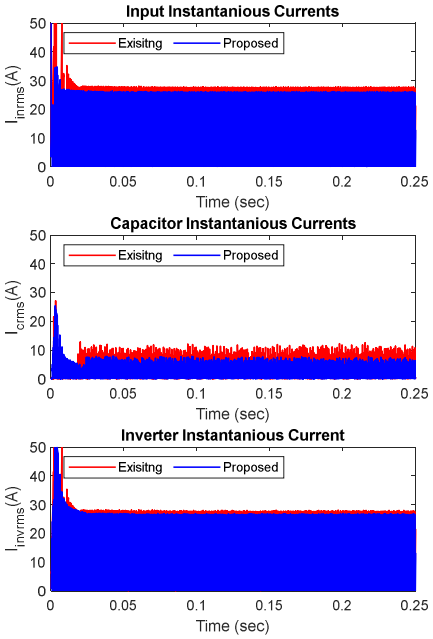

Fig.11. Comparison between conventional and proposed control algorithm for 3000 rev/min and 7N·m average torque condition: SRM Drive instantaneous (a) Input (b) DC-Link Capacitor (c) Inverter currents

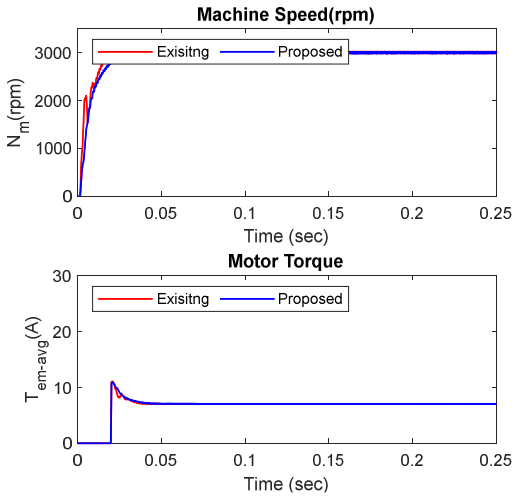

Fig.12. Comparison between conventional and proposed control algorithm for 3000 rev/min and 7N·m average torque condition. (a) Speed in rpm. (b) Machine torque.

From Fig.12, it can be understood that for offering the same mechanical work (3000rpm and 7Nm) in both the cases. For the same work done by SRM, the proposed scheme drawing 15.41%, 6.67% and 14.36% in input, dc link capacitor and inverter RMS currents less in the proposed method.

VIII. CONCLUSION

Current ripple in dc-link in a switched reluctance machine (SRM) can be reduced using a revolutionary approach suggested in this paper. The entire drive is simulated, and the effects of the measurement and conditioning circuit are considered in the control design. Circuit parameters are used to examine and express the control's bandwidth. The dc-link current ripple is greatly minimized by manipulating the phase currents. It has been shown that the proposed control successfully decreases ripple throughout a wide range of speeds. As a result of this, the capacitor bank's overall size is lowered greatly. Using the technique suggested, it is possible to attain small drive packaging and great volumetric power density. There is a bright future ahead for SRM drives, especially when it comes to automotive applications.

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