Switched Reluctance Machine Drive Analysis with Fault-Tolerant Power Converter

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ABSTRACT: There is a growing need for electrical drives to be reliable in a variety of industries. An important area of research in this regard is the switching reluctance machine's (SRM's) reliability. The failure of the drive power semiconductor is a major factor in its performance. Power semiconductor faults cannot be handled by typical SRM drive power conversion topologies. A fault-tolerant power converter topology is described here that allows the drive to function in the case of a switch failure. Changing the direction of the SRM winding current has no influence on machine behavior, hence this converter will be used. Because it can generate numerous phase voltages, SRM speed will determine the voltage levels that can be applied by the proposed power converter. In the Matlab Simulink environment, the SRM drive was tested in both normal and malfunctioning situations. In order to check the performance of the drive, fault-tolerance, we gathered data from a variety of devices and failure modes. The drive's multilayer operation may be verified as well.

INDEX TERMS: Switched reluctance motor (SRM), multilevel power converter, fault tolerance, bidirectional current excitation.

I. INTRODUCTION

However, compared to other electrical machines, the Switched Reluctance Machine (SRM) is not as often utilized in everyday applications. Because of the machine's restrictions, such as the necessity for a power converter, the presence of torque ripple and acoustic noise, as well as the requirement for an encoder, this is the primary reason for this. There are many advantages to this equipment when compared to others, such as its resilience, simple design, high dependability, minimal maintenance, and massively low production costs, the shortcomings of this machine have become less relevant. A growing number of companies are looking to incorporate SRM into their products, from electric automobiles to aircraft to wind turbines. [1]–[2]. The ability of SRM drives to tolerate faults is a critical characteristic linked to the study's central question. A few studies have been done on this important topic [3–4]. This solution for fault tolerance in [5] involves changing the converter topology in the event of a short-circuit faults. Power semiconductors' switching states could be tweaked, according to [6]. Genetic algorithms and Artificial neural networks [7], as well as classic Proportional Integral (PI) and Integral-Proportion (IP) regulators [8], fault detection systems [9], and even system geometry modification utilizing dual-channel SRM [10] have been used in other techniques. SRMs are used in [11] and [12] as a fault tolerant control approach; the SRMs are mutually coupled dual three-phase SRMs

Many industries are embracing the advantages offered by multi-level converters [13, 14]. For reducing torque ripple, an inverter-fed SRM is proposed in a new study by [15]. According to [16], A three-level asymmetric neutral point diode clamped converter has some advantages over a two-level half-bridge converter in some situations. For a four-phase SRM drive, [17] depicts an asymmetric NPC converter with integrated voltage booster capacitors for the dc-link. At high speeds, the driving performance of SRM is impaired due to the back electromagnetic force, and [18] offers a multilayer converter with enhanced performance (EMF). Multi-level converters are used in [19, 20] to reduce torque ripple. The use of multilayer converters in SRM drives is also emphasized by [21]. Failure tolerance is achieved by switching states that are damaging to the normal NPC architecture. [22] When operating in normal mode, a new fault-tolerant multilayer output converter can benefit from these advantages. As an alternative, [7] suggested creating a multilayer converter with built-in Boost functionality. There are SRMs supplied to plug-in hybrid electric car applications in [5,] an integrated multilayer converter of SRMs. One issue that must be handled in some multilevel systems is the balance of DC voltage capacitors via redundant switching states. Inverters such as the NPC, T-Type, and flying capacitor were developed to solve this issue [8–9]. NPC multilevel topology with redundant states is also presented in [20-21]. But the issue of using redundant states for capacitor balance or transistor failure condition is not addressed in these works, which are still relevant.

In the past, several topologies and methods for fault-tolerant SRMs have been proven. Most of these ideas, however, were put forth with the idea of a motor with a single-direction current flow in the forefront of their minds. This is a feature of the particular motor in question. Inverting the current flow in the windings, as demonstrated in the following section, allows this motor to continue rotating in the same direction and with the same torque characteristics. By eliminating mechanical and static relays, we are able to provide a highly efficient power converter, and a cheaper cost because of this work's fault tolerant topology based on this notion. Only a few concepts exist for fault tolerant topologies that can handle SRMs and multilevel operations with full fault tolerance. Consequently, the suggested topology allows for SRMs to operate at several levels in addition to fault tolerance. Additionally, this approach addresses the issue of input capacitor balancing. As a result, a proposal for using redundant states in normal and fault-tolerant settings for the balance of those capacitors is made.

II. SWITCHED RELUCTANCE MACHINE

Keep in mind that the rotor position affects the magnetic circuit's reluctance and, therefore, the SRM's working principle. Even though SRM geometry and other construction elements such the type of Ferro-magnetic material utilized, its thickness, and lamination factor have an effect on the magnetic reluctance circuit. By accurately managing the timing of the energizing and de-energizing stator phases, the torque (reluctance torque) in this machine may be regulated. The magnetic circuit's nonlinearity makes the mathematical model difficult. To avoid magnetic interference between phases, the electrical SRM equation can be stated as (1) for each phase, Typically, mutual inductance is ignored.

$$u_j = R_j i_j + \frac{d\psi_j(\theta_r, i_j)}{dt} \quad (1)$$

where u_j represents the phase voltage, i_j represents the phase current, R_j represents the phase resistance, θ_r represents the rotor position, j represents the considered phase, and $\psi_j(\theta_r, i_j)$ represents the phase linkage flux. Equation (1) is rewritten as follows:

$$u_j = R_j i_j + \frac{\partial\psi_{(\theta_r, i_j)}}{\partial i_j}\frac{di_j}{dt} + \frac{\partial\psi_{j(\theta_r, i_j)}}{\partial\theta_r}\omega_r \quad (2)$$

Where ω_r is the rotor speed, and the final phrase is back EMF. Back EMF and input voltage must be increased to maintain phase current in a motor operating at high speeds. A high DC voltage can be imposed with the help of a multilayer converter in this situation. To reduce the commutation time between phases and the possibility of negative phase torque, high voltage values are particularly desirable during phase energizing or deenergizing periods Using a multilayer converter at lower speeds can enhance efficiency, especially if lower voltage values are used, which can lower the switching frequency.

In order to finish the SRM mathematical model, write an equation for each phase's torque (T_j). Every time a phase generates power, it is added together to get the overall torque. The fluctuation in magnetic co-energy (W_C) produced in each phase's magnetic circuit in relation to the torque for each phase is determined by rotor position variation, which is expressed as (3).

$$T_j(\theta_r, i_j) = \frac{\partial W_C(\theta_{r,} i_j)}{\partial\theta_r}\Big| i_j = const \quad (3)$$

where the formula defines the magnetic co-energy:

$$W_C(\theta_r, i_j) = \int_0^{i_j} \psi_j(\theta_r, i)di \quad (4)$$

Each phase's linkage flux can be expressed as follows:

$$\varphi_j(\theta_r, i_j) = L_j(\theta_r) i_j \quad (5)$$

(L_j)was added and regarded to be independent of the phase current, i_j, in this study, However, it is non-linear and is depending on the rotor position [50].

The torque produced by each phase and expressed in (3) can be rewritten as follows using (5):

$$T_j(\theta_r, i_j) = \frac{1}{2}\frac{dL_j}{d\theta_r} i_j^2 \quad (6)$$

As a result, the value of the phase current has no effect on its value. This paper relies heavily on this element to validate its methods.

Assuming magnetic independence of the motor phases, the SRM can continue to work even when the motor-converter unit fails. Aircraft and electric cars, for example, benefit from this inherent fault tolerance. However, the existence of defects increases the speed fluctuation and torque ripple, which results in unwanted behavior.

III. PROPOSED CONVERTER WITH FAULT-TOLERANT CAPABILITY

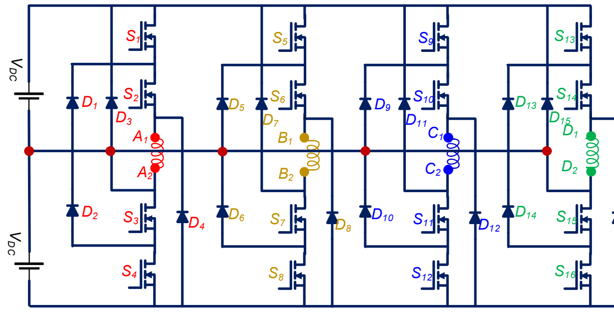


FIGURE 1. Neutral point clamped asymmetrical half-bridge converter (*NPC-AHB*) topology for *SRM* drives.

There are several different configurations of power converter topologies that can be used by SRM drives. The asymmetrical half-bridge converter, on the other hand, is the most frequent and most widely used [4]. Depending on the switching states, this topology can be utilized to generate three different voltage levels: $+V_{DC}$, 0 and $-V_{DC}$. Fault tolerance is not supported by this converter in addition to the limited voltage levels it can handle. Indeed, if one of the power semiconductors has an open or short-circuit problem, the SRM's operation will be severely disrupted. As a result of these limitations, SRM makes use of multiple power converters. A half-bridge converter with neutral point clamping is one of several architectures proposed (NPC-AHB). Each leg has two regulated power semiconductors and one diode, as well as two serially connected DC capacitors with their common point connected to each leg through a clamped diode in this design, as illustrated in fig.1. This construction enables the application of higher voltage levels to the windings. There are up to five distinct voltage levels that can be used (two negatives, two positives, and a voltage of zero).

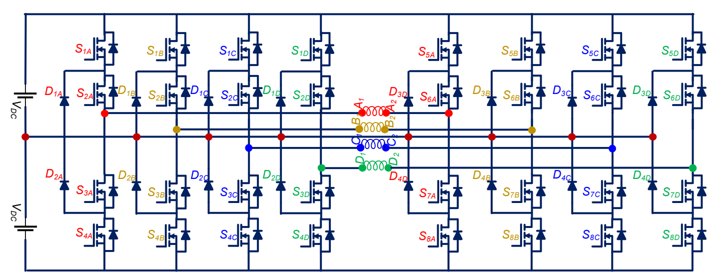


FIGURE 2. Proposed neutral point clamped converter with fault tolerant capability for *SRM* drives.

A fault-tolerant feature is also included in this architecture, in addition to the higher voltages that it can achieve. However, a short in the outside transistors has no influence on the SRM's performance A defect in the transistors will limit the voltage was applied to the winding during the magnetization process, reduce the DC bus voltage to half. The voltage applied to the winding can be impacted if there is a problem with the inner transistor. The winding cannot be magnetized if there is an open circuit. When one of the isolated diodes fails, we have a serious problem on our hands. This could have a significant effect on the system, as one of the capacitors has a short circuit or the bus will create another short-circuit. Thus, a power semiconductor fault may cause the phase winding to operate abnormally, resulting in the motor operating less efficiently due to substantial speed and torque changes.

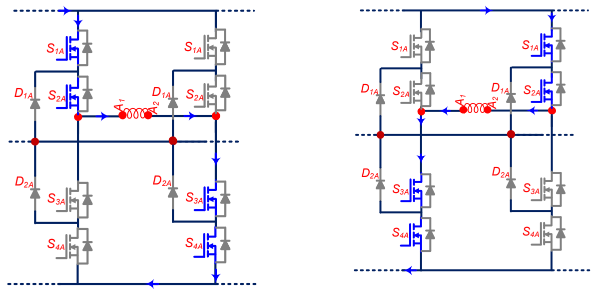


FIGURE 3. Operation modes for the proposed converter in normal operation for the maximum DC voltages.

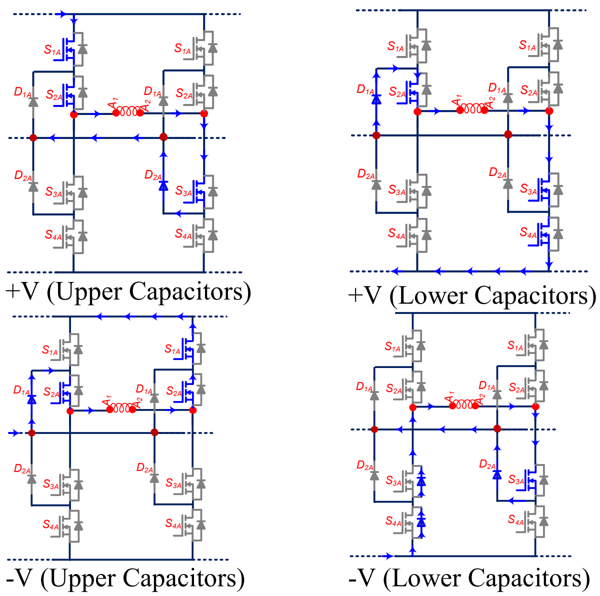


FIGURE 4. Operation modes for the proposed converter in normal operation for the intermediate DC voltages.

It is proposed in this study that rather than an asymmetrical half-bridge converter, it is recommended that a full bridge neutral point clamped converter be utilized. as seen in figure 2. One diode is replaced by four completely regulated power semiconductors and antiparallel diodes in this design. The SRM drive's simple structure is due to the fact that this topology is widely used in industry for conventional electrical machine drives. Here, we propose that this machine's torque is a function of the square current flowing through each phase (eq. 6). The direction of the winding current has no effect on the rotational motion of the rotor, hence this current can be inverted.

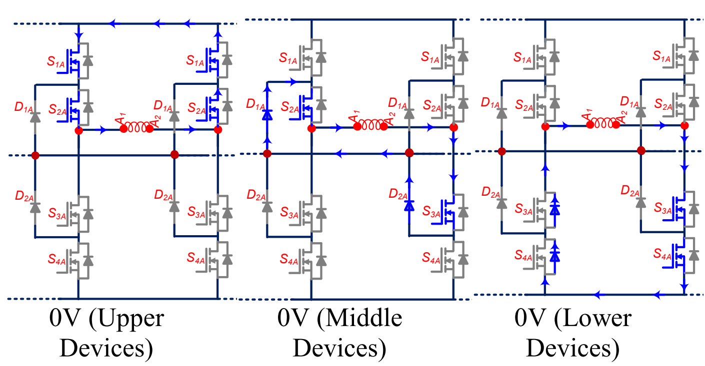


FIGURE 5. Operation modes for the proposed converter in normal operation to achieve zero voltage.

If the SRM operation point is set correctly, there are up to nine possible modes of operation for each winding in the proposed power converter. There are two operation modes (fig. 3 a and b) that can be used when maximum DC voltages are necessary, for example. There are four modes of operation that can be used where only half of the maximum DC voltage is required (fig. 4 a) b) c) and d) However, the DC bus voltage capacitors must maintain their voltage balance in this instance. This is what happens when you use half the DC voltage because of the duplicate states (fig. 4). At zero voltage, there are three possible operating modes, as shown in Figure 5. Inverted currents can also benefit from a similar approach.

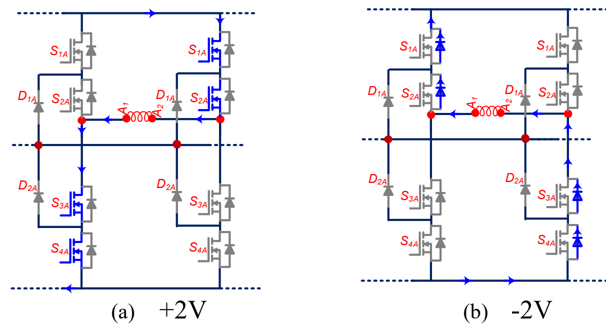


FIGURE 6. Operation modes for the proposed converter in fault tolerant mode (inversion of the current excitation) for the maximum DC voltages.

By adopting a bidirectional current excitation technique, the SRM drive can achieve a high circuit reconfiguration capability. Conventional half-bridge asymmetrical power converters are used in normal operation of the power adapter. It is, however, SRM current excitation can be inverted in the event of a power semiconductor failure. There are a total of nine different operating modes for each of these windings, as indicated in figures 6, 7, and 8. As a result, two modes of operation (Fig. 6 a and b) are available for achieving the highest possible DC voltage. When only half of the DC voltage is utilized, redundant states are needed to keep the DC bus voltage capacitors balanced.

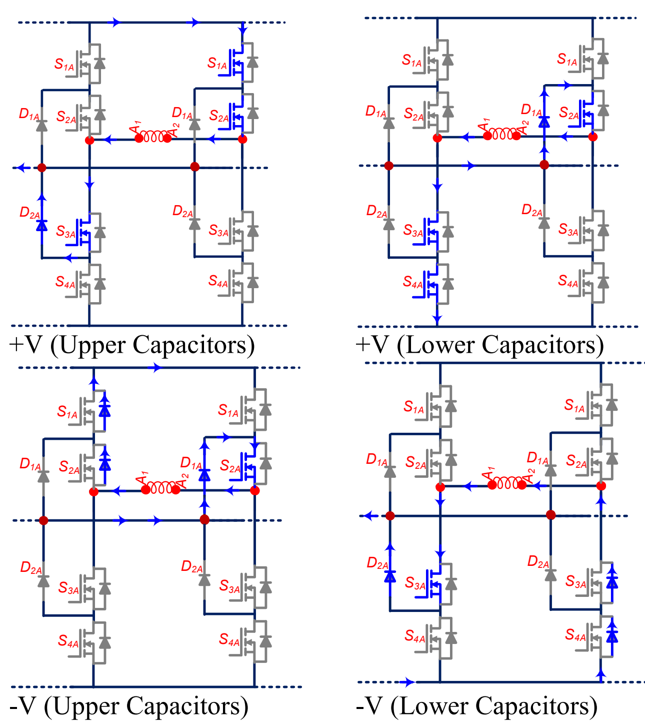
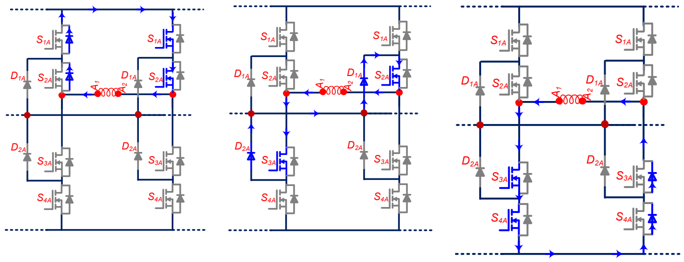


FIGURE 7. Operation modes for the proposed converter in fault tolerant mode (inversion of the current excitation) for the intermediate DC voltages.



0V (Upper Devices) | 0V (Middle Devices) | 0V (Lower Devices)

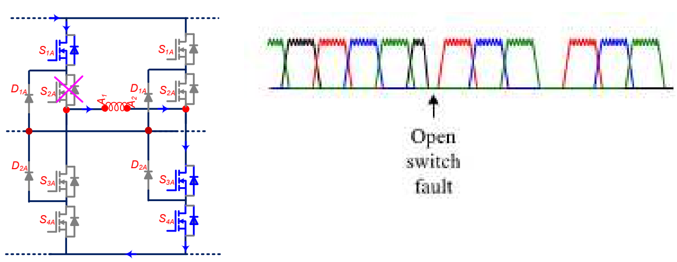
FIGURE 8. Operation modes for the proposed converter in normal operation (inversion of the current excitation) to achieve zero voltage.

The ability to alter the winding current direction increases the fault tolerance of power semiconductors, as shown in this study (from positive to negative). When the machine winding does not get a positive or negative voltage, it can be compensated for by changing the control of the switches. Switch $S_{2A}$is an example of a switch that cannot be used to provide the necessary voltage to phase A's winding if it has an open fault.

IV. OPERATION IN FAULT-TOLERANT MODE

The motor's performance will be reduced if a power semiconductor fails, as previously indicated. Open and short-circuit failures are the two most common types of semiconductor failure. These defects can have varying degrees of consequence. Windings can no longer be magnetized in an open circuit semiconductor failure condition. In this way, even if the phase is lost, the SRM will still work. As a result, there is an unsteady and elevated torque ripple. The phase current associated with the damaged semiconductor will be high in the short-circuit failure mode. As a result, high negative torque values and severe winding heating may emerge, reducing the SRM's performance significantly.

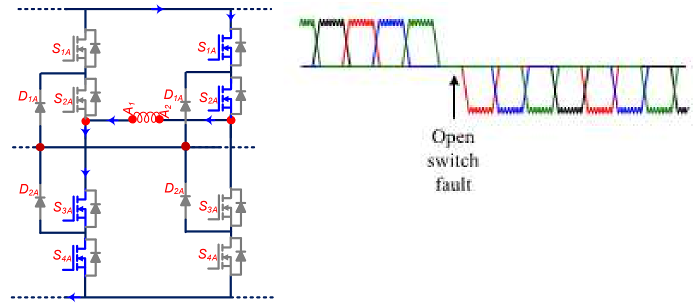
Under normal circumstances, it is anticipated that the controllable power semiconductors will be positioned on the upper legs of each winding, and on the lower legs of each winding, to evaluate the proposed power converter (Figure 3 depicts the operation modes). As a result, the winding currents will be categorized as "positive." Phase A examples will be used in the analysis of the power converter's failure and tolerance modes.



(a) (b)

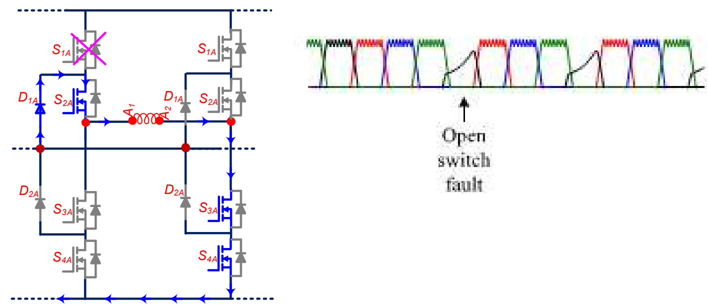
FIGURE 9. Impact of *S*2*A* open-circuit failure: a) Power circuit; b) Winding currents before and after the fault.

If S_{2A} or S_{7A}, one of the inner-controlled power semiconductors, fails open-circuit, the current in the winding is shut off (see fig. 9). Following a power outage, the winding currents must be reversed to ensure full fault tolerance because their performance will not be limited by the SRM in negative excitation condition. Power semiconductors S_{1A}, S_{2A}, $S_{7A}$and S_{8A}must be turned off permanently after the fault, and power semiconductors S_{3A}, S_{4A}, $S_{5A}$and S_{6A}will be used to regulate the current of the winding (see fig. 10).



(a) (b)

FIGURE 10. Operation in fault tolerant mode after a *S*2*A* open-circuit failure (inversion of the current excitation): a) Power circuit; b) Winding currents before and after the failure.

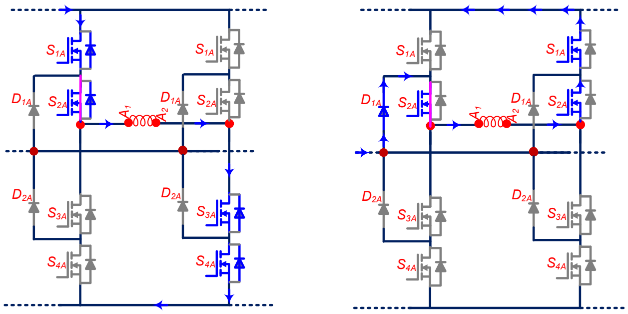


(a) (b)

FIGURE 11. Impact of *S*1*A* open-circuit failure: a) Power circuit; b) Winding currents before and after the fault.

There is no stoppage of current in that winding if an open fault develops in the outer controlled power semiconductors (S_{1A}or S_{8A}). The magnetization process, however, will be hampered because the applied voltage to the winding is limited to half of the total DC voltage. Due to the limited supplied voltage to the winding in high-speed operation modes, the phase under fault will be unable to provide the required current (just half the voltage). The effect of this fault state is depicted in Figure 11. This difficulty, however, can be solved in the same way as the previous one was. by using the SRM in a negative excitation situation.

A power semiconductor's behavior when subjected to a short circuit fault differs dramatically from that of an open circuit fault. The effect on SRM performance will vary depending on where the malfunctioning component is located. A short-circuit fault in the outer controlled semiconductors (S_{1A}or S_{8A}) is one of the issues that could harm the SRM. Because $S_{2A}$is in serial connection with S_{1A}, Semiconductors S_{2A}, S_{7A} and S_{8A} may still control the voltage applied to the winding in the event of a short circuit in S_{1A}. Only when the semiconductors S_{2A}, S_{7A} and S_{8A} are controlled to apply half of the maximum DC voltage will the impact of this problem be obvious. As a result, the switching frequency of the defective leg will increase in several operational modes. Furthermore, When the SRM is in a negative excitation condition, this problem can be treated in the same way as an open circuit failure. If a short circuit happens in one of the inner regulated power semiconductors, the performance of the SRM will be affected differentially. Because two voltage levels can be employed, the magnetization process will be unaffected. However, because the winding can only receive half of the maximum DC voltage, the demagnetization process would be hampered. If there is power semiconductor S_{2A} shorted out during the demagnetization process, that semiconductor will always conduct current (see fig. 12). However, because the effect is limited to demagnetization procedure, the required current can always be maintained (This does not occur when an open circuit fault occurs in the outer controller power switches). Aside from that, this flaw may have another consequence. The capacitor voltage balance can be impacted in this case, as indicated in the following section.



(a) (b)

FIGURE 12. Impact of *S2A* short-circuit failure in the demagnetization process: a) Magnetization mode; b) Demagnetization mode.

An investigation into the theoretical failure probability of the both converters (Figures 1 and 2 depict the NPC-AHB and the suggested topology, respectively) following failure in the IGBTs of one phase (winding A), a comparison with the existing multilevel power converter is shown. Both modes of failure (short and open circuit) were addressed independently in this investigation, as was the ability to obtain the appropriate voltage level. To make this analysis easier, especially in the event of short-circuit failure, it was also assumed that the following failures show the same manner for each failure mode. R(t) is a time function that Determines the likelihood of a system failing within a specific time period [0, t]. The following exponential distribution (7) is commonly used to estimate the reliability of a component with a constant failure rate, λ:

$$R(t) = e^{-\lambda t} \tag{7}$$

An investigation into the theoretical failure probability of both to show a comparison with the existing multilayer power converter, the Poisson distribution (8) is utilized to explain the reliability of stand-by redundancy systems with ideal switching without repair and similar and constant failure rates.

$$R(t) = \sum_{k=0}^{n-1} \frac{(\lambda t)^k}{k!} \mathbf{e}^{-\lambda t} \tag{8}$$

The failure probability is then calculated using (9):

$$Q(t) = 1 - R(t) \tag{9}$$

After the first failure, the NPC-AHB and proposed topology have a failure rate of $\lambda = 10^{-6} h^{-1}$ as indicated in the tables below, which represent the estimated chance of failure after five years (43800 hours) of operation.

Table 1: estimated probability of failure to 5 year of operation after the first failure (NPC-AHB)

	Open circuit failures		
Device Failure	+2V	+V	0V
S_1	Fail	0.1231(*)	0.0446
S_2	Fail	Fail	0.0838
S_3	Fail	Fail	0.0838
S_4	Fail	0.1231(*)	0.0446

The failure of an open circuit mode study shows that the proposed method is considerably more dependable, independent of the malfunctioning equipment or the required voltage level, regardless of the voltage level.

When compared to short-circuit as the mode of failure, the suggested only when the failed device is external does topology become more trustworthy. (e.g. S_{1A}, S_{3A}, S_{5A}, S_{8A})or when 0 V is required. The reliability of the remaining devices is the same.

Table2: estimated probability of failure to 5 years of operation after the first failure (proposed topology), admitting the proposed changes in the control strategy.

	Open circuit failure		
Device Failure	±2V	±V	0V
S_{1A}	0.1607	0.0105	0.0019
S_{2A}	0.1607	0.0855	0.0037
S_{3A}	0.1607	0.0855	0.0037
S_{4A}	0.1607	0.0105	0.0019
S_{5A}	0.1607	0.0105	0.0019
S_{6A}	0.1607	0.0855	0.0037
S_{7A}	0.1607	0.0855	0.0037
S_{8A}	0.1607	0.0105	0.0019

V. SIMULATION TESTS

Matlab/built-in Simulink's simulation system was used to test the proposed SRM drive. Using the Simscape Power Systems component libraries, components of the fault tolerant converter's power supply were simulated With a 300 volt DC power source, four 8/6 SRMs, and 100 μF capacitors, this system is complete. A flat-top current controller with a 6 A current reference was used to control the SRM. Several testing in various situations, including normal, short-circuit fault, open transistor fault, and fault tolerant, validated the features of the proposed drive.

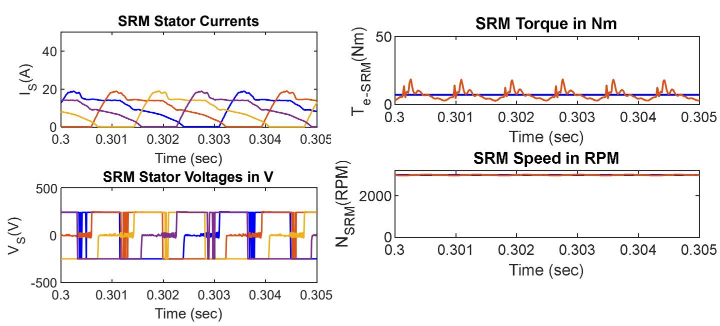


FIGURE 13. Simulation results for the *SRM* in normal operation for a speed of 3000 rpm: a) Winding currents; b) Applied voltage to winding A; c) Torque; d) Speed.

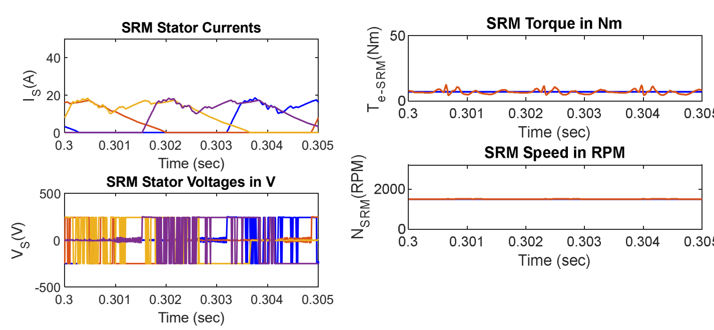


FIGURE 14. Simulation results for the *SRM* in normal operation for of speed 1500 rpm: a) Winding currents; b) Applied voltage to winding A; c) Torque; d) Speed.

Figure 13 depicts the results of a regular operation test at 3000 rpm. The waveforms of the SRM winding currents and the corresponding voltage applied to winding A are shown in the figure below. These waveforms show the voltage delivered to the windings nears the maximum DC voltage bus and flips between the highest and lowest values ($+V_{DC}$and $+V_{DC}/2$). It also indicates the capacitance's voltage balance. It was done in standard mode but at a different speed for the second simulation (1500 rpm). Waveforms of winding currents from the SRM are illustrated in Figure 14 together with the associated voltage that is provided to winding A. The voltage provided to the windings in the magnetizing and demagnetizing modes falls as the speed lowers (taking in half of the data from the previous experiment), switching between $+V_{DC}/2$ and 0. The applied voltage is greatest when the coil is magnetized for the first time to guarantee an efficient transition between phases. The capacitors' voltage balance is also balanced.

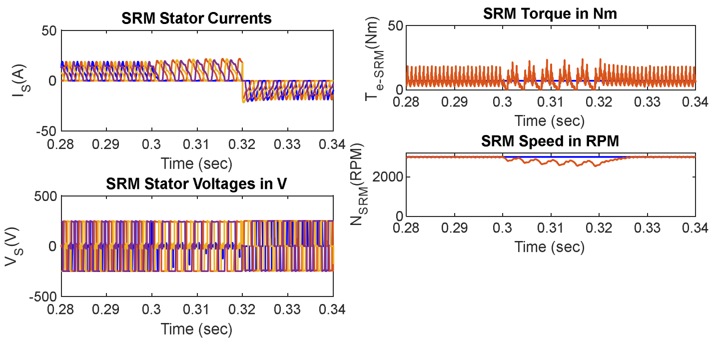


FIGURE 15. Simulation results for the *SRM* in open-circuit transistor (*S2A*) failure and fault tolerant condition operating at 3000 rpm: a) Winding currents in failure mode; b) Applied voltage to winding A in failure mode; c) Torque; d) Speed.

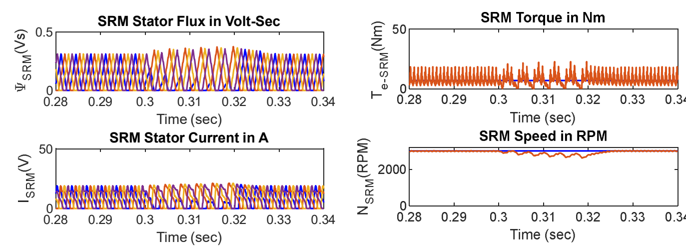


FIGURE 16. Simulation results for the *SRM* in open-circuit transistor (*S1A*) failure operating at 3000 rpm: a) Winding currents; b) Applied voltage to winding A; c) Torque; d) Speed.

Operation that is fault-tolerant is seen in Figure 15. S_{2A} open-circuit fault with a high-speed power transistor yielded these findings. Winding A's current and voltage waveforms are depicted in this diagram. When an open-circuit fault occurs, winding A's current is always zero, as can be seen by analyzing these findings. Figures 15 c) and d) indicate that this problem is alleviated when the circuit is operating in fault-tolerant mode. S_{1A}, a different power semiconductor, was used in a second open-circuit failure mode experiment. Fig. 16 depicts the Winding current and applied voltage simulation waveforms for winding A. According to these findings, the voltage in the excitation mode is half that of the highest DC bus voltage. Because of this, the faulty leg's winding current will have an impact. Because the winding cannot receive the full DC voltage, the current will not reach the desired level. An increase in capacitor voltage ripple (see fig. 16 c) is also a problem when this failure scenario occurs. This means that the lower capacitor will constantly be charging and the higher capacitor will always be discharging. Fault-tolerant operation, notably current inversion, can alleviate these issues, as it did in the previous example. Figures 15 c) and d) show how the circuit works in this fault-tolerant state.

VI. CONCLUSION

SRM drives with fault tolerance and many levels have been proposed in this article. Using an NPC modular topology, the suggested drive has five voltage levels that can be applied to the SRM windings. Analysis of the possible defects in the proposed power converter was carried out. To keep performance as good as possible or even achieve a completely fault-tolerant mode of operation, this study found that inverting the current excitation can be used in conjunction with many modifications to the power converter. In the control system, flat-top current control was employed. Using a current controller equipped with a hierarchical hysteretic comparator, a multilevel system might be implemented. Additionally, an approach for managing the drive that appropriately maintains capacitor voltage balance was presented and experimentally proven. The proposed fault-tolerant architecture was validated through a series of experiments and simulations utilizing a four-phase 8/6 SRM. Based on the results of the tests, it was determined that this drive is a viable option for high-reliability industrial applications.

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