A Three-Phase Semi-Single Stage PV Inverter With Voltage Boosting and Leakage Current Minimization

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***Abstract*—This brief presents an integrated three-phase transformerless inverter configuration for PV systems, which is capable of synthesizing a three-level (3L) voltage waveform at its output from a single PV source. Furthermore, high-frequency transitions in the voltage across the parasitic capacitive branch are altogether eliminated for effective suppression of the leakage current, which is of paramount interest in transformerless PV systems. It is shown that the proposed configuration is capable of achieving a voltage boosting factor of two with the aid of an interleaved dual-output buck-boost converter. The efficiency of the proposed power converter is considerably improved, as a significant amount of the PV power is transferred directly to the load. Further, mathematical equations are derived using the theory of switching functions to assess the amount of power that can be transferred directly to the load via inverting stage. Experimental studies validate the operating principle of the proposed power converter configuration in both steady-state and dynamic conditions.**

***Index Terms*—Leakage current, transformerless PV inverter, pulse width modulation (PWM), partial power transfer capability.**

I. Introduction

In VIEW of the ever-increasing demand for emission-free energy, industries, and research communities are continuously engaged to develop technologies pertaining to renewable energy systems. In this context, transformerless PV inverter systems have become popular, as they offer advantages such as high energy density, high efficiency, and low cost, compared to the bulky transformer-based configurations [1]. However, the absence of galvanic isolation in transformerless PV systems results in a significant leakage current, which poses safety issues as well as a reduction of the life span of PV panels. The magnitude of the leakage current mainly depends on two factors: (i) the value of the parasitic capacitance between the PV panels and the frame, and (ii) the voltage transitions across the parasitic elements.

In general, the variations in atmospheric conditions cause significant parametric changes in the parasitic elements, leading to an increased leakage current. Also, the magnitude and the frequency of voltage transitions across the parasitic elements increase leakage current for the PV system. Several new inverter configurations and modulation techniques have been proposed by various researchers to mitigate the leakage current. In the research work reported in [2], it is shown that both dc- and ac-decoupled structures, which are originally proposed for the single-phase transformerless inverter configurations, can also be extended for three-phase systems. The modulation strategy and the power circuit configuration proposed in [3]–[4] effectively reduce the leakage current in three-phase inverters. However, the output voltage levels of these configurations are limited to two-level.

A modified NPC-based 3-phase, 3-level VSI configuration, proposed in [5], results in the reduction of leakage current. However, the proposed modulation strategy increases the filtering requirements and the *dv/dt* stress on the semiconductor switches. Furthermore, this topology uses two isolated PV sources, increasing the complexity of implementing the MPPT loop under the conditions of asymmetric irradiance. In addition to that, the RMS value of the leakage current depends on the switching frequency and the dc-link voltage, as the voltage transitions across the PV parasitic elements are not eliminated.

The power circuit configuration and the associated modulation technique proposed in [6] are also capable of reducing the leakage current. The drawback with this scheme is that this configuration requires more switching resources along with the dc-link capacitors. A similar approach with a reduced number of switching devices is proposed in [7]. However, it suffers from various drawbacks such as the requirement of four isolated PV sources and the under-utilization of the dc-link. Also, the requirement of multiple-loop-based MPPT further increases control complexity under the conditions of variable irradiance. A switched-capacitor (SC) based modified NPC inverter configuration is introduced in [8] to achieve the voltage boosting capability along with the multilevel operation. Though this configuration is capable of reducing the problem of leakage current, the hard-charging of the SCs incurs a higher power loss in the switching devices.

Some interesting circuit topologies are proposed in [9]–[10], wherein the voltage boosting stage is merged with the inverter configuration. These configurations are capable of mitigating the leakage current, while the loss of the dc-link utilization is compensated from the voltage boosting unit. However, these topologies transfer the total PV power through the boosting stage, which results in a significant power loss in the voltage boosting unit.

In view of the status of the present literature, there exists a requirement for a three-phase transformerless PV system, which simultaneously achieves the multiple objectives of: (i) reducing the leakage current, (ii) improving the efficiency

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of the voltage boosting stage, and (iii) improving the harmonic performance at the output with the multilevel operation.

This manuscript proposes a single PV source-based modified configuration, which is obtained by the fusion of a 3-phase 3-level inverter and a voltage boosting unit. Another advantage of the proposed system is that any existing three-phase, 3-level VSI is compatible with its boosting stage. Thus, it serves as a retrofit solution for any existing 3-phase, 3-level inverter topologies such as the cascaded H-bridge, the NPC, and the ANPC based inverter configurations [11]. The proposed power converter topology along with its modulation technique is capable of reducing the leakage current without sacrificing the multilevel voltage at the output. The analysis of the partial power transfer capability is also carried out with the help of the switching function.

II. Schematic of the Proposed 3-Phase TBMLI

The circuit diagram of the proposed three-phase T-type transformerless boost inverter (3-ϕ TBMLI) for the PV applications is shown in Fig. 1(a). The presented inverter configuration requires a single solar-string, two dc-link capacitors (C_2, C_3), and two switched capacitors (SCs: C_1 and C_4). The proposed power circuit configuration consists of three sections: (i) the voltage boosting unit (VBU), (ii) the level selector unit (LSU) and, (iii) the phase generation unit (PGU). The VBU is realized with a back-to-back connection of an inverting and a non-inverting buck-boost converter as shown in Fig. 1(a). The LSU consists of two half-bridge legs, which are connected across the SCs. Thus, the T-legs of each output phase can be connected to the appropriate junction points (J_0, $J_1 \ldots J_4$) through the LSU [Fig. 1(a)]. The output terminals of the 3-level VSI are connected to a star-connected load. The three-phase load currents are indicated as i_R, i_Y, and i_B for the corresponding three phases R, Y, and B. An equivalent branch for the parasitic elements of the PV panel is represented by a series connection of a resistor (R_p) and a capacitor (C_p) as shown in Fig. 1(a). The parasitic voltage (v_{Pg}) and the leakage current (i_{leak}) can also be measured across this branch.

III. Modulation Technique and Voltage Control Strategy

An emphasis is laid on the optimization of the switching resources in the proposed power circuit is that the switching devices corresponding to the LSU [Figs. 1(a)] are kept common for all the three output phases rather than replicating them for each phase. This optimization is possible because, the adopted modulation technique optimally chooses those space vectors, which would not result in any transition of voltage across the parasitic branch of the PV panel (consisting of R_P and C_P, Fig. 1). In view of this fact, 49 voltage space vectors are obtained against all possible switching combinations for the proposed configurations as shown in Fig. 2. Figs. 1 (b–f) summarizes the voltage levels for the pole voltage 'V_{RO}' and the corresponding states of the switching devices pertaining to that phase. Also, symbols 'S_R' and 'V_{PV}' respectively represent the *space vector index* corresponding to the 'R-phase' and the PV-input voltage [Fig. 1(b–f)]. The pole voltages for the other two phases can be defined in a similar manner with the help of the space vector indices 'S_Y' and 'S_B'. The four combinations of the switching states of the switches in the LSU are summarized in Fig. 2 with their corresponding space-vector locations. In order to dissuade the transitions in the voltage across the parasitic branch, the voltage caused by all

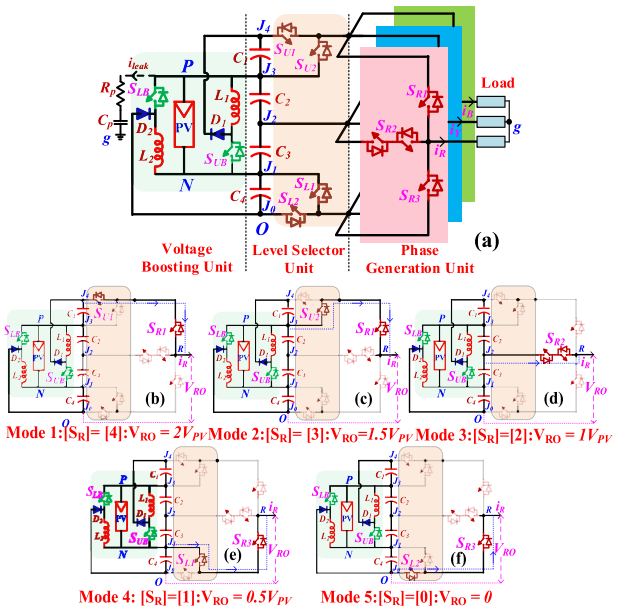

Fig. 1. (a) The proposed configuration and (b-f) modes of operation.

of the possible 49 vectors are first evaluated (using eqn.1). As the magnitude of the leakage current mainly depends on the magnitude and frequency of transitions in the voltage 'v_{Pg}', only those vectors are handpicked, which cause an identical magnitude of 'v_{Pg}':

$$v_{Pg} = [9 - (S_R + S_Y + S_B)]\frac{V_{PV}}{6} \tag{1}$$

Based on this selection criterion, it is observed that a group of 19 vectors comply with the above requirement and are fit to be deployed to implement the PWM scheme. Consequently, the space vectors employed in this work (shown numbered) are indicated in Fig. 2. It may be noted that these 19 vectors constitute a two-layered hexagonal structure with 24 sectors as shown in Fig. 2, facilitating three-level operation while maintaining a constant magnitude of v_{Pg}. This also eliminates all the corresponding transitions in the leakage current, which flows through the parasitic elements of PV panel. The common-mode voltage (v_{CMV}) of the proposed inverter can be expressed as follows:

$$v_{CMV} = (S_R + S_Y + S_B - 6)\frac{V_{PV}}{6} \tag{2}$$

The exclusively selected 19 space vector locations also result in the same magnitude of v_{CMV} (with a value of '0'), as v_{Pg} and v_{CMV} are distinguished only by the voltage across the capacitor C_2, which is a constant. Thus, it may further be appreciated that the proposed power converter overcomes the drawback associated with topologies such as the one proposed in [6], wherein the switching resources are underutilized to achieve a constant common-mode voltage. Furthermore, it is observed that the selected switching combinations possess a natural tendency to balance the inner dc-link capacitors (C_2, C_3) as they wield opposite influences on them in terms of charging and discharging in each $\pi/6$ duration.

The block diagram for the proposed modulation strategy is shown in Fig. 3. As the proposed configuration has a single input PV source, it requires only a single loop-based MPPT. A linear PI controller is employed to regulate the voltage of SCs (v_{C1}, v_{C4}) to half of the input voltage ($v_{PV}/2$). Also,

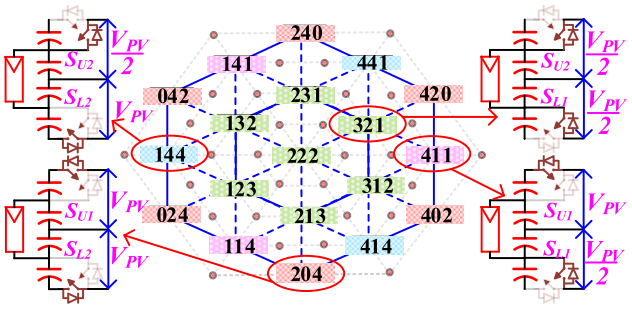

Fig. 2. Modified space vector diagram and switching combination for the LSU.

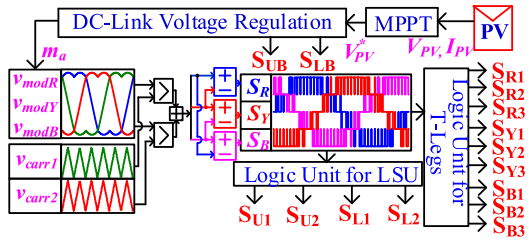

Fig. 3. The control scheme for the proposed configuration with MPPT control.

TABLE I
LOGICAL CONDITIONS FOR THE SWITCHES OF THE LSU

Device	S_{U1}	S_{U2}	S_{L1}	S_{L2}
Logical Condition to 'Turn-ON'	(S_R ==4) || (S_Y ==4) || (S_B ==4)	(S_R ==3) || (S_Y ==3) || (S_B ==3)	(S_R ==1) || (S_Y ==1) || (S_B ==1)	(S_R ==0) || (S_Y ==0) || (S_B ==0)

TABLE II
LOGICAL CONDITIONS FOR THE SWITCHES OF PGU (T-LEGS)

T-leg (Phase-R)		T-leg (Phase-Y)		T-leg (Phase-B)	
Device	Cond.	Device	Cond.	Device	Cond.
S_{R1}	S_R >2	S_{Y1}	S_Y >2	S_{B1}	S_B >2
S_{R2}	S_R ==2	S_{Y2}	S_Y ==2	S_{B2}	S_B ==2
S_{R3}	S_R <2	S_{Y3}	S_Y <2	S_{B3}	S_B<2

this controller directly determines the modulation index (m_a) for the inverting stage in a standalone system. However, in a grid-connected system, an inner current controller can be suitably inserted to determine the required modulation index. The modulation index (m_a) determines the amplitudes of the modulation signals (v_{modR}, v_{modY}, v_{modB}) for the three phases. These modulation signals are then compared with two level-shifted, in-phase carrier waveforms and are further processed as shown in Fig. 3 to generate the SV locations [S_R S_Y S_B] for the corresponding phases. Each space-vector index assumes one of the five values amongst [0, 1, 2, 3, 4]. Table I presents the conditions to be fulfilled to generate the PWM signals for the switching devices present in the LSU. Similarly, the devices of each output T-legs are switched based on the value of the corresponding space vector as given in Table II.

IV. ANALYSIS OF SEMI-SINGLE STAGE OPERATION

One of the important features of the proposed power circuit is that it can transfer a significant portion of the PV power directly to the load (referred to as 'single-stage operation'). The remaining portion of the generated PV power is processed through the VBU, shown in Fig. 1(a) (referred

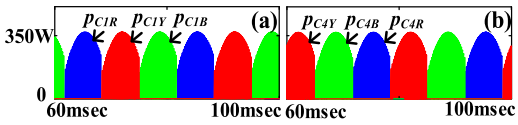

Fig. 4. (a) Power utilization of C_1 for each phases (i.e., p_{C1R}, p_{C1Y}, p_{C1B}), (b) Power utilization of C_4 for each phases (i.e., p_{C4R}, p_{C4Y}, p_{C4B}).

to as 'double-stage operation'). To establish the relationship between the total load power and the power processed through each power stage (single-stage and double-stage), instantaneous power equations are derived with the help of switching functions and three-phase load currents (i_R, i_Y, and i_B). The switching variable for any particular switch S_k (k $\in$ S_{R1}, S_{Y1}, S_{B1} ... etc.) is represented as S_{Sk} (i.e., S_{SR1}, S_{SY1} ...etc). The variable S_{Sk} assumes a value of '1' when the corresponding switch is turned on, and a value of '0' while it is turned off. The instantaneous power utilization (p_{C1} and p_{C4}) of the SCs are derived by summing up the power utilization corresponding to each phase as,

$$p_{C1} = p_{C1R} + p_{C1Y} + p_{C1B} = v_{C1}S_{SU1}(|i_R|S_{SR1} + |i_Y|S_{SY1} + |i_B|S_{SB1}) \quad (3)$$

$$p_{C4} = p_{C4R} + p_{C4Y} + p_{C4B} = v_{C4}S_{SL2}(|i_R|S_{SR3} + |i_Y|S_{SY3} + |i_B|S_{SB3}) \quad (4)$$

The symbols v_{C1} and v_{C4} respectively represent the voltages across the capacitors C_1 and C_4. The eqns. (3)-(4) are simulated assuming that the proposed power converter delivers a load of 1kW and the input voltage V_{PV} is 100V. Thus, the voltage across each capacitor is 50V, i.e., ($v_{C1} = v_{C2} = v_{C3} = v_{C4} = 50$V). The simulation results corresponding to the instantaneous powers p_{C1} and p_{C4} are shown in Figs. 4(a) and (b) respectively. The simulation results corresponding to the instantaneous powers p_{C1} and p_{C4} are shown in Figs. 4(a) and (b) respectively.

Similarly, the instantaneous powers (p_{C2} and p_{C3}) of the dc-link capacitors are derived as:

$$p_{C2} = v_{C2}(|i_R|S_{R1} + |i_Y|S_{Y1} + |i_B|S_{B1}) \quad (5)$$

$$p_{C3} = v_{C3}(|i_R|S_{R3} + |i_Y|S_{Y3} + |i_B|S_{B3}) \quad (6)$$

Now, the total power (p_{Total}) can also be derived as,

$$p_{Total} = p_{C1} + p_{C2} + p_{C3} + p_{C4} \quad (7)$$

In order to determine the average energy utilization of each capacitor, in each power cycle, the energy utilization factors (E_i, where $i \in C_1, C_2, C_3$, and C_4) are determined as,

$$E_{C1} = \frac{\int_0^\pi p_{C1}d(\omega t)}{\int_0^\pi p_{Total}d(\omega t)} = 20\%;\ E_{C4} = \frac{\int_0^\pi p_{C4}d(\omega t)}{\int_0^\pi p_{Total}d(\omega t)} = 20\% \quad (8)$$

$$E_{C2} = \frac{\int_0^\pi p_{C2}d(\omega t)}{\int_0^\pi p_{Total}d(\omega t)} = 30\%;\ E_{C3} = \frac{\int_0^\pi p_{C3}d(\omega t)}{\int_0^\pi p_{Total}d(\omega t)} = 30\% \quad (9)$$

It is evident from the above analysis that, the proposed configuration is capable of delivering 60% of the total PV energy through the single-stage operation (i.e., (E_{C2}+E_{C3})). Also, the two DC-link capacitors are self-balanced as the single-stage energy is equally divided between them. The rest of the 40% of the PV energy is transferred through the double-stage operation (i.e., ($E_{C1} + E_{C4}$)). Since this energy is also distributed equally among the upper and lower SCs, the power loss and the size of the passive elements are reduced. In contrast, with the conventional front-end boost stage, the total energy is processed through two stages, incurring higher power losses in

TABLE III
PARAMETERS FOR EXPERIMENTAL PROTOTYPE

Experimental Parameters							
V_{PV}	f_{sw}	Load	C_2,C_3	C_1,C_4	L_1, L_2	R_P	C_P
100V	5kHz	45Ω, 2mH	1mF	1mF	3mH	5Ω	100nF

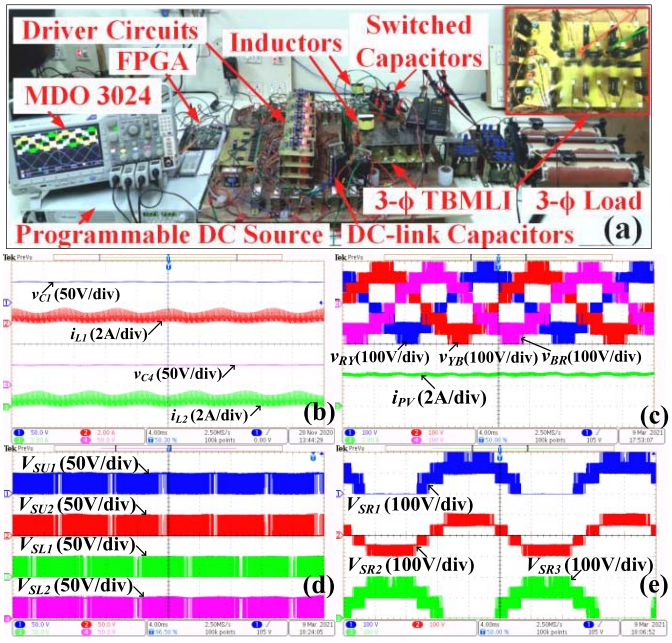

Fig. 5. (a) Experimental prototype, (b) SC voltages (v_{C1}, v_{C4}), and inductor currents (i_{L1}, i_{L2}), (c) three-phase voltage, input PV current, (d) and (e) blocking voltages of the switches in the LSU and R-phase respectively.

the dc-dc stage. In addition, the design of the passive elements (C_i, L_i) in the VBU can be derived using the following expressions:

$$C_i = \frac{4P_T}{\omega v_{ph} f_{sw} T_{fund} \Delta V}; L_i = \frac{\sqrt{2} P_T V_{PV}}{3 v_{Ph} f_{sw} I_{Li}^2} \tag{10}$$

where P_T represents the total load power, ω is the electrical angular frequency, v_{Ph} is the RMS values of the output phase voltage, f_{sw} is the switching frequency of VBU, T_{fund} represents the time duration of the fundamental power cycle, ΔV indicates voltage ripple in the SC and I_{Li} is the peak value of the inductor current.

V. EXPERIMENTAL RESULTS

The performance of the proposed power converter, along with the associated PWM technique, is assessed with experimental studies with the aid of a scaled-down prototype [Fig. 5(a)]. The circuit parameters, which are used for experimental validation, are listed in Table III. The MOSFET IRF 460 along with the HCPL-3120 gate-driver are used in the hardware prototype. The gating signals for the switching devices, with the adopted modulation strategy, are obtained with the aid of a SPARTAN-6 FPGA platform. A programmable dc-source with a voltage (V_{PV}) of 100V is connected across the P and N terminals [Fig. 1(a)]. The voltage waveforms of the SCs (v_{C1}, v_{C4}) and the corresponding currents (i_{L1}, i_{L2}) in the energy storage inductors are shown in Fig. 5(b). From Fig. 5(b), it is evident that the voltages across both of the SCs are regulated at 50V, while the total dc-link voltage ($v_{dc-link}$) is regulated at 200V. The three-phase

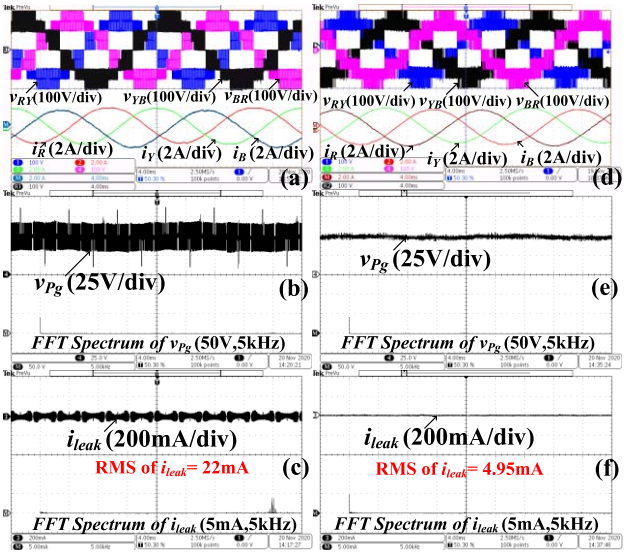

Fig. 6. Experimental results for three-phase line-voltages (v_{RY}, v_{YB}, v_{BR}) and currents (i_R, i_Y, i_B) for conventional SPWM (a-c) and proposed PWM (d-f).

line-to-line voltages (v_{RY}, v_{YB}, v_{BR}), along with input current (i_{PV}), are shown in Fig. 5(b). Furthermore, the blocking voltages of the switches in the LSU and one of the phases (R-phase) are shown in Figs. 5(d) and (e) respectively. From these experimental results, it is evident that the switches in LSU should be rated to withstand 1/4th of the total dc-link voltage (i.e., $v_{dc-link} = 200$V). Similarly, the top and bottom switches (e.g., S_{R1}, S_{R3}) of the phases and the bi-directional switch (e.g., S_{R2}) should be rated to withstand the voltages $v_{dc-link}$ and $v_{dc-link}/2$ respectively. Fig. 6 presents the comparison of the inverter operation between the conventional phase-shifted SPWM strategy and the proposed PWM scheme at the limit of linear modulation. From these waveforms, it is apparent that the proposed PWM scheme doesn't compromise on the harmonic performance compared to the conventional SPWM scheme. In addition, to analyze the influence of these modulation schemes on the leakage current, the parasitic voltage (v_{Pg}) and the leakage current (i_{leak}) are measured and presented in Figs. 6 [(b,c),(e,f)]. Though the conventional phase-shifted SPWM technique with the proposed configuration has the capability of reducing the magnitude of high-frequency transitions to 50% [12], the leakage current is still strongly influenced by the switching frequency and the input voltage of the inverter. However, the proposed modulation strategy is capable of eliminating all high-frequency transitions from the parasitic voltage (v_{Pg}) [Fig. 6(e)]. Consequently, the leakage current through the parasitic capacitive elements of the PV panel is reduced [Fig. 6(f)]. The RMS values of the respective leakage currents with the conventional phase-shifted and the proposed PWM (22mA and 4.95mA) support this fact. Thus, it is evident that the proposed configuration along with its modulation technique is capable of reducing the leakage current irrespective of the switching frequency and the input voltage of the inverter without sacrificing the harmonic performance and the dc-link utilization. Total elimination of transitions in parasitic voltage (v_{Pg}) reduces the requirement of additional common-mode chokes and EMI filters, which further improves the overall efficiency of the system. In addition, the dynamic behavior of the proposed configuration for the variation of the load current and irradiance are shown in Figs. 7(a) and (b) respectively. It is observed that the control scheme is capable of regulating the SC voltages for both of these dynamic conditions.

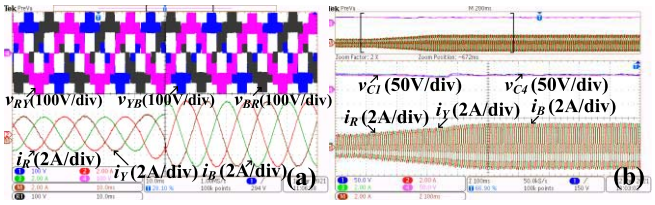

Fig. 7. Three-phase line-voltages (v_{RY}, v_{YB}, v_{BR}) and currents (i_R, i_Y, i_B) at (a) step-change in load current, (b) dynamic variation in atmosphere condition.

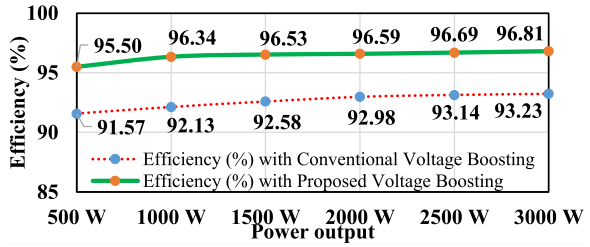

Fig. 8. The plot of efficiency vs. power output for the proposed configuration and conventional voltage boosting strategy.

TABLE IV
PARAMETERS FOR EXPERIMENTAL PROTOTYPE

Topology	A	B	C	D	E	F	G
[13]	24+0	6+0	4	3 p.u.	1	Constant	10mA
[6]	24+0	8+0	1	2 p.u.	1	Constant	10mA
[7]	16+0	4+0	4	2 p.u.	1	Constant	10mA
[5]	16+2	6+0	2	2 p.u.	1	Oscillating	120mA
Proposed	18+2	4+2	1	1 p.u.	2	Constant	12mA

A: Number of switches + diodes, **B:** Number of capacitors + inductors, **C**: Number of required isolated source, **D**: Total DC link voltage requirement, **E**: Boost factor = (total-dc link voltage)/ (input PV voltage), **F**: Nature of CMV, **G**: Peak magnitude of the leakage current.

VI. PERFORMANCE ANALYSIS

A power-loss analysis has been carried out (Fig. 8) using the PLECS software to compare the performance of the proposed voltage boosting strategy with the conventional boost strategy. The efficiency of the proposed system for both of the voltage boosting strategies is obtained at power output ranging from 500W to 3kW in steps of 500W as presented in Fig. 8. The detailed thermal model of the switching device (IKW30N60T) and its body diode are extracted from the manufacturer's datasheet. The power losses incurred in the passive elements of these converters are also considered for comparison. It is observed that the power loss incurred in the inverting stage is the same for both conventional and the proposed voltage boosting techniques. However, the power loss incurred in the voltage boosting stage is significantly higher with the conventional boosting strategy. Thus, the improved efficiency of the proposed converter can be attributed to its partial direct power transfer capability.

A comparison of the proposed power converter with those reported earlier is summarized in Table IV. Though the configurations introduced in [6], [7], and [13] are capable of reducing the leakage current, they require a higher number of switching devices and isolated PV sources. Though the topology presented in [5] requires a reduced number of devices, the CMV and the leakage current are strongly influenced by the inverter switching frequency and the input voltage. In contrast, the proposed topology is capable of eliminating all hi-frequency transitions in the CMV, leading to the reduction of the leakage current while achieving a voltage boosting factor of '2'.

VII. CONCLUSION

This brief proposes an integrated three-phase inverter configuration, which is capable of: (i) synthesizing a three-level voltage waveform from a single PV source (ii) obtaining a boosting factor of two while limiting the inrush currents in comparison to the existing switched-capacitor (SC) based networks (iii) eliminating all of the voltage transitions across the parasitic capacitance of the PV panels, paving the way to the reduction of the leakage current irrespective of the PV panel voltage and the switching frequency of the inverter. The most important feature of this configuration is its capability of transferring a larger portion (60%) of the PV energy directly to the load; only 40% of it is processed through the boosting stage. This feature improves the overall efficiency of the system in comparison with the conventional boosting scheme. The proposed boosting stage results in an improved power density and equalization of power loss amongst the two interleaved sections. Owing to these features, it is envisaged that the proposed 3-ϕ TBMLI configuration is suitable for PV systems with three-phase output.

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