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A New Dual Quasi Z-Source Based T-Type Five-Level Inverter with HERIC Structure for PV System

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***Abstract*—This paper presents a new dual quasi Z-Source (qZS) based T-type five level inverter with HERIC structure for PV system with the merits of single stage boosting, reduced device count, higher efficiency and reliability. The proposed topology is capable of providing reactive power support, which is an essential requirement of present PV inverters. Moreover, the high frequency oscillations due to the common mode voltage(CMV) are reduced by the passive filter, which also limits leakage current within the standards for transformer less operation. Level shifted PWM control scheme is implemented to study the steady state and dynamic behavior of the proposed topology in MATLAB environment. Finally, a detailed comparison is made with the existing topologies in the literature to highlight the merits of the proposed topology.**

Keywords—quasi Z-source, five-level inverter, level shifted PWM

I. Introduction

Renewable energy sources (RES) play a vital role in substituting the existing fossil fuel based generating stations since fossil fuel use has led to environmental concerns and diminishing fossil fuel reserves. Various RES based power generations such as Wind, Photovoltaic, Fuel Cell, etc. are becoming popular in the present scenario. Of these, Photovoltaic (PV) systems are highly promising as energy generators since these are inexpensive, compact in size and very reliable [1]. Therefore, the development of power electronic interface is getting popular for integrating PV panels into the utility/grid connected applications [2]. Because, it delivers DC power at low voltage. These can be done either with single stage DC/AC inverters or by a combination of DC/DC boost converter with DC/AC inverters i.e., by two-stage operation. The single stage DC/AC inverter is low cost, has compact size and promises higher efficiency [3]. But many PV panels are connected in series and parallel combination for increased voltage and power levels because of its buck nature. On the other hand, the two-stage system provides better MPPT operation, reactive power capability, lower leakage current and UPF grid current control [4]. However, it suffers from more component count, lower reliability and less efficiency.

In this context, a new topology of Z-source inverter was invented by Peng in 2002 with the benefits of single-stage boosting and DC/AC inversion [5]. It owns the merits of low EMI, and better shoot-through immunity problems in conventional voltage source inverters. Later, an improved version of quasi Z-source (qZS) inverter was developed with continuous current operation and low component ratings, which is the essential requirement for Photovoltaic applications [6]. Most of the research is available in the literature is invented based on qZS inverters due to the potential capability for single stage boosting inverter (SSBI) operations.

Recently, multilevel inverters (MLIs) are gaining attention due to reduced component count, low total harmonic distortion, less voltage stress across the semiconductors and lower filter requirement [7]. However, the conventional topologies of (a) NPC-MLIs, (b) FC-MLIs, and (c) CHB-MLIs suffer due to issues of more passive components and high complexity in DC-link voltage balancing for increased levels. Many topologies have been derived based on these MLI configurations [8]. However, all the topologies are buck in nature. Therefore, the present research focuses on the development of high efficient impedance source based MLIs which impose both the benefits.

Some of the topologies investigated with quasi Z-source networks with NPC, Cascaded-Bridge, Half-Bridge inverter and Modified qZS based MLIs were reported in [9]–[12]. However, the above said topologies suffers either because of the need of two PV sources or complexity in control. Moreover, most of the work reported above did not address the major requirement of low leakage current while connecting PV into the grid [13]. Therefore, in this paper, a new dual qZS based T-Type Five-Level Inverter with HERIC for PV systems is presented. Modified level shifted PWM is implemented with simple boost control shoot through technique to regulate the DC-Link voltage. A passive filter is used to limit the leakage current within the standards. Finally, the steady state as well as dynamic conditions of the proposed topology is tested through MATLAB simulation work.

II. Proposed Topology

Fig.1 shows the proposed new topology of dual qZS based T-Type Five-level inverter with HERIC structure for PV system. It consists of a dual qZS network cascaded with T-type five–level inverter and improved HERIC structure with Mid-point connection O. The parasitic capacitance and resistor are wired between the PV panels and the grid as per the standards to study issues due to leakage current. Moreover, to eliminate the high frequency oscillation generated by the CMV and to limit the leakage current a passive filter is introduced at the output of the inverter. For better understanding of the operation, the different modes of operations are as follows.

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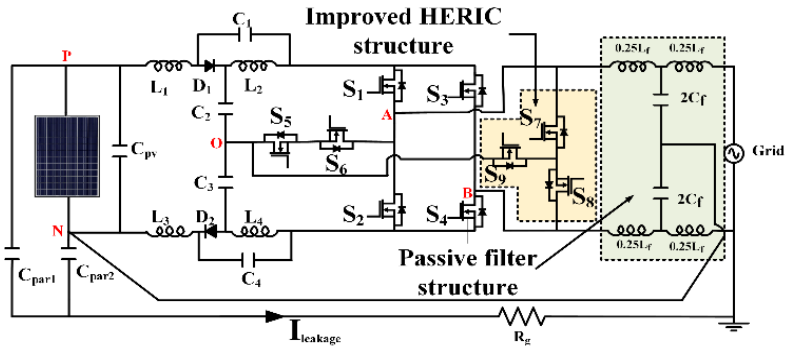

Fig.1 Proposed qZS based T-Type Five-level Inverter with HERIC Structure.

A. *Modes of Operation*

Fig.2. illustrates the different modes of operation of the proposed inverter. It is capable of developing five-level output waveforms. In order to achieve this, it is operates in two different modes of operation such as five Active, Non-shoot–through states, and two Shoot-through states. During Active, Non –shoot through states the output voltage levels $\pm V_{DC}/2$ generated in the output of the inverter are shown in Figs.2 (a)-(d). During the shoot-through states the boosting operation is achieved in two ways: upper shoot-through(UST) during the positive half cycle and lower shoot-through(LST) during the negative half cycle as shown in Figs.2 (e)-(f). Fig. 2(g) shows that the zero-state operation of the inverter is achieved by clamping the mid-point of the T-type inverter to reduce the CMV to zero. The complete voltage level generation and shoot-through periods by turning on the corresponding switches are given in Table I for better illustration.

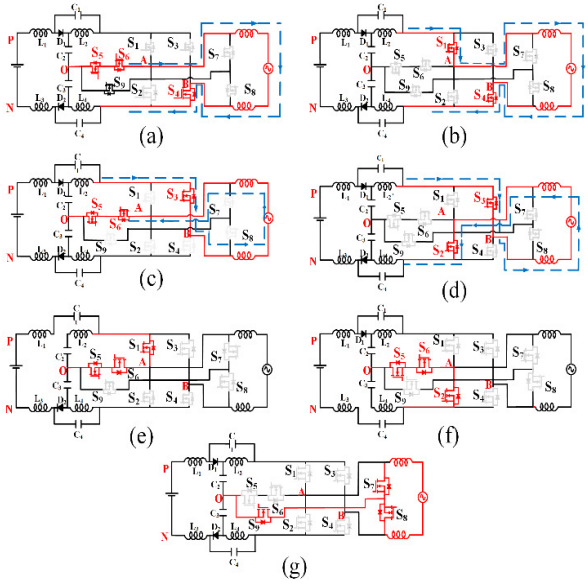

Fig. 2. Modes of operations (a)-(d) Level generations, (e) UST, (f) LST, (g) Zero state.

TABLE I SWITCHING SEQUENCE

Voltage levels	Turned-on Switches	Nature of the switching state
+V_{DC}/2	S_4, S_5 and S_6	Active, Non-shoot-through
+V_{DC}	S_1 and S_4	Active, Non-shoot-through
-V_{DC}/2	S_3, S_5 and S_6	Active, Non-shoot-through
-V_{DC}	S_2 and S_3	Active, Non-shoot-through
0	S_1, S_5 and S_6	Upper Shoot-through
0	S_2, S_5 and S_6	Lower shoot-through
0	S_7, S_8 and S_9	Zero-state

In order to achieve the shoot-through the condition to satisfy with the modulation index as follows;

$$D_S + m \leq 1 \tag{1}$$

Applying volt-sec balance, the condition to satisfy the voltage across capacitors is as follows [9];

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{(2-4D_S)} \tag{2}$$

$$V_{C2} = V_{C3} = \frac{(1-D_S)V_{IN}}{(2-4D_S)} \tag{3}$$

$$B = \frac{\hat{V}_{DC}}{V_{IN}} = \frac{1}{1-2D_S} \tag{4}$$

$$V_{out} = mBV_{in} \tag{5}$$

Where, B is the boost factor, V_{in} and V_{out} are input and output voltages, The average value of all the four capacitors of the qZs are $V_{C1}, V_{C2}, V_{C3}, V_{C4}$. The peak value of the measured DC-link voltage is the addition of all the four capacitors as follows,

$$\hat{V}_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{6}$$

B. *Modulation Scheme*

Fig. 3(a) shows the modified level shifted PWM implemented in this work. Four carrier waveforms are compared with one modulation sinusoidal waveform. The UST and LST were implemented by inserting a constant DC line at the top and bottom of the carrier waveforms. The logics involved in the generation of switching signals for S_1 to S_8 is shown in Fig. 3(b) to achieve the single stage boosting operation and the five-level output voltage waveform. Moreover, the proposed topology is capable of providing reactive power support. To achieve this, the modulation scheme provides the freewheeling path through the devices S_7, S_8 and S_9 during the negative power operation.

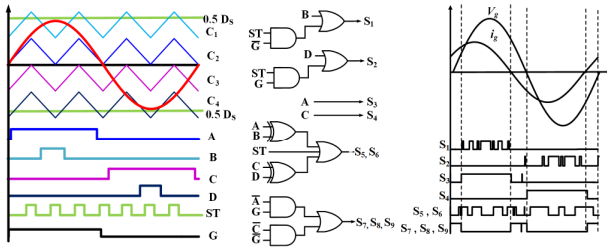

Fig. 3. Modified PWM Scheme implementation; (a) LSPWM scheme and corresponding signals. (b) Logic for generation of switching signals for S_1-S_8. (c) Switching signals during reactive loads.

III. Control Scheme

As proposed above, the steady state as well as dynamic performance of the proposed topology can be achieved by regulating the DC-link voltage of the inverter. Therefore, a two loop control is implemented, as shown in Fig.4. The DC-link voltage control is achieved with the help of capacitor voltages V_{C1} and V_{C2} in the outer loop while the inner current loop controls the inductor current (i_{L1}). Finally, the DC-link voltage is regulated for the corresponding changes in shoot-through duty ratio (D_s). A simple and well known perturb and Observe (P&O) algorithm is used to obtain the MPPT[14]. In order to generate the reference of peak output DC-link voltage (V^*_{DC}), the reference V^*_{PV} is compared with the actual input voltage and error is passed through the PI controller and this generates the reference value of the input current i^*_{L1}. The output of (i^*_{L1}-i_{L1}) is compensated by a simple P controller, which controls the output of the shoot-though duty ratio (D_s). It needs noting that D_s regulates the peak DC-link voltage under source as well as load disturbances. Finally, it is compared with the carrier waves and constant modulation signal to regulate the output of the inverter.

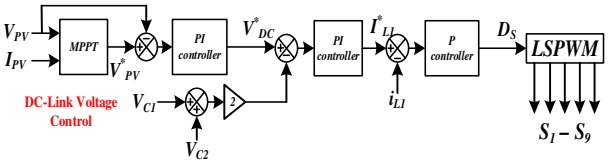

Fig. 4. Closed loop controller.

IV. Leakage Current Analysis

Suppression of leakage current is one of the major problems in transformerless PV inverters. The leakage current occurs due to the formation of parasitic capacitances and resistors between PV panels and grids, as shown in Fig.1. This is mainly due to time varying properties of change in common voltage (CMV) as discussed in session I. However, this can be minimized by avoiding high-frequency oscillations or by maintaining a constant CMV. The high frequency oscillations are mainly due to shoot-through mode of operation. The CMV of the proposed power converter (Fig.1) is as follows:

$$V_{CMV} = \frac{V_{AN}+V_{BN}}{2} \tag{7}$$

It can be noticed that from the above equation that the common voltage is the average of V_{AN} and V_{BN}. It can be effectively minimized by introducing filter. Fig. 1 shows a modified form of LC filter. The inductors are split into 4 parts and the capacitor into 2 parts. Whereas the mid-point of the capacitor is connected to the point 'N'. The lumped value of the LC-filter is given by:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{8}$$

V. Simulation Results

Here, the steady state performance of the proposed topology is verified through MATLAB environment, assuming the switches are ideal. Table II illustrates the parameters and their corresponding values considered for the simulation. An input voltage 100V, output voltage 110Vrms and modulation index (M_a) of 0.7 and D_s of 0.27 were considered to obtain the boost factor of 2.2 for the study.

The steady state response of boosted DC-link voltage, five-level (5L) output voltage and the filtered output voltage of the proposed topology are shown in Fig. 5. It can be noticed that the DC-link output voltage is boosted from 100V to 220V, which satisfies the boost factor of 2.2. The 5L output voltage waveform is clearly illustrated with the levels of $\pm$Vdc, $\pm$Vdc/2, and 0 in Fig. 5(b). Moreover, the filtered output voltage and current are purely sinusoidal and show the effectiveness of the filter. Fig. 6 depicts the CMV measured across the inverter terminals V_{AN}, V_{BN} and V_{CMV}. It can be noticed that the waveform across CMV is trapezoidal in shape and the leakage current is as minimum as possible, less than 20 mA, which is within the limits of German standard *VDE 0126-1-1*. In addition, the reactive power capability of the proposed topology has been demonstrated in Fig.7 through output voltage and load current waveforms.

TABLE II Simulation Parameters

Parameters		Values
P_O		500 W
V_{in}		100 V
V_{out} (rms)		110 V
Inductors	L_1-L_4	1 mH
	L_f	4 mH
Capacitors	C_1-C_4	1000 µF
	C_f	2 µF
	C_{PAR}	100 nF
Frequency	f_s	10 kHz
	f_o	50 Hz
R_g		10 Ω

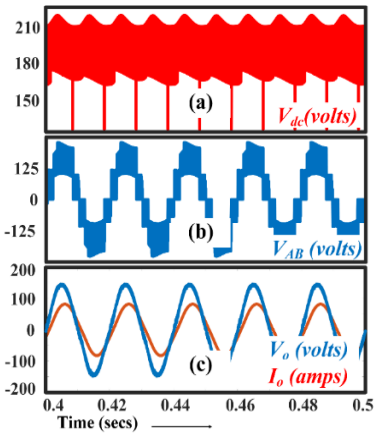

Fig. 5. Simulated waveform of the converter in steady state. (a) Boosted dc-link. (b) Level voltage across output terminals. (c) Output voltage and current.

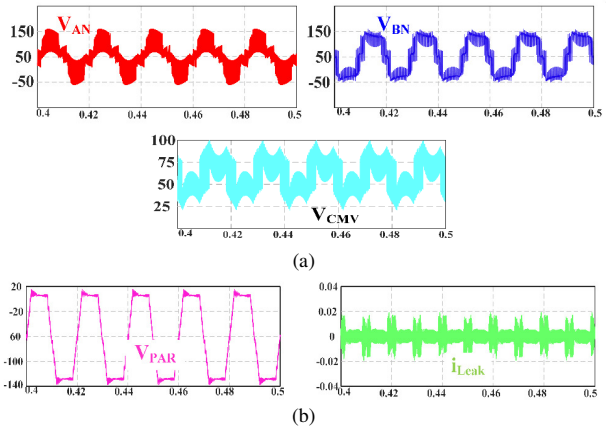

Fig. 6. Simulation results for parasitic elements; (a) Voltages across VAN, VBN and VCMV respectively. (b) Voltage across parasitic capacitance and leakage current.

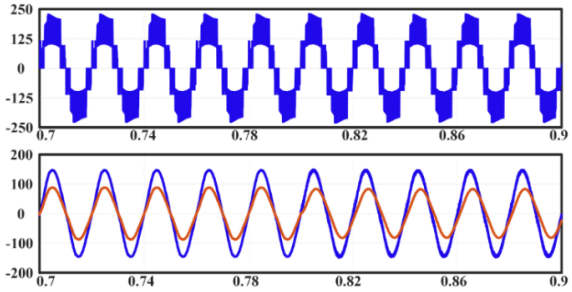

Fig. 7. Demonstration of reactive power capability through simulation (a) Level voltage of the converter. (b) Output voltage and current.

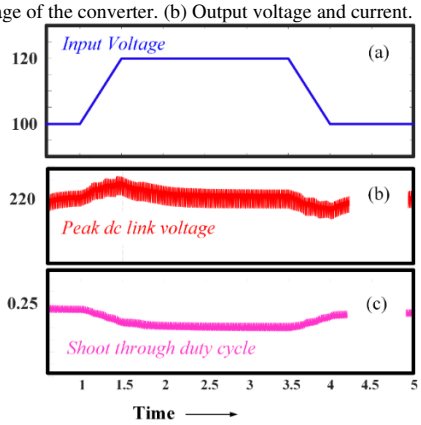

Fig. 8. Dynamic response of the converter for change in source. (a) Change in input voltage, (b) Peak dc-link voltage variation, (c) Change in shoot though duty cycle value.

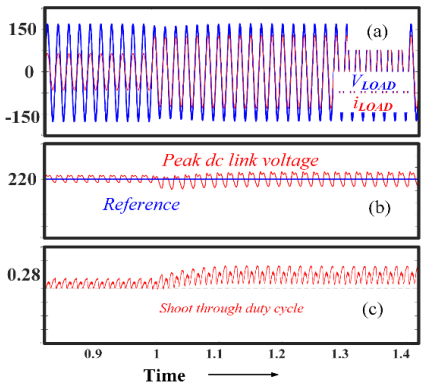

Fig. 9 Dynamic response of system subjected to load change. (a) Simulated waveform of load voltage and current during change. (b) Reference and Peak dc-link voltage. (c) Shoot through duty cycle.

TABLE III COMPARISON OF PROPOSED TOPOLOGY WITH EXISTING TOPOLOGIES

Type of converter		Proposed	[9]	[10]	[11]	[12]
Levels		5	5	5	5	5
Components	S*	8	8	9	8	8
	D*	6	2	2	3	2
	L*	4	4	4	2	4
	C*	4	4	4	4	4
TBV		$7.5V_{dc}$	$6V_{dc}$	$4V_{dc}$	$6V_{dc}$	$6V_{dc}$
Vin		1	1	2	1	2
Z*		3	4	4	4	3

S=Switches, D=Diodes, L=inductors, C=Capacitors, TBV=Total Blocking Voltage, Vin=Number of Sources, Z=No. of conducting switches

Moreover, the dynamic response of the topology is analyzed for input voltage changes from 100V to 120V in Fig. 8. Similarly, Fig. 9 shows the dynamic response of the topology for load disturbance. In both the cases, the peak DC-link voltage is well regulated by adjusting *Ds*. This shows the proposed topology is well-opted solution for PV applications.

Table III shows the comparison of various five-level impedance source based MLIs with the proposed topology in terms of device counts, total blocking voltage (TBV) and number of DC sources. It can be noticed that the proposed topology is the most opted for single source applications and with the merits of conduction of 3 switches during the Non-shoot through and Shoot-though states. This ensures maximum boosting as well as better efficiency. Though topology [10], [12] has similar components, it is not that efficient since there are higher conducting losses and there is the requirement of two input DC sources.

VI. CONCLUSION

In this work, a new topology of single-stage boosting dual qZs based T-Type five-level inverter with HERIC structure has been presented. It owns the merits of continuous input current, reduced voltage stress, and better quality of output voltage waveforms. Complete modes of operation, the control scheme and leakage analysis were presented. Moreover, it uses far fewer conducting devices compared to other topologies available in the literature that ensure more efficiency. Moreover, the steady state as well as dynamic performance of the proposed topology have been analyzed through source and load changes. The output voltage is regulated well by the control scheme designed for the purpose. The leakage current is also within the standards. This shows the proposed topology is suitable for transformerless operations of the PV system.

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