A Nine-Level Transformerless Boost Inverter With Leakage Current Reduction and Fractional Direct Power Transfer Capability for PV Applications

Sumon Dhara, *Graduate Student Member, IEEE*, and V. T. Somasekhar, *Member, IEEE*

***Abstract*— This article describes an integrated voltage-boosting technique, which is essential to achieve compatibility between low-voltage photovoltaic (PV) panels and high-voltage dc links needed for dc-to-ac conversion. To achieve the twin objectives of voltage-boosting and multilevel inversion, this article proposes a transformerless T-type nine-level hybrid boost inverter. To improve the efficiency in the boosting stage of the proposed converter system, a significant portion of the PV energy is directly transferred from the PV source to the load, while the other part is processed through an interleaved converter, which is fused with the inverter. Thus, the proposed converter ensures a higher power density and reduces the power ratings of the semiconductor devices. This article also introduces a modified zone-based pulsewidth modulation (PWM) technique, which achieves a complete elimination of the switching frequency voltage transitions in the total common-mode voltage (TCMV). Thus, this technique mitigates the generation of leakage current while preserving the advantages of conventional multilevel inverters such as low dv/dt and inductive power capability. Besides that, a rigorous mathematical analysis for the common-mode equivalent circuit of the proposed configuration is also presented in this article. Detailed simulation and experimental studies are carried out to validate the feasibility of the proposed configuration.**

***Index Terms*— Common-mode voltage (CMV), integrated voltage-boosting, leakage current, multilevel inverter, photovoltaic (PV) inverter, pulsewidth modulation (PWM) technique, transformerless inverter.**

I. Introduction

PHOTOVOLTAIC (PV) systems contribute a major portion of the total installed capacity of renewable energy systems across the world. PV-based industrial, commercial, and domestic applications are increasingly being used across the globe. Economic viability owing to the declining cost of the PV panels and abundant availability of solar power are the critical factors for the growth of the PV market in the upcoming years. Among all variants of single-phase PV inverter topologies, transformerless PV inverters have become more popular due to reduced volume, weight, cost, and higher energy density [1]. However, the absence of galvanic isolation results in a significant leakage current, which is mainly caused by the parasitic capacitance of the PV panel. Besides compromising the safety of the PV system [2], the leakage current deteriorates the system performance and life span of the PV panels. The root cause for the existence of the leakage current is the voltage transitions that appear across PV parasitic capacitance, which exists between the PV panels and frame. The voltage across the parasitic capacitance of the PV panel is often referred to as the total common-mode voltage (TCMV). The following equation relates the leakage current and the TCMV:

$$i_{\text{leak}} = C_{\text{PV}} \times \frac{d(V_{\text{TCMV}})}{\text{d}t}. \tag{1}$$

The commercial multi-level inverter (MLI) configurations for the PV inverter system can be classified as: 1) common-ground (CG); 2) dc-decoupling; and 3) ac-decoupling topologies. The CG configurations, such as 1) neutral point clamped (NPC) inverter [3]; 2) T-type inverter [4]; and 3) active virtual ground [5], achieve complete elimination of leakage current, as the voltage across the PV parasitic capacitance is constant in a given fundamental cycle. However, the conventional cascaded H-bridge (CHB), flying capacitor (FC) topologies are retrofitted with additional semiconductor devices to use decoupling-based modulation techniques to minimize the high-frequency voltage transitions across the PV parasitic capacitance. These configurations often require a high number of semiconductor devices, clamping diodes to realize five-level (5L) or seven-level (7L) topologies. Besides, the CG and FC topologies suffer from the under-utilization of dc link and the issue of voltage balancing of dc-link capacitors. Moreover, PV inverter configurations generally require a boosting stage to handle the problem of low PV voltage conditions caused by uncertain environmental conditions. A 5L inverter topology is proposed in [6], which uses a cascaded half-bridge (HB) in its structure. In this topology, the alleviation of the leakage current is achieved by the use of an appropriate modulation technique. However, the output voltage of the proposed inverter [Fig. 1(b)] suffers from two major disadvantage of: 1) high total harmonic distortion (THD) and 2) high dv/dt across the switches with respect to the conventional multilevel output voltage [Fig. 1(a)]. This topology is not capable of enhancing the voltage gain, thereby causing a high dc-link voltage requirement at its input. In [7], a new MLI configuration with a boosting feature is presented, but the configuration is not capable of producing reactive power and extending the number of voltage levels.

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The authors are with the Department of Electrical Engineering, National Institute of Technology at Warangal, Warangal 506004, India (e-mail: dsumon@student.nitw.ac.in; sekhar@nitw.ac.in).

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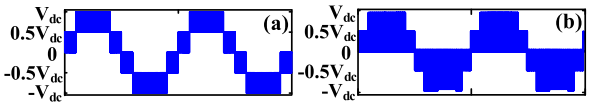

Fig. 1. (a) Conventional multilevel output. (b) Modified PWM techniques.

To address the issue of reduced efficiency and requirement of high-power ratings of the semiconductor devices in the voltage-boosting stage, a group of single-stage inverter configurations are reported in [8]–[12], which discard the requirement of high step-up converters at the front-end [8]. The converter described in [9] introduces the concept of switched capacitor (SC) to increase the number of voltage levels and the voltage-boosting capability.

In [10], a 7L inverter has been proposed, which uses two SCs and 16 switching devices to achieve a boost factor of 3. However, the issue of leakage current and TCMV are not addressed in this work. Another switched capacitor-based multi-level inverter (SCMLI) based step-up multilevel inverter is proposed in [11], which synthesizes $(2n+1)$ (where "n" is no of SC modules) voltage levels from a single dc source. It also archives self-balancing of all SCs. However, the more number of SCs in this configuration increases the size and reduces the power density of the overall inverter. Also, these topologies [8]–[12] suffer from the shortcoming of hard-charging of the SCs, which causes a high inrush current leading to high current stress on the components and degrades their performance and reliability.

To overcome the issue of inrush current, a 5L inverter is proposed in [13], which incorporates a modified buck–boost-based structure for generating multilevel output voltage. However, the inverter uses a modulation technique, which synthesizes the voltage levels, as shown in Fig. 1(b), thereby increasing high $d\upsilon/dt$ across the switches and increasing the filter requirements. Another modified SCMLI topology is proposed in [14], which uses a quasi-resonant charging path. A resonant inductor is incorporated in this power circuit configuration to realize a soft-charging current path for the capacitors. However, this configuration suffers from the high-frequency voltage transition in TCMV, which causes a high leakage current. An improved bidirectional buck–boost converter-based CG transformerless inverter has been introduced in [15] and [16] to alleviate the issue of current stress on switches and transitions in TCMV. However, this configuration is penalized by the number of output voltage levels (two-level).

From the foregoing discussion, it is clear that there is a need for a multilevel single-phase transformerless inverter topology with the following features:

1) complete dc bus utilization as opposed to HB-based configurations;
2) voltage-boosting capability with reduced current stress on the semiconductor devices as opposed to the conventional SC-based topology;
3) elimination of switching frequency transitions from the TCMV waveform only with modulation technique (i.e., without any additional circuitry);

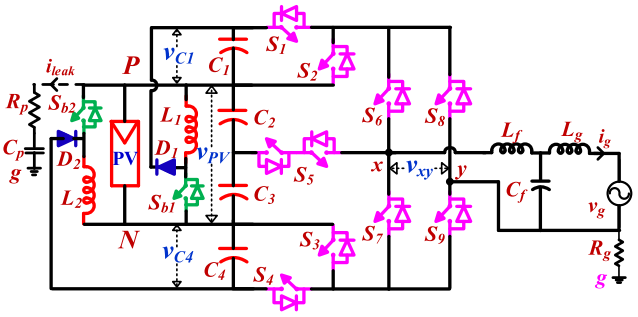

Fig. 2. Circuit schematic of the proposed 9L-T-HBI topology.

TABLE I
SWITCHING STATES OF VOLTAGE LEVELS

Sw. Seq.	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	v_{ab}
S^{+3}	1	0	0	1	0	1	0	0	1	$+3V_{PV}$
S^{+2A}	0	1	0	1	0	1	0	0	1	$+2V_{PV}$
S^{+2B}	1	0	1	0	0	1	0	0	1	$+2V_{PV}$
S^{+1A}	0	1	1	0	0	1	0	0	1	$+V_{PV}$
$S^{+0.5A}$	0	1	1	0	1	0	0	0	1	$+0.5V_{PV}$
S^{+0}	0	1	1	0	0	0	1	0	1	0
S^{-0}	0	1	1	0	0	1	0	1	0	0
$S^{-0.5A}$	0	1	1	0	1	0	0	1	0	$-0.5V_{PV}$
S^{-1A}	0	1	1	0	0	0	1	1	0	$-V_{PV}$
S^{-2A}	0	1	0	1	0	0	1	1	0	$-2V_{PV}$
S^{-2B}	1	0	1	0	0	0	1	1	0	$-2V_{PV}$
S^{-3}	1	0	0	1	0	0	1	1	0	$-3V_{PV}$

4) generation of MLI output voltage from a single PV source to avoid the complexity of multiloop maximum power point tracking (MPPT) algorithms for multiple PV sources;
5) ability to handle inductive loads (similar to the conventional MLIs), without any additional clamping diodes or capacitors.

This article presents a new integrated transformerless 9L-MLI, wherein an interleaved buck–boost converter is fused with a level generation unit to realize the above-mentioned features. The main contribution of this article is to introduce a new power circuit configuration with semidouble staged multilevel inversion along with a modified modulation strategy. In addition, the proposed configuration exhibits a symmetrical structure, which increases the redundancy among the switching combinations. This feature facilitates to devise a pulsewidth modulation (PWM) scheme, which uses the cyclic utilization of the dc-link capacitors and an even distribution of power losses among the interleaving sections of the boosting stage. It is also shown that the system is also capable of complying with the VDE-0126-1-1 standards for the PV inverter [17]. A common-mode model of the proposed topology along with the mathematical derivation of the TCMV is also presented in this article.

II. OPERATION OF PROPOSED 9L INVERTER

The power circuit configuration of the proposed nine-level T-type hybrid boost inverter (9L-T-HBI) is shown in Fig. 2. This MLI configuration uses two HB, one bidirectional

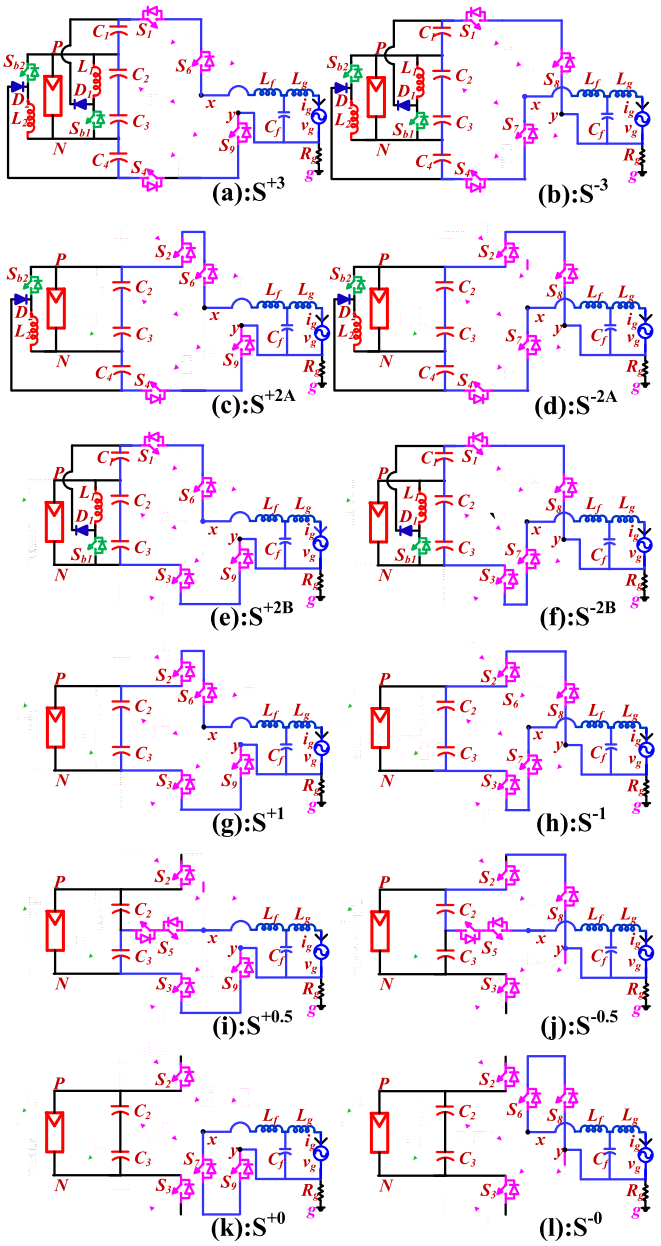

Fig. 3. Mode I. (a) $+3\ V_{PV}$. (b) $-3\ V_{PV}$. Mode IIA. (c) $+2\ V_{PV}$. (d) $-2\ V_{PV}$. Mode IIB. (e) $+2\ V_{PV}$. (f) $+2\ V_{PV}$. Mode III. (g) $+\ V_{PV}$. (h) $-V_{PV}$. Mode IV. (i) $+0.5\ V_{PV}$. (j) $-0.5\ V_{PV}$; Mode V. (k) Freewheeling. (l) Freewheeling.

T-branch, and one polarity generator H-bridge in its structure. This power circuit configuration comprises nine power switches ($S_1, S_2, \ldots, S_9$) for the generation of distinct nine voltage levels at the output. An interleaved buck–boost converter, which is constituted by two switches (S_{b1} and S_{b2}), two inductors (L_1 and L_2), and two diodes (D_1 and D_2), energizes the SCs (C_1, C_4). However, the dc-link capacitors (C_2, C_3) are directly connected across the PV source. This configuration decouples the dependence of the charging durations of the SCs from the inverter modulation scheme. This further helps in independent design of SCs, compared with the requirement of bulky SCs in recent SC-based boosting topologies [8]–[11].

The switching states of the individual switching devices to obtain individual voltage levels are listed in Table I, wherein the turn-on and turn-off states of them are indicated as "1" and "0," respectively. The modes of operation to synthesize nine distinct voltage levels are presented in Fig. 3. The switching sequences of Mode I ($\pm 3V_{PV}$) are indicated as S^{+3} and S^{-3} in Table I, respectively, for positive and negative half-cycles. It is observed that in this mode, the total dc-link voltage is realized by the PV source and the two SCs (C_1 and C_4). It may be observed that Mode II ($\pm 2V_{PV}$) exhibits redundant switching states; these are represented as S^{+2A} and S^{+2B} for the positive half cycle, and S^{-2A} and S^{-2B} for the negative half cycle, respectively. In Mode III ($\pm V_{PV}$) and Mode IV ($\pm 0.5V_{PV}$), both the boosting circuits are disabled, as the power directly flows from the PV source to the load. The switching sequences for Modes III and IV are represented as (S^{+1} and S^{-1}) and ($S^{+0.5}$ and $S^{-0.5}$), respectively, for the positive and negative half-cycles. From Fig. 3, it is evident that the proposed 9L-T-HBI configuration allows a path for the load current in both the directions (i.e., positive and negative) in all modes. Thus, it may be noted that the proposed configuration can also handle reactive loads [18], [19].

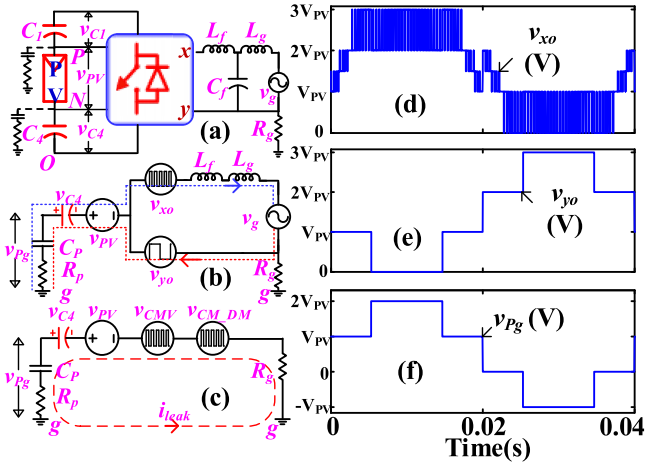

Fig. 4. (a)–(c) Common-mode equivalent circuit. Pole voltage: (d) v_{xo}, (e) v_{yo}, and (f) TCMV (v_{Pg}).

TABLE II
POLE VOLTAGE AND TCMV FOR ALL SWITCHING STATES

i	Sw. Seq.	v_{xo}	v_{yo}	v_{xy}	TCMV(v_{Pg})
1	S^{+3}	$3V_{PV}$	0	$3V_{PV}$	$2V_{PV}$
2	S^{+2A}	$2V_{PV}$	0	$2V_{PV}$	$2V_{PV}$
3	S^{+2B}	$3V_{PV}$	V_{PV}	$2V_{PV}$	V_{PV}
4	S^{+1}	$2V_{PV}$	V_{PV}	V_{PV}	V_{PV}
5	$S^{+0.5}$	$1.5V_{PV}$	V_{PV}	$0.5V_{PV}$	V_{PV}
6	S^{+0}	V_{PV}	V_{PV}	0	V_{PV}
7	S^{-0}	$2V_{PV}$	$2V_{PV}$	0	0
8	$S^{-0.5}$	$1.5V_{PV}$	$2V_{PV}$	$-0.5\ V_{PV}$	0
9	S^{-1}	V_{PV}	$2V_{PV}$	$-V_{PV}$	0
10	S^{-2A}	0	$2V_{PV}$	$-2V_{PV}$	0
11	S^{-2B}	V_{PV}	$3V_{PV}$	$-2V_{PV}$	$-V_{PV}$
12	S^{-3}	0	$3V_{PV}$	$-3V_{PV}$	$-V_{PV}$

III. COMMON-MODE ANALYSIS

The common-mode equivalent circuit for the proposed inverter configuration is presented in Fig. 4(a)–(c), wherein the PV parasitic element is modeled as a series connection of an equivalent resistor R_P and capacitor C_P. R_g specifies the

ground impedance with respect to load neutral. According to the common-mode model presented in Fig. 4(c), the TCMV (v_{Pg}) feeds the parasitic path, which eventually induces the leakage current. As the PV parasitic elements are capacitive in nature, it offers a low impedance path to high-frequency voltage components present in the TCMV.

A thorough TCMV analysis is carried out with the aid of the switching function analysis for the proposed configuration. The switching variables used in the study are indicated as S_{SX}, wherein "SX" denotes the corresponding switch ($S_1, S_2, \ldots S_9$). The value of the switching function S_{SX} is either "1" or "0" depending on the switching states of that switch. Furthermore, the common-mode equivalent circuits of the proposed 9L-T-HBI topology are derived as per the procedures derived in [19] and [20]. To obtain the mathematical expression of the TCMV (v_{Pg}), it is convenient to express the pole voltages ($v_{x\mathrm{o}}, v_{y\mathrm{o}}$) of each output terminals (x, y) with respect to the reference node "O" of the proposed configuration as shown in Fig. 4(c). The pole voltages can be expressed as per the following equations:

$$v_{x\mathrm{O}} = \big[(1 - S_{\mathrm{S8}})(S_{\mathrm{S1}}(2 - S_{\mathrm{S6}}) + S_{\mathrm{S6}} + S_{\mathrm{S5}} + 1) + S_{\mathrm{S8}}(S_{\mathrm{S3}}(2 - S_{\mathrm{S7}}))\big] \times V_{\mathrm{PV}} \quad (2)$$

$$v_{y\mathrm{O}} = ((2 - S_{\mathrm{S3}} + S_{\mathrm{S1}})S_{\mathrm{S8}} + S_{\mathrm{S3}}) \times V_{\mathrm{PV}}. \quad (3)$$

The voltage waveforms of $v_{x\mathrm{o}}$ and $v_{y\mathrm{o}}$ are shown in Fig. 4(d) and (e), respectively. Similarly, the CMV (v_{CMV}) and the differential mode voltage (v_{xy}) can be derived from the following equations:

$$v_{\mathrm{CMV}} = \frac{v_{x\mathrm{O}} + v_{y\mathrm{O}}}{2} \quad (4)$$

$$v_{xy} = v_{x\mathrm{o}} - v_{y\mathrm{o}}. \quad (5)$$

Moreover, the TCMV equation can also be realized with the aid of Millman's theorem as follows [20]:

$$v_{\mathrm{Pg}} = V_{\mathrm{PV}} + V_{C4} - V_{\mathrm{eqv}} \quad (6)$$

where

$$v_{\mathrm{eqv}} = v_{\mathrm{CMV}} + \frac{(L_2 - L_1)}{2(L_1 + L_2)} v_{xy} = v_{\mathrm{CMV}} - \frac{v_{xy}}{2} \quad (7)$$

where $L_2 = 0$ and $L_1 = L_{\mathrm{f}}$, as the configuration is a single inductor-based topology. Now, simplifying (6) and (7), the TCMV can be written as follows:

$$v_{\mathrm{Pg}} = V_{\mathrm{PV}} + V_{C4} - v_{y\mathrm{O}}. \quad (8)$$

The waveform of the TCMV (v_{Pg}) is shown in Fig. 4(f). Furthermore, from Fig. 4(c), the TCMV equation can be expressed in terms of i_{leak} as follows:

$$v_{\mathrm{Pg}} = \left(R_{\mathrm{G}} + R_{\mathrm{P}} + \frac{1}{sC_{\mathrm{P}}}\right) i_{\mathrm{leak}} = z_{\mathrm{leak}} i_{\mathrm{leak}} \quad (9)$$

where z_{leak} is the parasitic impedance of the PV panel. Therefore, the leakage current can also be estimated for the proposed configuration as per the following equation:

$$i_{\mathrm{leak}} = \frac{v_{\mathrm{Pg}}}{z_{\mathrm{leak}}} = \frac{V_{\mathrm{PV}} + V_{C4} - v_{y\mathrm{O}}}{z_{\mathrm{leak}}}. \quad (10)$$

Thus, the TCMV for each switching state can be determined from (3) and (8) using the switching states listed in Table I.

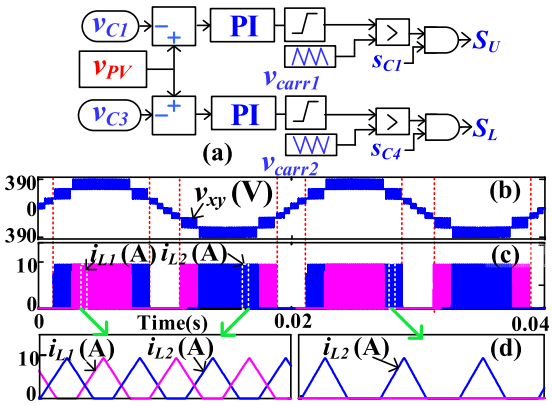

Fig. 5. (a) Closed-loop control strategy for voltage-boosting. (b) Inverter output voltage (v_{xy}). (c) Inductor currents (i_{L1}, i_{L2}). (d) Zoomed-in view of (i_{L1}, i_{L2}).

The leakage current can also be estimated mathematically using (10). The critical observation from Table II is that the switching sequences S^{+2A} and S^{+2B} result in the same output voltage, that is, 2 V_{PV} whereas the TCMV of the switching sequences is 2 V_{PV} and V_{PV}, respectively. Similarly, both the switching sequences (S^{-2A}, S^{-2B}) output the same voltage level (i.e., -2 V_{PV}) despite their difference in the corresponding TCMV magnitude.

It is evident that the proposed MLI configuration results in four different magnitudes in TCMV, namely, 2 V_{PV}, V_{PV}, 0, and $-V_{\mathrm{PV}}$.

When the inverter switches between two consecutive voltage levels, which possess two different TCMV magnitudes, switching transitions appear in the TCMV. These transitions cause leakage current. It is also observed that the maximum difference between any two magnitudes of the TCMV in consecutive levels is V_{PV}, which is one-third of the total dc-link voltage, as given in the following equation:

$$\max\left(\left|v_{\mathrm{Pg}}^{i} - v_{\mathrm{Pg}}^{i+1}\right|\right) = V_{\mathrm{PV}}. \quad (11)$$

IV. Voltage Boosting Scheme and Analysis of Modulation Strategy

A. Voltage Boosting Control

In this article, a time-sharing-based PWM is used for the front-end symmetrical interleaved buck–boost converter to charge the SCs from the PV source with reduced peak current stress on the semiconductor devices. The implementation of the control logic for the upper and lower sections of the boosting circuit is given in Fig. 5(a). Furthermore, the converter is always made to operate in the discontinuous mode of conduction (DCM) by an appropriate choice of the energy storage inductors (L_1 and L_2) pertaining to the boosting stage [21]. In DCM, whenever the inductor current fallbacks to zero [Fig. 5(d)], the trapped energy in the inductors is dissipated in each switching cycle. It may be noted that when operated in DCM, the switch and diode are both operated in zero current switching (ZCS) during the turn-on and turn-off times, respectively. This eventually leads to the reduction in the switching power loss incurred in the semiconductor devices. Furthermore, the operation in DCM results in smaller values

TABLE III
IDENTIFICATION OF ZONE OF OPERATION

Zones	z_s	z_1	z_2	z_3	z_4
R_1	1	0	0	0	1
R_2	1	0	0	1	0
R_3	1	0	1	0	0
R_4	1	1	0	0	0
R_5	0	1	0	0	0
R_6	0	0	1	0	0
R_7	0	0	0	1	0
R_8	0	0	0	0	1

of the inductors. Consequently, the right hand pole (RHP) zero associated with the system transfer function is placed far to the right compared with the switching frequency [22]. Hence, a simple proportional integrator (PI)-regulator-based voltage mode control can be implemented to regulate the voltages at the SCs (C_1, C_4). The PWM pulses for the switches S_U and S_L are finally generated after the "AND" operation of pulses obtained after the comparison with respective carrier signals (v_{carr1} and v_{carr2}) and the corresponding utilization signals of SCs (i.e., s_{C1} and s_{C4}), which are based on the modes of operation as explained in Section II. It also evident from Fig. 5(a) and (b) that L_1 supplies boosted energy in $+3$ V_{PV}, $+2$ V_{PV}, and -3 V_{PV} states, whereas L_2 supplies it in $+2$ V_{PV}, -2 V_{PV}, and -3 V_{PV} states. The closed-loop control also regulates the voltage across the SCs during the dynamic operation of the inverter.

B. Proposed PWM Strategy

The phase disposition sinusoidal pulsewidth modulation (PDSPWM) method is widely used for MLIs due to their superior harmonic performance and ease of implementation with commercial digital controllers [23]. A modified PDSPWM is used for the proposed inverter configuration as shown in Fig. 6(b). It can be observed that a modified sinusoidal modulation wave is compared with a triangular carrier to generate all nine voltage levels. The modified signal (v_{mod}) is synthesized from the fundamental modulation signal (r) with a modulation index m_a

$$r = m_a \sin \omega t. \tag{12}$$

The modified modulation (v_{mod}) waveform can be written as per the following equation:

$$v_{mod} = 6|r|z_1 + (6|r| - 1)z_2 + (3|r| - 1)z_3 + (3|r| - 2)z_4 \tag{13}$$

where $z_1 = 1$ when $(0 \le 6|r| < 1)$; $z_2 = 1$ when $(0 \le 6|r| - 1 < 1)$; $z_3 = 1$ when $(0 \le 3|r| - 1 < 1)$; $z_4 = 1$ when $(0 \le 3|r| - 2 < 1)$; $z_s = 1$ when $(r > 0)$. Furthermore, all nine voltage levels are grouped into eight zones $(R_1, R_2, \ldots, R_8)$ based on the values of z_1, z_2, z_3, z_4, and z_s as given in Table III.

A typical switching sequence showing the voltage levels corresponding to the aforementioned eight zones is shown in Fig. 6(a). The modified reference signal and the generation of PWM signals for each switch are shown in Fig. 6(b). The PWM modulator is programmed to output the switching

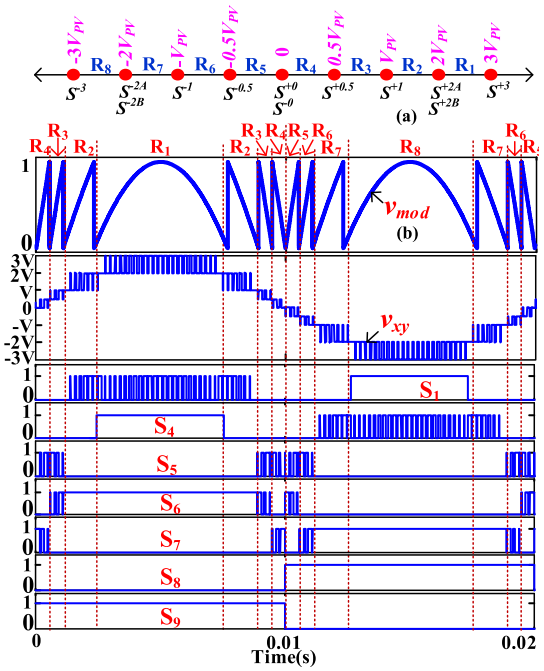

Fig. 6. (a) Eight regions in output voltage vector. (b) Generation of the modified modulation signal and the PWM signals for the switches.

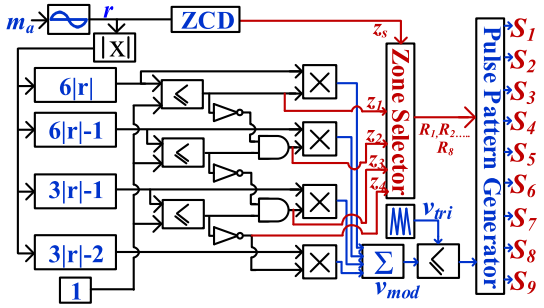

Fig. 7. Block diagram of the proposed modulation technique.

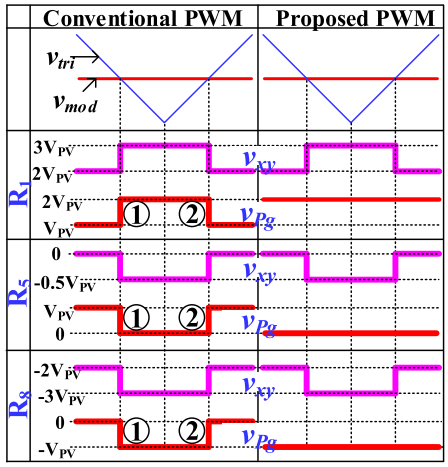

Fig. 8. Number of voltage transitions during each switching cycle in the output voltage (v_{xy}) and the TCMV (v_{Pg}) for zones R_1, R_5, and R_8.

sequence corresponding to each zone. These sequences can be selected independently of the available switching combinations (as given in Table I). It may be noted from Fig. 6(b) that each zone comprises two consecutive voltage levels. To avoid the voltage transitions across the parasitic capacitor (C_P), the adjacent voltage levels in any given zone should have an

TABLE IV
NUMBER OF VOLTAGE TRANSITIONS

Z	N_C	N_P
R_1	$11f_{swi}$	0
R_2	2	2
R_3	0	0
R_4	0	0
R_5	$3f_{swi}$	2
R_6	0	0
R_7	0	0
R_8	$11f_{swi}$	2
T	$25f_{swi}$	6

*f_{swi} (in kHz)

identical magnitude of TCMV. The proposed PWM strategy realizes this objective by an appropriate selection of switching sequences, as suggested by Table II. Thus, the proposed PWM is capable of eliminating all switching frequency transitions in each operating zone, which reduces the rms value of the leakage current. In general, in a closed-loop PV system, the output of the MPPT controller determines the modulation index (m_a) for the inverter. Fig. 7, which shows the block diagram for the implementation of the proposed modulation technique, indicates that the modulation index is input to this block diagram to generate the switching pulses for the inverter.

C. Comparison With Conventional SPWM Strategy

The number of transitions in TCMV is determined for both the conventional SPWM [4], [23] and the proposed PWM technique. When the conventional SPWM technique is used, the switching sequence for a particular voltage level is chosen irrespective of the zone of operation. This leads to affect the zones R_1, R_5, and R_8 with high-frequency (switching frequency) voltage transitions in TCMV. The voltage transitions in each switching period in zones R_1, R_5, and R_8 for the proposed PWM technique and the conventional SPWM technique are shown in Fig. 8. With the conventional PWM, in zone R_1,, the output voltage switches between 3 V_{PV} and 2 V_{PV}, and simultaneously, the TCMV switches between 2 V_{PV} and V_{PV}. Hence, with the conventional SPWM technique, during zone R_1, TCMV displays two transitions in each switching period. Furthermore, to find out the total number of voltage transitions in a fundamental cycle, the time period of each zone and its relationship with the switching frequency of the inverter (f_{swi}) are determined. The number of transitions in zone R_1 would then correspond to 11 times that of the value of switching frequency ($11f_{swi}$, where f_{swi} is the inverter switching frequency in kHz). In contrast, no transitions are encountered when the proposed PWM technique is used, as shown in Table IV. A similar number of transitions are also encountered in zones R_5 and R_8, where the TCMV switches between V_{PV} and 0, and 0 and $-V_{PV}$, respectively. Table IV presents the total number of transitions in the TCMV over a fundamental cycle by summing up all the transitions in each zone in Table IV), and the symbols **Z**, $\mathbf{N_C}$, $\mathbf{N_P}$, and **T**, respectively, denote the zone, the number of voltage transitions in TCMV with the conventional SPWM, the number of voltage transitions in TCMV with the proposed PWM, and the total number of voltage transitions in TCMV during a fundamental cycle.

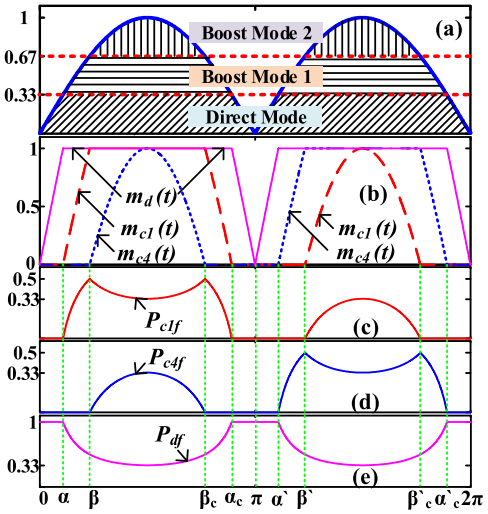

Fig. 9. (a) Direct and boost modes of operation. (b) Modulating function for direct mode and boost modes. Power utilization factors: (c) P_{C1f}, (d) P_{C2f}, and (e) P_{df}.

It is evident from Table IV, that the proposed PWM technique induces only six transitions in each fundamental cycle in the TCMV, whereas the conventional SPWM induces a total of $25f_{swi}$ transitions in each fundamental cycle. Thus, for the conventional SPWM the leakage current increases with the value of switching frequency (f_{swi}) of the inverter. In contrast, with the proposed PWM technique, the number of transitions per cycle is reduced. Also, it becomes independent of the switching frequency of the inverter.

D. Evaluation of Power Utilization Factors

From Section II, it is obvious that the proposed configuration extracts the PV power in both single-stage (direct mode) and double-stage (boost modes 1 and 2) operating modes. The time periods of these modes are presented in Fig. 9(a). In Fig. 9(a), the variables α and β are defined as: $\alpha = \sin^{-1}(1/3)$ and $\beta = \sin^{-1}(2/3)$. The rest of the time periods can be determined from the waveform symmetry. In the direct mode, the PV power is directly routed to the load through the inverter. In contrast, in boost modes 1 and 2, the power is processed through the combination of the interleaved buck–boost converters before multilevel inversion. To determine the ratings of the components and assess the power loss associated with the power conversion stage, the power utilization factors need to be determined. In this context, the power transferred in the direct mode (P_d) and boost modes (P_{C1}, P_{C4}) is derived using the following equations:

$$P_{C1} = m_{C1} V_{C1} i_g \tag{14}$$

$$P_{C4} = m_{C4} V_{C4} i_g \tag{15}$$

$$P_d = m_S V_{PV} i_g \tag{16}$$

$$i_g = I_m \sin(\omega t - \varphi) \tag{17}$$

where V_{C1} and V_{C4} are the voltages across the SCs C_1 and C_4. The amplitude of the load current is denoted by the symbol I_m. The functions $m_d(t), m_{C1}(t)$, and $m_{C4}(t)$, respectively, represent the modulating function referred to the PV source in the direct mode and the two boost modes [Fig. 9(b)]. These

modulating functions can also be defined from the following equations:

$$m_S(t) = 6|r|z_1 + (z_2 + z_3 + z_4) \tag{18}$$

$$m_{C1}(t) = ((6|r| - 1)z_2 + z_3 + z_4)z_s + (6|r| - 2)(z_3 + z_4)(1 - z_s) \tag{19}$$

$$m_{C4}(t) = (6|r| - 2)(z_3 + z_4)z_s + ((6|r| - 1)z_2 + z_3 + z_4)z_s. \tag{20}$$

The total power processed by the inverter can now be written as follows:

$$P_T = P_{C1} + P_{C4} + P_S. \tag{21}$$

The utilization factor for the direct mode (P_{df}), as well as each of the boost modes (P_{C1f}, P_{C4f}), can be determined by the ratio of each power component to the total power (P_T). The waveforms of the power utilization factors corresponding to the boost modes (P_{C1f} and P_{C4f}) and direct mode (P_{Sf}) are shown in Fig. 9(c)–(e), respectively. It can be observed that both the SCs attain a maximum power utilization factor of 0.5. Thus, it is evident that each section of the interleaved buck–boost converter processes a maximum of 50% of the load requirement. This key observation paves the way to the selection of the components pertaining to the boosting stage of the proposed converter.

Furthermore, to determine the amount of energy processed in each mode, namely: 1) direct mode and 2) boost modes in a given power cycle, (14)–(16) are integrated over time. The total energy processed by the inverter can be written as follows (17):

$$E_T = \int_0^{2\pi} (P_{C1} + P_{C4} + P_S)\mathrm{d}(\omega t). \tag{22}$$

The energy processed in the direct mode (E_d) and boost modes (E_{C1} and E_{C4}) can also be derived from the following equations:

$$E_S = V_{PV}\left[4\int_0^{\alpha} m_S i_g \mathrm{d}(\omega t) + 2\int_{\alpha}^{\pi-\alpha} i_g d(\omega t)\right] \tag{23}$$

$$E_{C1} = V_{PV}\left[2\int_{\alpha}^{\beta} m_{C1} i_g \mathrm{d}(\omega t) + \int_{\beta}^{\pi-\beta} i_g d(\omega t) + \int_{\beta'}^{\pi-\beta'} m_{C1} i_g \mathrm{d}(\omega t)\right] \tag{24}$$

$$E_{C4} = V_{PV}\left[\int_{\beta}^{\pi-\beta} m_{C4} i_g \mathrm{d}(\omega t) + 2\int_{\alpha'}^{\beta'} m_{C4} i_g d(\omega t) + \int_{\beta'}^{\pi-\beta'} i_g d(\omega t)\right]. \tag{25}$$

The average energy utilization factors over a fundamental cycle are obtained by evaluating the integrals, which appear in (22)–(25)

$$E_{Sf} = \frac{E_S}{E_T} \times 100\% = 41.6\% \tag{26}$$

$$E_{C1f} = \frac{E_{C1}}{E_T} \times 100\% = 29.2\% \tag{27}$$

$$E_{C4f} = \frac{E_{C4}}{E_T} \times 100\% = 29.2\%. \tag{28}$$

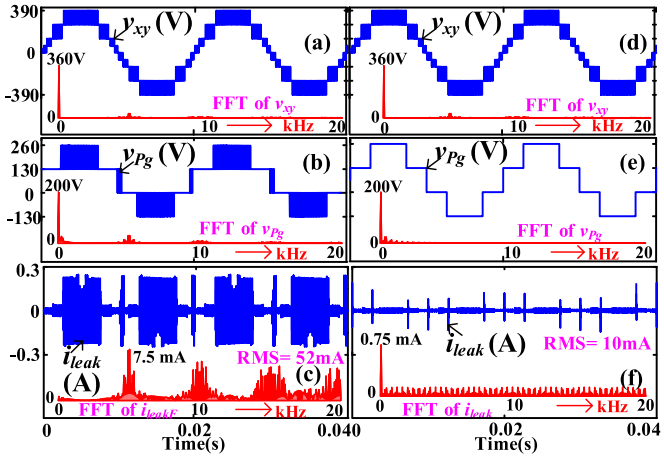

Fig. 10. Simulated results. (a) v_{xy}, (b) v_{Pg}, and (c) i_{leak} for conventional SPWM. (d) v_{xy}, (e) v_{Pg}, and (f) i_{leak} for the proposed PWM technique at $m_a = 0.9$.

TABLE V
CIRCUIT PARAMETERS FOR SIMULATION

Parameter	Values	Parameter	Values
V_{PV}	130 V	C_1, C_4	470 uF
$V_{DC\text{-}link}$	400 V	C_2, C_3	1 mF
P_{rated}	1.5 kW	L_1,L_2	0.5 mH
f_m	50 Hz	L_f, L_g	2.5 mH
f_{swi}	5kHz	C_f	0.1 uF
f_{swb}	10kHz	R_p,C_p	10 Ω,100nF

It is evident from the above-derived numerical values that the proposed modulation technique enables the proposed configuration to transfer an amount of 42% of the total energy in the direct mode. The rest of the 58% of the total energy is transferred through the interleaved converter. Furthermore, the foregoing analysis reveals that each interleaving section of the converter needs to handle only 29% of the total load requirement. In contrast, the conventional boosting methods demand that the total (i.e., 100%) load power be processed through the dc–dc conversion stage. Thus, the proposed power circuit configuration reduces the effective power loss incurred in the interleaved converter, while boosting the input PV voltage. Moreover, as per the obtained numerical values in (26)–(28), it implies that the average energies transferred in each fundamental cycle for both the SCs (C_1 and C_4) are the same. Furthermore, the design of these SCs can be carried out using the charge balance equation and the constraint of the allowed voltage ripple as described in [24] and [25]. The charge balance equation for these SCs is derived using the boosted energy from the interleaved buck–boost converter and the required energy by the load.

V. SIMULATION VALIDATION

The working principle and the performance of the proposed inverter configuration have been validated by simulation studies using the MATLAB–SIMULINK platform. The parameters used in the simulation of the proposed inverter and the associated modulation strategy are presented in Table V. The TCMV and the leakage current are assessed with the aid of a circuit branch consisting of parasitic elements, namely, a resistance (R_p) and a capacitance (C_p). This branch is placed across the

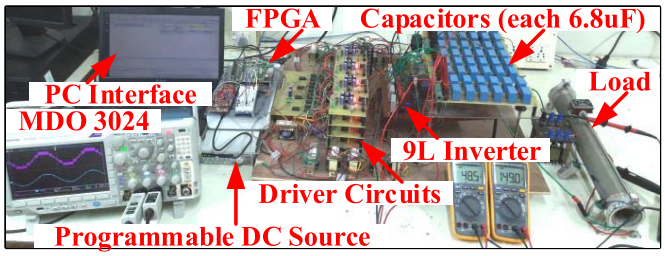

Fig. 11. Laboratory prototype for the proposed 9L-T-HBI configuration.

TABLE VI
CIRCUIT PARAMETERS FOR EXPERIMENTAL PROTOTYPE

Parameter	Values	Parameter	Values
V_{PV}	60 V	C_1, C_4	24 × 6.8 uF =160uF
$V_{DC\text{-}link}$	180 V	C_2, C_3	1 mF
VA_{rated}	500VA	L_1,L_2	0.5 mH
f_m	50 Hz	L_f	2 mH
f_{swi}	5kHz	C_f	0.1 uF
f_{swb}	10kHz	R_p,C_p	10 Ω,100nF

positive terminal of the PV source and the load neutral as shown in Fig. 2. According to [26] and [27], the value of parasitic capacitance ranges between 60–160 nF depending on the type of the PV panel and atmosphere conditions.

To emphasize the benefits of the proposed PWM technique, these simulation results are compared with those obtained with the conventional SPWM for the proposed 9L-T-HBI with identical parameters. The output voltage waveforms display nine distinct voltage levels, namely, ±390 V, ±260 V, ±130 V, ±65 V, and 0. The output voltage (v_{xy}) spectra obtained with these two modulation techniques [Fig. 10(a) and (d)] are identical. Significant harmonic components occur at frequencies corresponding to the integral multiples of the inverter switching frequency (f_{swi}), facilitating the criterion to design the filter inductor [24]. It is important to note that when the conventional SPWM is used, high-frequency voltage transitions appear in TCMV. In comparison, the proposed PWM strategy succeeds in eliminating the high-frequency transitions, as is evident from Fig. 10(b) and (e). TCMV obtained with the proposed PWM strategy contains only six transitions, wherein the magnitude of each transition is one-third of the total dc-link voltage (i.e., 130 V). Consequently, the leakage current would also display only six spikes in its waveform [Fig. 10(f)]. The obtained rms value of the leakage current is only 10 mA, which is well below the limit of 30 mA, stipulated by VDE0126-1-1 [26]. In contrast, the rms value of the leakage current caused by the application of the SPWM scheme is 52 mA, which is so large as to violate the VDE-0126-1-1 standard.

VI. EXPERIMENTAL VALIDATION

To provide experimental validation for the proposed 9L-T-HBI configuration and the associated control algorithm, a scaled-down hardware prototype has been developed (Fig. 11). The circuit parameters and the operating conditions are presented in Table VI. The following power semiconductor switching devices are used for the fabrication of the proposed power circuit configuration: IRF 840 (S_1, S_2, . . . , S_9), IRF 460 (S_{UP}, S_{LP}), and MBR1520 (D_1, D_2). The prototype is fed by a programmable dc source, which emulates the characteristic of a PV source [6], [12].

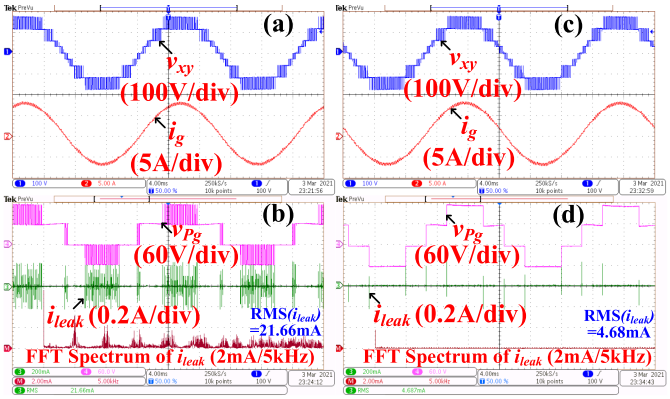

Fig. 12. Experimental results. (a) v_{xy}, i_g and (b) v_{Pg}, i_{leak} for conventional SPWM. (c) v_{xy}, i_g and (d) v_{Pg}, i_{leak} for the proposed PWM technique.

Each SC consists of a bank of 24 capacitors (metalized polyester type, each 6.8 μF). The proposed modulation strategy is implemented with a Spartan 6 field-programmable gate array (FPGA) platform. The equivalent parasitic impedance of the PV panel is connected across the load neutral terminal and the source positive terminal, which consists of resistance (R_{p}) with a series capacitor (C_{p}). The dynamic performance of the prototype at unity power factor (UPF) is assessed by connecting a resistive load, which is switched between required values of resistance [28]. Similarly, the reactive power capability is demonstrated with an equivalent *RL* load corresponding to a PF of 0.8 (lag) as suggested in [29]. Furthermore, the ratings of the passive components such as the dc-link capacitors and filter inductors are calculated using the procedures laid out in [30].

To demonstrate the advantage obtained with the proposed PWM strategy compared with the conventional SPWM technique, both these PWMs are applied to the proposed power converter. Fig. 12(a) and (c) shows that the output voltage waveforms with either of these modulation techniques are identical. Thus, the proposed converter and the proposed modulation technique retain all the advantages obtained with the conventional MLIs such as reduced $\mathrm{d}v/\mathrm{d}t$ stresses across the switches and reduction in the size of filters. Also, the THDs of the load current for both the modulation techniques are the same (1.05%). However, the TCMV waveform shows high-frequency voltage transitions (corresponding to the switching frequency) when the conventional SPWM is used. In contrast, with the proposed modulation strategy, the TCMV oscillates at the fundamental frequency. It is well-known that the presence of the voltage transitions in the TCMV waveform causes the leakage current as $i_{\text{leak}} = C_{\text{pv}}\ (\mathrm{d}v_{\text{Pg}}/\mathrm{d}t)$. It can be observed that the TCMV waveforms have six transitions in a given fundamental cycle. With identical values of the switching frequency (5 kHz), input voltage (60 V), and other circuit parameters, the proposed PWM results in a much lower rms value of the leakage current (4.68 mA, rms) compared with the one obtained with the conventional SPWM (21.66 mA, rms). Thus, the rms value of the leakage current obtained with the proposed PWM is about 4.5 times lesser than the one obtained with the conventional SPWM technique. It is also observed from Fig. 12(b) that the harmonic spectrum of leakage current obtained with the conventional SPWM contains significant peaks at f_{swi} and its higher order multiples. Thus, it is

evident that the size and order of the common-mode choke and electromagnetic interference (EMI) filters are reduced with the proposed configuration. These experimental results are in agreement with the simulation results, validating the operation and the working principle of the proposed power circuit configuration and the associated control algorithm.

Another set of experimental results have also been presented, corresponding to the modulation index (m_a) of 0.9, to validate the voltage-boosting capability for the proposed power converter. The nine distinct voltage levels output by the proposed 9L-T-HBI, namely, ±180 V, ±120 V, ±60 V, ±30 V, and 0, can easily be distinguished in Fig. 13(a). The SCs are charged to the input voltage (i.e., 60 V) as shown in Fig. 13(b). It is observed that the boosting circuit delivers power only when the inverter outputs more than ±60 V. This helps in balancing the voltages and reducing the power loss. Furthermore, as an interleaved PWM is used for the buck–boost stage, the inductor currents (i_{L1}, i_{L2}) appear to be antiphased with reference to each other as shown in the zoomed-in view of Fig. 13(b).

Furthermore, the voltage regulation of the SCs with load variation is demonstrated. Fig. 14(a) presents the transient response of the load current when the peak load current reference is suddenly varied from 4 to 7 A. This results in shifting the operating point on the PV characteristic, and eventually, the PV voltage (v_{PV}) undergoes a small change (∼2 V). It is observed that following the load disturbance, each of these two SC voltages is individually regulated to the PV voltage (v_{PV}) (i.e., around 60 V) and the voltage controller restores the voltage across the two SCs (i.e., v_{C1} and v_{C4}), in less than 20 ms. Also, the inverter output voltage (v_{xy}) does not suffer any distortion during this transient condition as demonstrated in the experimental result shown in Fig. 14(b). To further test the dynamic response of the proposed power converter, the load on the converter is suddenly changed from UPF to a lagging load with a PF of 0.8. The experimental result, presented in Fig. 14(c), reveals that the controller handles even this condition well, as no apparent distortion in the output waveform is observed. Furthermore, this experiment shows that the voltages across the SCs are regulated for this condition as well.

Fig. 15 shows the dynamic performance of the proposed 9L-T-HBI when the reference of the peak load current is altered from 4 to 8 A. The waveforms of the inverter output voltage (v_{xy}), the load current (i_g), the voltage across the load (v_{load}), TCMV (v_{Pg}), and the leakage current (i_{leak}) are shown (Fig. 15). It is seen from Fig. 15(a) that despite the load disturbance, the waveform of the inverter output voltage remains identical. This demonstrates the regulating capability of the controller against disturbances. From Fig. 15(b), it is evident that both the TCMV and the leakage current remain unaltered. Thus, it is demonstrated that the proposed configuration is capable of reducing the leakage current, independent of the magnitude and the nature of the load current.

Furthermore, to verify the reactive power sourcing capability of the proposed 9L-T-HBI converter, an impedance corresponding to PF = 0.8 is connected across the output terminals

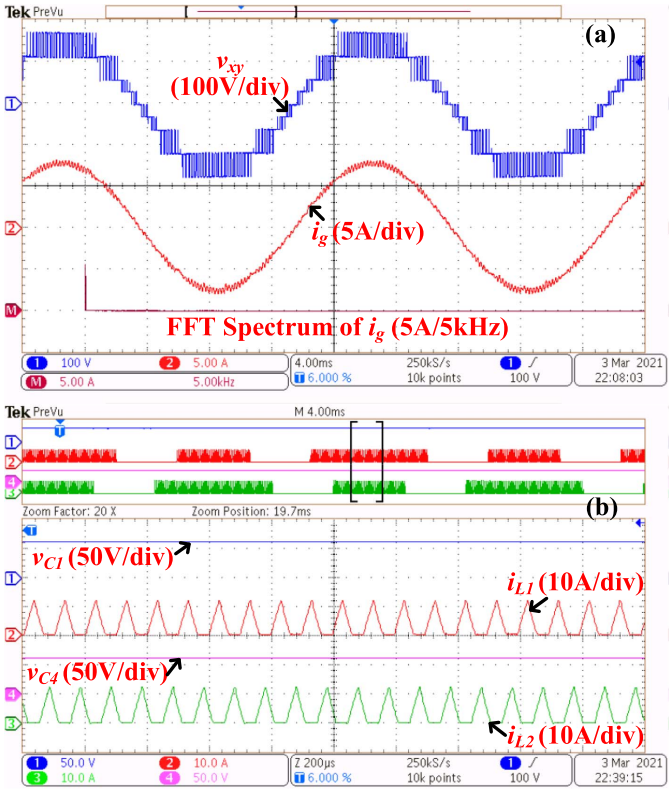

Fig. 13. Experimental results. (a) v_{xy}, i_g and (b) v_{C1}, v_{C4}, i_{L1}, i_{L2} for the proposed PWM technique at $m_a = 0.9$.

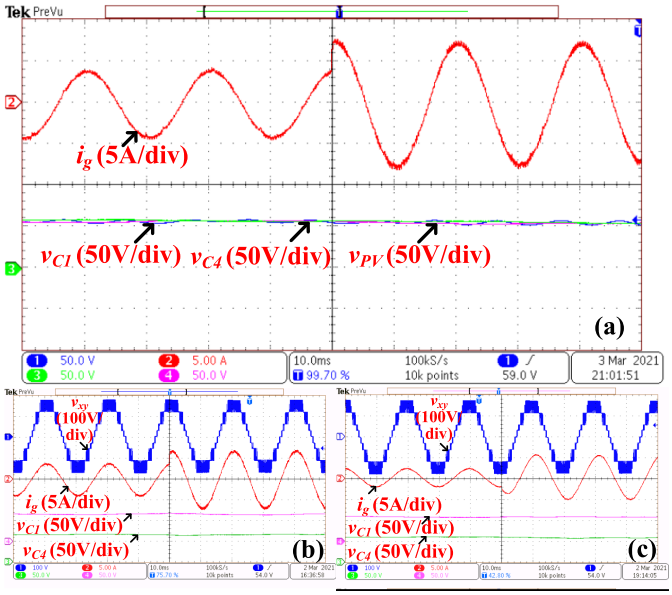

Fig. 14. Experimental results for the dynamic response of (a) voltages across the SCs (v_{C1}, v_{C4}) at step change of load current (i_g), (b) v_{xy}, i_g, v_{C1}, v_{C4} captured for load dynamics with UPF, and (c) v_{xy}, i_g, v_{C1}, v_{C4} captured for load dynamics with PF = 0.8.

of the inverter. The effect of the lagging load manifests as a significant phase difference between the inverter output voltage and load current (Fig. 16). It can be observed the performance of the TCMV and the leakage current is unaltered compared with the results obtained for unity PF load. Therefore, it is evident that the proposed inverter configuration is capable of delivering active and reactive power without sacrificing either

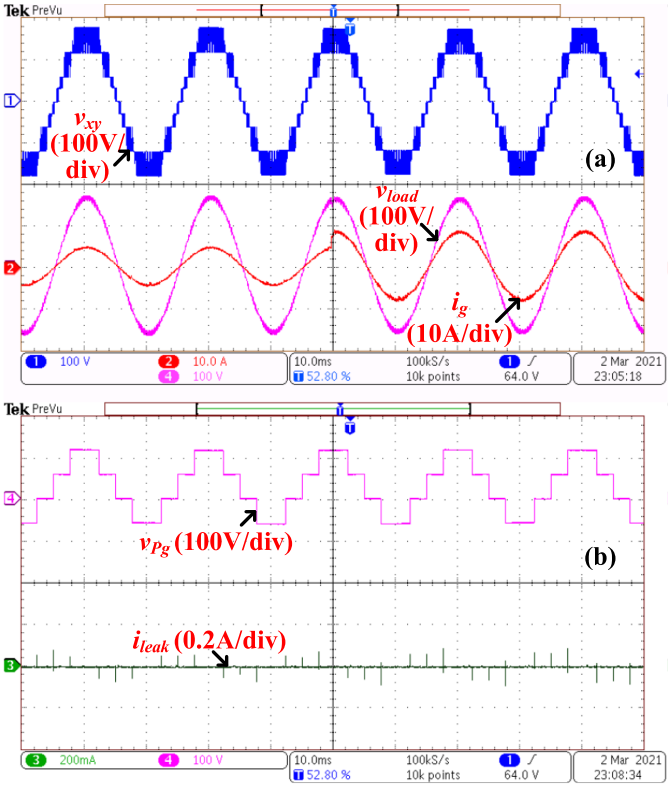

Fig. 15. Experimental results for the dynamic load change of the proposed configuration with the proposed modulation technique. (a) v_{xy}, v_{load}, i_g and (b) v_{Pg}, i_{leak} at UPF.

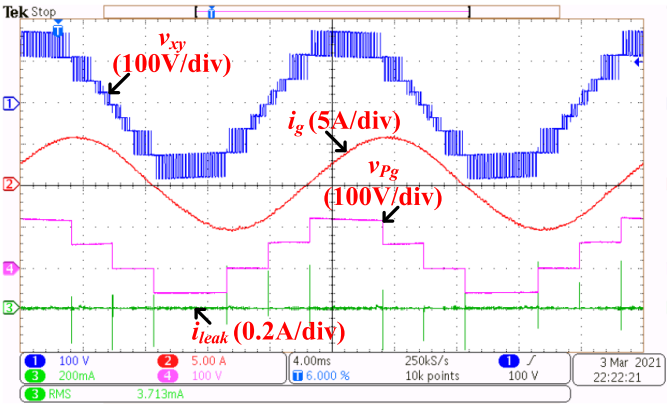

Fig. 16. Experimental results: v_{xy}, i_{g}, v_{Pg}, i_{leak} with lagging load (PF = 0.8).

the quality of output waveform or the reduction in the leakage current.

The experimental efficiency of the proposed configuration is measured with a precision digital power meter (Yokogawa WT332E). The measurement of power is carried out using two isolated channels of this meter. These two channels, respectively, provide data regarding the voltage and power at the input and the output of the proposed power converter [Fig. 17(b)]. Fig. 17(a) shows the voltage (v_{xy}), current (i_{g}), TCMV (v_{Pg}), and leakage current (i_{leak}) at the output of the inverter. To measure the power, THD, and the PF at the output of the inverter, a single-phase power analyzer (UNI-T UT283A) is also connected at the output of the inverter. Fig. 17(b) shows the measurements of the PV voltage (v_{PV}), the rms value of inverter output voltage (v_{XY}), the input

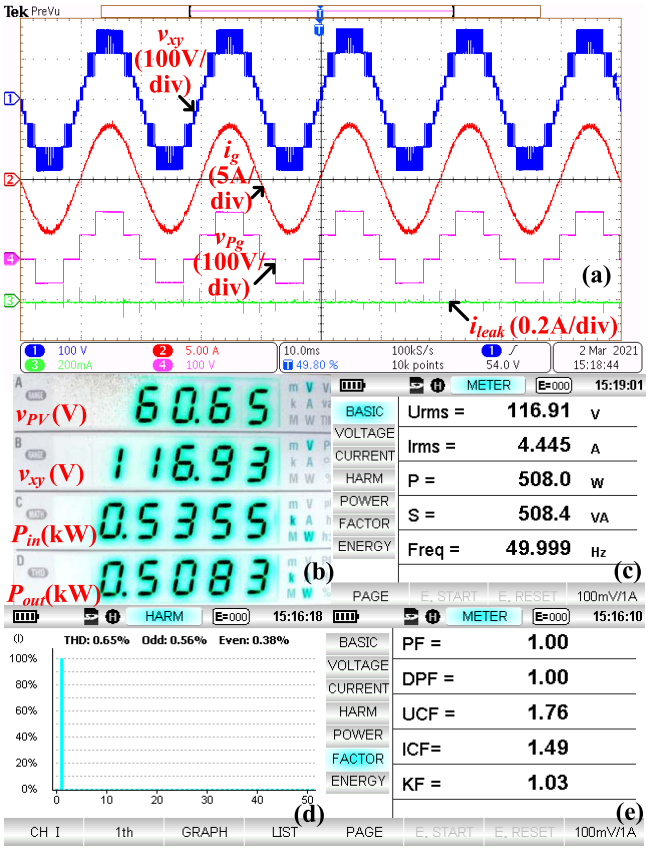

Fig. 17. Experimental results. (a) v_{xy}, i_{g}, v_{Pg}, i_{leak}. (b) Measurements of input PV voltage (v_{PV}), rms of inverter output voltage (v_{XY}), input power to the inverter (P_{in}), and output ac power (P_{out}) from the digital power meter. (c) RMS of the inverter voltage, active power (P), and apparent power (S). (d) THD and harmonic spectrum of the load current at $P_{\text{out}} = 508$ W. (e) PF of the load.

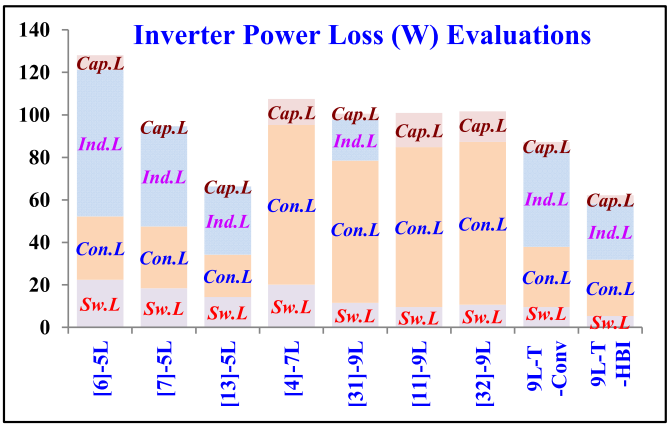

Fig. 18. Comparison of power losses [(1) switching power loss (Sw.L), (2) conduction loss (Con.L) of all semiconductor devices, (3) inductor ohmic loss (Ind.L), and (4) capacitor equivalent series resistance (ESR) loss (Cap.L)] of the inverter configurations.

power to the inverter (P_{in}), and the output ac power (P_{out}). From these measured values, the efficiency of the inverter is obtained as 94.90% at the given operating condition (the output power, $P_{\text{out}} = 508$ W). It may also be noted that the obtained THD of the load current is also well within the limit of IEEE-519-2014 standards [Fig. 17(d)]. It is envisaged that the efficiency can be further improved at higher power ratings

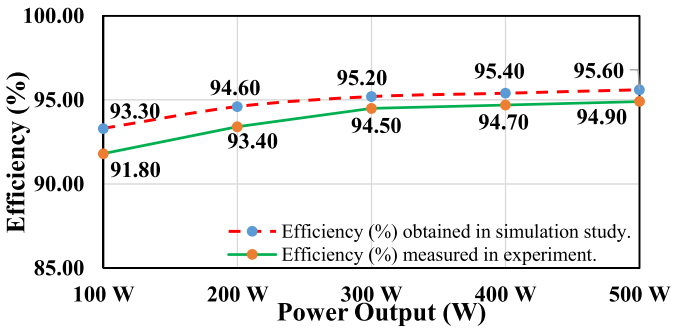

Fig. 19. Comparative efficiency plot of the proposed 9L-T-HBI configuration ranging from 100 to 500 W obtained in the simulation study and measured in the experiment.

TABLE VII
COMPARISON OF EXISTING TOPOLOGIES

	[6] -5L	[7] -5L	[13] -5L	[4] -7L	[31] -9L	[11] -9L	[32] -9L	9L-T- -HBI
A	7	8+4	9+1	10	10	19+3	8+3	12+2
B	2	4	2	4	3	3	3	4
C	0	2	1	0	1CI#	0	0	2
D (V)	400	200	200	267	800	133	100	133
E	5.5	5	7.5	7.3	8	4.75	5.75	8
F	-	-	Soft	Hard	Soft	Hard	Hard	Soft
G	1-2I_m	1-2I_m	2-3I_m	5-6I_m	1-2I_m	5-6I_m	5-6I_m	2-3I_m
H	f_o	f_o	f_o	0	0	f_{sw}	f_{sw}	f_o
I (mA)	2.8	410	110	2.2	3.5	73	820	10
J	small	high	high	small	small	high	high	small
K	No	No	Yes	Yes	Yes	Yes	Yes	Yes

A: (No of switches + No of diodes); **B:** No of capacitors; **C:** No of inductors; **D (in volt):** Required input voltage for 230V_{rms} application; **E:** Total standing voltage in per unit. (with respect to the peak value of the output voltage); **F:** hard-charging or soft-charging of the SCs; **G:** Peak current stress of the semiconductor devices in voltage boosting path, **H:** TCMV frequency, **I (in mA):** RMS of leakage current, **J:** Requirement of additional common mode filter, **K:** Capability of reactive power exchange.
where, f_o is grid-frequency, f_{sw} is switching-frequency, I_m peak value of the grid-current, **CI#** is coupled inductor.

by improving the design of the magnetic components and the use of advanced power semiconductor switching devices.

VII. COMPARISON WITH EXISTING TRANSFORMERLESS INVERTER TOPOLOGIES

The performances of the proposed 9L-T-HBI configuration vis-à-vis the recently reported topologies are compared to demonstrate its benefits and features. Table VII presents various parameters for which the performances are compared. The literature available on 9L transformerless inverter topologies, which requires one PV source and simultaneously achieves reactive power sourcing capability and mitigation of leakage current, is scanty. In view of this, single PV-source-based 7L and 5L inverter topologies are also considered for comparison. The topologies presented in [6] and [7] use an additional voltage-boosting stage to achieve the required voltage-boosting capability. Hence, these topologies incur higher power losses (Fig. 18) in the boosting inductors, as the boosting stage is constrained to transfer the entire power from the PV source to the load. The topology presented in [13] addresses this problem with the introduction of a novel boosting technique, which partially reduces the power losses in the boosting inductors. However, the PWM technique used in this work [13] causes a high (dv/dt) across the inverter switches. Though the topology described in [31] synthesizes nine levels and displays a better leakage current reduction, it lacks boosting capability and requires a higher input voltage. Furthermore, nine-level topologies are proposed in [11] and [32], which achieve voltage-boosting and a multilevel operation by the use of SCs. However, in these converters, the switching devices are subject to higher current stress due to the hard-charging of the SCs, calling for a conservative selection of the switching devices.

This would further affect the energy density of the converter. In contrast, the proposed topology alleviates the current stress on the switching devices, as the SCs are charged softly through the inductor while achieving a boost factor of 3.

Using the theoretical power loss equations [1], the efficiency of the proposed power converter can be assessed. The recent trend in this direction is to use a piecewise linear electrical circuit simulation (PLECS)-based simulation to evaluate various components of the power losses [30], [31]. Thus, a comparative simulation study of the proposed power converter is implemented in PLECS simulation software using the thermal model of the semiconductor devices IKW30N60T (Fig. 18). To facilitate a fair comparison, all configurations are analyzed with an input voltage of 130 V and an output power of 1.5 kW. However, for those topologies, which do not possess the voltage-boosting capability, a conventional voltage-boosting stage is incorporated as suggested in [2] and [29]. Furthermore, the power losses incurred with the conventional voltage-boosting technique (i.e., conventional boost converter) with the nine-level T-type inverter are also evaluated (9L-T-Conv) and presented in Fig. 18. The power loss incurred for the proposed configuration is indicated as 9L-T-HBI in Fig. 18.

Fig. 19 presents the simulated and the experimentally obtained efficiencies of the proposed 9L-T-HBI configuration. The efficiency is measured at power output ranging from 100 to 500 W in steps of 100 W. It may be noted that the experimentally obtained efficiencies are in close agreement with their simulated counterparts. Furthermore, at the rated condition, the scaled-down laboratory prototype results in an efficiency of 95% (approx.), which is close to the efficiency obtained through the simulation study.

VIII. CONCLUSION

In this article, a single PV-source-based 9L-T-HBI along with its PWM strategy is proposed. The proposed power converter and its associated PWM scheme achieve the dual objectives of voltage-boosting and leakage current reduction. Compared with the conventional voltage-boosting methodologies, the integrated boosting technique of the proposed system achieves a boosting factor of 3 and a reduced power loss. With the proposed power converter, a smooth transition between the single-stage and the double-stage operation is achieved while maintaining symmetric utilization of the SCs with reduced voltage ripple. The principal advantage of the proposed inverter configuration is that it achieves the direct transfer of about 42% of energy from the PV source to the load in a given fundamental cycle. The simulation and

experimental results reveal that the THD of the load current is less than 2%, which is well within the IEEE standard 519-2014. Besides that, as the proposed PWM technique eliminates all high-frequency voltage transitions from the TCMV, the rms value of the leakage current is also reduced compared with the conventional SPWM modulation technique. The rms value of the leakage current for the proposed PWM scheme is found to be well within the stipulated safety limit of the VDE-0126-1-1 standard. Owing to these features, it is envisaged that the proposed 9L-T-HBI configuration could be used for both residential and grid-connected PV applications.

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