Electrical Engineering (2022) 104:463–472
https://doi.org/10.1007/s00202-021-01312-7

ORIGINAL PAPER

Supercapacitor-based transient power supply for DC microgrid applications

C. R. Arunkumar[1] · Udaya Bhasker Manthati[1] · Srinivas Punna[1]

Received: 2 December 2019 / Accepted: 7 May 2021 / Published online: 24 May 2021

Abstract
Energy storage systems have become inevitable components of a DC microgrid in terms of pacifying voltage/current fluctuations that are unavoidable due to the unpredictable, intermittent nature of renewable energy system and load. These fluctuations normally result in power quality issues in addition to stability issues. The transient pressure on the DC bus increases with an increase in distance between the source and load. Further, it affects the other connected loads in a single-bus system. Hence, this paper proposes a multi-bus dc microgrid structure integrated with a supercapacitor transient power supply to deal with the fluctuating DC loads. In the proposed model, the steady-state power requirement of the load is expected to be met by the DC bus, while the dedicated supercapacitor bank would compensate for the transient power requirements. The proposed model has been developed and simulated in MATLAB/Simulink. The simulation results shows that the proposed scheme is capable to reduce the transient pressure on the DC bus and improve the power quality of the DC microgrid. Also, hardware experiments have been conducted to validate the accuracy and feasibility of the proposed system.

Keywords Supercapacitor · DC microgrid · PI controller · Fluctuating loads · Energy storage system · Bidirectional DC–DC converter

1 Introduction

In recent years, the technological advancement in renewable energy integration and energy efficient electrical loads has led to significant changes in the modern power system [1]. Due to easy adaptability of renewable energy system (RES) and its less challenging control strategy, there has been a remarkable evolution in the field of DC microgrids compared to its AC counterpart [2,3]. The conventional DC microgrid follows single-bus structure, which allows easy implementation and analysis. The multiple DC bus system is used to meet the specific load demand and regulation.

The proposed multi-bus structure of a DC microgrid designed for fluctuating loads with power electronic interfaces is shown in Fig. 1 [4,5]. The RES and energy storage systems (ESS) are placed together to work in sync to effectively control the power flow in the system. The fluctuating load represents high duty pulsed loads and other frequent variable power loads. These loads demand high transient current from DC main bus [6] which in turn increases stress on the sources as well as affects the directly connected loads.

Batteries are widely used in DC microgrids for maintaining power balance under steady-state conditions, but the use of batteries for high-power fluctuating loads could lead to deterioration of battery life [7,8]. This drawback could easily and effectively be resolved by using batteries concurrently with reliable fast acting devices such as supercapacitor (SC) to handle transient power requirements. Such a system is called hybrid energy storage system (HESS) [9–11]. The HESS-based pulsed load system would share the power based on source availability. The steady-state power is supplied by the battery and the DC bus, while transient power flow is regulated by the supercapacitor unit [12–14]. Though a highly efficient alternative, the combined use of battery and supercapacitor would add to the size and cost of the system to a great extent.

✉ C. R. Arunkumar
acr_research@student.nitw.ac.in

Udaya Bhasker Manthati
ub@nitw.ac.in

Srinivas Punna
srinu240@student.nitw.ac.in

[1] Electrical Engineering Department, National Institute of Technology Warangal, Warangal, Telangana 506004, India

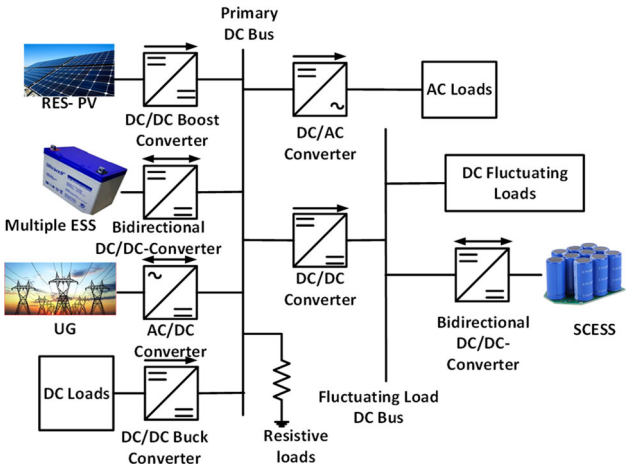

Fig. 1 Conventional DC microgrid showing fluctuating DC loads and SC transient power supply

This paper suggests a fluctuating load bus incorporated with SC-based transient power supply to effectively resolve the aforementioned problems. The high power density and moderate energy density of SC make it more convenient for transient applications [15–17]. The SC-based ESS (SCESS) is capable of supporting loads under intermittent transients so that the source DC bus would handle the steady-state power demand [18,19]. Commonly, SCESS in parallel with load is used to mitigate the high fluctuation in DC power [20–22]. In [21], Mustafa Farhadi et. al. designed an SC-based system for pulsed loads, in which the SC is connected in parallel with the pulsed load through a switch to improve the SC utilization. A model predictive control-based SCESS system for DC microgrid application is introduced in [22]. However, in all the above cases, SCESS is connected in parallel with the pulsed load. This necessitates the usage of high-rated supercapacitor units, which in turn increases the cost and size of the unit. Furthermore, the supercapacitor must be charged to the reference voltage for maintaining load voltage. To overcome these issues, this paper proposes the use of a power electronic interfaced SCESS. In this setup, a lower rated supercapacitor is sufficient to regulate the higher DC voltages and to supply transient power at the time of disturbance.

A droop controlled DC microgrid with SCESS power supply for fluctuating loads is presented in [23]. This method would assist the system during transient disturbances, although all the other sources and loads are exposed to transient power during that period. Further, the droop control strategy increases the system's complexity.

From the above discussion, it can be summarized that direct connection of supercapacitor improves the transient response of the system, but it demands high rated and charged SCESS for smooth functioning. Further, the fluctuations could affect the direct connected loads in a single-bus DC microgrid system. Hence, this paper proposes a DC microgrid structure with a dedicated fluctuating load bus integrated with independent transient power supply. The contributions of this paper are summarized as follows:

1. A multi-bus DC microgrid structure for fluctuating loads is presented in which a supercapacitor is integrated to the dedicated DC bus such that the primary bus is unaffected by the high power load transients.
2. A rate-limiter low-pass filter-based controller is designed and implemented to control the SCESS operation. This allows the supercapacitor to charge/discharge during transients and reduce the SCESS current to zero during steady-state operation.
3. The operation of supercapacitor depends on the selection of controller parameters. Hence, a detailed controller design and parameter selection for the system is proposed. The simulated results were validated by hardware testing and proved the accuracy and feasibility of the proposed system in reducing the stress on the DC bus during transient disturbances.
4. The available literature focuses mainly on power electronic converter-based approach on a single bus system, whereas this paper incorporates a multi-bus system.

Remaining of the paper is organized as follows: The system configuration and design of the proposed system are discussed in Sect. 2. The LPF-based controller design is presented in Sect. 3. The simulation and hardware results are discussed in Sect. 4. Section 5 verifies the proposed system, and Sect. 6 presents the conclusion.

2 System configuration and design

Figure 2 depicts the DC microgrid with a dedicated DC bus for fluctuating loads. The SC bank connects to the DC bus through a bidirectional DC–DC converter. A variety of loads are connected to the DC bus at different intervals to imitate load fluctuations.

2.1 Supercapacitor energy storage system (SCESS)

Out of the various SC models available, the dynamic model displayed in Fig. 3 [15] is adopted for high-frequency operations. The frequency dependency of C_{dynamic} allows SC to charge and discharge during the transients. The R_{dynamic} reduces the SC current close to zero at low frequencies.

The maximum energy of SCESS is given by

$$E_{\text{sc,max}} = \frac{1}{2} C_{\text{sc}} V_{\text{sc,max}}^2 \tag{1}$$

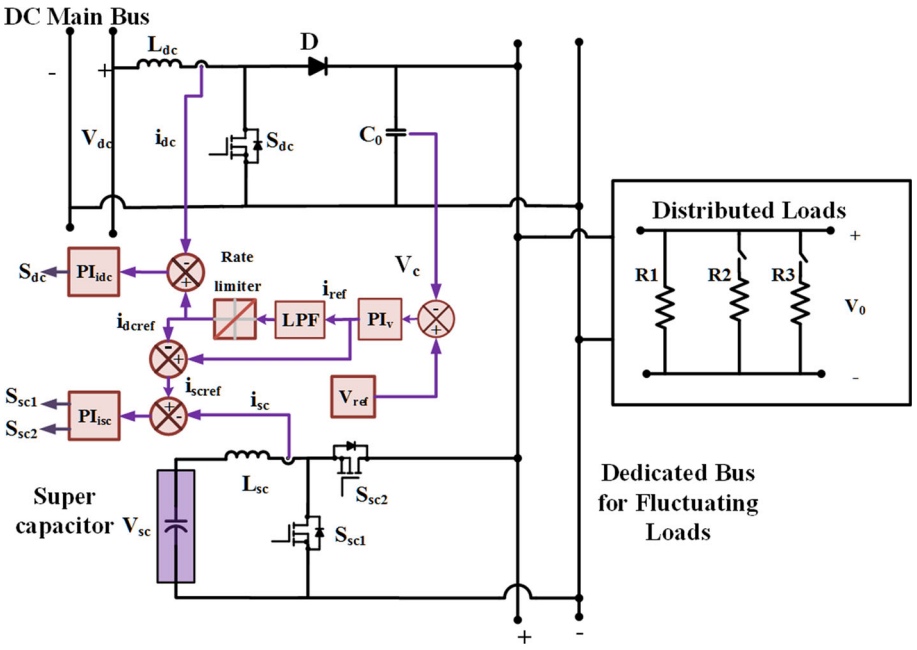

Fig. 2 Proposed SC-based transient power supply system for fluctuating DC loads

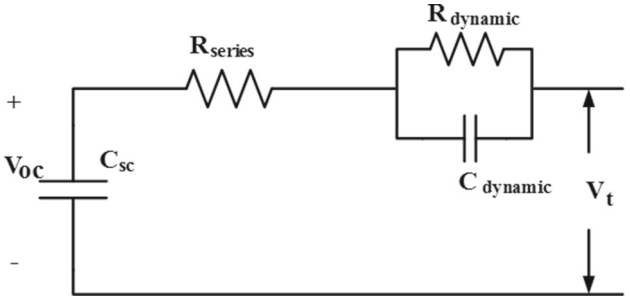

Fig. 3 SC dynamic model [10]

The energy stored by the SCESS at any instant of time ($E_{sc}(t)$) is given by

$$E_{sc}(t) = \frac{1}{2} C_{sc} V_{sc}^2(t) \tag{2}$$

The relation between $E_{sc}(t)$ and SOC of SCESS is given by

$$\text{SOC}_{sc} = \frac{E_{sc}(t)}{E_{sc,max}} \tag{3}$$

The SOC of SC shows variation of energy with time; hence, SOC is expressed in terms of charge as shown in Eq. (4):

$$\text{SOC}_{sc} = \frac{Q_{int} - \int_0^t i(\tau)\mathrm{d}\tau}{Q_T} \tag{4}$$

The fluctuating loads require higher instantaneous power, so using a single energy source for such applications would result in thermal and power quality issues. The integration of SC mitigates all these issues and improves system stability. In this work, fluctuating loads are created by connecting different power loads in parallel through controlled switches [23].

2.2 Design of DC–DC boost converter

The equations used to design standard boost converter can be found in [24]. The design of the boost converter considers continuous conduction mode of operation. Inductor L_{dc} and L_{sc} values are calculated using Eq. (5).

$$L_i = \frac{V_0 D_i}{\Delta i_{is} f_{isw}} \tag{5}$$

where i represents the dc or sc; f_{isw} is the switching frequency of load converter and SC converter; D_i is the corresponding duty ratio. Inductor current ripple Δi_{is} choose to be 5% of load current. The output capacitor (C_i) can be designed using Eq. (6)

$$C_i = \frac{V_0 D_i}{\Delta v_0 R_L f_{isw}} \tag{6}$$

where V_0 is the output voltage and ΔV_0 is the allowable output voltage ripple. For analysis Δv_0 is chosen as 2% of output voltage. The duty ratio is given by

$$D_i = \frac{V_0 - V_i}{V_0} \tag{7}$$

Table 1 The system parameters for simulation (S.No—serial number)

S.No	Parameters	Values
1	DC bus voltage, V_{dc}	48 V
2	Supercapacitor voltage, V_{sc}	56 V, 130 F
3	Load resistance, R_1, R_2 and R_3	18.5 Ω, 30 Ω and 20 Ω in parallel
4	Source inductance, L_{dc}	2.3 mH
5	SC inductance, L_{sc}	2.2 mH
6	Output capacitance, C_0	230 μF
7	Power output, P_{out}	1 kW
8	Switching frequency, f_{sw}	20 kHz
9	Load voltage, V_0	96 V

Table 2 The controller transfer functions based on SSM

(a) Load converter: Current control transfer function

$$\frac{\hat{I_{Ldc}}}{\hat{d}} = \frac{41739(s+1667)}{S^2+833.3s+90.58e04}$$

(b) SC converter: Current control transfer function

$$\frac{\hat{I_{Lsc}}}{\hat{d}} = \frac{43103(s+1818)}{s^2+909.1s+13.65e05}$$

(c) Voltage loop: Voltage control transfer function

$$\frac{\hat{V_0}}{\hat{I_{Lsc}}} = \frac{-3.5109(s-1502)}{s+1818}$$

The converters are designed for handling maximum power of 1 kW with minimum input voltage. The design values for simulation are shown in Table 1.

2.2.1 Small signal modeling of boost converter

The converter control transfer functions are derived using small-signal modeling (SSM). Since both are bidirectional boost converters, the analysis is identical for both. The input current for the converter depends on the load requirement. The equations for inductor voltage and current through capacitor over one switching period are given in Eqs. (8) and (9), respectively.

$$L_x \frac{di_{Lx}(t)}{dt} = v_x - (1-d_x)v_{cx} \tag{8}$$

$$C_{0x} \frac{dv_{cx}(t)}{dt} = (1-d_x)i_{Lx} - \frac{v_{cx}}{R_L} \tag{9}$$

where 'x' indicates, 'sc' stands for SCESS converter, and it is 'dc' for DC bus converter. The useful transfer functions are extracted using MATLAB to minimize the calculation and to avoid the divergence from what the paper intends to address. The most relevant transfer functions are given in Table 2.

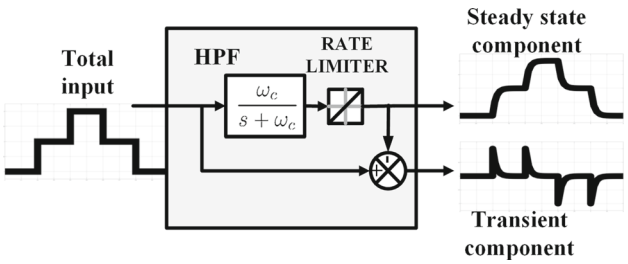

Fig. 4 LPF-rate limiter-based SC control strategy

3 Control system design

The allocation of power between DC bus and SCESS is accomplished by a filter-based control strategy. As stated earlier, the role of SCESS is to mitigate the load transients. Therefore, the SC current controller reference signal must contain the transient part of the total load current. A rate limiter-based LPF control strategy for SCESS converters has been adopted in this paper [12]. The advantage of the limiter is that it always limits the rate of change of DC bus current in the controller operation.

3.1 Supercapacitor control strategy

The SCESS control strategy primarily focuses on the division of the input signal into high- and low-frequency components. The control based on LPF is a popular technique for SC reference current generation. The LPF-rate limiter control strategy for SCESS is shown in Fig. 4. Here, the input is a staircase waveform, while the output divides into two states as the steady state and transient state. The cut-off frequency of the filter is ω_c. Further, (1-LPF) gives the high-frequency component, and it is known as a high-pass filter (HPF). The rate-limiter limits the rate of change of input current, which ensures the safe operation within the system.

3.2 Design of load-SCESS converter control system

The suggested converter control is shown in Fig. 2. The controller consists of an outer voltage loop and an inner current loop. The outer voltage loop generates a current reference signal that corresponds to the required load voltage. As discussed earlier, the current reference gets split into a high-frequency and low-frequency component with LPF. The cut-off frequency of LPF is selected as 5 Hz to obtain a high-frequency reference of SCESS [17]. LPF is given by:

$$G_{LPF}(s) = \frac{\omega_c}{s+\omega_c} \tag{10}$$

$$i_{dcref} = i_{ref}\frac{\omega_c}{s+\omega_c} \tag{11}$$

$$i_{scref} = i_{ref}G_{HPF}(s) \tag{12}$$

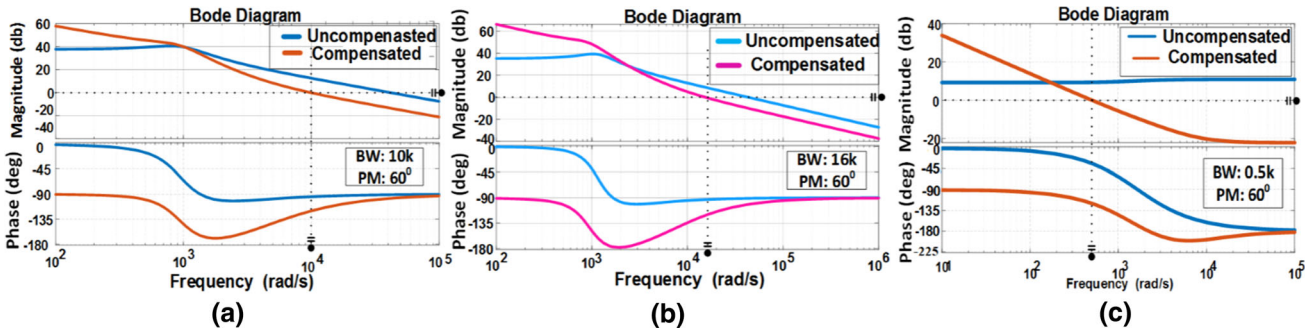

Fig. 5 Bode plot for **a** DC bus current control loop, **b** SCESS current control loop, **c** outer voltage control loop

Table 3 PI controller parameters

S.No	Control loop	PI gains	
		K_p	K_i
1	SC current loop	0.32	2649.6
2	Load converter current loop	0.21	1006
3	Outer voltage loop	0.0224	170

where $G_{HPF}(s)$ is the transfer function of HPf and is given by

$$G_{HPF}(s) = 1 - G_{LPF}(s) = \frac{s}{s + \omega_c} \tag{13}$$

where i_{ref} is the required total current with respect to the corresponding load voltage reference V_{ref}. The i_{dcref} and i_{scref} are the current references for the load and the SCESS converter, respectively.

PI controller is used for controlling the system. The general form of PI controller is

$$PI_{ix} = K_{px} + \frac{K_{ix}}{s} \tag{14}$$

where 'x' represents the loop and it will be 'isc' for SC current loop, 'idc' for load converter current loop and 'v' for outer voltage control loop.

3.2.1 Design of inner current loop

The control transfer function used to design the SC inner current loop is given in Table 2. The SC inner current loop is built with a bandwidth of 16 krad/s to ensure fast operation of SC during load transients. The phase margin is selected 60° as suitable value for stable closed-loop operation. Table 3 shows the PI controller parameters. The bode diagram for the compensated and uncompensated SC current loop is shown in Fig. 5b.

The load converter is unidirectional. The controller constants of the load converter are designed based on load requirements. The inner loop designs are in such a way that it meets the steady-state requirements. The response of the inner load current loop should be slower than the SC inner current loop. To meet this, the bandwidth of the inner current loop is selected as 10 krad/s, whereas the phase margin is 60°. The Bode diagram for the compensated and uncompensated DC bus current loop is shown in Fig. 5a.

3.2.2 Outer loop controller design

The outer voltage controller is designed based on the characteristics of the SC converter [12]. The inner loop gain is taken as a unit because the higher bandwidth prevents the current disturbance from reaching the outer loop. The outer voltage loop transfer function is given in Table 2. The controller designs with the help of the MATLAB/SISO Toolbox [23]. The selected outer loop bandwidth is 0.5 krad/s and the phase margin is 60°. The corresponding PI values for the outer loop are shown in Table 3. The Bode plot with and without compensator is shown in Fig. 5c.

4 Simulation results

Detailed simulation studies were conducted using MATLAB/Simulink software to validate the proposed system. A controlled DC source is used in the simulation as the main DC bus. The system performance is analyzed by introducing perturbations at the source and the load side. The source disturbances are introduced particularly at $t = 0.2$ s and $t = 0.4$ s. At $t = 0.2$ s, the bus voltage is increased from 48 to 63 V and at $t = 0.4$ switch is decreased back to 48 V as shown in Fig. 6a. Three resistances R_1, R_2 and R_3 in parallel through controlled switches represent the fluctuating load.

4.1 System under source disturbance

The DC bus voltage, SCESS voltage, and SOC of SCESS subjected to source disturbances are shown in Fig. 6a–c. The initial voltage of SCESS considered for the simulation is 48 V,

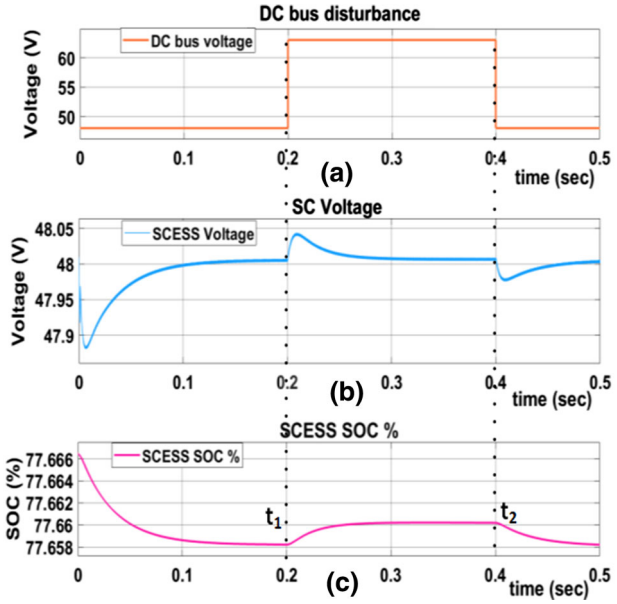

Fig. 6 Simulation results—under source disturbance **a** DC bus voltage, **b** SC voltage, **c** SCESS SOC

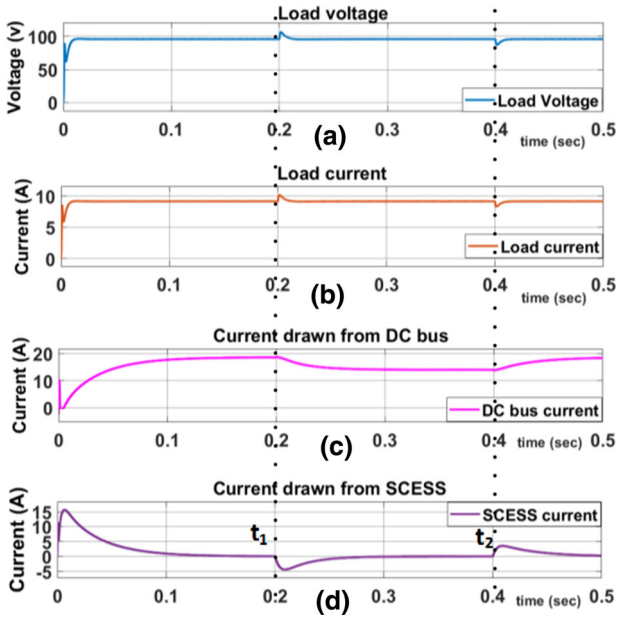

Fig. 7 Simulation results—under source disturbance **a** load voltage, **b** load current, **c** DC bus current, (d) SCESS current

and the corresponding SOC is 77.66%. The system response under the source disturbance is shown in Fig. 7. The load voltage and load current have small variation under the source disturbances, which regains the actual value after a short period as shown in Fig. 7a, b. The corresponding source current of the DC bus and SCESS is shown in Fig. 7c, d. It is clear from the waveforms that the load voltage and the load current gets regulated at 96 V and 9.15 A respectively. Also, the load current is shared accordingly between DC main bus and

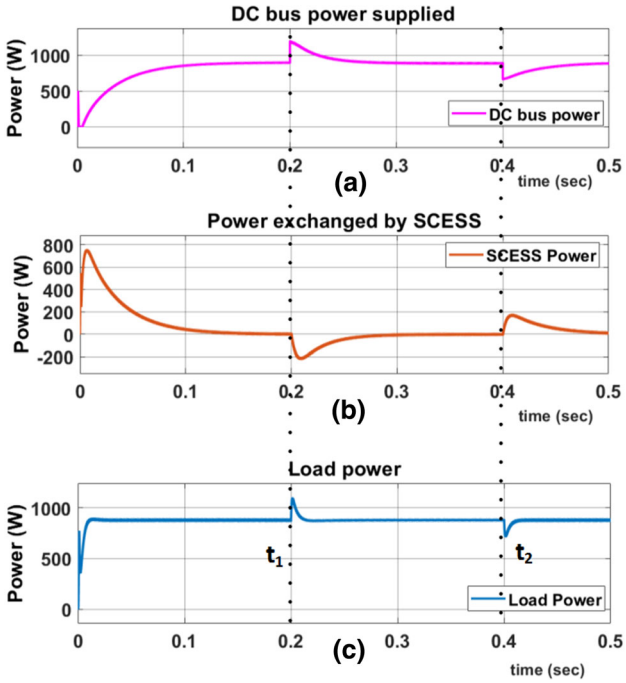

Fig. 8 Simulation results—under source disturbance **a** power supplied by DC bus, **b** SCESS power, **c** load power

SCESS. The SCESS absorbs the additional power supplied to the load bus when the source voltage increases at $t = 0.2$ s. Hence, I_{sc} becomes negative at $t = 0.2$ s and is given in Fig. 7d. Similarly, when the source voltage decreases, SCESS discharges to meet the initial transient current, at $t = 0.4$ s.

It is necessary to check the power-sharing between the source and the loads to understand the efficacy of SCESS. The power supplied by DC bus, SCESS power, and the power consumed by the load is shown in Fig. 8a–c, respectively. The total power required by the load is 880 W. The total load power is shared between the DC bus and SCESS, as shown in Fig. 8a, b. During the transient period and in the source disturbance period, the SC is discharging or charging depending on the load power demand. From Fig. 7c, it is inferred that the peaks and sudden changes in DC bus current are limited, allowing for improved overall performance of a multiple bus system.

4.2 System under load disturbance

Load disturbances are introduced at four different instances to test the system under load fluctuations. The resistor R_1 is always connected with load side, and the power consumed by the same is (P_{R_1}) 500 W. Similarly, P_{R_2} and P_{R_3} represent the power consumed by R_2 and R_3, and the values

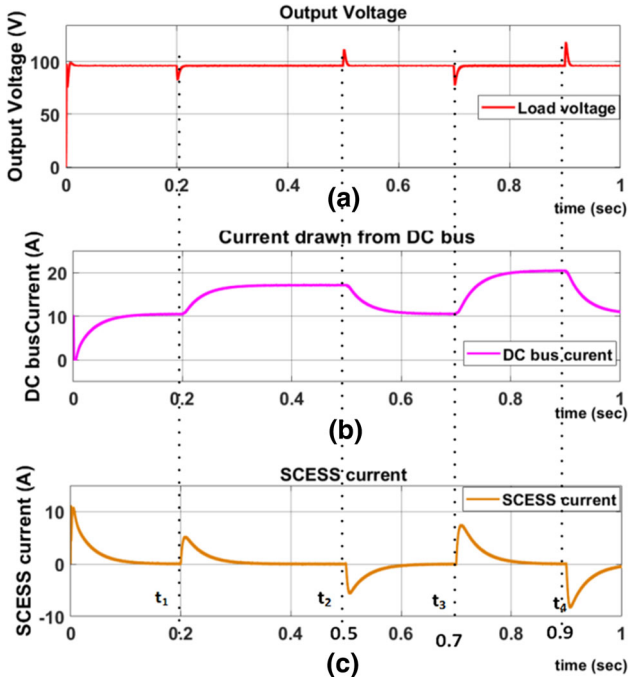

Fig. 9 Simulation results—under fluctuating load **a** output voltage, **b** current drawn from DC bus, **c** SCESS current

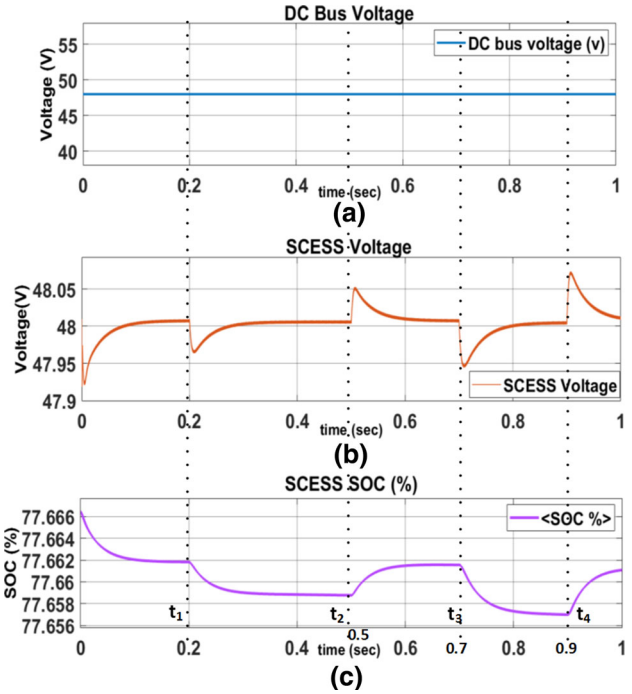

Fig. 10 Simulation results—under fluctuating load **a** DC bus voltage, **b** SC voltage, **c** SCESS SOC

are 300 W and 450 W, respectively. The resistor R_2 is connected at $t = 0.2$ s and is removed at $t = 0.5$ s. Similarly, the resistor R_3 is connected at $t = 0.7$ s and removed at $t = 0.9$ s.

Whenever additional loads are connected in parallel, the required load power and the current drawn from the supply would increase. The load voltage, source current and SC current are shown in Fig. 9a–c, respectively. At t_1 and t_2, the increase in source current results in simultaneous increase in load current. Figure 9c clearly shows that the initial transient current is supplied solely by the SCESS. Furthermore, constant load voltage is maintained irrespective of the system disturbances. The load is disconnected at instances t_2 and t_4, and the DC bus current slowly reaches a new value during this period. The transient power developed at the load bus is absorbed by the SCESS.

Figure 10a–c represents the DC bus voltage, SC voltage and SOC of SCESS, respectively. The SOC variations of SCESS are limited due to the tight control, as shown in Fig. 10c. Figure 11a, b shows the power supplied by DC bus and SCESS, respectively. The DC bus supplies steady-state power and SCESS controls the transient power flow. The fluctuating load power under different instances is shown in Fig. 12. Here, Fig. 12a represents the total power consumed by the load and Fig. 12b–d represents the power dissipated at resistors R_1, R_2 and R_3, respectively.

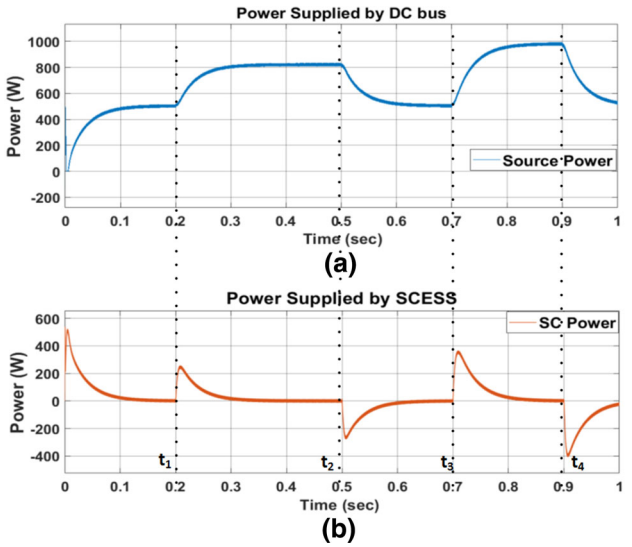

Fig. 11 Simulation results—under fluctuating load **a** power supplied by DC bus, **b** SCESS power

4.3 Comparison of proposed strategy

4.3.1 Comparison of fluctuating loads with and without SCESS

The performance analysis of the DC bus system with and without SCESS is compared in this section. The waveform for DC bus current with and without SCESS is shown in

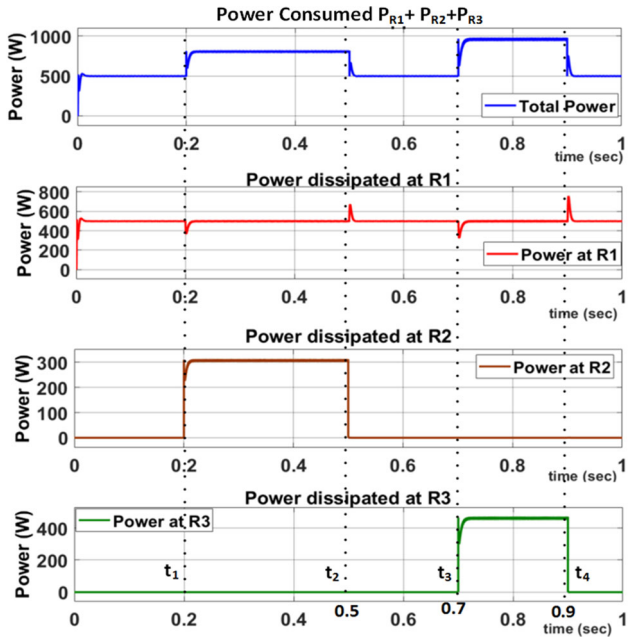

Fig. 12 Simulation results—under fluctuating load **a** total power consumed (P_{R_1}+P_{R_2}+P_{R_3}), **b** power at P_{R_1}, **c** power at P_{R_2}, **d** power at P_{R_3}

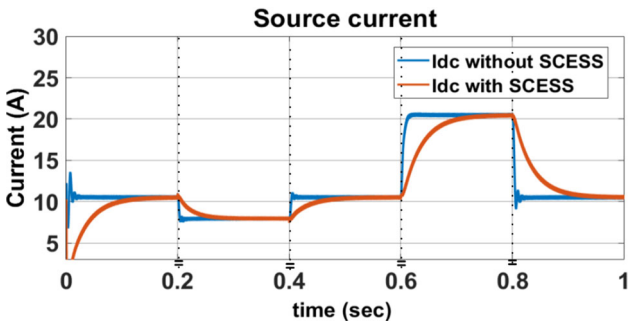

Fig. 13 DC bus current comparison—with and without SCESS

Fig. 13. The source disturbances are created at $t = 0.2$ s and $t = 0.4$ s as shown in Fig. 6a. Similarly, the load disturbances are created at $t = 0.6$ s and $t = 0.8$ s. The waveform clearly shows that the DC bus system with SCESS withdraws minimal transient current compared to the system without SCESS. Further, the smooth transition of the DC bus current reduces the sudden spikes in the system.

The load–voltage waveforms prove that the SCESS integrated DC bus system performs much better than the system without SCESS. Such enhancement is due to the reduction of the ripple current and faster settling of load bus voltage with the incorporation of SCESS. The output voltage waveform is shown in Fig. 14. During source disturbances, the DC bus system without SCESS shows a 12 V variation in the output voltage, while the same with SCESS shows only 6.5 V variation.

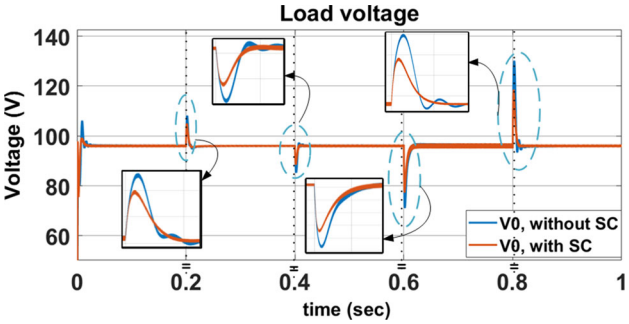

Fig. 14 Load voltage comparison—with and without SCESS

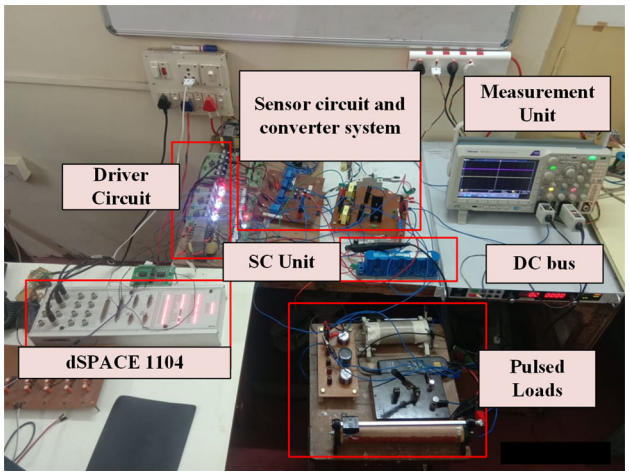

Fig. 15 The experimental setup

The proposed system shows only a variation of 15 V in its output voltage, while the system without SCESS endures a large variation of 30 V at the time of load disturbance of 500 W. From these data, it is clear that DC bus systems without SCESS undergo large voltage fluctuations under source and load disturbances. However, the DC bus system with SCESS shows better performance under these acute variations of load/source conditions.

5 Experimental results and discussion

A prototype developed for testing the feasibility of the proposed SCESS supply system is shown in Fig. 15. A DC power supply is used instead of the main DC bus, and Maxwell 16 V, 58 F SC is used as the SCESS. At the beginning, the SC voltage is 80%. The closed-loop operation is implemented in dSPACE 1104. The prototype is built for a power rating of $\frac{1}{10}^{th}$ of the simulation study.

The input voltage range is 20–25 V and the desired output voltage is 40 V for the prototype. The fluctuating load is made by connecting two 50 Ω resistors in parallel. The operating power of the system is 48 W, and the system is tested under various disturbances.

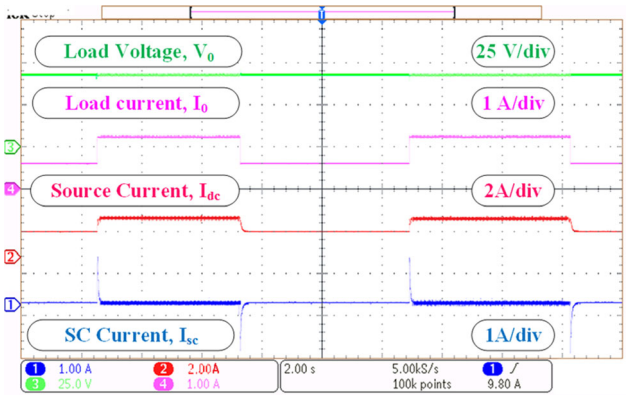

Fig. 16 Experimental result under fluctuating load: load voltage and current wave forms

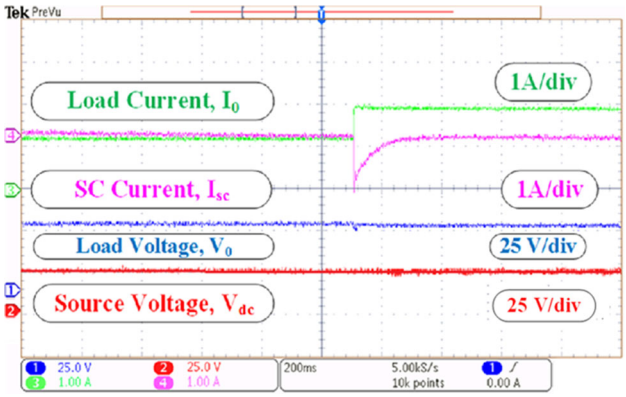

Fig. 18 Experimental result under fluctuating load: magnified portion of SC current at load increment

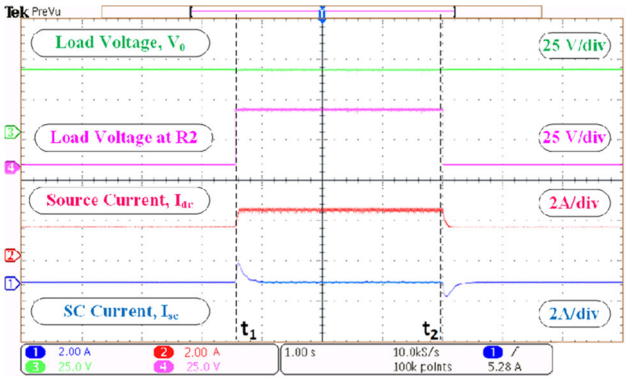

Fig. 17 Experimental result under fluctuating load: R_1 connected at t_1 and disconnected at t_2

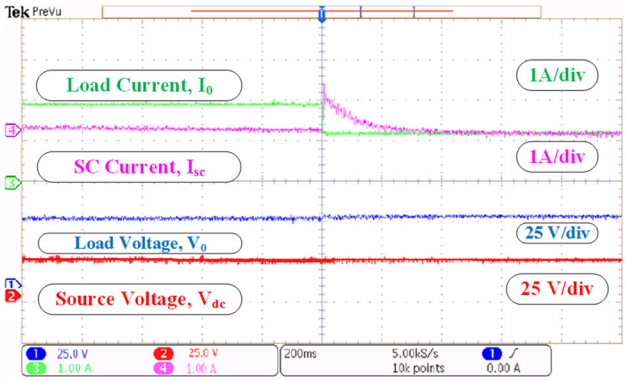

Fig. 19 Experimental result under fluctuating load: magnified portion of SC current at load decrement

5.1 System under fluctuating load

A pulsed load is created by connecting two parallel rheostats using a control switch. The sudden closure of the switch demands high load power. As a result, the load draws more current from the DC bus. The load voltage, DC bus current, load current, and SCESS current are shown in Fig. 16. The load voltage is maintained at 40 V. Whenever the load changes, the SC supplies the fast varying transient current and the DC bus converter current (I_{dc}) rises slowly. During the time period from t_1 to t_2, an additional (R_2) load is connected across the main load (R_1). The voltage across (R_2) is shown in Fig. 17.

A magnified portion of SC current and DC bus current is shown in Figs. 18 and 19 to explain current sharing between SCESS and DC bus. The sudden increase in the load current during load change and the SC supply of the initial transient current to support the DC bus are shown in Fig. 18. Similarly, when the load is disconnected, the SC utilizes the additional current from the source for charging as shown in Fig. 19. During this period, the source voltage and the load voltage are maintained at 20 V and 40 V, respectively.

5.2 Step change in DC bus voltage

The source variation is created by changing the DC bus voltage from 20 to 25 V at t_1 and then back to 20 V at t_2. The load voltage is kept steady throughout this period, and the source current gets reduced to maintain constant power. The smooth conversion of the main DC bus current is achieved by SCESS. The experimental results during source disturbance are shown in Fig. 20. Regardless of the changes in input voltage and current, the load voltage is maintained constant at 40 V. Due to the switching of the converter during normal operation, a slight ripple current flows through SCESS. However, transient current from the supply at the time of disruption is absorbed by the SC.

The parallel connection of controlled SCESS with the DC load bus improves the system response as well as reduces the current stress on the DC microgrid. The sudden shift in the load bus or main DC bus is neutralized with the aid of SCESS. Furthermore, the system's power quality is reshaped as the SC absorbs the high-frequency fluctuations out of the load. It is the reason for fewer ripples in the load voltage and loads current.

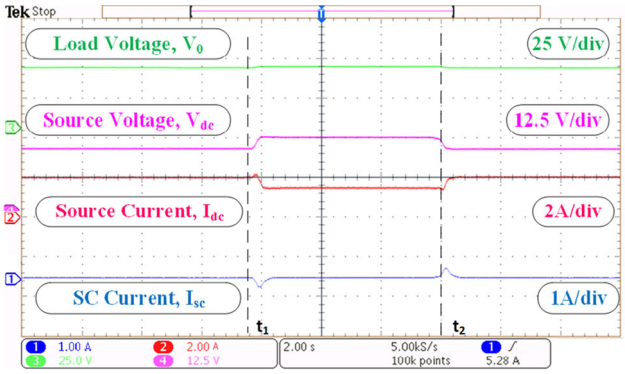

Fig. 20 Experimental result under source variation: t_1 : V_{dc} increment, t_2 : V_{dc} decrement

6 Conclusion

This paper introduced an SC-based transient power supply to stabilize the output of DC microgrid under fluctuating loads. The fast-responding nature of SCESS is utilized to mitigate the transient effect on DC microgrids such that the changes in the DC main bus are minimal. System realization is carried out by connecting a controlled SCESS network in parallel with a dedicated fluctuating load bus. The low-pass filter-rate limiter regulates the SCESS operation. The simulation study discloses the feasibility of the system. The DC bus current varies smoothly, and the SCESS compensates the transient power requirement. The experimental results confirm that the SCESS strongly supports the DC microgrid under all fluctuations and adverse conditions. Thus, the proposed method could be a long-lasting solution to improve the power quality issues related to fluctuating loads of future DC microgrids.

References

1. Dragičević T, Lu X, Vasquez JC, Guerrero JM (2015) DC microgrids-part II: a review of power architectures, applications, and standardization issues. IEEE Trans Power Electron 31(5):3528–3549
2. Vazquez S, Lukic SM, Galvan E, Franquelo LG, Carrasco JM (2010) Energy storage systems for transport and grid applications. IEEE Trans Ind Electron 57(12):3881–3895
3. Mathew P, Madichetty S, Mishra S (2019) A multi-level control and optimization scheme for islanded pv based microgrid: a control frame work. IEEE J Photovolt 9(3):822–831
4. Eghtedarpour N, Farjah E (2014) Distributed charge/discharge control of energy storages in a renewable-energy-based DC micro-grid. IET Renew Power Gener 8(1):45–57
5. Jose JJ, Manthati UB (2016) Two-input bidirectional converter controlled hybrid energy storage system (HESS) for micro grids. In: 2016 IEEE 1st international conference on power electronics, intelligent control and energy systems (ICPEICES), pp 1–4
6. Crider JM, Sudhoff SD (2010) Reducing impact of pulsed power loads on microgrid power systems. IEEE Trans Smart Grid 1(3):270–277
7. Xiao J, Wang P, Setyawan L (2015) Hierarchical control of hybrid energy storage system in DC microgrids. IEEE Trans Ind Electron 62(8):4915–4924
8. Punna S, Manthati UB (2020) Optimum design and analysis of a dynamic energy management scheme for HESS in renewable power generation applications. SN Appl Sci 2(3):1–13
9. Faddel S, Saad AA, El Hariri M, Mohammed OA (2019) Coordination of hybrid energy storage for ship power systems with pulsed loads. IEEE Trans Ind Appl 56(2):1136–1145
10. Ahmadi MMH, Aghasi SH, Salemnia A (2018) Hybrid energy storage for DC microgrid performance improvement under nonlinear and pulsed load conditions. In: 2018 smart grid conference (SGC), pp 1–6
11. Lashway CR, Elsayed AT, Mohammed OA (2016) Hybrid energy storage management in ship power systems with multiple pulsed loads. Electr Power Syst Res 141:50–62
12. Kollimalla SK, Mishra MK, Ukil A, Gooi HB (2016) DC grid voltage regulation using new HESS control strategy. IEEE Trans Sustain Energy 8(2):772–781
13. Kuperman A, Aharon I (2011) Battery-ultracapacitor hybrids for pulsed current loads: a review. Renew Sustain Energy Rev 15(2):981–992
14. Arunkumar CR, Manthati UB (2019) Design and small signal modelling of battery-supercapacitor HESS for DC microgrid. In: TENCON 2019–2019 IEEE region 10 conference (TENCON). IEEE, pp 2216–2221
15. Berrueta A, Ursua A, San Martin I, Eftekhari A, Sanchis P (2019) Supercapacitors: electrical characteristics, modeling, applications, and future trends. IEEE Access 7:50869–50896
16. Azizi I, Radjeai H (2018) A new strategy for battery and supercapacitor energy management for an urban electric vehicle. Electr Eng 100(2):667–676
17. Kotra S, Mishra MK (2017) A supervisory power management system for a hybrid microgrid with HESS. IEEE Trans Ind Electron 64(5):3640–3649
18. Zhang L, Hu X, Wang Z, Sun F, Deng J, Dorrell DG (2017) Multi-objective optimal sizing of hybrid energy storage system for electric vehicles. IEEE Trans Veh Technol 67(2):1027–1035
19. Zhang Q, Li G (2019) A predictive energy management system for hybrid energy storage systems in electric vehicles. Electr Eng 101(3):759–770
20. Farhadi M, Mohammed O (2014) Adaptive energy management in redundant hybrid DC microgrid for pulse load mitigation. IEEE Tran Smart Grid 6(1):54–62
21. Farhadi M, Mohammed O (2014) Performance enhancement of actively controlled hybrid DC microgrid with pulsed load. In: 2014 IEEE industry application society annual meeting, pp 1–8
22. Mardani MM, Khooban MH, Masoudian A, Dragičević T (2018) Model predictive control of DC–DC converters to mitigate the effects of pulsed power loads in naval DC microgrids. IEEE Trans Ind Electron 66(7):5676–5685
23. Zhang Y, Li YW (2016) Energy management strategy for supercapacitor in droop-controlled DC microgrid using virtual impedance. IEEE Trans Power Electron 32(4):2704–2716
24. Erickson RW, Maksimovic D (2007) Fundamentals of power electronics. Springer