A Quasi-Z-Source-Based Space-Vector-Modulated Cascaded Four-Level Inverter for Photovoltaic Applications

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***Abstract*— This article proposes a single-stage buck–boost topology for photovoltaic (PV) applications with a three-phase output. This power converter is constituted by three quasi-Z-source (qZS) networks that are integrated with a four-level cascaded multilevel inverter (FCMI). Compared to the conventional multilevel inverter (MLI) configurations, such as the neutral-point-clamped (NPC) and the cascaded H-bridge (CHB) inverters, the proposed topology is structurally simple with lesser number of components. The proposed power converter and its modulation scheme enhance the boost factor by 50% compared to the aforementioned topologies while alleviating the voltage stress on the switching devices. It is shown that the proposed converter can regulate the output voltage in the stand-alone mode by controlling the shoot-through duty ratio of the qZS networks. Furthermore, it is shown that the proposed converter can be interfaced with the grid by controlling the modulation index along with the shoot-through duty ratio to achieve the twin objectives of maximum power point tracking (MPPT) and the unity power factor (UPF) operation with the grid. The simulation studies and experimentation on a scaled-down laboratory prototype verify the steady-state and dynamic performances of the proposed power circuit configuration and the associated control strategy.**

***Index Terms*— Four-level cascaded multilevel inverter (FCMI), level-shifted pulse width modulation (PWM), quasi Z-source (qZS), voltage boosting.**

I. Introduction

THE importance of renewable energy sources needs not to be overemphasized in the present scenario of dwindling resources of conventional energy. The efforts to contain environmental pollution resulted in the emergence of solar photovoltaic (PV) systems. Solar energy is increasingly being used in applications, such as water pumping, street lighting, air conditioning, and refrigeration. Declining costs, durability, and lower maintenance are the contributing factors to the proliferation of solar energy systems. Also, PV systems are pivotal to the realization of distribution generation (DG) systems. PV systems can be used in low and medium scales for standalone and grid-connected applications.

Solar PV systems often require conversion of low output voltages of PV panels into ac of required voltage and frequency to cater to the requirements of consumers. In practice, it is often accomplished by a two-stage conversion process. First, the low dc voltage output by the PV panels is boosted to attain the required dc voltage level using a dc–dc boost converter. Apart from voltage boosting, this converter plays the pivotal role of rendering the maximum power point tracking (MPPT) capability to the solar PV system. The dc voltage, thus boosted, is then converted into ac using a conventional voltage-source inverter (VSI) to deliver ac power of required voltage and frequency to the end users. Despite its popularity, the two-stage conversion system increases the cost and complexity, taxing the efficiency and the reliability of the power circuit [1], [2]. On the other hand, a single-stage dc/ac conversion system with the conventional VSI (which should output the required ac voltage, even with a lower PV voltage) results in an overrated design of the system [3].

These disadvantages are overcome with the Z-source inverter (ZSI), which is a single-stage power circuit configuration. It is capable of handling low PV voltage with a wide voltage range while providing inherent protection from the shoot-through fault [4], [5]. The disadvantage associated with the conventional ZSI, namely, the discontinuous input current, is overcome with the quasi-Z-source (qZS) inverters [6]. Furthermore, the voltage rating of one of the capacitors is significantly reduced in qZSIs compared to the conventional ZSIs.

On the other hand, multilevel inverters (MLIs) are extensively employed in PV applications. Unlike the conventional two-level VSIs, they are capable of producing output voltage waveforms with lesser total harmonic distortion (THD), lower electromagnetic interference (EMI), and lesser *dv/dt* stress on the semiconductor devices. Thus, the combination of the qZS network with MLIs can inherit the benefits associated with both of these topologies [7], [8].

Most of the research work regarding the integration of Z-source and MLIs is carried out considering the conventional neutral-point-clamped (NPC) and cascaded H-bridge (CHB) converter topologies. In the work reported in [9] and [10],

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two isolated dc sources are connected to two Z-sources to obtain the required buck–boost capability. The boosted dc-link is connected to a three-level NPC MLI at the back end. The resulting system is a typical single-stage system as the shoot-through time period required for the Z-source is provided by the back-end three-level inverter. However, it is an expensive proposition due to the additional clamping diodes and the requirement of a complex modulation technique for proper balancing of the shoot-through in the Z-source network.

The single Z-source topology, reported in [11], also requires two dc sources. Compared to [9], it needs only one impedance network. However, the cost of the system is not reduced, as the size and component ratings of the passive elements are doubled. Following these developments, few more power circuit configurations have been proposed, which employ a single dc source and a single Z-source [12]. However, the main disadvantage with these topologies is the discontinuous input current, which should be avoided in PV applications. The requirement of achieving a continuous input current led to the development of three-level qZS-NPC topologies [13]. An early topology belonging to this category consists of a symmetrical combination of two qZS networks that form a T-type structure with a common neutral point. A modified qZS-based power circuit configuration is proposed in [14], which needs fewer switching devices. In this power converter, two qZS networks are connected to a three-level T-type inverter. Both of these topologies display drawbacks, such as: 1) deviation of the neutral point voltage due to the unbalancing of the capacitor voltages; 2) additional clamping diodes; and 3) the nonimprovement of boost factor compared to the traditional qZSI [13], [14].

CHB-MLIs comprise multiple units of H-bridge inverters, which reduces the requirement of the dc-link voltage for each inverter. They also provide an output voltage waveform with much lesser THD and *dv/dt* [15]–[17]. Recently, a combination of qZS and CHB-MLI is proposed, which combines the advantages of both CHB-MLIs and the qZSs [18], [19]. In these configurations, individual qZS networks are connected to each H-bridge inverter to obtain the required voltage boosting. However, these systems require individual MPPT and dc-link voltage [20], [21].

The single-stage, three-phase qZS-CHB MLI proposed in [20] requires nine isolated PV sources, 36 semiconductor switching devices, and the associated gate-drive circuitry. Though the qZS-CHB MLI converter displays a higher efficiency, the cost and complexity of control increase with the number of levels in the output voltage. This is due to the requirement of implementing MPPT individually for each qZS and controlling its dc-link voltage.

In general, multilevel inversion can be obtained with a relatively new topology known as the cascaded multilevel inverter (CMI) [22]. This topology brings in a considerable reduction in the number of dc sources and switching devices compared to the CHB-MLI configuration. Unlike the NPC and the flying capacitor (FC) MLI topologies, the CMI does not require clamping diodes/capacitors. For a comparable number of voltage levels in the output (phase voltage) waveform, CMIs require fewer numbers of dc input power supplies and power

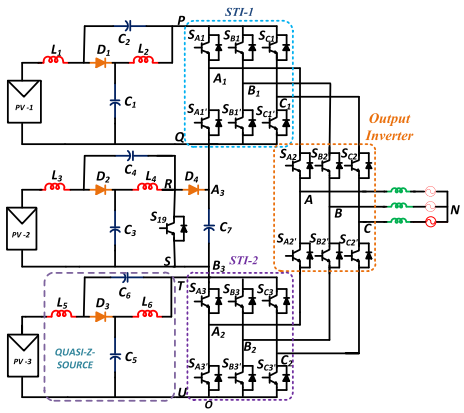

Fig. 1. Proposed qZS-FCMI.

semiconductor switching devices. Due to the reduced number of components, the reliability of a CMI would be higher compared to the aforementioned power converter configurations.

This article proposes a new power converter configuration, which is obtained by the amalgamation of qZS networks with a four-level CMI (FCMI) to achieve single-stage conversion. This article also shows that, when the proposed converter is modulated with a carrier-based level-shifted space-vector pulse width modulation (LSPWM) scheme, it would result in 50% higher boosting capability compared to the NPC three-level and CHB-based systems. Furthermore, the proposed converter outputs a higher number of voltage levels compared to the aforementioned topologies, causing a better spectral performance. It is also shown that the proposed LSPWM scheme implements the shoot-through state, required for the qZS, using the FCMI without any additional power loss in the semiconductor switching devices. The steady-state and dynamic performances of the proposed converter are assessed with simulation studies. The proof of concept is provided with experimentation using a laboratory prototype.

II. Proposed qZS-FCMI

A. Power Converter

The proposed PV-fed qZS-based four-level CMI (qZS-FCMI) is shown in Fig. 1. In this circuit configuration, four-level inversion is achieved by the cascaded connection of three basic two-level VSIs. Two of these inverters are pivotal in implementing the shoot-through mode, which is essential for the operation of the qZS networks. Thus, these are named shoot-through inverter-1 (STI-1) and shoot-through inverter-2 (STI-2), respectively.

The output terminals of STI-1 (A_1–C_1) and STI-2 (A_2–C_2) are connected to the dc input terminals of the third VSI (see Fig. 1), which steers the output of these two shoot-through inverters to the load/grid. Hence, it is named the output inverter.

These VSIs are fed with three identical qZS networks that boost the low input voltages of isolated PV panels to the desired levels. The middle qZS network is accompanied by a switch (S_{19}), a dc-link capacitor (C_7), and a diode (D_4). These components provide a constant dc-link voltage at terminal points (A_3, B_3).

TABLE I
POLE VOLTAGE (V_{AO}) FOR DIFFERENT SWITCHING COMBINATIONS

State type	Pole Voltage (V_{AO})	Level No	Pole (A) terminal connection (See Fig.1)	Switching states (1-ON, 0-OFF)					
				S_{A1}	$S_{A1'}$	S_{A2}	$S_{A2'}$	S_{A3}	$S_{A3'}$
NST	V_{DC}	3	P	1	0	1	0	0	0
NST	$\frac{2V_{DC}}{3}$	2	Q	0	1	1	0	0	0
UST				1	1	1	0	1	0
NST	$\frac{V_{DC}}{3}$	1	T	0	0	0	1	1	0
NST	0	0	U	0	0	0	1	0	1
LST				0	1	0	1	1	1

NST**-Non shoot-through,UST**-Upper shoot-through,***LST**-Lower shoot-through.

Similar to the conventional ZSI, the qZSI operates in two modes, namely: 1) the shoot-through mode and 2) the nonshoot-through mode. In the shoot-through mode, energy from the PV source and the capacitors (C_1, C_2) is stored in the inductors (L_1, L_2) by turning on the switches in each phase of the inverter. This stored energy in the inductors is then transferred to the load during the nonshoot-through mode of qZSI. The presence of the impedance networks before the inverters avoids the requirement of the dead-band circuitry for protection against the shoot-through fault. This topology consists of 19 power semiconductor switching devices (S_1–S_{19}). The shoot-through mode is inserted for the top and the bottom qZSs through the phase legs of the STI-1 and STI-2 inverters. A separate switch (S_{19}) is used to introduce the shoot-through mode in the middle qZS.

B. Switching States and the Output Voltage of the Four-Level Inverter

The pole voltages (the voltages of the "A," "B," and "C" points shown in Fig. 1 with reference to point "O") of the qZS four-level inverter are denoted as V_{AO}, V_{BO}, and V_{CO}, respectively. Table I shows the details regarding the switching states of the individual devices pertaining to the A-phase of the proposed FCMI and the pole voltage (V_{AO}).

In Table I, as well as for the rest of this article, the logic levels "1" and "0," respectively, indicate the "on" and "off" states of the switching devices present in the proposed power converter. From Table I, it is evident that each pole voltage of the proposed converter is capable of assuming four levels, thus making it a four-level VSI.

The shoot-through switching states for phase-A of the STI-1 and STI-2 inverters are also shown in Table I. From this table, it may be noted that, whenever a shoot-through state is inserted in any given phase in the STI-1, the pole voltage of that phase falls from a level of "V_{dc}" to a level of "$2V_{dc}/3$." Similarly, whenever a shoot-through state is inserted in any given phase leg in the STI-2, the pole voltage of that phase becomes 0 V.

The pole voltages of the cascaded qZS four-level inverter can be expressed as

$$V_{AO} = S_{A2} * S_{A1} + \frac{(S_{A2'} * S_{A3})}{3} + \frac{(S_{A1'} * S_{A2}) * 2}{3} \quad (1)$$

$$V_{BO} = S_{B2} * S_{B1} + \frac{(S_{B2'} * S_{B3})}{3} + \frac{(S_{B1'} * S_{B2}) * 2}{3} \quad (2)$$

$$V_{CO} = S_{C2} * S_{C1} + \frac{(S_{C2'} * S_{C3})}{3} + \frac{(S_{C1'} * S_{C2}) * 2}{3}. \quad (3)$$

The common-mode voltage will be the average of three-pole voltages as follows:

$$V_{CM} = (V_{AO} + V_{BO} + V_{CO})/3. \quad (4)$$

The phase voltage of the inverter using the above equations

$$V_{AN} = V_{AO} - V_{CM} \quad (5)$$

$$V_{BN} = V_{BO} - V_{CM} \quad (6)$$

$$V_{CN} = V_{CO} - V_{CM}. \quad (7)$$

Thus, the phase voltages are expressed as

$$V_{AN} = \left(2^* V_{AO}\right)/3 - (V_{BO}/3) - (V_{CO}/3) \quad (8)$$

$$V_{BN} = \left(2^* V_{BO}\right)/3 - (V_{CO}/3) - (V_{AO}/3) \quad (9)$$

$$V_{CN} = \left(2^* V_{CO}\right)/3 - (V_{BO}/3) - (V_{CO}/3). \quad (10)$$

III. CONTROL STRATEGY FOR THE PROPOSED QZS-FCMI

A. Implementation of the SVPWM Scheme

In general, the space-vector PWM (SVPWM) is preferred as it results in 15% more utilization of the dc-link voltage compared to the sine-triangle PWM (STPWM). In this work, the SVPWM is implemented by adopting the switching scheme described in [23], wherein the concept of imaginary switching time periods is introduced. Operating only on the references (denoted by v_a^*, v_b^* and v_c^*), this scheme directly outputs the gating waveforms for a two-level VSI. The on-time periods of the gating signals pertaining to the top switching devices in a two-level VSI (i.e., devices connected to the positive dc rail) are denoted by the time periods T_{ga}, T_{gb}, and T_{gc}.These time periods replicate the waveforms of the references (i.e., v_a^*, v_b^*, and v_c^*). This article uses the normalized modulating signals denoted as T_{ga}^*, T_{gb}^*, and T_{gc}^*, which are the per-unit values, obtained on the base value of the sampling time period of T_s.

In general, the implementation of SVPWM can be either sample-based or carrier-based. This article uses the latter, as it is more convenient to implement for the present system. Of the several variants of the carrier-based implementations, the level-shifted PWM (LSPWM) is selected to implement the SVPWM scheme, as it offers advantages such as ease of implementation. In the LSPWM technique, phase disposed (PD) carrier waveforms are used, where the three triangular carrier waves are in phase and are displaced vertically by an equal amount of 1/3. These reference waves (T_{ga}^*, T_{gb}^*, and T_{gc}^*) are compared with the top, middle, and bottom carrier waves to produce the switching signals for the three two-level inverters, as shown in Fig. 2.

B. Insertion of the Shoot-Through in the FCMI

In order to introduce the shoot-through, the maximum and minimum envelopes of the reference waves are generated using the following:

$$T_{g\max} = \mathrm{MAX}\left(T_{ga}^*, T_{gb}^*, T_{gc}^*\right) \quad (11)$$

$$T_{g\min} = \mathrm{MIN}\left(T_{ga}^*, T_{gb}^*, T_{gc}^*\right). \quad (12)$$

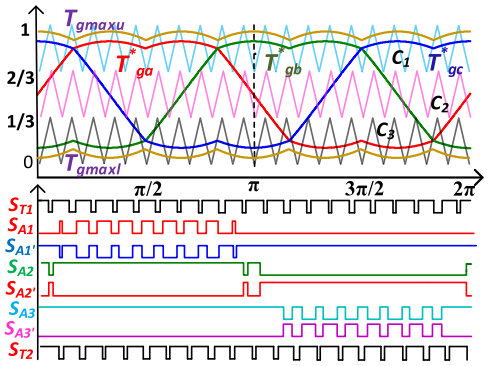

Fig. 2. Implementation of phase-A switching for qZS-FCMI.

These envelopes (T_{gmax}) and (T_{gmin}) are modified by shifting them in opposite directions by half of the required shoot-through time (denoted as T_{sh}). The modified references are, respectively, denoted as (T_{gmaxu}) and (T_{gminl}), which are given in the following:

$$T_{g\max u} = T_{g\max} + (D/2) \tag{13}$$

$$T_{g\min l} = 1 - T_{g\min} - (D/2). \tag{14}$$

The shoot-through duty factor "D" is defined as $D = (T_{\text{sh}}/T_s)$.

The modified envelopes given by (13) and (14) are compared with the respective carriers to obtain the *shoot-through pulses* for the STI-1 and STI-2, as shown in Fig. 2. To obtain the desired gating signals to implement the required shoot-through time period, a logical "OR" operation is performed between the shoot-through pulses (S_{T1}, S_{T2}) and the original gating signals (which are produced by the comparison of the original references T^*_{ga}, T^*_{gb}, and T^*_{gc} and the carrier waveforms). Thus, the required voltage boosting is obtained.

The implementation of shoot-through for the proposed converter is explained with the space-vector diagram of the FCMI, which consists of three concentric hexagons (see Fig. 3), which consists of three concentric hexagons. While the tip of the reference vector is located in the innermost hexagon for two-level operation, it is located in the middle and outer layers, respectively, for three- and four-level operations. From Table I, it is evident that each pole voltage assumes four switching states independent of the other two, resulting in a total of 64 (4^3) useful switching states for the four-level FCMI. These (64) switching states result in 37-V space vectors. It may be noted from Fig. 3 that the entire space-vector diagram is divided into 54 sectors.

Let an instant be considered, wherein the reference voltage vector ($\vec{OT}$) is situated in the sector "HVW," as shown in Fig. 3. The objective of the LSPWM scheme is to synthesize this reference voltage vector in the average sense, over the sampling time period (denoted as "T_s"). The switching sequence required to synthesize this reference voltage is given by [210]–[310]–[320]–[321], as shown in Fig. 4. The phase-disposition (PD) strategy ensures that the nearest vectors, which are situated in the closest proximity to the reference voltage vector, are switched while allowing only one transition between the switching of the successive vectors.

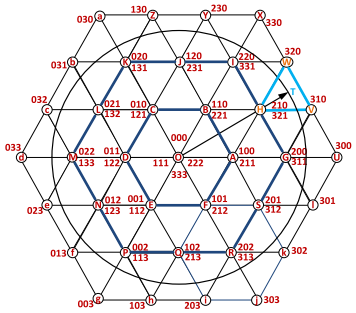

Fig. 3. Space-vector diagram of FCMI.

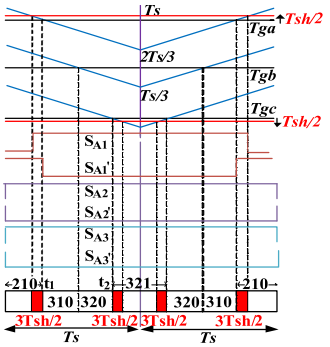

Fig. 4. Switching sequence of FCMI when the reference phasor is in sector HVW.

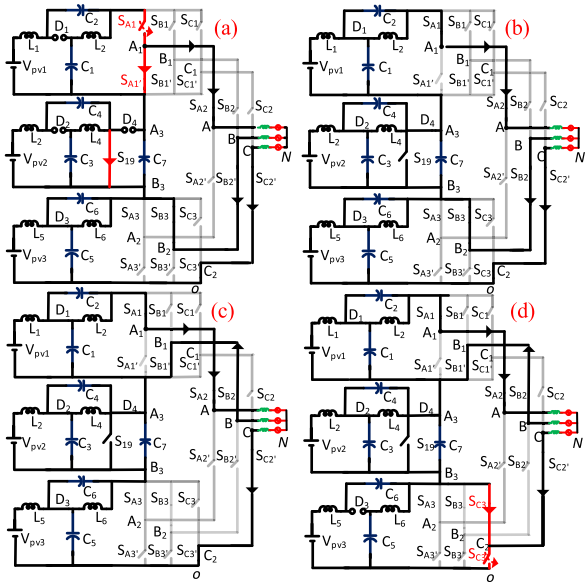

Fig. 5. Circuit diagrams for switching states mentioned in Fig. 4. (a) [210] state. (b) [310] state. (c) [320] state. (d) [321] state in a given sample time T_s.

A typical sequence [210] denotes that pole-A is connected to the point "Q," pole-B is connected to the point "T," and pole-C is connected to point-U, as shown in Fig. 5(a). It may be noted that all the three output points of the STI-1 (A_1–C_1) are clamped to the negative rail of the top qZS network when the vector [210] is switched (i.e., the STI-1 is operated with a null vector). This facilitates the introduction of the shoot-through state in the STI-1, by turning on switch S_{A1}, as shown in Fig. 5(a). The implementation of the shoot-through state in the [210] state is shown in Fig. 4 (region in red color).

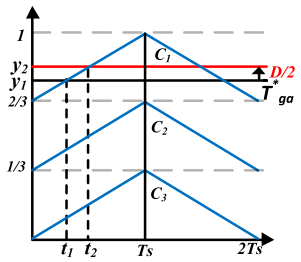

Fig. 6. Scaling of boost factor by LSPWM technique.

When a transition occurs from the vector [210] to the vector [310], as shown in Fig. 5(b), the rising edge of the gating signal to the top-device S_{A1} is advanced by a duration of $3T_{sh}/2$, while the turn-off of the bottom-device $S_{A1'}$ remains unaltered (i.e., it occurs at "t_1" as before). Thus, the insertion of the shoot-through state does not incur additional switching power loss. In the state [310], it may be noted that: 1) the pole-A is connected to the point "P" of STI-1; 2) the pole-B is connected to the point "T" of STI-2; and 3) the pole-C is connected to the terminal "U" of the STI-2 [as shown in Fig. 5(b)]. Consequently, both STI-1 and STI-2 are in their active states, and power is transferred from their respective qZ sources to the load through the output inverter.

When the proposed converter is switched to the [320] state, poles A–C are connected to the "P," "Q," and "U" terminals, as shown in Fig. 5(c). Thus, both STI-1 and STI-2 are in their active states as in the case of the state [310].

The occurrence of shoot-through in the A-phase of the STI-1 leads to the boosting of the dc-link of the top qZS network. To ensure a balanced operation between the top- and bottom-qZS networks, the shoot-through time is equally distributed in the STI-1 and STI-2 in a given sample time period (T_s). When the vector [321] is switched, the STI-2 is operated with a null vector. All the three output points of the STI-2 (A_2–C_2) are clamped to the positive rail of the bottom qZS network, as shown in Fig. 5(d). Thus, this state is also amenable for the introduction of the shoot-through state by turning on the switch $S_{C3'}$.

From the foregoing discussion, it is obvious that there is no mechanism to introduce the shoot-through state in the middle qZS. Hence, an additional switch is provided (S_{19}; see Fig. 1) to implement the shoot-through state and boost the low voltage output by the middle string of the PV panel.

C. Analysis of the Boost Factor of the qZSs With the Proposed PWM Scheme

The references and the carrier signals corresponding to STI-1 are shown in Fig. 6.

This diagram is drawn for a period, wherein the maximum value among the three references is assumed by the A-phase. This diagram helps to evaluate the modified boost factor in the proposed power converter. It may be observed that the slope of the top carrier wave (C_1) is 1/3.

From Fig. 6, the point of intersection between the upper carrier wave and the reference occurs at (t_1, y_1).The coordinates t_1 and y_1 are related by the following expression:

$$y_1 = \frac{1}{3}t_1 + \frac{2}{3} \tag{15}$$

$$y_2 = \frac{1}{3}t_2 + \frac{2}{3}. \tag{16}$$

The difference in (16) and (15) results in

$$y_2 - y_1 = \frac{1}{3}(t_2 - t_1). \tag{17}$$

From Fig. 6, it may be noted that

$$y_2 - y_1 = (D/2).$$

Hence,

$$t_2 - t_1 = (3D/2). \tag{18}$$

From the above equations, it is evident that an increment of (D/2) to the modulating signal "T^*_{ga}" manifests as an increase in the shoot-through time period of ($3D$/2) (introduced in phase-A) for STI-1. Thus, it can be stated that the LSPWM results in the scaling-up of the shoot-through time period by a factor of 3 compared to the shoot-through time period of a Z-source or a qZS-fed two-level inverter (which is equal to "D"). A similar conclusion can be drawn for the STI-2 as well by decrementing the reference signal T^*_{gc} by D/2 on the *lower* carrier wave (see Fig. 6).

The increment in the shoot-through time period increases the boosting capability of the inverter. As the shoot-through duty factor is modified to ($3D$/2), the equation governing the relationship between the shoot-through duty period (D) and the boost factor (B) is also modified. The relationship between the shoot-through duty (D) and the boost factor (B) for the conventional Z-source or quasi Z-source-fed inverter proposed in [6] is given by

$$B_{\text{conv}} = \frac{1}{1-2D}. \tag{19}$$

The boost factor for the proposed converter operated with the proposed control scheme is obtained by simply replacing the shoot-through duty (D) with ($3D$/2)

$$B_{\text{new}} = \frac{1}{1-2\left(\frac{3D}{2}\right)} = \frac{1}{1-(3D)}. \tag{20}$$

It suggests that there is a considerable improvement in the boost factor with the proposed control strategy compared to the conventional scheme. For example, when $D = 0.2$, the boost factor in the conventional scheme is given by 1.667. For the same shoot-through duty, the boost factor increases to 2.5 with the proposed power converter (an increase by 50%)

$$\hat{V} = \frac{1}{\sqrt{3}} * M * B_{\text{new}} * V_{\text{input}}. \tag{21}$$

It expresses the peak fundamental output phase voltage ("$\hat{V}$") of the qZS four-level inverter.

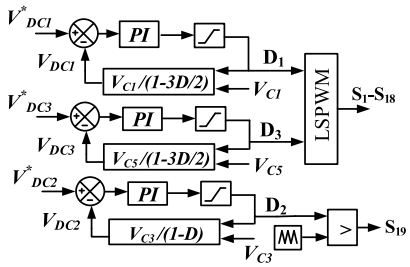

Fig. 7. DC-link voltage control scheme for the proposed FCMI.

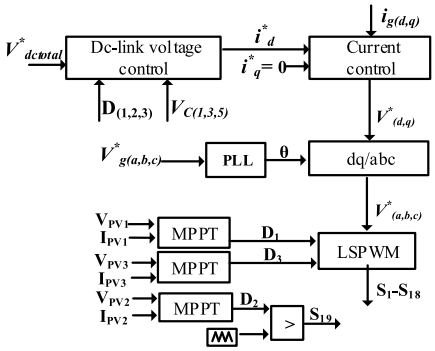

Fig. 8. Block diagram of the grid control scheme.

IV. Control Scheme of qZS-FCMI for Stand-Alone and Grid-Connected Operations

A. Stand-Alone Mode

The overall gain of the proposed converter is given by the product of the boost factor (B) of the front-end qZS section and the modulation index (M) of the back-end four-level inverter. It is evident that both these sections are mutually dependent on each other. While the front-end qZS provides the dc-link for the four-level inverter, the latter facilitates the much required shoot-through state for the former. As the shoot-through state is inserted in the zero (null) state, the momentary short-circuiting of the dc-link (due to the insertion of the shoot-through state) does not affect the waveform of the output voltage of the four-level inverter. Generally, the modulation index (M) that controls the output voltage of the four-level inverter is held constant in the standalone mode.

As the dc-link voltage of the four-level inverter varies due to the fluctuations in the PV voltage, the boost factor (B) of the qZS is adjusted to regulate the dc-link voltage with closed-loop control and also to regulate the output voltage of the four-level inverter at the required voltage level. As the boost factor (B) depends on the shoot-through duty factor [*D,* (20)], the output voltage is regulated simply by controlling the shoot-through duty ration "*D.*" Fig. 7 shows the control scheme for the regulation of the dc-link voltage for the four-level inverter using the shoot-through duty ratio. As the dc-links of STI-1 and STI-2 are fed from qZS networks, a pulsating voltage waveform is produced at the terminals of the dc-links (terminals P–S and T, U as marked in Fig. 1) when the shoot-through mode is inserted in each phase leg.

This pulsating waveform, such as the voltage across the points "P" and "Q" (see Fig. 1), can neither be sensed directly nor can it be used as the feedback signal to regulate the dc-link voltage. Hence, the actual dc-link voltage is estimated by sensing the capacitor voltage and the shoot-through duty ratio (D) of the individual inverters.

The dc-link voltages V_{dc1} and V_{dc3} are compared with the references V^*_{dc1} and V^*_{dc3}, respectively, and the corresponding errors are input to the individual PI controllers. The PI controllers then produce the control signals, which controls the shoot-through duty ratios "D_1" and "D_3." These duty ratio signals are then utilized to generate the gating signals for STI-1 and STI-2, using the LSPWM scheme, as explained in Section III-A. As the shoot-through state for the middle qZS is inserted using a switch (S_{19}), the dc-link voltage of the output inverter is regulated by controlling its duty-ratio "D_2"(see Fig. 7). Thus, the three peak dc-link voltages (V_{dc1}, V_{dc2}, and V_{dc3}) of the inverters are regulated using the closed-loop feedback control to obtain a regulated output voltage at the consumer end.

B. Grid-Connected Mode

The following objectives should be fulfilled by the FCMI for grid connectivity: 1) independent MPPT control for the three qZS networks; 2) voltage control of the dc-link; and 3) maintaining unity power factor (UPF) with the grid. As the proposed converter is operated with two control parameters, namely, the shoot-through duty ratio (D) and the modulation index (M), the first of these three objectives is achieved by the exclusive control of the shoot-through duty ratio "D," while the latter two objectives are realized by the exclusive control of "M."

Fig. 8 shows the block diagram to implement the grid control for the proposed converter. To extract the maximum power from the PV panels, the well-known perturb and observe algorithm is adopted. The respective voltages and currents of the three isolated PV sources are sensed and fed to the individual MPPT controllers to generate the required shoot-through duty ratio signals "D_1," "D_2," and "D_3." To track the maximum power from the top and bottom PV sources, the shoot-through duty ratios "D_1" and "D_3" (which are equal to "D" in steady-state conditions, as shown in Fig. 4) are fed to the LSPWM scheme to implement the shoot-through in STI-1 and STI-2, respectively. The shoot-through time period of the middle qZS network is controlled by an individual switch S_{19}. Consequently, the MPPT for PV-2 is implemented by controlling the duty ratio of switch "S_{19}."

To control the total dc-link voltage (V_{dctotal}) of the FCMI, every individual dc-link voltages "V_{dc1}," "V_{dc2}," and "V_{dc3}" are to be estimated. As in the case of standalone operation explained earlier, the total dc-link voltage (V_{dctotal}) is the sum of V_{dc1}, V_{dc2}, and V_{dc3}, which are estimated by sensing the capacitor voltages and duty ratios. The PI controller, which is present in the outer voltage loop, compares the actual dc-link voltage (V_{dctotal}) with its reference (V^*_{dctotal}) and outputs the d-axis reference current (i^*_d) to the inner current loop. However, the q-axis component (i^*_q) is set to zero to achieve a UPF. These current references (i^*_d, i^*_q) are compared with the actual d- and q-components of the grid currents (which are obtained by using Park's transformation to the measured

TABLE II
SIMULATION PARAMETERS

Parameters	Values
DC input voltage(V_{DC})	300 V
Inductors	3.3mH
Capacitors	500μF
Nominal output phase voltage	230V (RMS)
Load resistance	158 Ω
Load inductance	22.5mH
Power	1kW
Switching frequency	10kHz

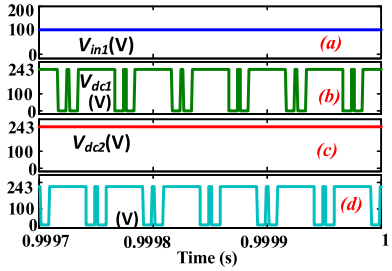

Fig. 9. Simulation results of (a) input voltage of single PV source (V_{in1}), (b) boosted dc-link voltage of STI-1 (V_{dc1}), (c) boosted dc-link voltage of output inverter (V_{dc2}), and (d) boosted dc-link voltage of STI-2 inverter (V_{dc3}).

three-phase currents) to generate the d- and q-axis references voltages (V_d^*, V_q^*) that determine the required modulation index [24].

From these d–q reference voltages (V_d^*, V_q^*), the actual modulating signals corresponding to the "ABC" phases are obtained with the help of the inverse-Park's transformation. The synchronization between the modulating signals and the grid is obtained by using a phase-locked loop (PLL). The LSPWM scheme is implemented (see Fig. 4) with these modulating signals to generate the required gating signals for the power semiconductor switching devices for the FCMI.

V. SIMULATION RESULTS

The proposed single-stage power converter is validated using MATLAB and Simulink. The parameters used in the simulation are shown in Table II.

Initially, all the input PV voltages are maintained at 100 V. In this case, the total input voltage (300 V) is not adequate to provide the necessary dc-link voltage for the inverter to output the desirable phase voltage of 230 V (rms).

As suggested by the theoretical analysis, a maximum shoot-through duty ratio (D) of 0.2 is inserted to provide the required boost to the dc-link voltage. A modulation index (M) of 0.78 is chosen to provide the necessary zero time and the output phase voltage of 230 V rms. As per (20), derived in the earlier section, the proposed control technique with a shoot-through duty ratio of 0.20 boosts the input voltages by a factor of 2.5.

Fig. 9 shows the input voltage [see Fig. 9(a)] and the three dc-link voltages corresponding to the STI-1, STI-2, and output inverter [see Fig. 9(b)–(d)]. It may be observed that both top and bottom dc-link voltages pulsate between the values of 0 and 243 V. Whenever shoot-through occurs in phase legs in the STI-1 and STI-2, the dc-link voltage of that inverter drops to zero. During the power transfer mode, a voltage of 243 V appears at the dc-links of these two inverters. In contrast,

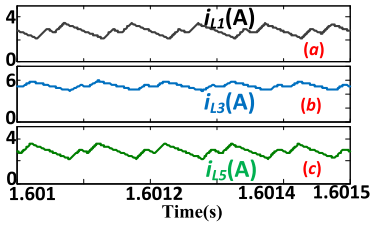

Fig. 10. Simulation results of (a) inductor current (i_{L1}), (b) inductor current (i_{L3}), and (c) inductor current (i_{L5}).

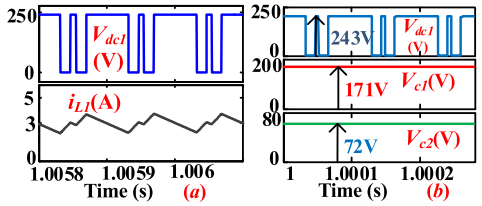

Fig. 11. Simulation results of (a) dc-link voltage (V_{dc1}) and inductor current (i_{L1}) and (b) dc-link voltage (V_{dc1}) and capacitor voltages V_{c1} and V_{c2}.

a constant voltage of 243 V is maintained at the dc input of the output inverter as it is fed from the capacitor C_7 of the middle qZS network. It may be noted that these results are in close agreement with the theoretical analysis presented in Section III-C, which calculates these dc-link voltages to be equal to 250 V [i.e. with a boost factor of 2.5, (20)].

The inductor currents of the top, middle, and bottom qZSs are demonstrated in Fig. 10 in the same order. It may be observed that the average values of the top and bottom qZS show the same average value (approx. 3 A), as the shoot-through duty ratio is equally distributed to the STI-1 and STI-2, while the inductor current of the middle qZS shows a higher current (approx. 5 A).

Fig. 11(a) presents the steady-state waveforms of dc-link voltage (top) and input inductor current (bottom) for the top-qZS. From these plots, it may be observed that the inductor current increases during the shoot-through state and falls during the nonshoot-through state. One of the advantages of the qZS compared to its traditional counterpart is the reduced voltage stress on the capacitors. This is demonstrated in Fig. 11(b), wherein the voltages across the capacitors C_1 and C_3 belonging to the top qZS are demonstrated along with the peak dc-link voltage of the STI-1. The theoretical analysis stipulates these voltages to be in the ratio of (1-3D/2): 3D/2. When $D = 0.2$, this ratio works out to be 7:3. Thus, when the theoretical peak dc-link voltage is 250 V (for an input dc voltage of 100 V), the ratio of these two voltages should be 175:75 V. The simulated voltages across the capacitors C_1 and C_3 are 172 and 72 V, respectively, which are in close agreement to the theoretical results [see Fig. 11(b)]. This feature offers designers to use capacitors of lower voltage ratings in qZS converters compared to its traditional counterpart.

Fig. 12 presents the pole voltage (top trace), the phase voltage (second trace), the line voltage (the third trace), and the phase current (bottom trace) of the FCMI. From the pole voltage waveform, the four-level operation is evident, as it displays four distinct voltage levels at 0, 243, 486, and 729 V.

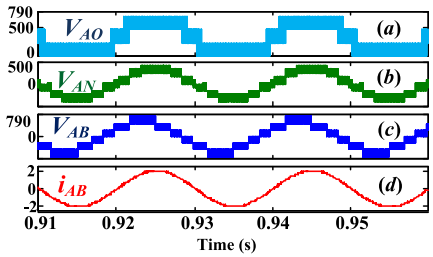

Fig. 12. Simulation results of (a) pole voltage (V_{AO}), (b) phase voltage (V_{AN}), (c) line voltage (V_{AB}), and (d) phase current (i_{AB}) waveforms for FCMI.

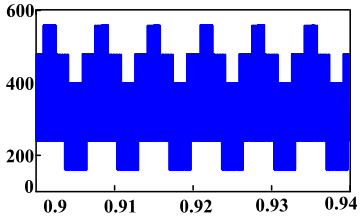

Fig. 13. Simulation results of common-mode voltage waveforms for FCMI.

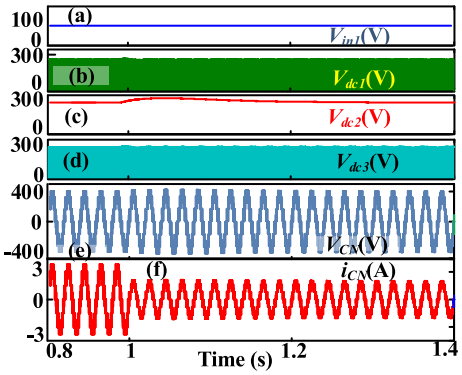

Fig. 14. Simulation results of (a) input voltage (V_{in1}) and dc-link voltages (b) V_{dc1}, (c) V_{dc2}, and (d) V_{dc3} of FCMI during load variation, (e) phase voltage, and (f) phase current of FCMI during load variation.

The phase voltages are computed using (21), which appears as nine-level stepped waveforms ranging from −500 to +500 V. As the total dc-link voltage of the FCMI is 729 V, the output line voltage, which shows a seven-level stepped waveform, ranges from −729 to +729 V. The current is almost sinusoidal with small harmonic distortion due to the presence of adequate load inductance.

Fig. 13 shows the common-mode voltage of the FCMI. As the FCMI is operated with a modulation index of $M = 0.77$, the space vector rotates in the outer hexagon, as shown in Fig. 3. This results in the generation of four levels in the pole voltage waveforms V_{AO}, V_{BO}, and V_{CO}, which leads to the CMV ranging from $(2/9)(B.V_{dc})$ to $(7/9)(B.V_{dc})$, where V_{dc} is the input voltage and B is the boost factor.

In order to verify the voltage regulation of the dc-links, all the three input PV voltages are maintained at 100 V initially. The load current is then suddenly decreased by about 50% by increasing the load resistance. Fig. 14(a) shows the input voltage and the three dc-link voltages [see Fig. 14(b)–(d)] of the FCMI. It may be observed that, following the load disturbance, there is a small increase in dc-link voltage suggesting a decrease in the load. To maintain the dc-link voltage, the shoot-through duty ratio (D) is automatically adjusted by the PI controllers shown in Fig. 7. The phase voltage and phase current of the FCMI are shown in Fig. 14(e) and (f). It may be observed that, at $t = 1$ s, the output phase voltage is maintained constant despite a sudden change in load.

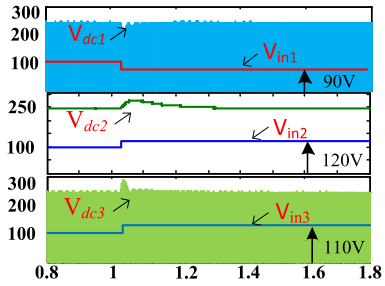

Fig. 15. Simulation results of input voltages (V_{in1}, V_{in2}, and V_{in3}) and dc-link voltages (V_{dc1}, V_{dc2}, and V_{dc3}) for source variation.

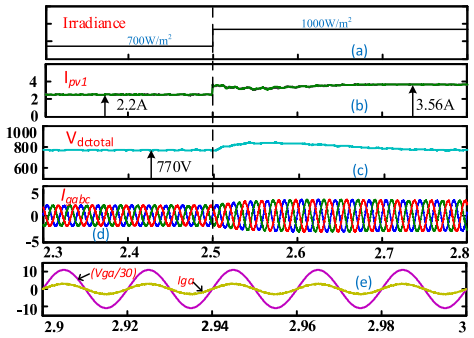

Fig. 16. Simulation results of (a) step change in irradiance and (b) PV current (I_{PV1}). (c) Total dc-link voltage ($V_{dctotal}$). (d) Grid currents (I_{gabc}). (e) Grid voltage (V_{ga}) and grid current (I_{ga}).

In PV generation, temperature variations lead to different PV output voltages. In order to assess the effectiveness of the dc-link regulation, such perturbations are imposed on the input voltages of the qZS networks. Initially, all the three input voltages of the qZS networks are maintained at 100 V, and then, the input voltages are changed to 90, 120, and 110 V, respectively, for the top, middle, and bottom sources. From the results presented in Fig. 15, it may be noted that the dc-link voltages are effectively regulated even when inequalities exist in the input voltages. The methodology adopted to synchronize the proposed power converter with the grid is also verified using simulation studies.

It may be noted from Fig. 16 that, when a step change of irradiation is applied (from 700 to 1000 W/m^2 at 2.5 s), the proposed MPPT control method adjusts the shoot-through duty ratios ("D_1," "D_2," and "D_3," Fig. 8), until the maximum power point (MPP) is attained. Fig. 16(c) clearly illustrates the regulation of the dc-link voltage. The increase in the insolation level manifests as the increased injection of power into the grid at UPF, as is evident from Fig. 16(d) and (e).

VI. Experimental Results

A scaled-down experimental prototype of the proposed power converter has been developed to validate the simulation results (see Fig. 17).

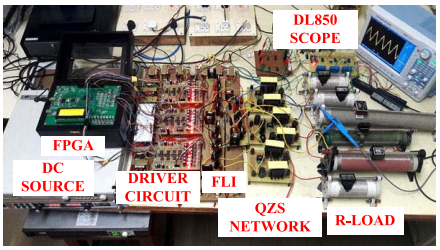

Fig. 17. Experimental hardware prototype.

TABLE III
HARDWARE PROTOTYPE PARAMETERS

Parameters	Values
DC input voltage(V_{DC})	210V
Total boosted DC-link voltage	420 V
Rated power	870W
Nominal output phase voltage	135V (RMS)/50Hz
Switching frequency	10kHz
Modulation Index (M)	0.77
Inductors	3mH, EE65 CORE
Electrolytic Capacitors	400μF,300V
Fast recovery diode	MUR1560CT

The details regarding the hardware components and the operating parameters are summarized in Table III. Three programmable dc sources with CV–CC characteristics are employed to emulate the PV supply. The dc-link voltage control of the proposed power converter is implemented with an FPGA platform.

The proposed modulation technique has been implemented using the Xilinx block-set available with the MATLAB and Simulink environment. The code is deployed to the Spartan-6 FPGA module. The DL850E Yokogawa power oscilloscope is used for capturing the hardware results.

The top trace of Fig. 18 shows the input voltage (V_{in1}) applied to all three qZS networks, each of which is equal to 70 V. The qZS inputs are operated with a shoot-through duty ratio of 0.166 as in the case of simulation discussed in the previous section. It may be observed that the dc-link voltages (V_{dc1}, V_{dc2}, and V_{dc3}) of all three inverters are boosted to 140 V. Thus, the boost factor of 2 is obtained with experimentation, which is in agreement with the analytical and simulation results (see (20) and Fig. 9). From Fig. 18, it is also evident that the dc-link voltages of STI-1 and STI-2 pulsate between the levels of 0 and 140 V as the shoot-through time period is inserted in each phase leg of these inverters. In contrast, the dc-link voltage of the output inverter is regulated at a constant voltage of 140 V by the qZSI network and capacitor C_7.

The benefit obtained with the qZS in terms of the alleviation of voltage stresses across the capacitors is demonstrated in the experimental result presented in Fig. 19(a). With an input dc voltage of 70 V (top trace) and a shoot-through duty factor (D) of 0.166, a pulsating dc-link voltage of 140 V is obtained (second trace). The voltage of the dc-link (140 V) is distributed in the ratio of 1-3D/2: 3D/2 in capacitors C_1 and C_2. The lower two traces of Fig. 19(a), which present these voltages, verify these results experimentally, as the voltages across these two capacitors are 105 and 35 V, respectively.

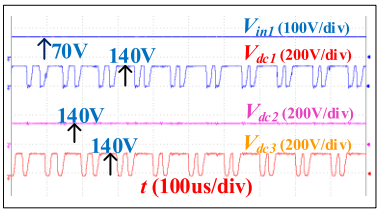

Fig. 18. Experimental results of input voltage (V_{in1}) and dc-link voltages (V_{dc1}, V_{dc2}, and V_{dc3}) of FCMI.

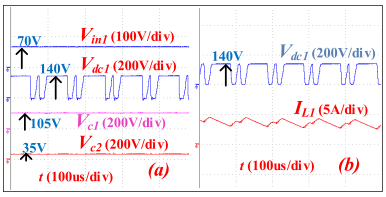

Fig. 19. Experimental results of (a) input voltage (V_{in1}), dc-link voltage (V_{dc1}), and capacitor voltages (V_{c1}, V_{c2}) of top qZS network and (b) dc-link voltage (V_{dc1}) and inductor current (I_{L1}).

Fig. 19(b) shows the dc-link voltage (V_{dc1}) and inductor current (i_{L1}) of the qZS network. It may be noted that an average current of 3.75 A flows through the qZS inductors. These experimental waveforms clearly show the effect of the shoot-through time period on these inductor currents, as they increase linearly during these time periods. During the nonshoot-through states, these currents decrease linearly. It should be noted that this experimental result is also in agreement with the simulation presented in Fig. 11.

The output of the back-end four-level inverter is presented in Fig. 20 when the modulation index (M) is set to a value of 0.77, as indicated in Table I. The pole voltage of the A-phase (V_{BO} in Fig. 20), presented as the top trace, displays four distinct levels ranging from 0 to 420 V in steps of 140 V. The line and phase voltages (V_{BN} and V_{BC} in Fig. 20) are presented in the middle and bottom traces in this figure respectively. The comparison of these waveforms is in agreement with their simulated counterparts, as presented in Fig. 12.

Fig. 21 shows the harmonic spectrum of the output phase voltage and the phase current, wherein the rms value of the fundamental component is 135 V (rms) and 2.19 A. The fundamental output voltage is in agreement with the theoretical value calculated on the basis of the overall gain of the proposed converter, which is given by the product of the modulation index (M) and the boost factor (B) derived in (21). For an input voltage of 70 V, a modulation index (M) of 0.77, and a shoot-through duty factor (D) of 0.166, the theoretical value of the output phase voltage would be 135 V (rms). Thus, the practically obtained phase voltage is concurrent with the theoretically obtained value.

Fig. 22 shows the effectiveness of the closed-loop control scheme (as shown in Fig. 7) for the proposed power converter against the load disturbance while operating in the stand-alone mode. The top three traces of Fig. 22(a) show the dc-links voltages (V_{dc1}, V_{dc2}, and V_{dc3}). The bottom trace of this figure shows the voltage and current in one of the load phases. To study the effect of the load disturbance, the load current is suddenly doubled (from 0.67 to 1.35 A) and, then, after a while, is restored to the predisturbance value.

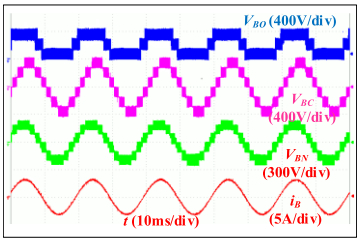

Fig. 20. Experimental results of pole voltage waveform (V_{BO}), line voltage (V_{BC}), phase voltage (V_{BN}), and phase current (i_B) of FCMI.

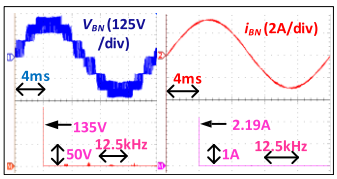

Fig. 21. Harmonic spectrum of the output phase voltage (V_{BN}) and phase current (i_{BN}).

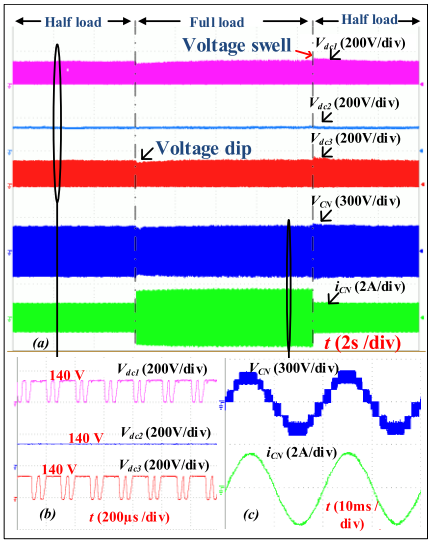

Fig. 22. Experimental results. (a) DC-link voltage waveforms of qZS-FCMI and the load voltage and current in phase C. (b) Zoomed-in view of the dc-link voltages. (c) Zoomed-in view of the load voltage and current in phase C.

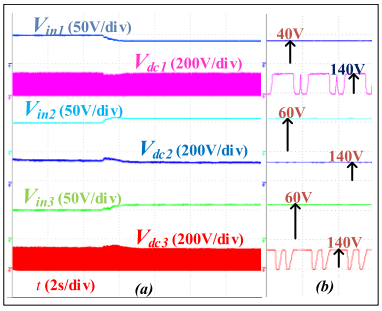

Fig. 23. Experimental results. (a) DC-link voltages and input voltage waveforms of FCMI during source disturbance. (b) Zoomed-in view of the dc-link voltages of the FCMI.

Fig. 22(b) and (c) displays the zoomed pictures of the dc-link voltage, the output phase voltage, and the output phase current. From Fig. 22(a), it is evident from Fig. 22(a) that sudden changes in the load current disturb the dc-link voltages momentarily, and the closed-loop controller effectively regulates the dc-links against the load disturbances.

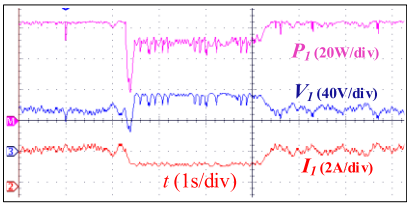

Fig. 24. Experimental results of MPPT control of PV-1.

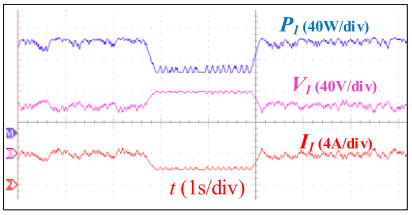

Fig. 25. Experimental results of MPPT control of PV-2.

Fig. 23 demonstrates the regulation of the dc-link voltages against the supply disturbance with the closed-loop controller. In this experiment, all three dc inputs [V_{in1}, V_{in2}, and V_{in3}, Fig. 23(a)] are initialized to 50 V. Then, each input is disturbed by about 25%. First, the input voltage V_{in1} is decreased by 10 V, and then, the other two input voltages are increased by 10 V. It may be noted that the corresponding dc-link voltages, which are displayed below their respective input voltages, show momentary changes; they are quickly regulated by the closed-loop action of the controller. As in the case of the load disturbance, the controller automatically adjusts the respective shoot-through duty ratios to regulate the dc-link voltages.

To evaluate the dynamic performance of the MPPT controller of the qZS converters, programmable dc sources are used to emulate the P_{PV} versus V_{PV} characteristics of the PV panels [29], [30]. The programmable dc sources are operated in the constant voltage mode with variable current limits. Figs. 24 and 25 show the experimental validation of MPPT control for the top and middle PV sources. The top traces in Figs. 24 and 25 show the power, while the middle and bottom traces, respectively, show the voltage and the current of the PV source.

To verify the dynamics of MPPT, the source current limit is first decreased and is then restored back to its predisturbance value to emulate varying irradiation, as shown in Figs. 24 and 25. When the change in irradiation is detected by the respective MPPT controllers, they immediately control the shoot-through duty ratio, thereby extracting the maximum power from the PV sources. Figs. 24 and 25 clearly demonstrate the tracking capability of the MPPT controllers corresponding to the top and middle PV sources. The MPPT algorithms for both of the sources are run at a sampling frequency of 1 kHz. Due to the fact that, in the day-to-day experience, the change in irradiation is a slow phenomenon; it is evident that the dynamic response of the MPPT controller is satisfactory for the bandwidth corresponding to the chosen sampling frequency.

Fig. 26 shows the real-time simulation results, pertaining to the synchronization of the proposed converter with the

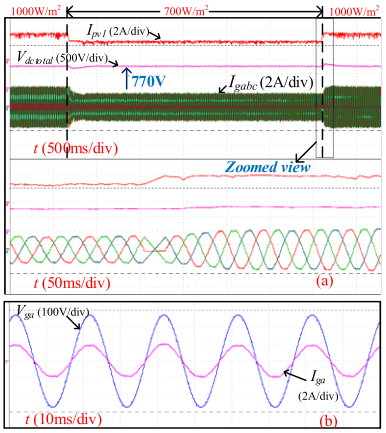

Fig. 26. Experimental results. (a) PV current (I_{pv1}), total dc-link voltage (V_{dctotal}), and grid currents (I_{gabc}). (b) Grid voltage and grid current.

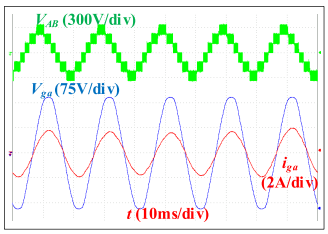

Fig. 27. Experimental result of inverter line voltage (V_{AB}) and grid voltage (V_{ga}) and grid current (i_{ga}) waveforms.

grid. These simulations are carried out using the OPAL-RT simulator (OP4500) [25]. OP4500 is equipped with a high-end Intel multicore processor, Xilinx kintex 7 FPGA with analog and digital channels. Thus, the RT-Lab environment enables parallel processing and provides real-time simulation results, which are often considered equivalent to the experimental results obtained with a hardware prototype [26].

From Fig. 26, it is evident that, when the insolation level is suddenly decreased and then increased (from 1000 to 700 W/m^2 and vice versa), the PV current also changes correspondingly (from 3.5 to 2.1 A, as shown in the top trace). It may be noted that the dc-link voltage is regulated at 770 V (middle trace) despite a change in insolation, as explained in the previous section (see Fig. 8). Also, the three-phase currents injected into the grid undergo a corresponding variation (bottom trace) depending on the maximum power extracted from the PV sources using the MPPT algorithm explained earlier. Fig. 26(b) shows the grid voltage (V_{ga}) and grid current (I_{ga}) of phase-A. The effectiveness of the proposed control method is evident as the converter injects active power into the grid at UPF. Fig. 27 demonstrates the capability of the proposed power converter to inject power into the grid in the grid-tied mode of operation.

The qZS-FLI injects a current (per-phase) of 1.34 A (rms) at UPF, while the grid voltage (per-phase) is maintained at 115 V (rms). The inverter line to line voltage (V_{AB}) is also shown in Fig. 27 to validate the operation of the proposed qZS-FLI during the grid connection mode.

To summarize, the experimental results are concurrent with the simulation results and serve as the proof of concept to the proposed power converter and its control scheme.

VII. Comparison With the Proposed qZS FCMI

To show the advantages of the proposed topology, comparative analyses have been carried out, which are summarized in Table IV.

As there are no impedance-source-based four-level topologies available in the literature, all the recent three-level topologies along with a seven-level topology are considered for comparison. Table IV presents the number of active and passive components and compares the voltage stress, boost factor, gain, and inductor current ripple for these converters.

The proposed converter produces a higher number of voltage levels compared to all the topologies except qZS-CHB [20]. Except for the topologies described in [14] and [32], the proposed FLI uses equal or lesser number of power diodes. As the number of voltage levels (N_L) is not identical across the compared topologies, the number of switches (N_{sw}) and the total standing voltage (TSV) (the sum of blocking voltages of all the switches and diodes with respect to the peak voltage value) are calculated [34]. The ratio (N_{sw}/N_L) is a figure of merit, which quantifies the switching resources required per voltage level. In this aspect, the proposed topology works out to be better than the one described in [20] and almost equivalent to the topologies described in [31]–[33]. Similarly, the ratio (TSV/N_L) is another holistic figure of merit, which quantifies the specific blocking voltage of any given topology. The proposed topology registers a lower (TSV/N_L) ratio compared to the other MLI topologies. This signifies that, even though the switch count is higher in the proposed converter, the blocking voltages are lower compared to other MLI configurations. As seen from Table IV, the boost factor and the gain of the proposed power converter are dependent on the shoot-through duty ratio and vary exponentially with D. When $D > 0.25$, the proposed MLI displays a higher boosting factor and gain compared to all other topologies. For $D < 0.25$, the proposed MLI shows a better boosting factor and gain than all other topologies except [33].

For all the seven power converters, voltage stresses across the devices and the passive elements are calculated based on the *per-unit* basis, with V_{dc} (the total dc-input voltage) as the base value. All the topologies are evaluated for a total input voltage of 300-V dc from the PV source so that the desired phase voltage of 230 V (rms) is output by them. The proposed topology results in lesser voltage stress across the switches, capacitors, and diodes except [20], as all the three-level topologies require a higher boost factor to derive the required output voltage of 230 V/Ph (rms) for the input of 300-V dc. Assuming identical values for switching frequency, duty ratio, and inductors, the value of the ripple current in the inductors is minimum for the proposed topology compared to the topologies reported in [10], [14], [31], and [33], which results in lesser size of the inductor. From the above comparison, it is evident that, despite the higher number of components, the proposed four-level inverter results in lower voltage stress on the switches, diodes, and capacitors, which leads to the lower ratings of the devices compared to the three-level topologies. The proposed FCMI shows a better boost factor compared to all other topologies

TABLE IV
COMPARISON OF DIFFERENT IMPEDANCE TOPOLOGIES WITH THE PROPOSED TOPOLOGY

	ZS-NPC[10]	qZS-CHB [20]	LC-NPC[31]	qZS-3LT[14]	qSB-3LT[32]	AI-3LT[33]	Proposed
Levels(N_L)	Three	Seven	Three	Three	Three	Three	Four
Sources	2	9	2	1	1	1	3
Capacitors	4	18	2	4	2	2	7
Inductors	4	18	2	4	1	1	6
N_{SW}/N_L	4	5.1	4.66	4	4.66	4.33	4.75
Diodes	8	9	8	2	4	2	4
TSV/N_L	3.32	2.16	4	3.33	3	2.5	1.91
Boost	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)}$	$\frac{2}{(1-2D)}$	$\frac{1}{(1-3D)}$
Gain	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{M}{(2M-1)}$	$\frac{2M}{(2M-1)}$	$\frac{M}{(3M-2)}$
Switch voltage stress	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)3}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)2}$, $\frac{1}{(1-2D)}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-3D)3}$
Capacitor voltage stress	$\frac{(1-D)}{(1-2D)2}$	$\frac{(1-D)}{(1-2D)3}$ for C_1 $\frac{(D)}{(1-2D)3}$ for C_2	$\frac{1}{(1-2D)2}$	$\frac{(1-D)}{(1-2D)2}$ for C_2,C_3 $\frac{(D)}{(1-2D)2}$ for C_1,C_4	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)}$	$\frac{(1-3D/2)}{(1-3D)3}$ for C_1 $\frac{(3D/2)}{(1-3D)3}$ for C_2
Diode voltage stress	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)3}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)2}$	$\frac{1}{(1-2D)}$	$\frac{1}{(1-3D)3}$
Inductor current ripple	$\frac{(1-D)DT}{(1-2D)2L}$	$\frac{(1-D)DT}{(1-2D)3L}$	$\frac{(1-D)DT}{(1-2D)L}$	$\frac{(1-D)DT}{(1-2D)2L}$	$\frac{DT}{2L}$	$\frac{2D(1-D)T}{(1-2D)L}$	$\frac{(1-D)DT}{(1-2D)3L}$

for higher duty ratios. Also, the inductors have a lower current ripple, which leads to a lower value of inductors

VIII. POWER LOSS ANALYSIS FOR THE PROPOSED QZS-FCMI

In this section, the power losses incurred in the power semiconductor devices and the passive components are assessed for the proposed configuration. In order to evaluate these power losses, the proposed configuration is simulated with the thermal models of the semiconductor devices for a power output of 1 kW in the Piecewise Linear Electrical Circuit Simulation (PLECS) software. A reference power model of insulated gate bipolar transistor (IGBT) along with a body diode (*IKW30N60T*) is considered for simulation. The following power loss components are considered while analyzing the converter loss: 1) switching and conduction losses in the IGBTs (denoted by P_{SW} and P_{CON}); 2) diode switching and conduction losses (denoted by P_{SD} and P_{CD}); 3) inductor conduction loss (P_{ind}); and 4) capacitor equivalent series resistor (ESR) loss (P_{cap}). Apart from these losses, the conduction losses in the inductors and the ESR losses in the capacitors are calculated based on the equivalent parasitic resistance [27]. These losses have been evaluated at $M = 0.77$, $D = 0.2$, $V_{in1} = V_{in2} = V_{in3} = 100$ V, $V_{dc1} = 243$ V, fs = 10 kHz, $Po = 1$ kW, $PF = 1$, and Vo (ph-rms) = 230 V. The summary of the losses is presented in Fig. 28.

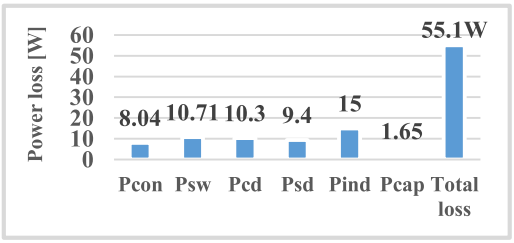

Fig. 28. Loss distribution in the device for qZS-FCMI.

Such data are generated for various values of the output power ranging from 0.5 to 2.5 kW for the input voltages of 100 and 120 V. The data so generated are plotted in Fig. 29. These data suggest that the efficiency curve is practically flat with average efficiencies of 93% and 94%, respectively, for the aforementioned values of the input voltages.

These data suggest that the efficiency curve is practically flat with average efficiencies of 93% and 94%, respectively, for the aforementioned values of the input voltages. These data further suggest that the efficiency of the proposed power converter increases as the input voltages increase. This is because an increased input voltage results in a decrease in the boosting factors, leading to the reduction of the power loss. It may be observed from Fig. 29 that, at 120-V dc input voltage, we require a shoot-through duty ratio of 0.17 to achieve desired output voltage of (230 V). This requires a lower voltage boosting, which helps in the reduction of the inductor losses, thereby increasing the efficiency, compared to the lower input voltage of 100 V. To validate the hardware efficiency of the prototype, a precision digital power meter (Yokogawa WT332E) is used to measure the input power of the proposed qZS-FLI, and a power analyzer (UNI-T UT283A) is used to measure the output power.

IX. POWER LOSS ANALYSIS FOR THE PROPOSED QZS-FCMI

In this section, the power losses incurred in the power semiconductor devices and the passive components are assessed for the proposed configuration. In order to evaluate these power losses, the proposed configuration is simulated with the thermal models of the semiconductor devices for a power output of 1 kW in the PLECS software. A reference power

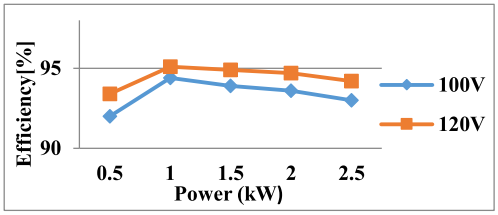

Fig. 29. Calculated efficiency of the proposed qZSI-FLI for two different input voltages.

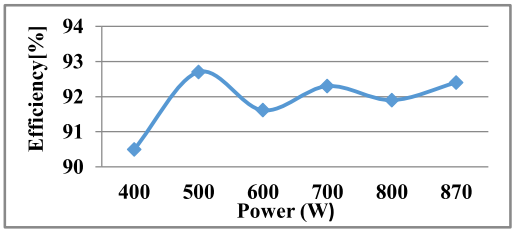

Fig. 30. Experimental efficiency of the proposed qZSI-FLI.

model of IGBT along with a body diode (*IKW30N60T*) is considered for simulation. The following power loss components are considered while analyzing the converter loss: 1) switching and conduction losses in the IGBTs (denoted by P_{SW} and P_{CON}); 2) diode switching and conduction losses (denoted by P_{SD} and P_{CD}); 3) inductor conduction loss (P_{ind}); and 4) capacitor ESR loss (P_{cap}). Apart from these losses, the conduction losses in the inductors and the ESR losses in the capacitors are calculated based on the equivalent parasitic resistance [27]. These losses have been evaluated at $M = 0.77$, $D = 0.2$, $V_{in1} = V_{in2} = V_{in3} = 100$ V, $V_{dc1} = 243$ V, fs $=$ 10 kHz, $Po = 1$ kW, $PF = 1$, and Vo (ph-rms) $= 230$ V. The summary of the losses is presented in Fig. 28.

The experiment is conducted for a step change of 100 W ranging from 400 to 870 W. Fig. 30 shows the experimental efficiency curve of the qZS-FLI. From the above plot, it may be noted that the average experimental efficiency of the prototype hovers around 92%. It may be observed that the experimental efficiency is in close approximation to the simulated efficiency (as shown in Fig. 29), which is around 93%–94%.

X. Conclusion

This article reports the research work carried out in the area of *single-stage* solar PV power conversion systems with three-phase output for stand-alone and grid-connected applications. Single-stage power conversion is obtained by the amalgamation of two mutually interdependent subsystems, namely, the front-end qZS networks and the back-end FCMI. It is shown that the LSPWM technique renders a 50% higher boost factor compared to the power circuit configurations reported in the earlier literature. Also, this power circuit configuration is structurally simpler and requires fewer components compared to the NPC- or CHB-based systems. The steady-state and dynamic behaviors of the proposed power converter in the stand-alone mode have been assessed with off-line simulation studies and then followed up with experimental validation. Simulation studies and the experimental results indicate that the dc-links of the proposed power converter are regulated simply by the adjustment of the shoot-through duty factor. This feature makes the proposed power converter suitable for stand-alone applications. The performance of the proposed power converter in the grid-connected mode is evaluated with the aid of real-time simulations. It is shown that it is possible to implement the MPPT by varying the shoot-through duty factor, while the output of the FCMI is controlled by varying the modulation index. It is also shown that the proposed power converter, with the aid of a PLL, is capable of injecting the active power into the grid at UPF. The power loss analysis, carried out with simulation studies, reveals that the proposed converter is capable of rendering efficiency of 94%.

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