Novel Single-Phase Packed U-Cell based Symmetrical Multilevel Inverters

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***Abstract* — This paper presents a packed U-Cell based symmetrical multilevel inverters for grid-connected Photovoltaic (PV) systems. The proposed MLI can raise the number of levels in the output voltage with reduced power electronic devices compared with the popular MLI structures. The level-shifted sinusoidal pulse width modulation technique is employed to generate the triggering pulses. In addition, the proposed MLI has the ability to operate during the non-unity power factor conditions without any limitations. Furthermore, the proposed topologies are tested for 9-Level generation under different loading conditions. Moreover, a comparison with the modern MLI topologies is presented in terms of device count to show the merits of the proposed MLI. MATLAB/Simulink toolbox is used to validate the performance of the proposed MLI under different loading conditions.**

Keywords — Symmetrical multilevel Inverter, Reduced switch count, Single-phase, Level shifted pulse width modulation scheme, Distributed power generation.

I. INTRODUCTION

Single-phase multilevel inverters (MLIs) have received more attraction in renewable energy systems such as photovoltaic, fuel cell and wind energy conversion systems because of their advantages as follows: (i) reduced switching losses with low dv/dt stress, (ii) high-quality output waveforms with low harmonic content (iii) reduced filter size and cost, and (iv) improved efficiency [1] – [3]. However, all these merits are attained by compromising the total number of active and passive components, such as DC sources, switches, diodes, and capacitors. Therefore, proposing novel MLIs that can enhance the number of levels with low component count is the one of the interesting research objectives in this area [4].

A detailed review, classification, and description of different MLI topologies are presented in the references [5]-[7]. The popular MLI configurations are neutral-point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) inverters as depicted in Fig. 1, and these topologies are widely named as 'classical MLI topologies'. The limitations of these classical MLIs are more device count, DC voltage balancing issues and control complexity for an increased number of levels. To alleviate afore-said drawbacks, a significant amount of MLI topologies are proposed based on the classical structures. Among those, CHB based topologies have attracted more attention due to their modularity and simplicity in control [8].

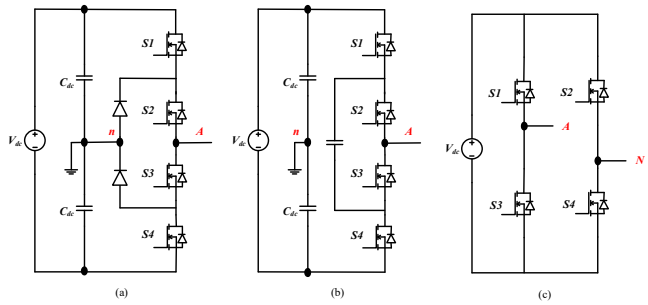

Fig. 1. Classical MLI topologies: (a) NPC, (b) FC, and (c) CHB

In ref [9], a T-type symmetrical multilevel inverter (T-SMLI) is derived based on the CHB structure (in Fig. 2(a)) to overcome the voltage balancing issues as seen in NPC and FC topologies. But, the reduction in the component count is not achieved with this topology. To reduce the component count, a transistor clamped symmetrical multilevel inverter (TC-SMLI) is proposed in Ref [10], and it is depicted in Fig. 2(b). One switch and four diodes form a transistor clamped circuit to increase the output levels. Unfortunately, the total number of diodes required for realizing the multilevel operation is more and it limits the application of this topology in real-time. Another interesting switched transistor symmetrical multilevel inverter (ST-SMLI) is proposed in ref [11] – [12], and it is drawn in Fig. 2(c). The total number of devices are significantly reduced in ST-SMLI compared to the references [9], [10]. CHB module operates at a lower switching frequency and generates the polarity (i.e either positive, negative and zero) in both TC-SMLI and ST-SMLI topologies. However, the total components required to obtain the same number of levels in one complete cycle are more and it results in increased device conduction and switching losses of the inverters presented in the above references.

Therefore, to overcome the afore-said limitations, the authors proposed a novel 9-level packed U-cell based switched bi-directional mosfet (SBM-PUC) and switched mosfet (SM-PUC) SMLI topologies in this paper. The proposed topologies realize the same number of output levels with fewer devices in the current path when compared with topologies presented in the literature. Furthermore, the quality of output waveforms is ensured without limitation on the power factor of the load/grid. Therefore, the proposed topologies will be cost-efficient, more compact, light weight and higher efficiency.

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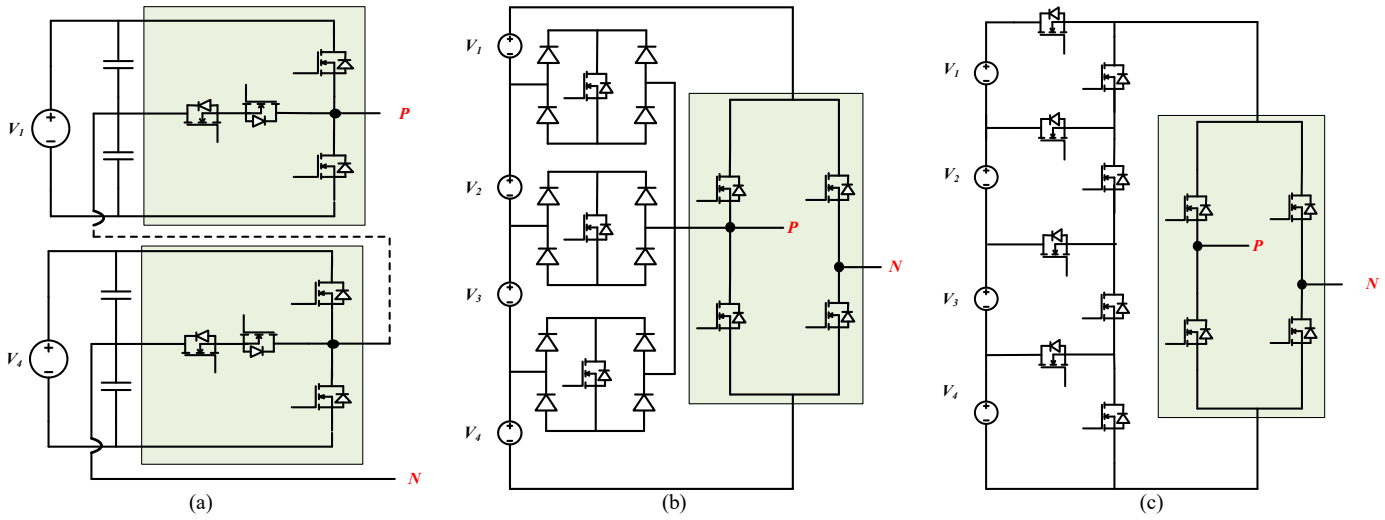

Fig. 2. SMLI topologies (a) T-Type MLI [9], (b) TC-MLI [10], (3) ST-MLI [11]

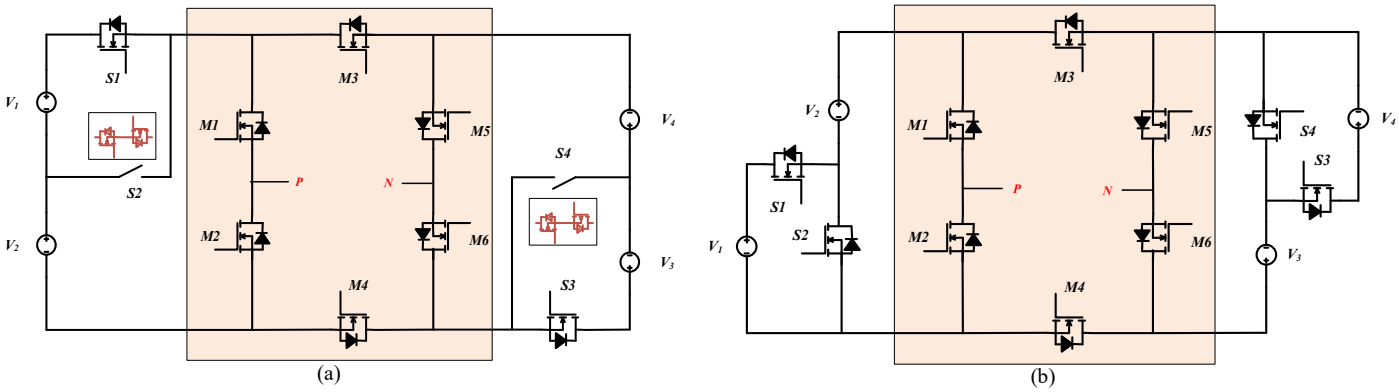

Fig. 3. Proposed (a) SBM – PUC SMLI, (b) SM - PUC SMLI

II. Proposed SMLI Topologies

In this section, the proposed SMLIs, operating states and pulse generation along with the calculation of total blocking voltage will be discussed. In both the topologies, the DC sources connected on left half side of the PUC will be opposite to the DC sources connected on right half side. The multilevel output will be produced by adding all voltages of the four DC sources in various permutations at a time which is selected by different switches.

A. Circuit Configurations

Circuit configurations of the proposed SBM – PUC SMLI and SM – PUC SMLI are illustrated in Figs. 3(a) and 3(b) respectively. It comprises level generating and polarity generating units. In both the topologies, PUC will generate polarity, i.e., either positive, negative and zero by switching the mosfets *M1* to *M6*. Operation of the mosfets *M1*, *M3*, and *M5* are complementary to the mosfets *M2, M4,* and *M6* respectively. Based on the requirement of voltage level the other switches, namely *S1, S2, S3* and *S4* will be turn – on or off. In the following subsection, the operating states of the inverter are explained in detail in both positive and negative current directions for the same voltage level.

TABLE I. Switching Table with respect to Voltage level

Voltage level	*S1*	*S2*	*M1*	*M2*	*M3*	*M4*	*M5*	*M6*	*S3*	*S4*
4V	1	0	1	0	0	1	1	0	1	0
3V	1	0	1	0	0	1	1	0	0	1
2V	1	0	1	0	0	1	0	1	0	0
V	0	1	1	0	0	1	0	1	0	0
0	0	0	1	0	1	0	1	0	0	0
-V	0	1	0	1	1	0	1	0	0	0
-2V	1	0	0	1	1	0	1	0	0	0
-3V	1	0	0	1	1	0	0	1	0	1
-4V	1	0	0	1	1	0	0	1	1	0

B. Operating states of the proposed SMLI topologies

The operating states of the proposed inverters are explained in nine switching states. As stated earlier in this paper, except the PUC unit generates four states of the output voltage and they are further extended to nine states by using the PUC structure.

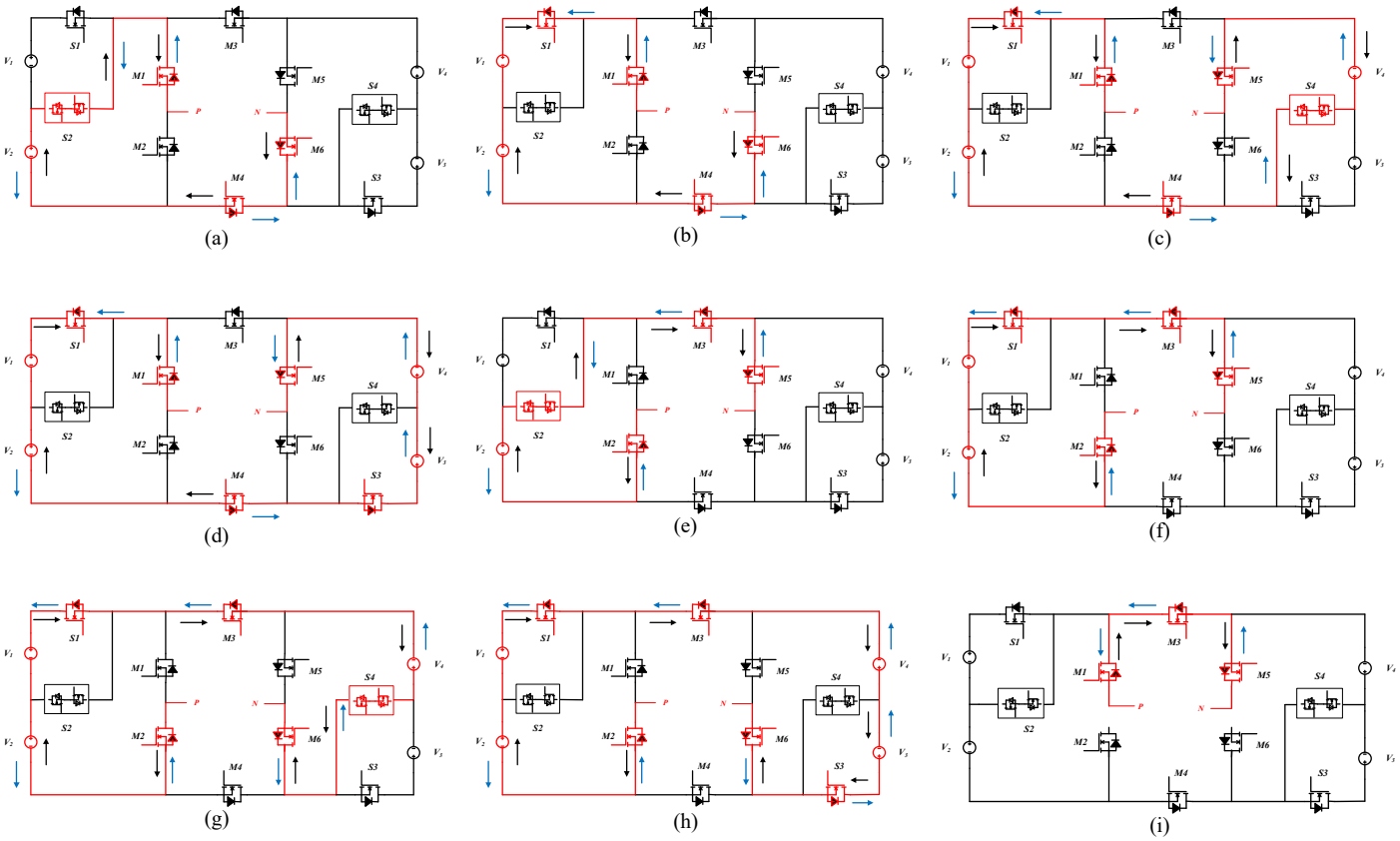

Fig. 4. Operating states of the proposed SBM – PUC SMLI, (a) $V_{PN} = V$, (b) $V_{PN} = 2V$, (c) $V_{PN} = 3V$, (d) $V_{PN} = 4V$, (e) $V_{PN} = -V$, (f) $V_{PN} = -2V$, (g) $V_{PN} = -3V$, (h) $V_{PN} = -4V$ and (i) $V_{PN} = 0$

Moreover, operating states, switching tables and PWM schemes are the same for both the topologies. Also, it is very easy to analyze the operation of other topologies. Thus, in this paper, only SBM – PUC SMLI operation is explained in detail. All the source voltages are assumed to be equal in magnitude (i.e., *V1 = V2 = V3 = V4 = V*) and also the terminals P and N are connected with RL load (V_{PN}).

1) State I: In this state, $V_{PN} = V$, the switches *S2, M1, M4* and *M6* are tuned on and the remaining are turned off as shown in Fig. 4(a). The bi-directional current path from source to load and vice-versa is also shown in Fig. 4(a) with black and blue arrows respectively.

2) State II: The equivalent circuit corresponds to this state is illustrated in Fig. 4(b) in which the switches *S1, M1, M4* and *M6* are turned on and the remaining are turned off to obtain $V_{PN} = 2V$ and the current flows from source to load. Body diodes of the switches *S1, M1, M4* and switch *M6* will provide reverse current path from load to source for the same voltage level during non-unity power factor operation.

3) State III: In this state, $V_{PN} = 3V$, the switches *S1, M1, M4, M5* and *S4* are tuned on and the remaining are turned off as shown in Fig. 4(c). The bi-directional current path from source to load and vice-versa is also shown in Fig. 4(a) with black and blue arrows respectively.

4) State IV: This state corresponds top level i.e., $V_{PN} = 4V$ in which all the DC sources are added by switching on the mosfets *S1, M1, M4, M5* and *S3*. The bi-directional current path from source load and vice-versa is shown in Fig. 4(d).

5) State V: In this state, $V_{PN} = -V$, the switches *S2, M2, M3* and *M5* are tuned on and the remaining are turned off as shown in Fig. 4(e). The bi-directional current path from source to load and vice-versa is also shown in Fig. 4(e) with black and blue arrows respectively.

6) State VI: The equivalent circuit corresponds to this state is illustrated in Fig. 4(f), in which the switches *S1, M2, M3* and *M5* are turned on and the remaining are turned off to obtain $V_{PN} = -2V$ and the current flows from the source to load. Body diodes of the switches *S1, M2, M3* and switch *M5* will provide reverse current path from load to source for the same voltage level during non-unity power factor operation.

7) State VII: In this state, $V_{PN} = -3V$, the switches *S1, M2, M3, M6* and *S4* are turned on and the remaining are turned off as shown in Fig. 4(g). The bi-directional current path from source to load and vice-versa is also shown in Fig. 4(g) with black and blue arrows respectively.

8) State VIII: This state corresponds to negative top level i.e., $V_{PN} = -4V$ in which all the DC sources are added by

switching on the mosfets *S1, M2, M3, M6* and *S3*. The bi-directional current path from source load and vice-versa is shown in Fig. 4(h).

9) State IX: For this state, the switches *M1, M3* and *M5* are turned on and the remaining are turned off to form a freewheeling period as shown in Fig. 4(i). The output voltage across the load will be zero and the current freewheels through the switches *M1, M3* and *M5* or the body diodes of the same switches based on the current direction.

From the above operating states, it is identified that the switches *M1, M3* and *M5* are complementary in operation with the switches *M2, M4* and *M6*. Also, the switches *M1* and *M2* are operating with the fundamental frequency. Switches *S1, S2, S3* and *S4* are turning on based on the required voltage level in four different combinations, as shown in Table. I. Moreover, switch *S1* is conducting most of the time and *S2, S3*, and *S4* are operating only two times in a complete cycle. Therefore, the switching and conduction losses of the overall inverter will be less.

C. Pulse generation

Sinusoidal level-shifted pulse width modulation technique is applied to generate the triggering pulses to proposed SMLI and it is depicted in Fig. 5(a). Total four carrier signals and one rectified reference sine signal are compared to generate the pulses and they were applied to the basic logic gates to obtain the desired pulses to the switches as per the switching table shown in Table. I. Various pulses applied to the inverter switches are shown in Fig. 5(b) and (c). The modulation index for the nine-level generation is defined as $M_a = \frac{V_{ref}}{4V_{Car}}$, where V_{ref} and V_{car} will be the reference and carrier signal magnitudes respectively.

D. Blocking voltage and Efficiency calculation

The blocking voltage of each device of the proposed 9-Level SMLIs is shown in Table II, which will also be used to evaluate the total blocking voltage (TBV) as follows:

$$TBV = \left(2 \times V_P + 4 \times \frac{V_P}{2} + 2 \times 0.35V_P + 2 \times 0.45V_P\right) = 5.6 \times V_P \quad (1)$$

TABLE II. BLOCKING VOLTAGE OF INDIVIDUAL SWITCHES

Voltage Stress	*S1& S2*	*M1, M2, M5 & M6*	*M3 & M4*	*S3 & S4*
	$0.35V_P$	$0.5V_P$	V_P	$0.45V_P$

- Where $V_P = V_1+V_2+V_3+V_4$

A similar procedure is applied for the SM – PUC SMLI for the generation of triggering pulses to the inverter. Instead of a bi-directional switch only a single switch is considered in the case of SM – PUC SMLI and the remaining all is as same as SBM – PUC SMLI.

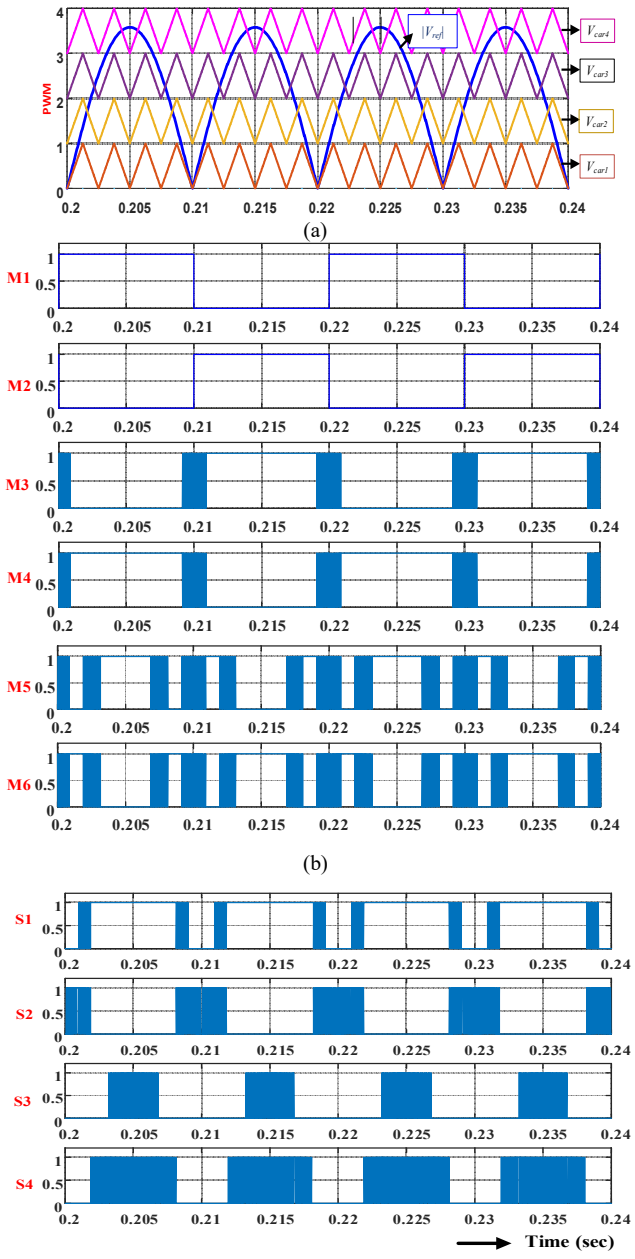

Fig. 5. (a). Sinusoidal level shifted PWM, (b) Triggering pulses for the PUC, (c) Triggering pulses for the level selector

TABLE III. SYSTEM PARAMETERS

S.No	Parameter	Range
1	Power	1000W
2	DC Voltage	100V each source
3	Load voltage	230V, 50Hz
4	Switching Frequency f_s	10000 Hz
5	Filter elements L_f and C_f	4 mH, 2 µF
6	Modulation index	0.9

III. Performance Evaulation

Performance of the proposed 9-level SMLI is verified by simulation studies using MATLAB/Simulink platform. A 1 kW inverter is designed to verify the performance and the corresponding parameters are listed in Table. III. Operation of the SMLI topologies is also tested during non-unity power factor operations of the load (i.e., under 0.95 lagging and leading conditions). Also, the THD of the load current is measured under different loading conditions.

9-level voltage and current waveforms under unity, 0.95 lagging and 0.95 leading load without filtering are shown in Fig. 6. (a), (b) and (c) respectively. It is noticed that the shape of the level voltage is not distorted under lagging or leading loads, which shows the superiority of the proposed topologies and modulation scheme. Fig. 7, illustrates the output voltage, current and FFT spectrum under different operating conditions of the load with filter. The corresponding FFT spectrum of load current under unity, lagging and leading loads with filtering are 0.30%, 0.10% and 0.32% respectively, which are well agreement with IEEE 519 standard and it can be seen from Fig. 7(b), (d) and (f). Only the simulation results of SBM – PUC SMLI are presented in this paper due to the same operation and control in comparison with others.

Furthermore, a comparative analysis between the proposed topologies and the existing topologies has been carried out in terms of device count and it is shown in Table. IV. All the topologies are able to generate 9-level with symmetrical DC sources. The number of voltage sources required in NPC and FC is very less, but the voltage balancing issues and component count are very much high in comparison with others. The parameters like a total number of switches, diodes and capacitors are less in the proposed PUC based SMLI topologies than other topologies.

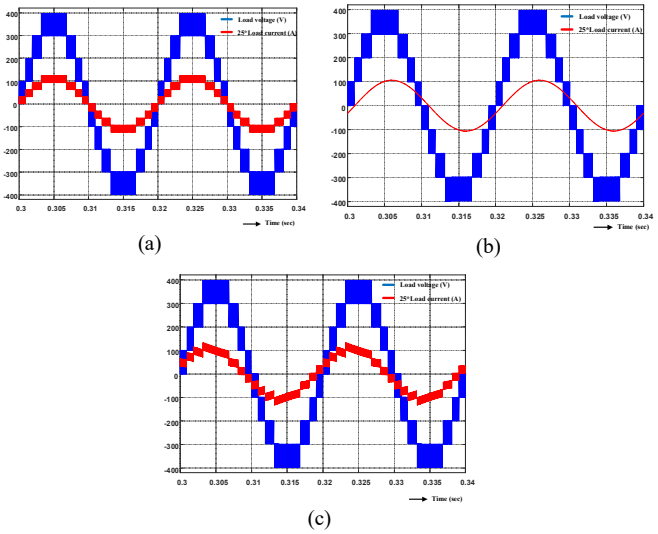

Fig. 6. Load voltage and current without filter under (a). Unity power factor, (b) 0.95 lagging power factor, (c) 0.95 leading power factor.

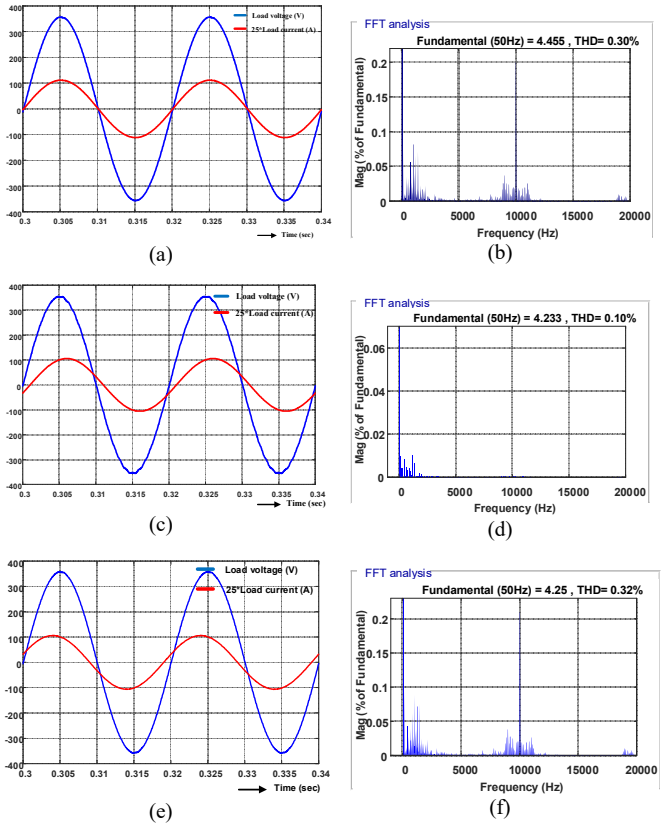

Fig. 7. Load voltage and current with filter (a). Unity power factor, (b) FFT spectrum (c). 0.95 lagging power factor, (d) FFT spectrum (e) 0.95 leading power factor, (f). FFT spectrum.

Therefore, the proposed SMLIs produce a same number of levels at lower cost and size. Moreover, SM-SMLI offers higher efficiency than the SBM-PUC SMLI, because of reduced number of switches is conducting for the level selection. But, the driver requirement is the same for both the proposed topologies. Moreover, the efficiency of the proposed SMLI topologies is tested using PSIM thermal module toolbox with IRFP460N Mosfet and it is illustrated in Fig. 8 [13]. From the efficiency curve it is noticed that the proposed topologies offering maximum efficiency of 98%. But, the efficiency of SBM – PUC SMLI is slightly lower than the SM – PUC SMLI due to increased switching loss in the bi-directional branch.

Table IV. Compative Analysis

MLI	Sources	Switches	Diodes	Capacitors
NPC	1	16	10	8
FC	1	16	0	7
CHB	4	16	0	0
T-type	4	16	0	8
TC – MLI	4	7	12	0
SBM – MLI	4	12	0	0
SM-PUC	4	10	0	0
SM-PUC	4	10	0	0

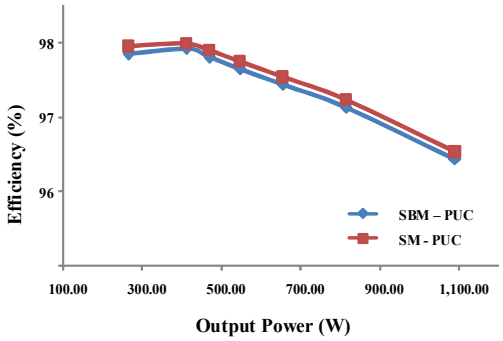

Fig. 8. Efficiency curve

IV. Conculsion

In this paper, novel single-phase packed U-cell based 9-level symmetrical inverter topologies are presented. The operating modes and working of the proposed topologies are validated through simulation studies and the results are presented under various operating conditions of the load. Moreover, the proposed topologies can generate 9-level output with an alleviated number of components as compared to the other existing topologies. Furthermore, the modulation scheme and the topologies allow current in both the positive and negative power regions without distorting the quality of level voltage. Finally, the proposed inverters are also offer a peak efficiency of 97.8%, which can improve the energy conversion for various applications. Experimental validation with a multi-output front-end boost converter is underway and the corresponding analysis and results will be presented in the extended version of the manuscript in the journal publication.

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