A Quasi-Z-Source-Based Five-Level PV Inverter With Leakage Current Reduction

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***Abstract*—Impedance-source-based solar PV systems are capable of achieving both voltage boosting and inversion in a single stage, resulting in a simple design thereby enhancing reliability. One of the major concerns of PV systems is their leakage current, as it can cause hazardous operational insecurity and reliability. This article introduces a quasi-Z-source (qZS)-based five-level inverter, which displays the following advantages: 1) reactive power handling capability, 2) single-stage boosting, 3) shoot-through immunity, and 4) reduced leakage current based on VDE 0126-1-1. The proposed single-stage power converter is constituted by the fusion of a boosting stage, consisting of two back-to-back connected qZSs, with a five-level inverter produced by the combination of T-type and neutral point clamped arms. The problem of the leakage current is addressed by a modified modulation technique and a passive filter structure, which filters high-frequency variations in the common mode voltage. The working principle of the proposed power converter and the effectiveness of the modulation scheme to reduce the leakage current are assessed with the aid of simulation studies in both standalone and the grid-connected modes. The simulation results are experimentally validated with the aid of a laboratory prototype of 500 W rating.**

***Index Terms*—Common mode voltage (CMV), neutral point clamped (NPC), quasi-Z source inverter (qZSI), reduced leakage current, shoot-through (ST).**

I. Introduction

CONTEMPORARY research is directed toward the promotion of renewable energy sources (RES) to counter the harmful effects of consuming fossil fuels. Solar photovoltaic (PV), wind, and fuel-cell are some of the popular RESs to produce such a clean power. PV power has seen a huge growth in its capacity in the last decade. With a worldwide installation capacity of 612GW and having a growth rate of 12% in 2019 [1], it is poised to become the major source of energy in the foreseeable future. However, the main drawback of PV systems is that they produce dc power, requiring a power conversion system to convert it into the ac form, either to be consumed in standalone networks or to inject the generated power into the grid. This task is often accomplished by multilevel inverters (MLI) [2]. MLIs have attracted researchers in the past few decades due to 1) operability of high dc input voltages with power semiconductor switching devices of low-voltage ratings, 2) low total harmonic distortion in the output voltage, 3) low filter requirements for grid interfacing, and 4) lower electromagnetic interference. Numerous topologies have been reported in literature pertaining to the MLIs [3]–[5]. The generic topologies of MLI's are mainly divided into three categories namely: 1) the neutral point clamped (NPC-MLI), 2) flying capacitor, and 3) cascaded H-bridge; the rest of the topologies are derived from three basic configurations. All of these inverters have a common drawback in that, they all belong to the "buck" category. Consequently, a large number of PV panels need to be connected in series and parallel to obtain the required power at the required voltage level. In the past, two-stage topologies have been suggested to circumvent this problem [6]–[9]. These systems display a good maximum power point tracking (MPPT) capability due the availability of an additional dc–dc boost converter. The other attractive features of the two-stage systems include reactive power capability, lower leakage current, constant common mode voltage (CMV) and unity power factor (UPF) grid current control [8], [9]. However, the demerits of these systems are low reliability, less efficiency and increased complexity. These shortcomings motivate researchers to lean toward the single-stage boost-inverters (SSBIs).

Several power circuit configurations have been proposed in the past to realize SSBIs. Of the available topologies in the literature, the quasi-z-source inverters (qZSI) based topologies appear to possess a good potential [10]. qZSIs are a family of inverters derived from the basic Z-source inverter (ZSI) proposed in [11]. The positive features that distinguish the qZSIs from the ZSIs are continuous input current, ease of integration with RES, and low component ratings. At present, a new breed of inverters namely, the quasi-Z-source-based MLIs (qZS-MLI), are actively being investigated. As one might expect, they inherit the advantages of both qZSs and MLIs. Various types of ZSI/qZSI based inverter configurations are described in [12] and [13]. One of the merits

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of ZSIs or qZSIs is that, they utilize the shoot-through time period to boost the input voltage to the required level of the dc-link voltage. In general, the boosting of the input PV voltage is obtained by resorting to the three basic methods known as 1) the simple boost control, 2) the constant boost control, and 3) the maximum boost control [14], [15]. Additionally, few more hybrid or modified shoot-through techniques have also been described in the available literature to obtain the desired boosting factor [16]. It is also important to have an effective control system to feed the harnessed PV power into the grid (at UPF), as most of the PV systems are grid connected.

Suppression of the leakage current is one of the important requirements while connecting an RES to the grid. The leakage current is principally caused by the time-variant nature of the CMV across the load terminals with respect to source ground [17]. The conventional approach to avoid the leakage current is to provide galvanic isolation (by using a transformer either on the low-frequency side or on the high-frequency side) between the RES and the grid. Apart from the galvanic isolation, the other methods of avoiding the leakage current are 1) separation of the ac and the dc sides, 2) connecting the grid neutral to the negative terminal of the input, and 3) connecting the midpoint of the dc-link to the grid neutral [18]. These methods are used either to make the CMV constant or allow only a slow (i.e., low frequency) variation in it to reduce the leakage current. The nongalvanic isolation techniques are majorly categorized based on 1) the carrier, 2) the topology, and 3) the modulation technique.

Most of the PV systems described in the available literature are two-staged, which are complex and loss incurring. When compared to these, the research work carried out on the ZSI/qZSI based systems is relatively scanty. Modulation strategies, which aim to reduce/eliminate the leakage current either by decoupling the ac and the dc sides, or by the reduction/elimination of the high-frequency variations in the CMV of ZSI/qZSI are described in [19]–[24].

In the research work reported in [19], the reduction in the CMV is achieved by the odd PWM, wherein odd active vectors were used to make the CMV constant. The reduction in the CMV of a 3-Ph ZSI is achieved by employing a modified nearest vector space vector modulation technique [20]. A high-frequency notch filter with constant area SVM was proposed which eliminated the low-frequency harmonics to make the CMV constant in [21].

For three-phase qZS 3LT^{2}I, a novel modulation scheme was proposed in [22], which automatically balances the neutral point voltage and forces the CMV to be one-sixth of the dc-link voltage. For a three-phase four-leg qZS system, two more new PWM schemes were introduced in [23] and [24], wherein [23] uses effective vectors from large, medium, small, and zero vectors to make CMV constant and in [24] the CMV is forced to be a constant by replacing the zero-vector with an opposite active vector. However, the advantage associated with this scheme is partially nullified by the increased number of commutations, which incur a higher switching power loss.

The research work reported in [8]–[25] and [34] present new topologies and the associated modulation schemes for single-phase qZS systems. A new ZS circuit configuration, based on HERIC was introduced in [25]. This circuit adds two more switches and diodes on the ac side of the inverter to decouple the ac and the dc sides. A qZSI has been proposed in [26], which is based on the concept of active power filtering. This topology, along with its modified PWM scheme, manages to reduce the ripple corresponding to twice of the output frequency (i.e., the "2ω" component) in addition to the reduction of the CMV.

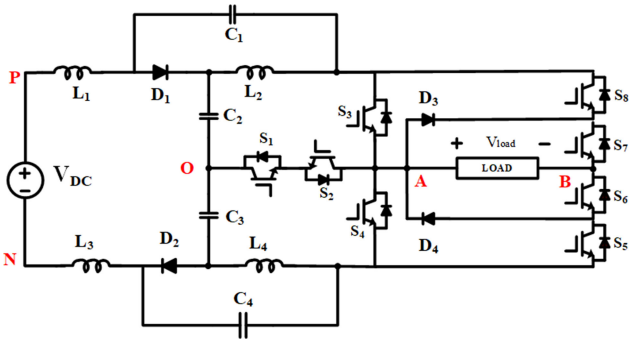

Fig. 1. Proposed qZS-based NPC inverter.

A new topology was introduced in [27], wherein two more switches are added to an existing H-bridge structure to facilitate the connection of the grid neutral to the negative rail of the input. This results in a considerable reduction in the variation of the high-frequency components in the CMV. In contrast, the power converter configuration reported in [28] employs two additional switches, which conduct during freewheeling period to isolate the source from the grid.

Only three-level inverter configurations, which are based on the ZS/qZS have been studied till date and no literature is available on five-level qZSI with reduced leakage current. This article proposes an NPC-based qZS T-type inverter (qZS-NPC-T^{2}I) that outputs a five-level voltage with a reduced leakage current. A modified modulation technique has also been proposed to achieve the desired output voltage waveform. The leakage current is reduced by decoupling the dc side from the ac side to deny a path to it. A modified shoot-through technique has also been introduced for proper boosting of the dc-link voltage. The modified modulation scheme does not only reduce the leakage current but also balances the neutral point voltage. Also, the proposed converter possesses the ability to supply reactive power to the grid/standalone system.

II. System Description

A. Proposed Topology

This article proposes an improved NPC-based qZSI for single-phase applications [34]. It comprises of an NPC arm and a T-type arm (Fig. 1). The proposed configuration contains eight switches (S_1–S_8), four inductors (L_1–L_4), four capacitors (C_1–C_4), and four diodes (D_1–D_4). Of these, the devices S_1 and S_2 constitute a bidirectional switch. The junction of the inner capacitors of the two qZS networks forms the neural point "O" (Fig. 1). The load is connected between the midpoint of T-type arm (which is connected to the junction of the clamping diodes of the NPC arm)

and the midpoint of the NPC arms (Fig. 1). This modification facilitates power circulation during the freewheeling period while disconnecting the load side from the source side. This converter can produce five voltage levels, viz. 0, $\pm V_{\mathbf{dc}}/2$ and $\pm V_{\mathbf{dc}}$. The total dc-link voltage $V_{\mathbf{dc}}$ is the sum of all the four capacitor voltages. The working principle of the proposed power converter and the modified modulation scheme are explained in detail in the subsequent sections. A new hybrid shoot-through technique has been implemented to obtain the required voltage boosting and to ensure an effective utilization of all components. This method also helps in balancing the neutral point "O" (Fig. 1).

B. Working Principle

The working principle of the proposed converter is explained in detail covering the aspects of 1) generation of output levels, 2) the operation in the freewheeling states, and 3) the operation in the shoot-through states.

First, the output levels of $\pm V_{\rm dc}/2$ and $\pm V_{\rm dc}$ (which are the active states) may be realized in two alternative ways, accounting for four modes of operation. Second, there exist three types of shoot-through modes for the proposed converter namely 1) the upper-half shoot-through mode, 2) the lower-half shoot-through mode, and 3) the complete shoot-through (CST) mode. Last, there exists a zero (i.e., a null) mode, which provides the freewheeling of power. With the aid of Fig. 2, these eight modes of operation are described as follows:

Mode 1:- The Positive Powering Mode-1

This mode produces the voltage level of $+ V_{\rm dc}/2$. The switches S_1, S_2, S_5, and S_6 are utilized, while other devices are turned OFF. Fig. 2(a) shows the direction of the current in this mode. The power is positive as both voltage and current are in the same direction.

Mode 2:- The Positive Powering Mode-2

The voltage level of $+V_{\rm dc}$ is obtained by turning ON the switches S_3, S_5, and S_6. The path of current is shown in Fig. 2(b).

Mode 3:- The Negative Powering Mode-1

Fig. 2(c) shows the method of developing the voltage level of $-V_{\rm dc}/2$. The switching devices S_7, S_8, and the bidirectional switches are used to generate this voltage level.

Mode 4:- The Negative Powering Mode-2

Switches of S_4, S_7, and S_8 are utilized to realize the voltage level of $-V_{\rm dc}$. Direction of the current for positive power is shown in Fig. 2(d).

Mode 5:- The Freewheeling (Zero or Null) Mode

The freewheeling modes are applied at the beginning and at the end of any half period. Fig. 2(e) shows the details pertaining to this operation.

Mode 6:- The Complete Shoot-Through Mode

The CST mode is achieved by short-circuiting both of the qZS networks. The path of current for this method is shown in Fig. 2(f). Switches S_3 and S_4 are used to obtain this mode of operation.

Mode 7:- The Upper Shoot-Through Mode

The upper shoot-through (UST) mode utilizes only the upper qZS part to obtain the voltage boosting. This shoot-through mode is created by turning ON the switches S_1, S_2, and S_3 [Fig. 2(h)]. During this time, the inductors of the upper qZS network get charged and supply power during the active mode.

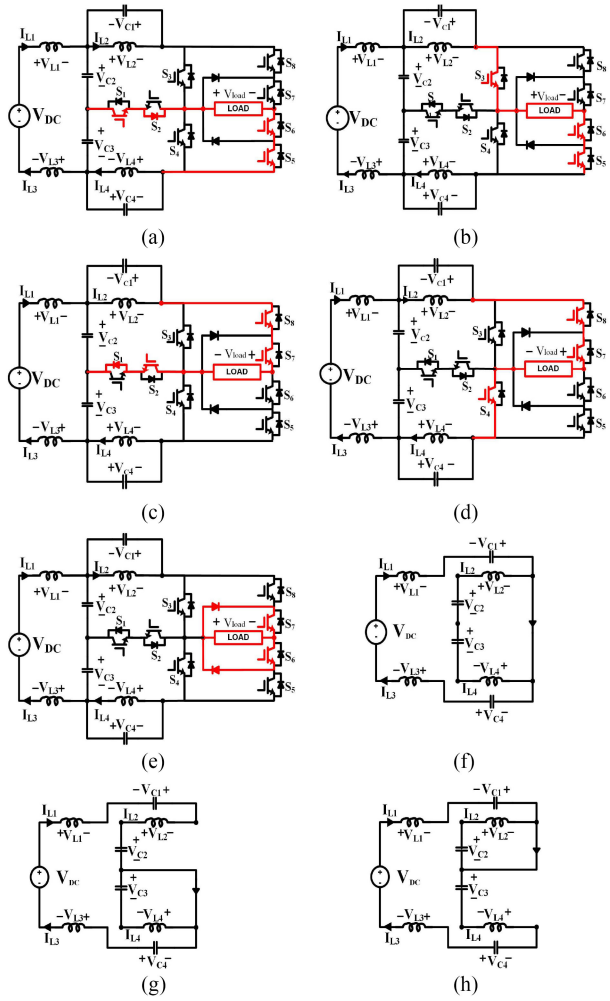

Fig. 2. Various operating modes of the proposed converter: (a)–(d) active modes, (e) freewheeling mode, and (f)–(h) various shoot-through modes.

Mode 8:- The Lower Shoot-Through Mode

The lower shoot-through (LST) mode is shown in Fig. 2(g). The path for current during the LST mode traverses through S_1, S_2, and S_4 pertaining to the lower qZS.

Modes 1–4 are the active states, which produce the required voltage levels, while modes 6–8 are the shoot-though states used for single-stage boosting. Assuming identical parameters for the passive elements ($L_1 = L_2 = L_3 = L_4 = L$ and $C_1 = C_2 = C_3 = C_4 = C$), the following equations can be derived. The equations applicable for the UST and the LST are the subsets of the equations applicable for the CST. The total dc-link voltage of this qZSI is

$$V_{\rm dc} = V_{C1} + V_{C2} + V_{C3} + V_{C4}. \tag{1}$$

The capacitor voltages of the proposed inverter assuming symmetrical characteristics can be expressed as

$$V_{C1} = V_{C4} = \frac{D_{\rm SH} * V_{\rm IN}}{(1 - 2D_{\rm SH})} \tag{2}$$

TABLE I
SWITCHING STATES OF THE QZS-NPC-T^{2}I

Output Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Switching State
V_{DC}	0	0	1	0	1	1	0	0	Active
$V_{DC}/2$	1	1	0	0	1	1	0	0	Active
0	1	1	0	0	0	1	1	0	Zero
$-V_{DC}/2$	1	1	0	0	0	0	1	1	Active
$-V_{DC}$	0	0	0	1	0	0	1	1	Active
0	0	0	1	1	0	0	0	0	Upper Shoot through
0	1	0	0	1	0	0	0	0	Lower Shoot through
0	0	0	1	1	0	0	0	0	Complete Shoot through

$$V_{C2} = V_{C3} = \frac{(1 - D_{\rm SH}) * V_{\rm IN}}{(1 - 2D_{\rm SH})} \tag{3}$$

$$B = \frac{1}{1 - 2 * D_{\rm SH}}. \tag{4}$$

In (4), the term "*B*" represents the boost factor obtained by the proposed converter, which is the same as the conventional qZSI. The symbol $D_{\rm SH}$ represents the shoot-through duty cycle needed to achieve the required boosting level.

C. Modified Modulation Scheme

This article proposes a hybrid modulation technique, which is derived from the sine pulsewidth modulation. Phase disposition level-shift carrier waves are utilized to develop this modulation scheme for the switching devices. Table I provides the details regarding the switching devices, which are required to be turned ON (denoted by "1") to realize the five voltage levels, and the three shoot-through states for the proposed converter. Fig. 3 shows the level-shifting carrier PWM technique, which presents the four carrier signals (C_1–C_4), the sine modulating signal. The signals A, B, C, and D are obtained by the comparison of the modulating signal with these four carrier waveforms. The signal "G" is obtained by comparing modulating signal with zero and signal H is logical inversion of G. All of these signals are further decoded to generate the required gating signals for all of the switching devices, which constitute the proposed converter.

Based on the switching table provided above the modulating signal for each switch can be defined as

$$\boldsymbol{S}_1 = \boldsymbol{S}_2 = A \oplus B + C \oplus D\ ,\ \boldsymbol{S}_3 = B,\ \boldsymbol{S}_4 = D\ ,$$
$$\boldsymbol{S}_5 = A\ ,\ \boldsymbol{S}_6 = G + \bar{C}G,\ \boldsymbol{S}_7 = \bar{A}G + \bar{G}\ ,\ \boldsymbol{S}_8 = C. \tag{5}$$

In this article, a hybrid-shoot-through technique has been applied to achieve the appropriate voltage boosting, which employs the three types of shoot-through modes, viz. the LST, the UST, and the CST (the circuits for these shoot-through modes have been presented in the previous section). The LST and UST are, respectively, applied in the positive and negative half cycles while realizing the $+V_{\rm dc}/2$ and the $-V_{\rm dc}/2$ levels. In contrast, the CST is applied while switching the $+V_{\rm dc}$ and the $-V_{\rm dc}$ levels (i.e., during both positive and negative half cycles).

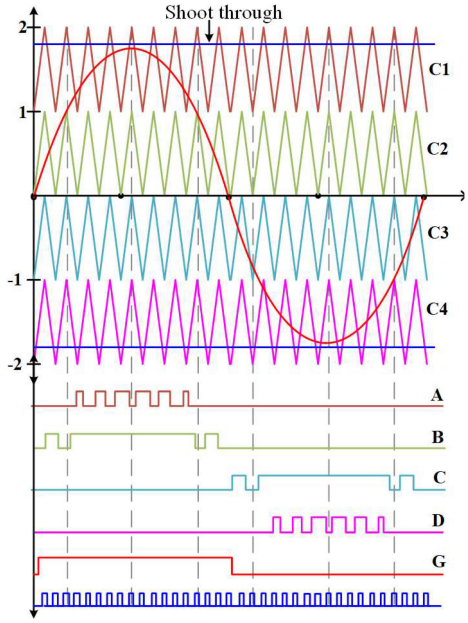

Fig. 3. LSPWM and corresponding signals.

D. Passive Component Selection

In a symmetrical dual-quasi structure, all passive components have similar values. One of the important factors in the calculation of the ratings of the passive components is the addition of the low-frequency ripple (at a frequency of "2ω") to the high-frequency ripple. Of these two ripple components, the low-frequency ripple component is typically caused by the circulation of the double-frequency component between the source and the load, while the high-frequency component is caused by the shoot-through states. The inductance (6) and the capacitance values (7) and (8) were calculated by using the following formulae:

$$L = \frac{4 * V_O^2 * (1 - 2D_{\rm SH}) * T_s * D_{\rm SH}}{(1 - D_{\rm SH}) * K_L * P_O} \tag{6}$$

$$C_1 = C_4 = \frac{T_S * P_O * (1 - D_{\rm SH})^2}{4 * k_{C1} V_O^2 (1 - 2D_{\rm SH})} \tag{7}$$

$$C_2 = C_3 = \frac{T_S * P_O * (1 - D_{\rm SH}) * D_{\rm SH}}{4 * k_{C1} V_O^2 (1 - 2D_{\rm SH})}. \tag{8}$$

In the above formulae, the symbols K_L, k_{C1}, and k_{C2}, respectively, denote the ripple factors of the inductors and the capacitors. A clear boundary between the continuous conduction mode and the discontinuous conduction mode is established in [29].

E. Control Structure

In this article, two types of control structures are considered, namely the standalone system and the grid-connected system. They are described in detail in the following paragraphs.

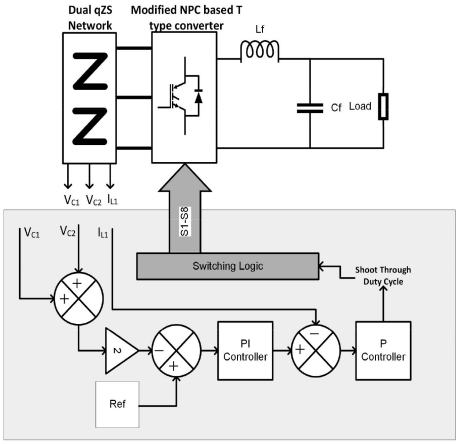

Fig. 4. Closed-loop control scheme for standalone system.

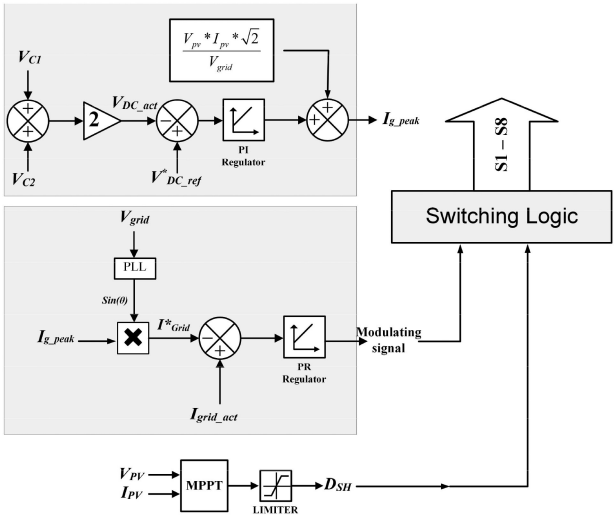

Fig. 5. Closed-loop control scheme for PV-grid-connected system.

1) Standalone System: A closed-loop control system consisting of two loops is used in the standalone control structure (Fig. 4). The objective of this control system is to maintain the dc-link voltage constant during the load and source disturbances. From Fig. 1, it may be noted that the dc-link voltage is the sum of all four capacitor voltages. Hence, four voltage sensors are needed to measure the peak value of the dc-link voltage. However, exploiting the symmetric nature of the proposed back-to-back qZS networks to advantage, only two capacitor voltages (V_{C1} and V_{C2}) are sensed using two voltage sensors. The sum of these two voltages is then multiplied by a factor of 2 to estimate the peak dc-link voltage. Thus, the closed-loop system uses three sensors in all; two for sensing the capacitor voltages and one for sensing the inductor current.

The outer loop consists of a PI controller, while the inner loop consists of a simple proportional (P) controller. In the outer loop, the measured value of the peak dc-link voltage is compared with its reference value. To compensate the error (if any) between the desired and the actual values of the dc-link voltage, the PI controller determines the required inductor current and sets this value as the reference for the inner controller, which controls the inductor current. This reference inductor current is then compared with the actual (i.e., the sensed) inductor to determine the required value of the shoot-through duty cycle.

2) Grid-Connected System: The performance of the proposed power converter has also been studied in the grid-connected mode. In this mode of operation, there are two objectives: 1) the MPPT and 2) realization of the UPF.

In this article, the MPPT for a given value of irradiance is accomplished by controlling the shoot-through duty cycle (denoted by the symbol "$D_{\rm sh}$"). Perturb and Observe (P&O) method is implemented to obtain the required value of reference, which is then compared with the top and the bottom carrier waves (Fig. 3) to generate the shoot-though pulse. The shoot-through pulse is then logically manipulated to create the upper, lower, and full shoot-through modes in the inverter.

Fig. 5 presents the control structure to realize the objective of controlling the grid current to achieve optimal injection of active power into the grid, which requires the UPF operation. The actual dc-link voltage is obtained by the addition of the capacitor voltages V_{C1} and V_{C2}, which are sensed and multiplied by a factor of "2" (as the total dc-link voltage is the sum of two identical back-to-back connected qZS networks). The actual dc-link voltage is then compared with the reference value and the error between them is compensated by a PI regulator. The output of the PI regulator represents the regulated error which is expected to zero. The output signal of the PI controller is then subtracted from the value obtained by dividing PV power by peak grid voltage to obtain the magnitude of the peak current, which needs to be injected into the grid to regulate the dc-link voltage and to achieve MPPT.

To achieve the UPF operation, a PLL is employed to synchronize the grid current with the grid voltage. The generated waveform template is multiplied with the magnitude of the peak value of the reference current to generate the sinusoidal reference for grid current. The reference grid current is then compared with the actual (i.e., the sensed) grid current and the resultant error is fed to a proportional–resonant controller to generate the modulation signal. The modulation signal is then compared with the carrier signals to implement the LSPWM scheme (Fig. 3).

F. Comparative Analysis

This section reports about the performance of the proposed qZS-NPC-T2I vis-à-vis the existing qZS-based single-phase topologies reported in the literature. Three five-level topologies are considered for the comparative evaluation, namely 1) qZS-NPC [28], 2) single-phase qZS-based CMI [30], and 3) modified qZS (MqZS) [31].

Table II presents the number of passive elements, switching devices, and the source requirement of the proposed topology with the topologies mentioned above. It may be noted that the proposed topology requires the same number of passive elements, compared to the qZS-NPC and qZS-CMI. However, it requires two more inductors, compared to the MqZS. While the proposed topology requires lesser number of diodes than the qZS-NPC, it needs one and two more diodes compared

TABLE II
COMPONENT COMPARISON OF PROPOSED TOPOLOGY WITH EXISTING TOPOLOGIES

Components	qZS-NPCT²I	MqZS modified hybrid inverter	qZS-CMI	qZS-NPC
Inductors	4	2	4	4
Capacitors	4	4	4	4
Diodes	4	3	2	6
Switches	8	8	8	8
DC sources	1	1	2	1

TABLE III
VOLTAGE STRESS COMPARISON

Components	qZS-NPCT²I		MqZS modified hybrid inverter		qZS-CMI		qZS-NPC	
Switches	$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}, \frac{\sqrt{2}}{(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$	
Capacitor	C_2, C_3	$\frac{1}{\sqrt{2}}$	C_1, C_2	$\frac{1}{\sqrt{2}}$	C_2, C_3	$\frac{1}{\sqrt{2}}$	C_1	$\frac{1}{\sqrt{2}}$
	C_1, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_3, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_1, C_4	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$	C_2	$\frac{1}{\sqrt{2}}\frac{D}{1-D}$
Diodes	$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$		$\frac{1}{\sqrt{2}(1-D)}$	

to the qZS-CMI and MqZS, respectively. Though the proposed topology needs a higher number of diodes, only two of them are utilized during the zero period. Also, the proposed topology requires only one voltage source to generate the five-level output voltage waveform, putting it on par to the other topologies except the qZS-CMI (which needs two sources).

From Table III, it is evident that the boost factor obtained by the proposed inverter is the same as that of the qZS-NPC and a single module of qZS-CMI. However, it is lower than the boost factor obtained with the MqZS base inverter by a factor of 0.5.

Table III compares all of the aforementioned topologies with respect to the voltage stress (which determines the voltage rating) across each component, taking ac output rms voltage as the base value. It may be noted that, similar to the topologies qZS-CMI and qZS-NPC, all of the switching devices of the proposed inverter are subjected to an equal voltage stress. In the MqZS topology, some of the switches are required to handle a higher voltage stress (double compared to the three previous topologies). The capacitors and diodes are required to handle the same voltage stress in all of the four topologies.

III. LEAKAGE CURRENT ANALYSIS

The equivalent common mode model of the proposed qZS-NPC-based PV system and its simplified version are presented in Fig. 6(a) and (b), respectively. The parameters R_g and R_f, respectively, represent the average ground impedance and the internal resistance of the filter. From Fig. 6(a), the CMV for the inverter can be estimated as

$$V_{\mathrm{CMV}} = \frac{V_{AN} + V_{BN}}{2} \tag{9}$$

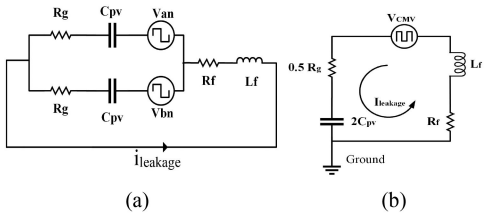

Fig. 6. Common mode circuit representation of the inverter.

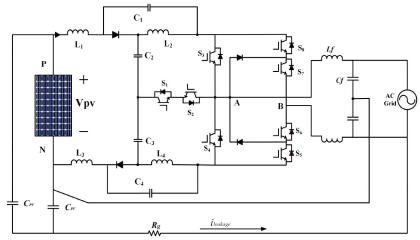

Fig. 7. Proposed topology with split LCL filters to reduce high-frequency variation in CMV.

where V_{AN} and V_{BN}, respectively, denote the phase-leg voltages of the inverter with respect to ground (Fig. 1).

The common mode current (CMC) or the leakage current flows from the PV panel to the ground (N) due to the time-variant nature of the CMV. The leakage current is related to the parasitic capacitor by

$$i_{\mathrm{leakage}} = C_{\mathrm{PV}} \frac{dV_{\mathrm{CPV}}}{dt} \tag{10}$$

where i_{leakage} is the leakage current in ground and C_{PV} and V_{CPV} are the capacitance and the voltage across the parasitic capacitor found from the PV panels to the ground.

As the leakage current is caused mainly due to the variation in the CMV, the high-frequency components in the CMV strongly influence it. Thus, the CMC can be suppressed by the following conditions:

1) Making the CMV constant.
2) Reducing the high-frequency variation.
3) Reducing the CMV.

Following the operating principle presented in Section II, it can be observed that the inverter has three principal working modes namely the active-, the zero-, and the shoot-through modes. The shoot-though mode, which is inserted between the active and the zero state, mainly contributes to the variation of the CMV. As three different types of shoot-through are inserted to get the required boosting factor, the CMV also varies based on which type of the shoot-though is applied, causing the voltage across the parasitic capacitor to vary. The proposed topology employs an active filter (Fig. 7), which accomplishes the tasks of both filtering the output voltage and suppressing the CMV. An active LCL filter is obtained by splitting the filter capacitor into two equal parts and connecting the midpoint of these capacitors to the negative rail of the input dc source. This type of structure does not only filter out the high-frequency components in the output voltage, but also checks the high-frequency variation

TABLE IV
PARAMETERS USED FOR EXPERIMENT

Parameters	Values
Power	500 watts
Input voltage	100 V
Grid Voltage (rms)	110 V
Inductor L_1-L_4, L_f	1mH, 4mH
Capacitor C_1-C_4, C_f	1000μF, 2μF
Switching Frequency	10kHz
Controller	Xilinx Spartan 6 FPGA
Switches (S_1-S_8)	STGB20H60DF
Diodes(D_1-D_4)	MURS1560

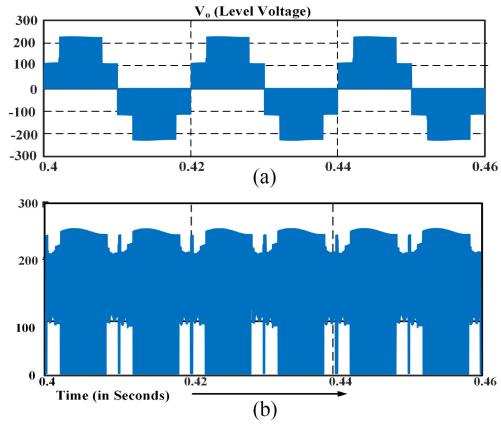

Fig. 8. Simulation results for proposed inverter. (a) Output level voltage. (b) DC-link voltage.

in the voltage across the parasitic capacitor, thus reducing the leakage current significantly.

IV. Simulation Results and Experimental Validation of the Proposed Power Converter

A. Simulation Results

The working principle of the proposed power circuit has been verified with simulation studies using MATLAB/Simulink and experimentally validated with a scaled down prototype. The operating conditions and the converter parameters are enumerated in Table IV. The values of passive components are calculated using (6)–(8). Fig. 8(a) shows all of the five voltage levels produced by the proposed inverter. Fig. 8(b) shows the fluctuating dc-link voltage. It is evident that whenever the shoot-through state is switched, the dc-link is short circuited and its voltage is brought down to zero. While the application of LST or UST the voltage floats at $0.5V_{\rm dc}$. It may also be noted that the CST mode is employed while operating at the voltage level of $V_{\rm dc}$.

Further, Fig. 9(a) shows the inductor current of the inverter. The inductor is energized during the shoot-through mode and its current increases. During the nonshoot-through modes, the inductor current decreases. Fig. 9(b) and (c), respectively, shows the voltages across the capacitors C_2 and C_1 (79.6 and 29.8 V). The voltages across the other two capacitors (C_3 and C_4) would be identical to the ones shown owing to topological symmetry of the back-to-back connected qZS networks (Fig. 1). These capacitor voltages are very close to the theoretically computed

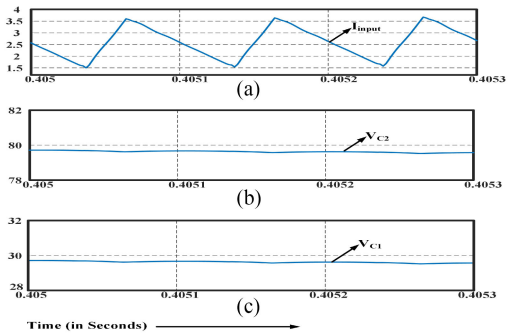

Fig. 9. Dynamics of passive components. (a) Inductor current for L_1. (b) Voltage across capacitor C_2. (c) Voltage across capacitor C_1.

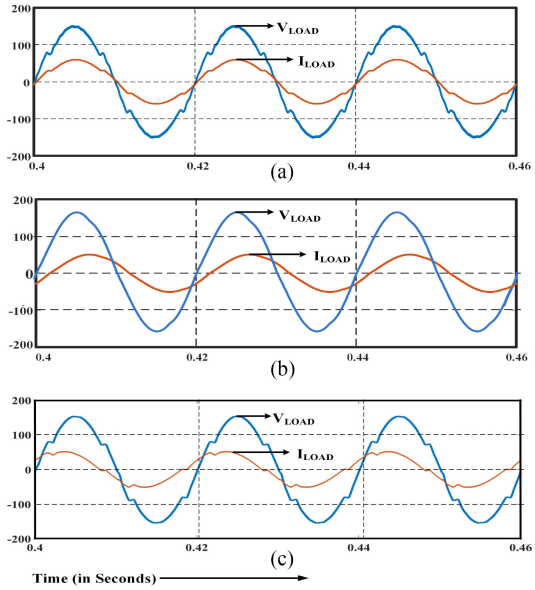

Fig. 10. Reactive power capability of converter. Output of converter for various load pf (a) UPF; (b) 0.8 Lagging PF; and (c) 0.8 Leading PF.

values given by (2) and (3) (81.6 and 30.18 V, respectively). Thus, the simulated results support the theoretical analyses presented in the earlier sections.

In this simulation study, the input voltage is 100 V and the ac output rms voltage is 110 V (or a peak value of 155 V). When the qZS networks are operated with a shoot-through duty ratio of 0.27, a boost factor of 2.2 (app.) is obtained (4). By noting the peak value of the dc-link voltage [Fig. 8(b)], it is evident that the required boost factor is obtained. From the circuit diagram of the proposed power converter (Fig. 1), it may be noted that the boosted dc-link voltage is obtained by summing all the four capacitor voltages. Accordingly, Fig. 8(b) shows that the peak value of the boosted dc-link voltage is the sum of all of the four capacitor voltages.

The capability of providing a free-wheeling path during the zero-period renders the reactive power handling capability to the proposed converter. This feature is demonstrated with the simulation results shown in Fig. 10. Fig. 10(a)–(c), respectively, shows the voltage (blue trace) and the current (red trace) across the load for UPF, 0.8 (lag) and 0.8 (lead), respectively.

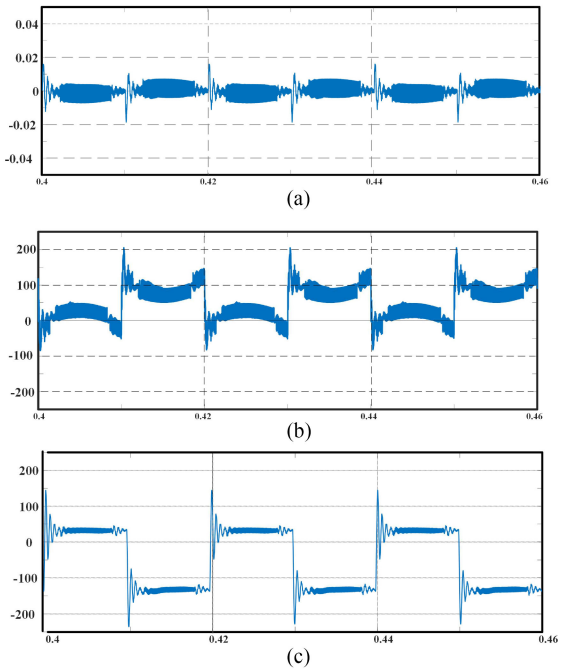

Fig. 11. Common mode parameters of the inverter (a) leakage current; (b) CMV; and (c) voltage across parasitic capacitor.

As stated earlier, the modulation scheme adopted in this article does not only provide the reactive power capability to the converter but also helps in the suppression of leakage current. As explained in the previous section, the split filter provided at the output reduces the high-frequency variation in the CMV appearing across the parasitic capacitor. Fig. 11 shows the simulation results pertaining to the suppression of the CMC. Fig. 11(a) displays the leakage current flowing from the source to the load. With a peak value less than 20 mA, the proposed power converter complies with the VDE 0126-1-1 grid standards. The CMV and the voltage across the parasitic coupling capacitor are shown in Fig. 11(b) and (c), respectively.

The dynamic performance of the proposed converter against both source and load disturbances for a standalone system are presented in Figs. 12 and 13, respectively. The closed-loop control system aims to regulate the dc-link voltage to a constant value by controlling the shoot-through duty cycle. The reference value for the dc-link voltage (peak value) was kept at 220 V. Fig. 12 shows the dynamic response of the proposed converter for the source disturbance, wherein the source voltage is suddenly varied from 100 to 120 V. The corresponding change in the shoot-through duty is presented in Fig. 12(b). From Fig. 12(c), it may be noted that the peak value of the dc-link voltage is regulated by the closed-loop controller (Fig. 4), as it gets back to its original value following the disturbance. The impact of the source disturbance on the load voltage and the current is shown in Fig. 12(d), wherefrom it is evident that the load voltage (and hence the load current for a constant load impedance) is practically immune to the source disturbance. This is attributed to the electrical inertia introduced by the filtering elements.

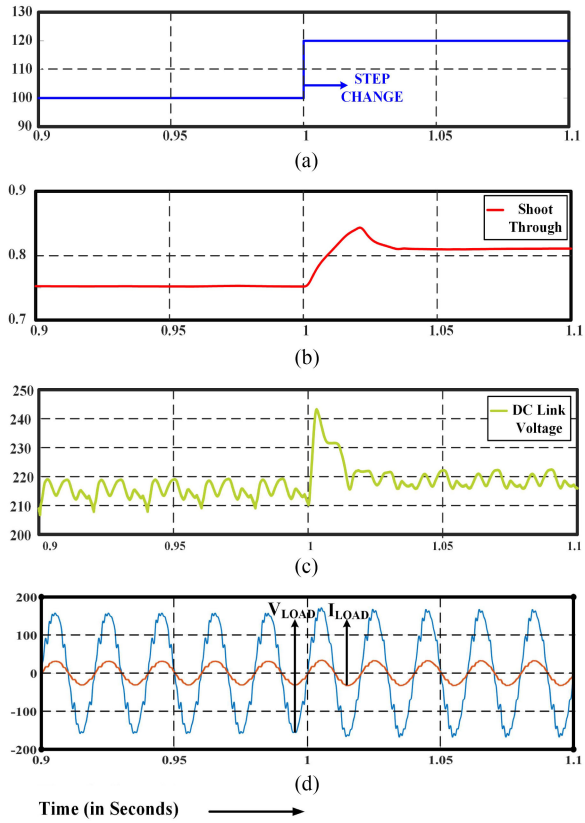

Fig. 12. Transient response of system for disturbances on source side. (a) Step change in input voltage. (b) Change in shoot-though duty cycle. (c) Peak dc-link voltage. (d) Output voltage and current.

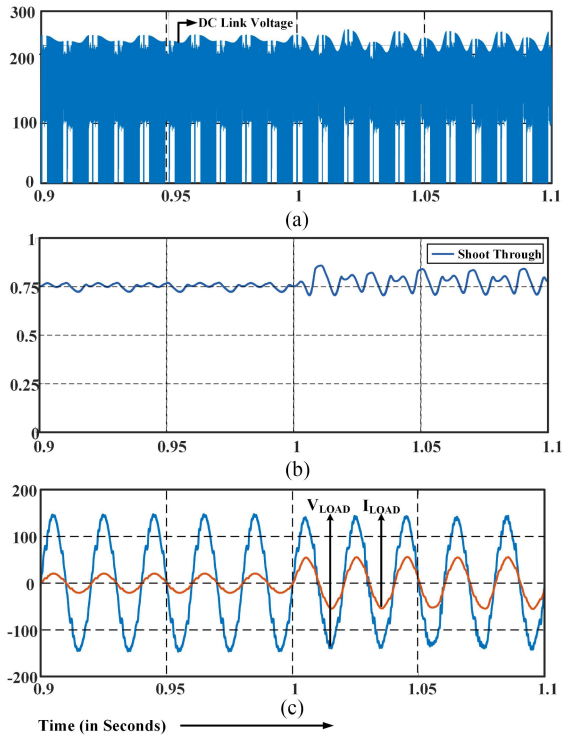

Fig. 13. Transient performance of the system for step change in load. (a) DC-link voltage. (b) Shoot-through duty cycle. (c) Output voltage and current.

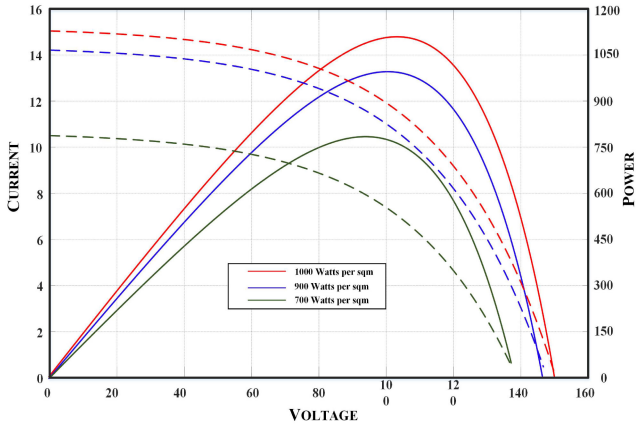

Fig. 14. P-V and I-V curve of the PV array.

The dynamic response of the proposed converter against a sudden load disturbance is presented in Fig. 13. Despite a sudden change in the load current from 2 to 5 A (due to the reduction of the load impedance), the output voltage does not show any significant difference. The reason for this is due to 1) the modulation index is kept constant, 2) the dc-link voltage is regulated with a fast closed-loop controller, and 3) the existence of a large electrical inertia at the output stage.

Fig. 14 shows the characteristics of the PV panels used to assess the performance of the proposed converter using both offline and the real-time simulation studies.

Fig. 15 shows the offline simulation results for the grid-connected system. The dynamic behavior of the proposed converter is studied when the irradiation decreases, while the temperature is constant. Fig. 15(a) shows the change in irradiance from 900 to 700 W/m^2, which is applied at 1 s of simulation. The corresponding change in power can be observed in Fig. 15(b). The change in the irradiation forces the P&O algorithm to adjust the shoot-through duty factor to reattain the MPP. The PV voltage and the PV current clearly indicate the effect of readjusting the shoot-through duty factor and the subsequent reattainment of the MPP with the changed irradiation. The decreased PV current (due to the decrease of irradiation) manifests as a decrease in the grid current, as the grid voltage is regulated by the regulation of the dc-link current (at a constant modulation index). The waveforms of the grid voltage and the grid current are presented in Fig. 15(d). It may be observed that following the environmental disturbance, the grid current decreases. It may also be observed that, owing to the control effort put in by the control system shown in Fig. 5, the grid current is always in phase to the grid voltage resulting in the UPF operation.

The PV panels used for simulation are rated for 95 W with the open-circuit voltage (V_{OC}) 25.9 V and the short-circuit current (I_{SC}) of 3.36 A. A total number12 panels were utilized. Six of them are connected in series to obtain the required voltage rating and two such strings are connected in parallel to obtain a total power rating of approximately 1150 W. The P-V characteristics for the array can be seen in Fig. 14 for various irradiance conditions at a temperature of 25°C.

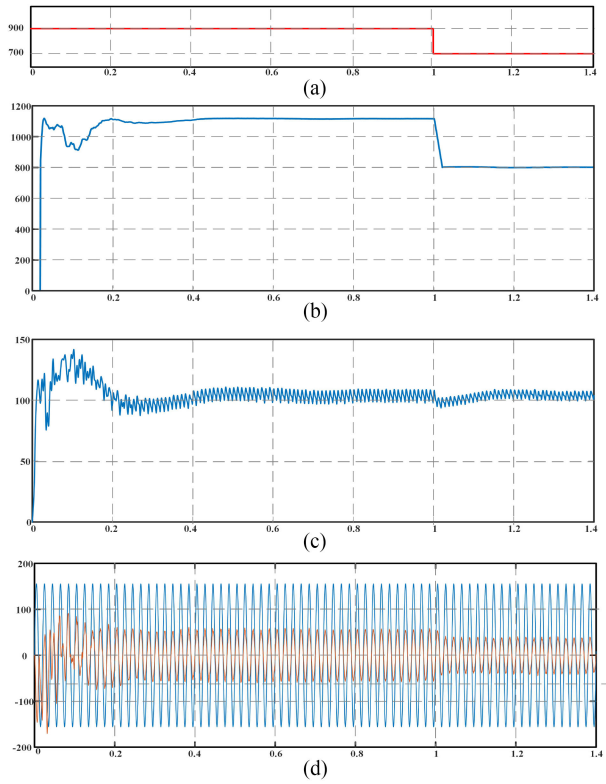

Fig. 15. Grid-based simulation for step change in irradiance. (a) Change in irradiance. (b) Change in PV array's power level. (c) PV voltage. (d) Grid voltage and current.

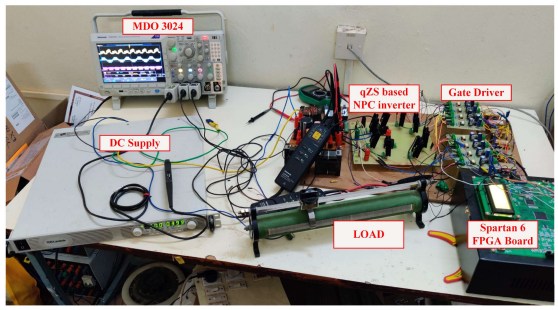

Fig. 16. Hardware setup of the proposed inverter.

P&O algorithm is used to reach the maximum power point (MPP). This algorithm is widely used because of its simplicity and ease of implementation. The algorithm is evaluated for every 1 ms and outputs the shoot-through duty cycle value.

B. Experimental Results

To validate the theoretical analyses and the simulation results, a 500 W laboratory prototype is developed and tested. The experimental setup of the proposed inverter is shown in Fig. 16. The passive components are designed using the formulae presented in (6)–(8). The power converter is realized with the IGBT switching devices (STGB20H60DF), while the controller and the PWM scheme are implemented with the FPGA Spartan 6 by Xilinx. Fig. 17(a) shows the experimental results pertaining

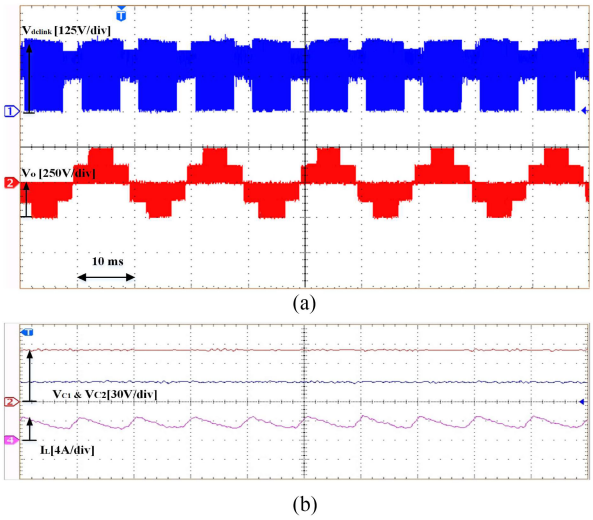

Fig. 17. Experimental results for proposed system in steady state. (a) DC-link voltage and output level voltage. (b) Capacitor voltages and inductor current.

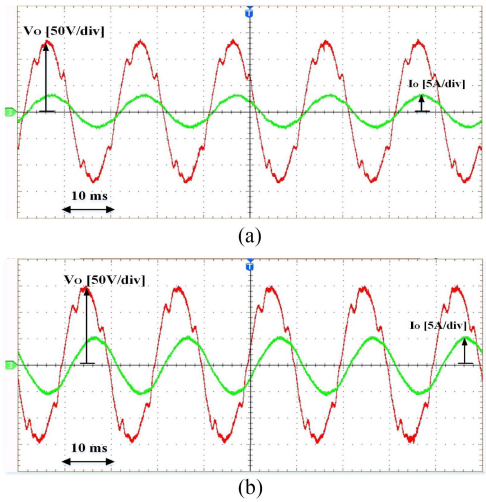

Fig. 18. Experimental waveform demonstrating reactive power capability of the inverter (a) UPF; and (b) 0.8 lagging PF.

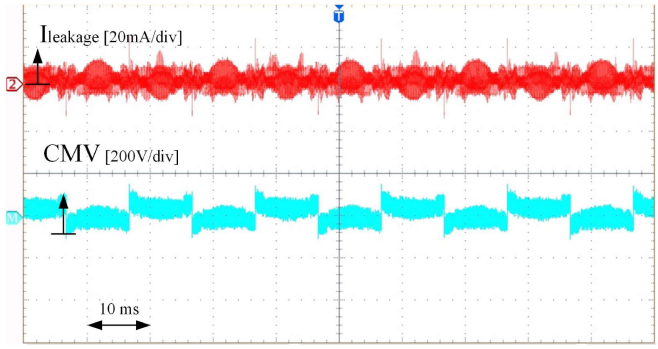

Fig. 19. Experimental results for leakage current and common mode voltage.

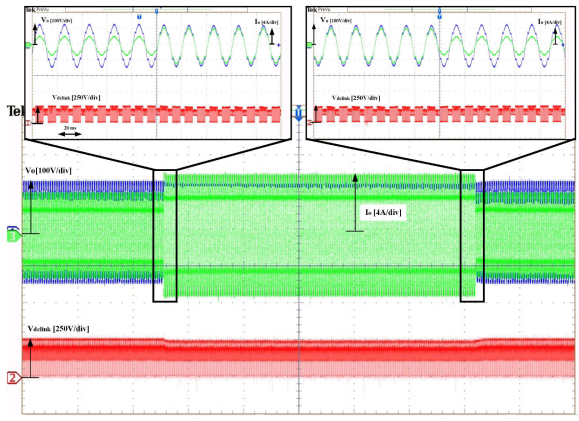

Fig. 20. Experimental results for transient response of system for step change in load.

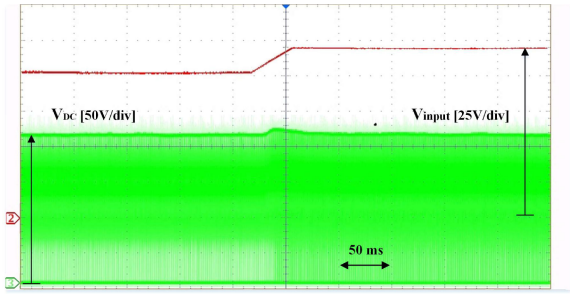

Fig. 21. Experimental result demonstrating transient response of system for change in source voltage.

to the steady-state performance of the dc-link voltage and the output voltage, while Fig. 17(b) presents the current flowing through the inductor (L1) and the voltage waveforms across the capacitors C_1 and C_2 in steady state (Fig. 1).

The waveforms of the output voltage and the load current in the steady-state condition and the reactive power handling capability of the converter are illustrated in Fig. 18. The figure shows the converter output for resistive and lagging power factor loads. There is a slight dip or flatness in the output voltage of the converter. This is due to the occurrence of the shoot-through mode along with the active voltage vector around those transition periods.

The performance of the converter in terms of suppressing the leakage current is shown in Fig. 19. The top and bottom traces, respectively, show the leakage current and the CMV across the parasitic branch. It is evident that the proposed modulation technique is capable of suppressing the leakage current and reducing the high-frequency variation in CMV. It may also be noted that the maximum value of the leakage current is only 20 mA, which is well below the German VDE 0126-1-1 grid standards.

The dynamic performance of the proposed power converter is presented in Figs. 20 and 21. Fig. 20 shows the dynamic behavior of the system against a sudden load disturbance. The load current is suddenly increased from 2 to 4 A, and then back to 2 A after a while. It can be observed that, when the load is changed, the dc-link of the converter is regulated at the desired value by the control system shown in Fig. 4. Fig. 21 shows

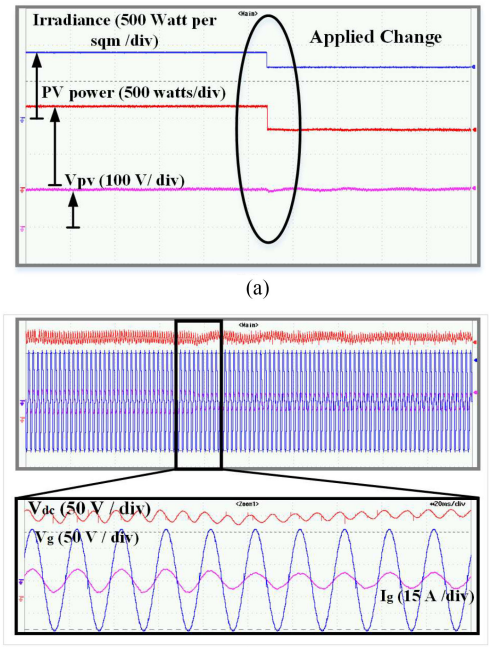

Fig. 22. Results for the grid-connected PV system. (a) Dynamics of input side parameters irradiance, PV array power, and voltage across PV array. (b) Dynamics of output side parameters peak dc-link voltage, grid voltage, and current, respectively.

the dynamic response of the converter, when it is subjected to a sudden source disturbance. The control system (Fig. 4) maintains the dc-link voltage at the desired value when the input voltage is suddenly changed from 100 to 120 V. Thus, the steady-state and the dynamic performance of the proposed converter are verified experimentally in the standalone mode of operation.

Further, as in the work reported in [32], the performance of the proposed converter in the grid-connected mode is assessed with real-time simulation studies using the Opal-RT 4500 real-time simulator platform. The real-time simulation results are presented in Fig. 22. Fig. 22(a) shows that, following the change in irradiance (from 900 to 700 W/m^2), both PV power and the PV voltage change. The MPPT algorithm then quickly restores the PV voltage by adjusting the shoot-through time. This action regulates the dc-link voltage as shown in the top trace of Fig. 22(b). The decrease in the PV current causes a corresponding change the current injected by the converter into the grid. These real-time simulation results reinforce the results obtained with the offline simulations in demonstrating the effectiveness of the proposed topology for standalone-/grid-connected PV applications.

The common mode parameters of the system in grid-connected mode are shown in Fig. 23. The waveforms of CMV (V_{CMV}), voltage across parasitic capacitor (V_{CPV}), and the leakage current (i_{leakage}) can be observed, respectively. It may be noted that the proposed control scheme works well in grid-connected mode keeping the leakage current ($i_{\mathrm{leakage,\ rms}} = 22$ mA) of proposed converter well under the German standards VDE-0126-1-1($i_{\mathrm{leakage,\ rms}} \leq 300$ mA).

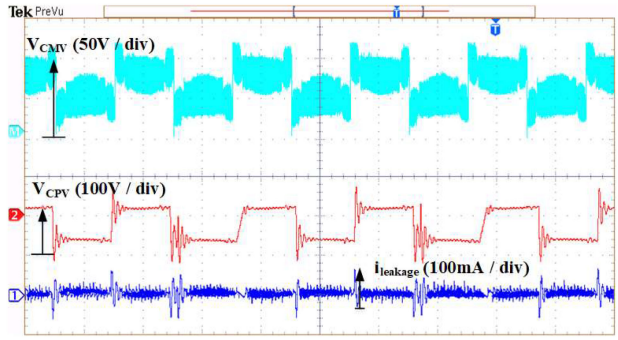

Fig. 23. Results for common mode properties during grid-connected mode.

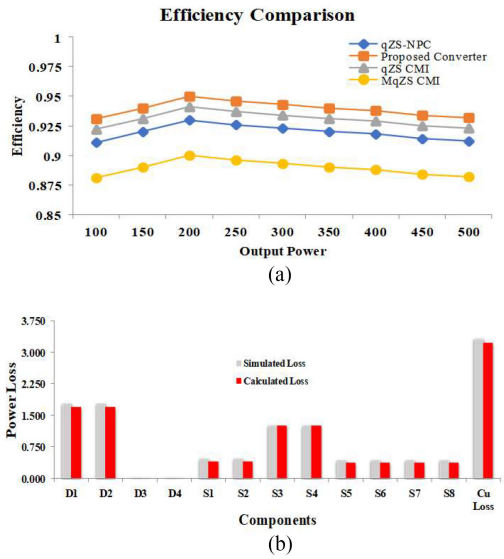

Fig. 24. Efficiency comparisons of various qZS-based inverters. (a) Efficiency vs. power output for various converter. (b) Comparison graph between calculated loss and simulated loss.

C. Efficiency Curve

The power-efficiency curves for the converter topologies considered in the previous section for comparative analyses are presented in Fig. 24(a). It is observed that the maximum efficiency of around 95.3% can be achieved by the proposed topology. The efficiencies of all of the power converters, which are being compared, are estimated using the thermal module of the Powersim software which imports the real characteristics of the switches and the passive components as described in [33]. The performance of these converters are evaluated at various loads keeping the input voltage ($V_{\mathrm{in}} = 100$ V), the modulation index ($m = 0.7$), and the shoot-through duty factor ($D_{\mathrm{sh}} = 0.27$) constant. The losses of the converter were calculated using the method provided in [26] and [30]. From Fig. 24(b) , it is evident that the calculated and simulated loss values agrees well with each other which proves the validity of efficiency curve. Though the numbers of the passive components are the same for all of these single-phase topologies (Table II), the proposed power converter displays a higher efficiency due to the reduced number of switching devices and the nonconduction of the internal diodes during the free-wheeling period.

V. Conclusion

A new qZS-based five-level inverter topology has been proposed in this article. The proposed converter is essentially a single-stage boost converter, consisting of a dual-qZS structure at the input side and the connection of an NPC arm and the T-type arm at the output side. It supports the freewheeling of power without using any of the anti-parallel diodes of the active switches. This feature, along with its single-stage boosting capability, improves the efficiency and the reliability of the converter. The modulation technique adopted in this article, along with the split filter at the output, reduces the leakage current by reducing the high-frequency variation across the parasitic coupling capacitance. Simulation and experimental results indicate that the leakage current is well within the limits stipulated by the VDE 0126-1-1 grid standards.

The steady-state and the dynamic performances of the proposed power converter, in the standalone mode of operation, are assessed by carrying out offline simulation studies and experimentally verifying them with the aid of a laboratory prototype. For the grid-connected mode of operation, real-time simulation studies are carried out to validate the same.

To sum up, it is shown that the proposed single-phase, five-level inverter topology displays the features of 1) single-stage boosting, 2) reactive power handling capability, 3) low leakage current, and 4) higher efficiency compared to the other comparable topologies. Owing to these advantages, it is envisaged that this converter could be an attractive proposition for PV generation.

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