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Floating-capacitor based inverter for open-ended winding induction motor drive with fault-tolerance

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ABSTRACT

Floating-capacitor-based nine-level inverter topology for open-ended winding induction motor (OWIM) drive is presented in this paper. The proposed multilevel inverter topology (PMLIT) essentially consists of four three-phase two-level voltage source inverters (VSI), three isolated DC sources and a floating-capacitor (FC). Out of four inverters, three inverters are fed from DC sources, and the fourth inverter is connected with the FC. The advantage of the PMLIT is that the maximum output voltage will be twice the source voltage with nine levels across each phase winding. The PMLIT employs least number of components which makes the inverter cost-effective and has lowered control complexity. The PMLIT can deliver seven, five or three-level output voltage with a decrease in modulation index. Conventional sinusoidal pulse-width modulation (PWM) techniques can be employed to generate switch-gate pulses. The intermediate-voltage levels are realised by proper charging and discharging of the FC. The performance of the PMLIT under possible switch faults is investigated, and modified switching logics are proposed to deliver a balanced supply for the OWIM drive in post-fault operation. Simulations are performed in the MATLAB/Simulink environment, and an experimental setup is designed to validate the simulations, and the results are presented.

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KEYWORDS
Nine-level inverter; Open-ended winding; floating capacitor; Switch-faults; Fault-tolerance

1. Introduction

The concept of multilevel power converters has evolved in the late 1960s, and since then, many multilevel inverter (MLI) topologies were proposed (Lai et al., 1996). Among them, specifically three inverters, namely, the cascaded H-bridge (CHB) inverter, the neutral-point-clamped (NPC) inverter and the flying-capacitor inverter, are acknowledged as conventional topologies. These topologies are the utmost used voltage source inverters in the industry present day, and each of them have their own merits and demerits (Massoud et al., 2003). Apart from aforementioned conventional multilevel topologies, numerous other MLI topologies have been proposed (Rodriguez et al., 2002; Zhang et al., 2020; Saeedian et al., 2019 & Ramaiah et al., 2020). The trend of developing MLIs for high-power medium-voltage drives applications have led to the evolution of numerous novel topologies. Dual inverter configuration is one more topology other than the conventional

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topologies that is widely accepted in industrial applications. In this topology, the multi-level output voltage structure is accomplished by feeding the motor stator windings from both ends through the inverters (Stemmler & Guggenbach, 1993). Different control schemes were proposed for dual inverter topology (Jia et al., 2020; Pratibha Naganathan et al., 2015, & Srinivasan et al., 2010), and following years witnessed the progress of numerous different MLI topologies belonging to this category in (Kshirsagar et al., 2018 ; K. Wang et al., 2017& Rajeevan et al., 2011).

In drive applications, MLIs are preferred because with an increase of levels in the output voltage, the total harmonic distortions will be reduced and eliminate the need of larger sized filters. However, MLIs when designed for higher number of voltage levels become complex and bulky due to larger component count which shows huge impact on reliability of the system; hence, the industry is reluctant to such MLIs since reliability is also an important concern (Mondal et al., 2009 & Rajeevan et al., 2013). This necessitates the designing of MLIs for higher number of voltage levels with least possible components (Gupta et al., 2016). Increase in components count of MLIs makes it less reliable because fault in even a single switch leads to shutdown of the entire system. Several topologies with tolerance for faults in switches in drive applications were proposed in (Bhaskar et al., 2020 & Jannati et al., 2017). Various schemes for identifying switch faults as well as diagnosis of the faults have been proposed in (Farhadi et al., 2017 & Salem et al., 2020).

MLI topologies with fault-tolerance capability based on redundant and non-redundant elements are presented in the literature. In non-redundant topologies, if fault occurs in any switch of the inverter, the entire leg of the inverter is to be isolated and the corresponding motor terminal is to be opened. As a consequence, the motor operates with an unbalanced supply and hence requires change in control scheme to continue the operation of the drive (Jannati et al., 2017; Naganathan & Srinivas, 2020; Narender Reddy & Pradabane, 2019; Raj et al., 2018; Narender Reddy & Pradabane, 2020;). Topologies with redundant elements are expensive, require larger space and are less reliable due to more component count. A MLI topology with flying capacitor and NPC is presented in (Ceballos et al., 2011), in which the fault tolerance capability is achieved by employing a substitute for the faulty-leg. Such fault tolerant MLI topologies with redundant legs are presented in (B. Wang et al., 2020; Jalhotra et al., 2020 & Pires et al., 2017). In the topology presented in (Welchko et al., 2004), the authors presented different types of redundant topology of an inverter with fault-tolerance capability that can be achieved by modifying the hardware circuit, with an increase in the cost of the circuit by 50% with a reduced output power capacity of 58%.

A nine-level inverter topology for OWIM drive with fault-tolerance to switch open-circuit (OC) and short-circuits (SC) is presented in this paper. The PMLIT is configured with least number of switching devices and is intended for an induction motor with six terminals of stator winding brought out. In this topology, the three windings of the induction motor are fed from three three-phase two-level inverters along with the floating-capacitor (FC) bridge. The PMLIT employs three isolated DC voltage sources each of a voltage $V_{DC}/2$, and the FC is utilised to realise intermittent voltage levels. The conventional modulation techniques are employed for switch gate-pulse generation, and the control scheme is designed to obtain intermittent voltage levels by charging and discharging of the FC from all the three-phases. The PMLIT employs lower voltage rating isolated dc sources and lower number of components than conventional topologies.

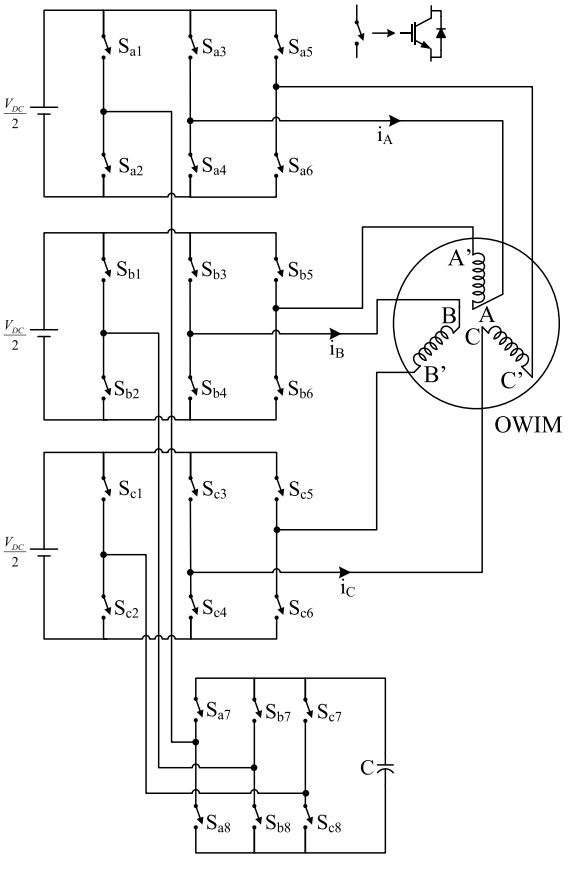

Figure 1. Proposed MLI topology.

2. Proposed floating-capacitor-based fault-tolerant MLI topology

The proposed FC-based MLI for OWIM drive is designed based on conventional three-phase two-level voltage source inverters (VSIs) and is illustrated in Figure 1. The PMLIT is designed with four VSIs and a FC. Out of the four inverters, three inverters are connected to the phase windings of the OWIM drive and each inverter is fed from an isolated dc source, whereas the fourth inverter is connected across a FC. Advantage of the PMLIT is that the maximum output voltage is twofold the magnitude of source voltage which is obtained by connecting the sources in series to realise the maximum output voltage across each phase. Hence, the magnitude of the dc sources required will be $V_{DC}/2$ (where V_{DC} is the magnitude of the source voltage required by a conventional two-level inverter); hence, energy sources with low output voltage such as solar photovoltaic systems or fuel cells can be employed. Also the number of active switching elements is only 24 which are minimum for nine-level inverters feeding OWIM drives.

In PMLIT, the six switches (S_{a1} to S_{a6}) in the three-phase two-level VSI along with switches (S_{a7} and S_{a8}) in the first leg of FC bridge establish inverter-a. Likewise, switches S_{b1} through S_{b8} establish inverter-b and switches S_{c1} through S_{c8} establish inverter-c. The connections in the PMLIT are done as follows: the mid-point of the switches S_{x1} and S_{x2} of

inverter-x is considered as connection port-1, likewise the mid-point of the switches S_{x3} and S_{x4} is considered as connection port-2 and the mid-point of the switches S_{x5} and S_{x6} is considered as connection port-3. The midpoint of the switches S_{x7} and S_{x8} is considered as connection port-4 of inverter-x (where x ϵ a, b, c). The connection port-1 of each inverter is connected to its connection port-4. Connection port-2 of each inverter is coupled to one end of phase windings (namely A, B and C) and port-3 is connected to the other ends of the windings (A′, B′ and C′). The scheme of connection for phase windings is that the end terminals of each winding are connected to two adjacent inverters so as to receive supply from both ends from two different inverters to produce nine-level voltage across each winding of the OWIM. For example, consider phase winding-A, terminal A is connected to connection port-2 of inverter-a and terminal A′ is connected to connection port-3 of inverter-b. Likewise, the other two phase windings are also connected in the same method.

The switching states to generate output voltage with nine levels, namely $\pm V_{DC}$, $\pm 3V_{DC}/4$, $\pm V_{DC}/2$, $\pm V_{DC}/4$, 0, across the phase winding terminals A-A′ of OWIM drive are illustrated in Table 1. It can be clearly observed from Table 1 that the FC is charged and discharged during the voltage levels $\pm 3V_{DC}/4$ and $\pm V_{DC}/4$ of output voltage across phase winding-A. The switching states are selected such that the time period is maintained equally for charging and discharging of the FC within a complete cycle of voltage waveform.

For the satisfactory operation of the PMLIT, the FC is charged and discharged to realise the intermittent voltages. The charging of FC is during the positive cycle and is discharged for the same duration of time in the negative cycle of the output voltage as presented in Table 1. Considering that the output voltage and the current are symmetrical, the average current (AVG[i_c]) flowing through the FC during the voltage levels $\pm 3V_{DC}/4$ and $\pm V_{DC}/4$ with a load impedance of Z can be given as:

$$\mathrm{AVG}\left[i_c^{+}\right]_{V_{DC}/4} = \frac{\frac{V_{DC}}{2} - V_c}{Z} \tag{1}$$

Table 1. Switching states for nine-level voltage generation across phase winding-A.

Voltage level	Inverter-a			Inverter-b			Capacitor state
	S_{a1}	S_{a3}	S_{a7}	S_{b1}	S_{b5}	S_{b7}	
V_{DC}	0	1	0	1	0	0	No change
$3V_{DC}/4$	0	1	0	1	0	1	Charging
	0	0	1	1	0	0	Discharging
$V_{DC}/2$	0/1	0/1	1	1	0	0	No change
	0/1	0/1	0	1	0	1	
$V_{DC}/4$	1/0	1/0	1/0	1/0	1/0	0	Discharging
	0/1	1	1/0	1	1/0	0/1	Charging
0	1/0	1/0	1/0	1/0	1/0	1/0	No change
	0/1	0/1	1/0	0/1	0/1	1/0	
$-V_{DC}/4$	1	0/1	1/0	0/1	0	0/1	Charging
	0	0	0	0/1	0/1	1	Discharging
$-V_{DC}/2$	1	0/1	0	0	0/1	0	No change
	1/0	0	1	1/0	1	1	
$-3V_{DC}/4$	1	0	0	0	0	1	Discharging
	1	0	1	0	1	0	Charging
$-V_{DC}$	1	0	0	0	1	0	No change

$$\mathrm{AVG}\left[i_c^-\right]_{3V_{DC}/4} = \frac{\frac{V_{DC}}{2} + V_c}{Z} \tag{2}$$

$$\mathrm{AVG}\left[i_c^+\right]_{3V_{DC}/4} = \frac{V_{DC} - V_c}{Z} \tag{3}$$

$$\mathrm{AVG}\left[i_c^-\right]_{V_{DC}/4} = \frac{V_c}{Z} \tag{4}$$

Hence, the resultant charge (Q) that is supplied or absorbed during a time period (T) can be expressed as

$$\begin{aligned} Q &= \left\{ \mathrm{AVG}\left[i_c^+\right]_{V_{DC}/4} + \mathrm{AVG}\left[i_c^+\right]_{3V_{DC}/4} - \mathrm{AVG}\left[i_c^-\right]_{V_{DC}/4} - \mathrm{AVG}\left[i_c^-\right]_{3V_{DC}/4} \right\} * T \\ &= \left\{ \frac{V_{DC} - 4V_c}{Z} \right\} \end{aligned} \tag{5}$$

Assuming half wave symmetry of the output current, the average charge Q over a cycle is zero. Considering the value of Q as zero in the equation (5) will result as $V_c = 0.25V_{DC}$, where the voltage rating of each source is $0.5V_{DC}$ in the PMLIT. The direction of load current defines the charging and discharging states of FC and does not require any additional complex control circuit. A constant voltage of $0.25V_{DC}$ is maintained across the FC by selecting proper switching states that will provide equal time periods for charging and discharging.

The voltage across the phase windings of the OWIM is determined by the switching states of the switches. Considering that the blocking state of a switch is represented by binary variable 0 and its conduction state is represented by variable 1. Considering $\hat{S}_{a1} = S_{a2}$, $\hat{S}_{a3} = S_{a4}$, $\hat{S}_{a5} = S_{a6}$, $\hat{S}_{a7} = S_{a8}$, $S_{a3} = S_{a5}$ and $S_{a4} = S_{a6}$, the voltage across the phase winding terminals A-A′ of OWIM can be written as

$$V_{AA'} = \frac{V_{DC}}{4} \left\{ \begin{array}{c} 2\hat{S}_{a7}\left[\hat{S}_{a1}S_{a3} - S_{a1}\hat{S}_{a3}\right] + \hat{S}_{a3}S_{a7}\left[S_{a1} - \hat{S}_{a1}\right] + 2\hat{S}_{b7}\left[S_{b1}\hat{S}_{b5} - \hat{S}_{b1}S_{b5}\right] + \\ \hat{S}_{b5}S_{b7}\left[\hat{S}_{b1} - S_{b1}\right] \end{array} \right\} \tag{6}$$

3. Modulation scheme

Sinusoidal pulse width modulation (SPWM) technique with modified reference wave and level shifted carriers is employed to generate gating pulses for the switches in the PMLIT. The high frequency carrier waves are compared with the sinusoidal reference signal (V_{Ref}) of fundamental frequency to generate the gating pulses. In conventional SPWM technique, the modulation index (M_a) is defined by the magnitude of the sinusoidal reference signal. If the magnitude of the V_{Ref} is taken as unity, then $M_a = 1$ and the magnitude of the carrier waves, here in this case, is half the magnitude of the reference voltage. With sinusoidal reference wave, the PMLIT requires four level shifted carriers with phase disposition. Hence, to reduce the computational encumbrance on the processors of digital platforms such as dSPACE and DSPs, the number of carriers required can be reduced[31]. The sinusoidal reference signal is modified to reduce the

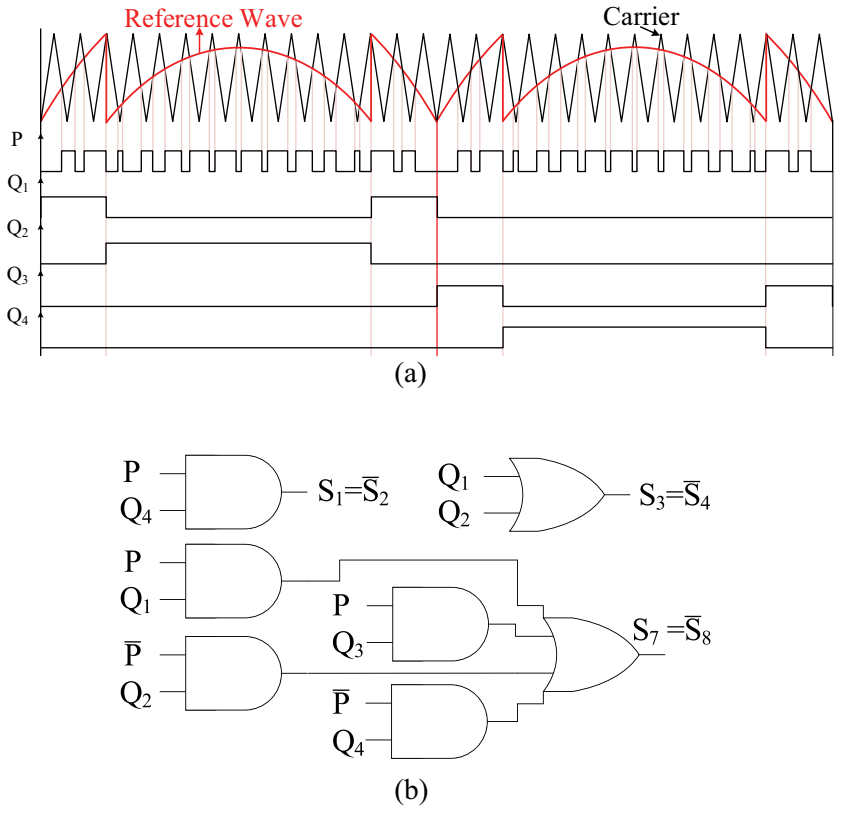

Figure 2. Modulation scheme: A, SPWM with modified sinusoidal reference and single carrier wave; B, Switching logics for switch-gate pulses.

need of carriers and is employed to generate the gating signals and are dispensed using dSPACE 1104 for the switches in the PMLIT. The SPWM with modified reference employed to produce switch gate pulses is illustrated in Figure 2a. Switching logics involved to generate gating pulses for the switches of the PMLIT are illustrated in Figure 2b.

4. Operation of the inverter during inverter switch faults

In the PMLIT, switches Sa1 through Sa8 constitute inverter-a, and out of these eight switches, four switches i.e., switches Sa3 through Sa6 will guide the polarity generation of the output voltage. Similarly, the other four switches will act as level generating elements and are connected together to form the neutral path for the PMLIT. Since the number of switches employed are least, fault in any one switch will greatly affect the output voltage and current fed to the OWIM. If a fault occurs in switches in FC bridge, then the PMLIT can be made to operate with rated output power as a five-level inverter, and if fault occurs in any other switch, then the PMLIT is operated as a five-level inverter with half the rated power. Therefore, to continue the operation of the PMLIT with switch-faults, Ma has to be reduced to 0.5 and hence operated as a five-level inverter with modified switching logic

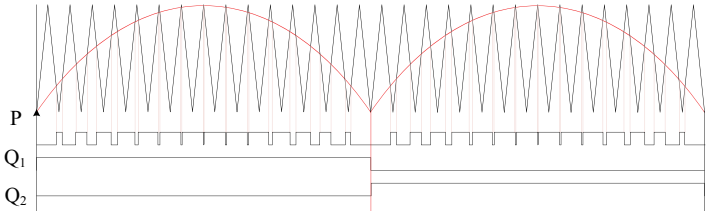

Figure 3. Modulation switching scheme with Ma = 0.5 and corresponding gate pulses.

Table 2. Modified switching logic under switch fault conditions.

Switch with Open-circuit fault	Inverter-a Switch					
	I. S_{a1}	II. S_{a2}	III. S_{a3} or S_{a5}	IV. S_{a4} or S_{a6}	V. S_{a7}	VI. S_{a8}
S_{a1}	0	$P^*(Q_1+Q_2)+\bar{P}^*(Q_1+Q_2)$	$P^*Q_2+\bar{P}^*(Q_1+Q_2)$	P^*Q_1	$P^*(Q_1+Q_2)$	$\bar{P}^*(Q_1+Q_2)$
S_{a2}	$P^*(Q_1+Q_2)+\bar{P}^*(Q_1+Q_2)$	0	$P^*Q_1+\bar{P}^*(Q_1+Q_2)$	P^*Q_1	$P^*(Q_1+Q_2)$	$\bar{P}^*(Q_1+Q_2)$
S_{a3} and S_{a5}	P^*Q_2	$P^*Q_1+\bar{P}^*(Q_1+Q_2)$	0	$P^*(Q_1+Q_2)+\bar{P}^*(Q_1+Q_2)$	$P^*(Q_1+Q_2)$	$\bar{P}^*(Q_1+Q_2)$
S_{a4} and S_{a6}	$P^*Q_1+\bar{P}^*(Q_1+Q_2)$	P^*Q_2	$P^*(Q_1+Q_2)+\bar{P}^*(Q_1+Q_2)$	0	$P^*(Q_1+Q_2)$	$\bar{P}^*(Q_1+Q_2)$
S_{a7}	$P^*Q_2+\bar{P}^*(Q_1+Q_2)$	P^*Q_1	$P^*Q_1+\bar{P}^*(Q_1+Q_2)$	P^*Q_2	0	$P^*(Q_1+Q_2)+\bar{P}^*(Q_1+Q_2)$
S_{a8}	$P^*Q_2+\bar{P}^*(Q_1+Q_2)$	P^*Q_1	$P^*Q_1+\bar{P}^*(Q_1+Q_2)$	P^*Q_2	$P^*(Q_1+Q_2)+\bar{P}^*(Q_1+Q_2)$	0

Note: Where P is the switching pulse and $\bar{P}$ is its complementary

(MSL) presented in Table-2 to ensure continuity in the supply for the OWIM. The SPWM scheme with Ma = 0.5 and the corresponding pulses are presented in Figure 3.

The switches in the inverter are prone for either open or short circuit faults. The PMLIT is capable of feeding the load during such switch fault conditions. In any of the switch of any inverter if an OC fault occurs, the MSL is designed in such a way that the modulation index is reduced to 0.5 and the healthy switch in the leg of faulty switch is to be turned on completely. The MSL produces switching pulses for the available healthy switches to produce balanced three-phase output voltage across all the phase windings of the OWIM. For example, if switch Sa1 is faulted with OC, then the remaining switches in the inverter-a are fed with switching logics presented in column-I in the Table 2. Likewise, the same switching logic would be given to corresponding switches in other two inverters as well to create identical switching of the inverters to produce balanced three-phase output voltages.

Similarly, if any switch in any of the inverters is faulted with a SC, immediately the healthy switch in such leg is turned-off to prevent a dead short across the source. The PMLIT is made to run as a five-level inverter by applying MSL provided in Table 2. The switching logics that are to be applied for the available healthy switches in such an inverter are the same switching logics that are applied for OC faults in other switches in the same leg. For example, if switch Sa1 is faulted with a SC, then the switching logic for Sa2 OC provided in column II of Table 2 is to be employed because switches Sa1 and Sa2

Table 3. Comparison of the PMLIT with existing MLI Topologies feeding OWIMs.

MLI Type	No. of Levels	No. of Switches	No. of Drivers	No. of Diodes	No. of Sources	No. of Capacitors	Component Count	Control Complexity
NPC	9	48	48	168	1	8	273	Very high
FC	9	48	48	48	1	84	229	High
CHB	9	48	48	48	12	0	156	Low
[15]	7	48	48	60	6	6	168	Very high
[12]	7	36	36	36	2	6	116	Low
[16]	9	36	36	36	2	6	116	High
[14]	9	36	36	36	1	8	117	High
[13]	9	24	24	24	1	6	79	High
[24]	9	24	24	24	3	6	81	Low
[25]	9	24	24	24	3	3	78	Low
PMLIT	9	24	24	24	3	1	76	Low

operate in complementary to each other. Therefore, the switching logic for SC fault in a switch is the same as that employed for OC fault of its complementary switch.

5. Assessment of the proposed mli topology

The PMLIT is related with conventional topologies and also with similar existing topologies feeding OWIM drives in terms of total number of components and control complexity and is demonstrated in Table 3. From Table 3, it is evident that the number of components for the PMLIT are minimum and control complexity is low in comparison with other existing nine-level MLI topologies feeding OWIM drives. Additionally, to evaluate the lucrative advantage of the PMLIT regarding inverter cost, an assessment depending on the components cost involved in the inverter design is carried out and is presented in Table 4. For this assessment, a case study is carried out considering a 2 kW load fed with an input voltage of 200 V. The component ratings are chosen according to the topology configuration considered for comparison[30]. The cost of each component used and overall cost of the topologies under comparison are enlisted in Table 4. This evaluation gives the same significance to the total number of components, their total blocking voltage (TBV) and peak inverse voltage (PIV) while considering voltage and current ratings without any margin. On the other hand, components with lower voltage rating are selected in view of their current ratings. From Tables 3 and 4, it is clear that the PMLIT employs the least number of components with which the cost of the inverter and the control complexity are lowered and makes its usage viable.

6. Determination of capacitance

The intermittent voltage levels are realised by a FC; hence, the value of capacitance required is to be evaluated. The peak value of load current (I_p), peak-to-peak ripple voltage (ΔV) and switching time period (ΔT) define the value of capacitance required. Considering these parameters, the minimum capacitance value (C) required and can be determined as[31]

$$I_p = C\frac{dv}{dt} = C$$

Table 4. Cost comparison of the PMLIT with other nine-level inverter topologies feeding OWIMDs.

Part	Part Number	Ratings	Unit Price*($)	NPC	FC	CHB	[15]	[12]	[16]	[14]	[13]	[24]	[25]	PMLIT
MOSFETs	IRFP140PBF	100 V, 20 A	2.03					12	12	24	12	24	12	18
	IRFIZ34GPBF	60 V,20 A	1.34	48	48	48	48	24	24	12	12		12	6
Diodes	STPS20SM60D	60 V, 20 A	1.42	168			12							
Capacitor	LLG2D222-MELC40	200 V, 2.2 mF	8.3							2	3			
	LLS2A222-MELA	100 V, 2.2 mF	3.85	8	84	0	6	6	6	6	3	6	3	1
Gate driver	IR2110STRPBF		2.86	48	48	48	48	36	36	36	24	24	24	24
Total cost ($)				470.96	525	201.6	164.22	182.58	182.58	207.46	145.53	140.46	120.63	117.07

Courtesy: www.galco.com, www.digikey.in. * Price may vary subjected to market growth.

$$C = I_{p'} = \frac{I_p}{*f_{sw}} \tag{7}$$

Where f_{sw} is the inverter switching frequency. If ΔV is to be limited to 4 V with a switching frequency of 1500 Hz, then the value of capacitance required will be 666 μF. Therefore, a capacitor of 1000 μF is employed in experimental setup.

7. Results and discussions

The PMLIT is designed such that the switches S_{x3}, S_{x4}, S_{x5} and S_{x6} (where x ϵ a, b, c) constitute polarity generator and the rest of the switches (S_{x1}, S_{x2}, S_{x7} and S_{x8}) with FC acts as level generator circuit. All these level generator circuits are assembled as a star connection and form the neutral path for the inverters. With this scheme of connection, the voltages across each phase winding will have nine levels ($\pm V_{DC}$, $\pm 3V_{DC}/4$, $\pm V_{DC}/2$, $\pm V_{DC}/4$, 0) in it with the peak value of twice the source voltage. For experimental validation, the PMLIT is fed from three isolated DC sources each of 100 V to feed 1-hp OWIM. The sinusoidal PWM technique with modified-reference wave employing single carrier wave of 1500 Hz is employed to produce gate pulses for the PMLIT. The required switch gate-pulses are generated using dSPACE 1104. Simulations are performed in the MATLAB/Simulink environment. The inverter and OWIM parameters are given in Appendix.

The experimental results for the PMLIT during normal operating conditions are illustrated in Figure 4. Figure 4a presents the phase voltages $V_{AA'}$ (blue trace), $V_{BB'}$ (red trace) and $V_{CC'}$ (green trace) across the terminals A-A′, B-B′ and C-C′ which represents phase windings A, B and C of the OWIM, respectively. The output voltage of each phase consists of nine levels, and the magnitude of each level of the voltage is equal to the magnitude of the capacitor voltage (V_C). Capacitor voltage across the FC (pink trace) and currents i_A (blue trace), i_B (red trace) and i_C (green trace) flowing through the phase windings of the OWIM at no-load condition is presented in Figure 4b. The voltage across the FC defines the magnitude of the voltage levels in the output waveform and hence is required to be constant as presented. The phase voltage $V_{AA'}$ for change in modulation index, Ma with values of 1, 0.75, 0.5, 0.25 are presented in Figure 4c. The waveform shows that the PMLIT is capable of delivering output voltage with respect to the change in modulation index. The fast Fourier transform (FFT) analysis for total harmonic distortion (THD) in the output phase voltage ($V_{AA'}$) and current (i_A) in phase A are illustrated in Figure 4(d,e) respectively. The value of THD in phase voltage and current is observed to be 9.7% and 3.8%, respectively. The voltage stress across the switches of inverter-a are illustrated in Figure 5(a,b). From Figure (5a,b), it can be observed that the switches in FC bridge with lower blocking voltage are switched at higher frequency and switches in neutral path such as S_{a1} and S_{a2} are switched at fundamental frequency. However, switches S_{a3} to S_{a6} are switched for longer time in one half cycle and remains constant for longer time in other half cycle. In other words, relatively these switches have switching instants only in one half cycle of the fundamental frequency that ensures reduced switching losses in the inverter. The implementation of system in MATLAB/Simulink environment is illustrated in Figure 6.

Although the MLIs are the best solution for generation of higher levels of voltage with lower voltage rating switches, the number of switching devices required are high. Hence,

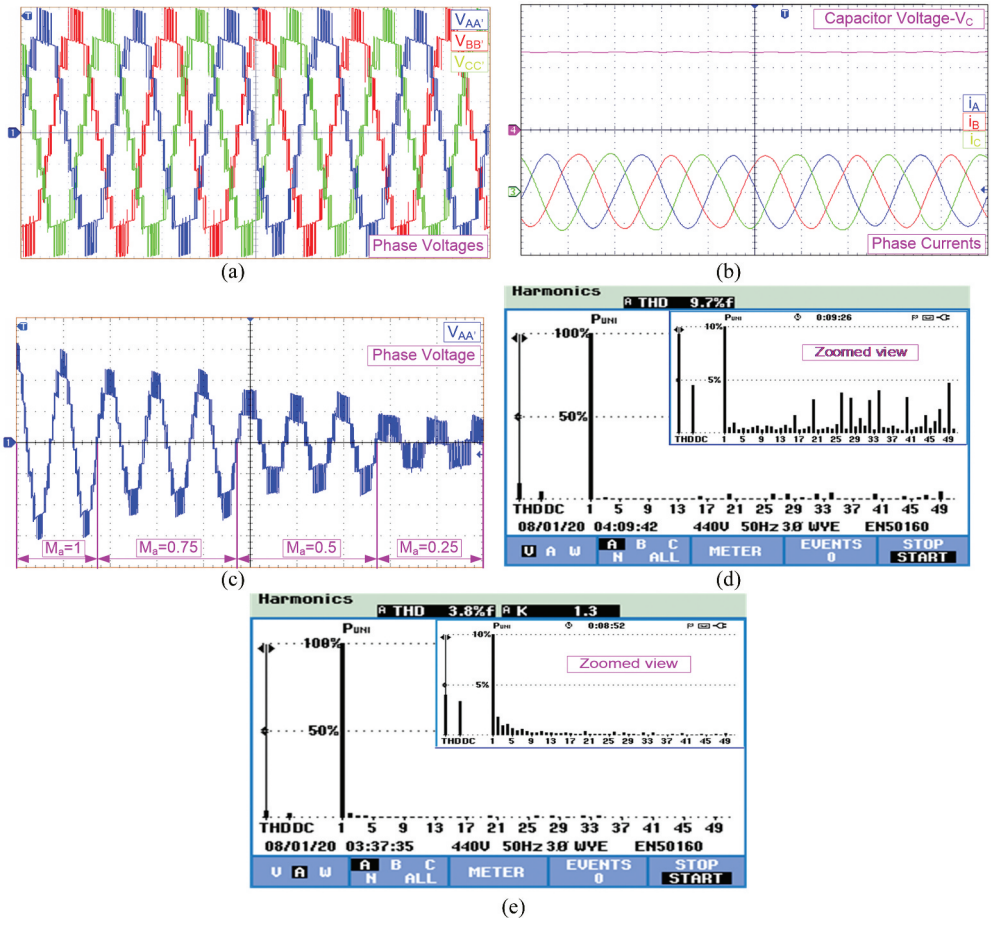

Figure 4. Experimental results of (X-axis:10 ms/div): A, Phase voltages $V_{AA'}$, $V_{BB'}$ and $V_{CC'}$(Y-axis: 50 V/div); B, Voltage (upper trace) across the floating capacitor (Y-axis: 20 V/div) and currents through three phase-windings (Y-axis: 1A/div); C, Output voltage $V_{AA'}$ with decrease in M_a; D, FFT of voltage $V_{AA'}$; E, FFT of current i_A.

fault in even a single switch would greatly affect the quality of the output and would result in supplying unbalanced three-phase voltages to the induction motor. Greater losses, a higher temperature rise of the machine, a deterioration in efficiency and a decline in generated torque are all detrimental impacts of voltage imbalance on the performance of three-phase induction motors. The reduction of the machine's rated power under unbalanced voltage is a significant consequence that was first introduced in 1963[32]. The efficiency of normal motor operating from an unbalanced supply is directly proportional to the degree of imbalance at the machine's terminals. Therefore, to overcome the effect of unbalanced voltages during switch fault conditions, the PMLIT is made to operate with MSL and does not require any extra hardware which avoids the need for redundant switching units.

In the post-fault operation, a balanced output voltage is obtained across all the phase windings by maintaining switching symmetry in all the inverters. To ensure symmetrical

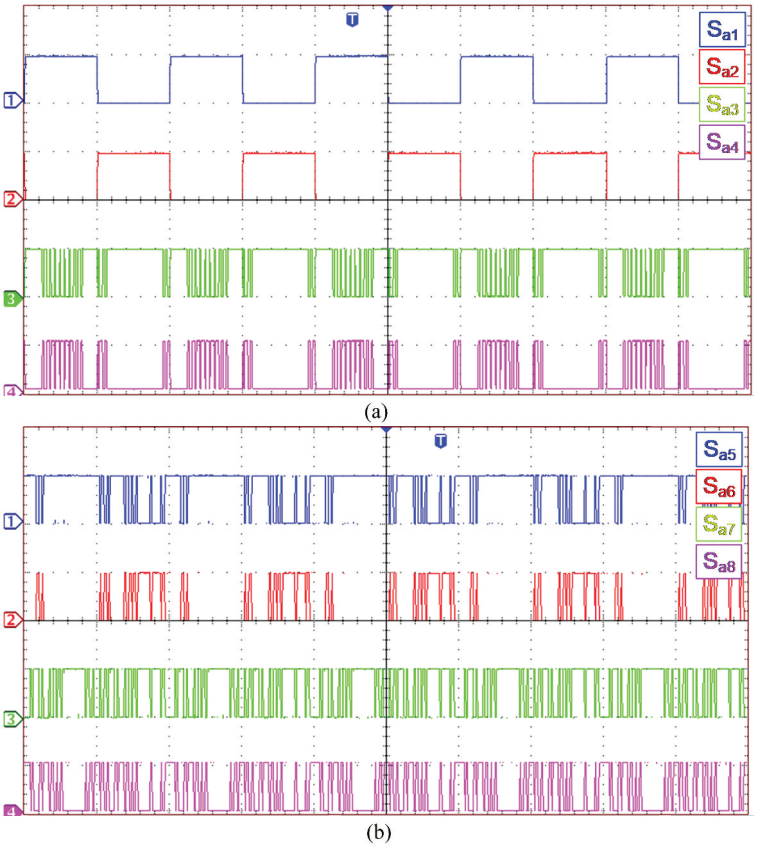

Figure 5. Experimental results for voltage stress across (X-axis:10 ms/div): A, switches S_{a1}, S_{a2}, S_{a3} and S_{a4} (Y-axis: 100 V/div); B, switches S_{a5}, S_{a6} (Y-axis: 100 V/div) and S_{a7}, S_{a8} (Y-axis: 50 V/div).

switching, some of the healthy switches are also left unused in post-fault operation. The PMLIT ensures balanced three-phase supply to the OWIM even during faults in the switches in the inverters and hence makes it reliable when used for low voltage medium power applications such as feeding motors in industrial and electric vehicular applications.

7.1. Performance of PMLIT under switch OC faults

The PMLIT is designed to yield nine-level output voltage by employing only one FC. The FC is charged and discharged through all the phases according to the switching logic, and a fault in any one switch will not disturb the capacitor voltage much. The OC fault in any one switch of this topology will result in unbalanced output voltages and thereby producing unbalanced currents in the load. The output voltages across the three phases ($V_{AA'}$, $V_{BB'}$ and $V_{CC'}$), no-load three phase currents (i_A, i_B and i_C) and voltage (V_C) across FC for OC faults in various switches of the inverter-a in the PMLIT are presented in this section.

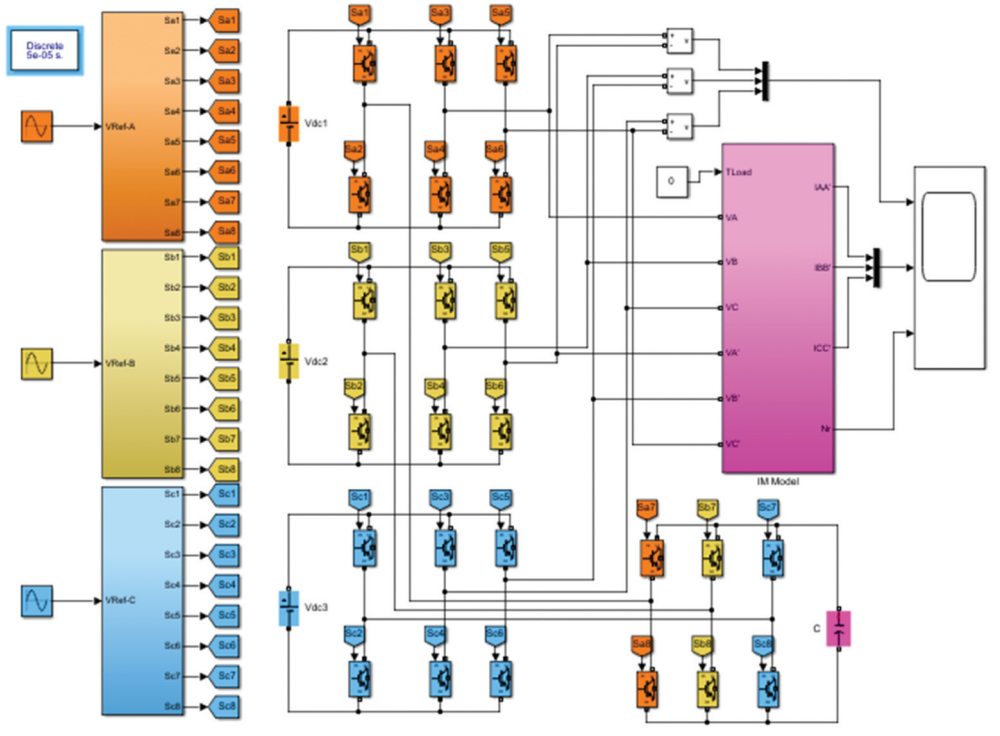

Figure 6. Implementation of the PMLIT in MATLAB/Simulink environment.

If switch S_{a1} is faulted with OC, then the voltages $V_{AA'}$ and $V_{CC'}$ get affected since the switch S_{a1} is in the neutral path of phase-A and phase-C. The three phase voltages during normal and switch S_{a1} OC condition will be as illustrated in Figure 7a. The switch fault is introduced at 50 msec, and the output voltages which were balanced three-phase nine level voltages will become unbalanced and disturbed. The positive peak of $V_{CC'}$ and negative peak of $V_{AA'}$ are affected due to this fault. However, the phase voltage $V_{BB'}$ remains unaltered momentarily and its magnitude increases as the time progresses. The FC voltage, V_C and the three phase no-load currents are presented in Figure 7b. Fault in switch S_{a1} create disturbance in the FC charging circuit and hence affects the charging voltage level of the FC. This will increase the FC voltage magnitude as the time progresses and the settle down at a magnitude equal to source voltage. Figure 8 presents the effect of switch S_{a3} OC on the output voltages, currents and FC voltage. Figure 8a presents the output phase voltages with S_{a3} OC initiated at 50 ms. Since the switch S_{a3} connects the source to phase-A winding, OC in S_{a3} affects the positive peak of $V_{AA'}$. The FC voltage and three phase no-load currents are illustrated in Figure 8b. Since the switch S_{a3} is OC, the current i_A will be a positive clamped wave and the maximum values of currents in other two phases gradually increases.

Figure 9 depicts the output voltages and currents along with FC voltage when an OC fault occurs in switch S_{a5}. The negative peak of phase voltage $V_{AA'}$ and the positive peak of $V_{CC'}$ are clamped when switch S_{a5} is open-circuited at 50 ms as illustrated in Figure 9a. Figure 9b presents FC voltage in the upper trace and the three phase currents at no-load

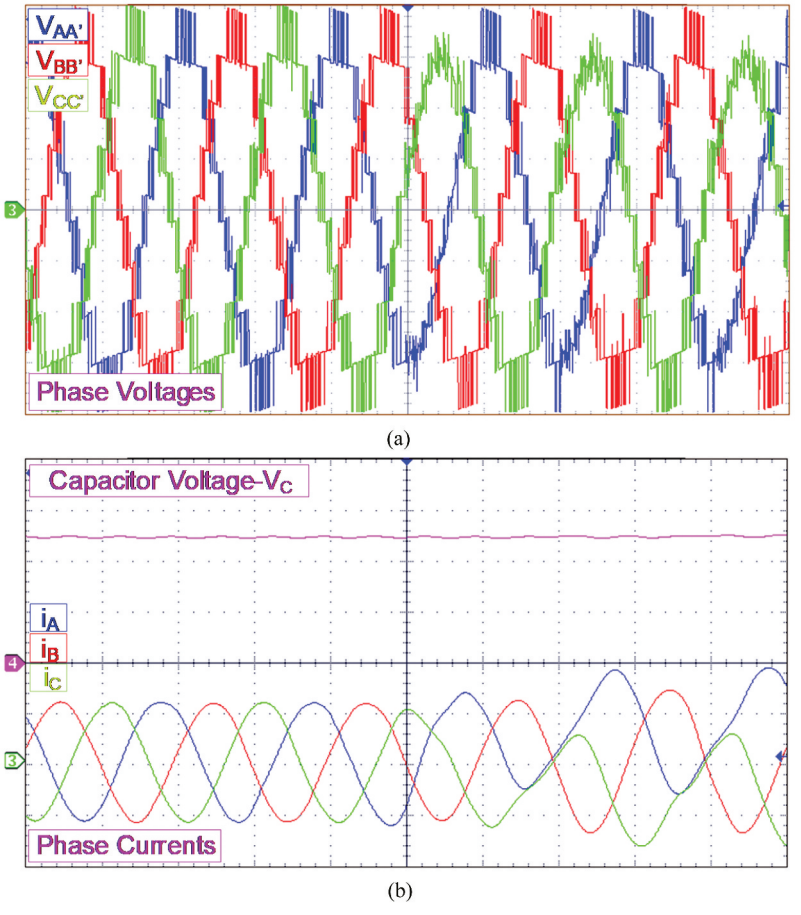

Figure 7. Waveforms of (X-axis:10 ms/div): A, three phase voltages (Y-axis: 50 V/div), B, FC voltage (Y-axis: 20 V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a1}.

in the lower traces. Since the switch S_{a5} is OC, the current i_C will be a negative clamped wave and the maximum values of currents in other two phases gradually increases. Figure 10 illustrates the output voltages and currents along with FC voltage when an OC fault occurs in switch S_{a7}. Figure 10a presents the three-phase output voltages with switch S_{a7} open-circuited at 50ms. The output voltages $V_{AA'}$ and $V_{CC'}$ get affected with this fault. Figure 10b presents FC voltage in the upper trace and the three phase currents at no-load in the lower traces. As like voltages, currents in phase-A and phase-C get affected with this fault. Faults in inverter switches will produce unbalanced voltages which will cause unbalanced currents in the phase windings of OWIM. Unbalanced currents will have impact on its performance such as increased losses, temperature rise, a reduction in torque, efficiency and the life of the motor insulation.

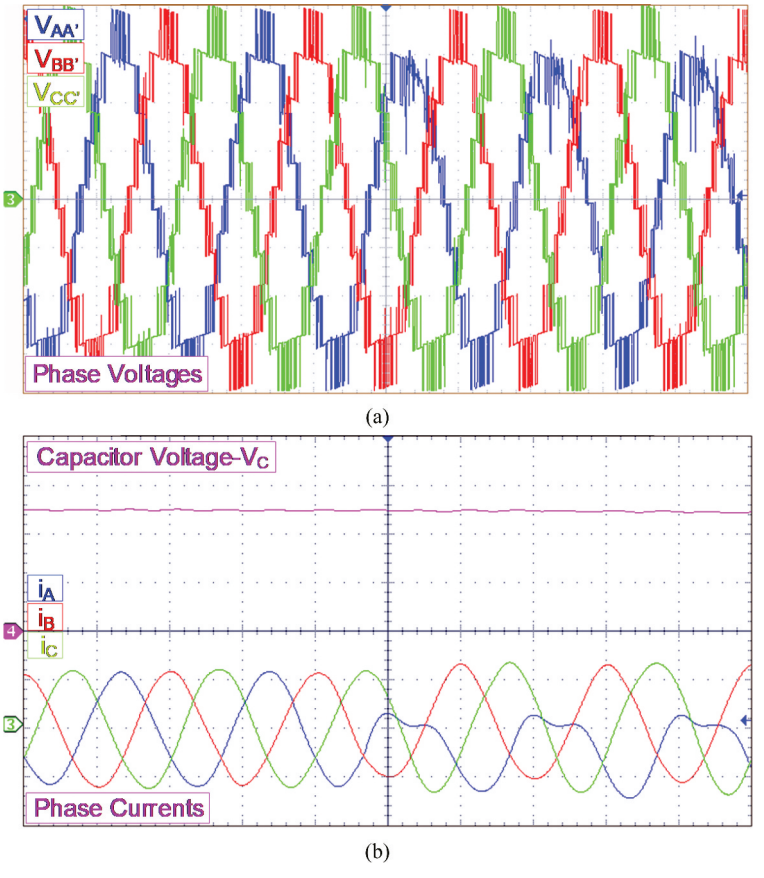

Figure 8. Waveforms of (X-axis:10 ms/div): A, Three phase voltages (Y-axis: 50 V/div); B, FC voltage (Y-axis: 20 V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a3}.

7.2. Performance of the PMLIT under switch SC faults

In the PMLIT, switch OC faults will result in unbalanced voltage at the output but an SC fault of switch in any of the inverter legs will result in a dead SC across the source when the healthy switch is turned on. Hence, whenever a SC fault occurs in any switch, then the healthy switch in such leg should be turned off completely to avoid SC of the source. This will disturb the identical switching of the inverters and unbalanced voltages will be produced at the output. To overcome this, the switching logic provided in Table 2 is to be employed.

The switching logic provided is for switch OC faults in which the logic is designed such that the healthy switch in the leg in which OC fault occurs is turned on completely in the post-fault operation. This gives an advantage in employing the same logic for switch SC faults but the complementary switch switching logic has to be employed under SC fault condition. Consider a SC fault in switch S_{a1} of inverter-a, then the switching logic under fault condition for switch S_{a2} given in column II of Table 2 is to be employed as switching logic. Similarly, the same logic is employed for SC faults in other switches in the PMLIT.

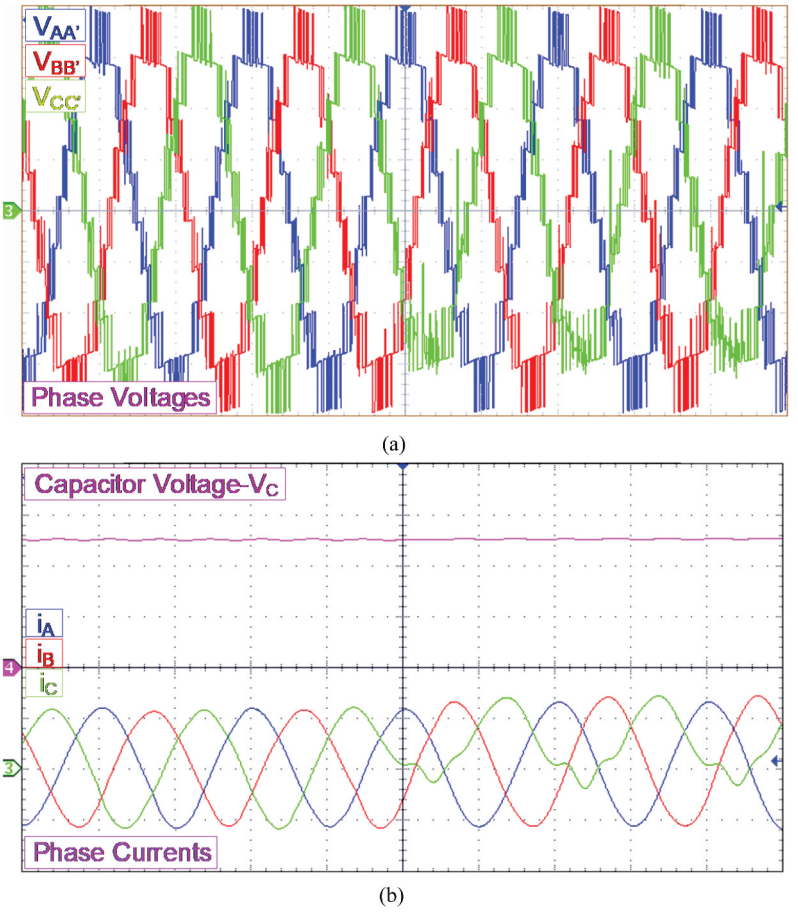

Figure 9. Waveforms of (X-axis:10 ms/div): A, three phase voltages (Y-axis: 50 V/div); B, FC voltage (Y-axis: 20 V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a5}.

7.3. Performance of the PMLIT with Modified Switching Logic (MSL)

The PMLIT is capable of operating and feeding the windings of OWIM drive even with fault in switches with MSL. The waveforms of the three-phase output voltages, currents and FC voltage with switch S_{a1} OC and with MSL for switch S_{a1} OC are presented in Figure 11. Due to OC fault in switch S_{a1}, the output voltages of phase windings connected to inverter-a namely phase-A and phase-C will be affected. The voltage across the FC is least affected because the other two phases still feed the FC. Due to fault in switch S_{a1}, in the post fault operation, the PMLIT produces five-level output voltage with reduced magnitude as illustrated in Figure 11a.

The FC voltage increases slightly more than the rated value due to OC in switch S_{a1}, and after applying the MSL, the FC voltage drops to the rated value and remains the same throughout the operation as illustrated in Figure 11b. The FFT analysis for total harmonic distortion (THD) in the output phase voltage (VAA') and current (iA) in phase-A with OC fault in switch Sa1 are presented in Figure 11(c,d), respectively. The FFT analysis for total

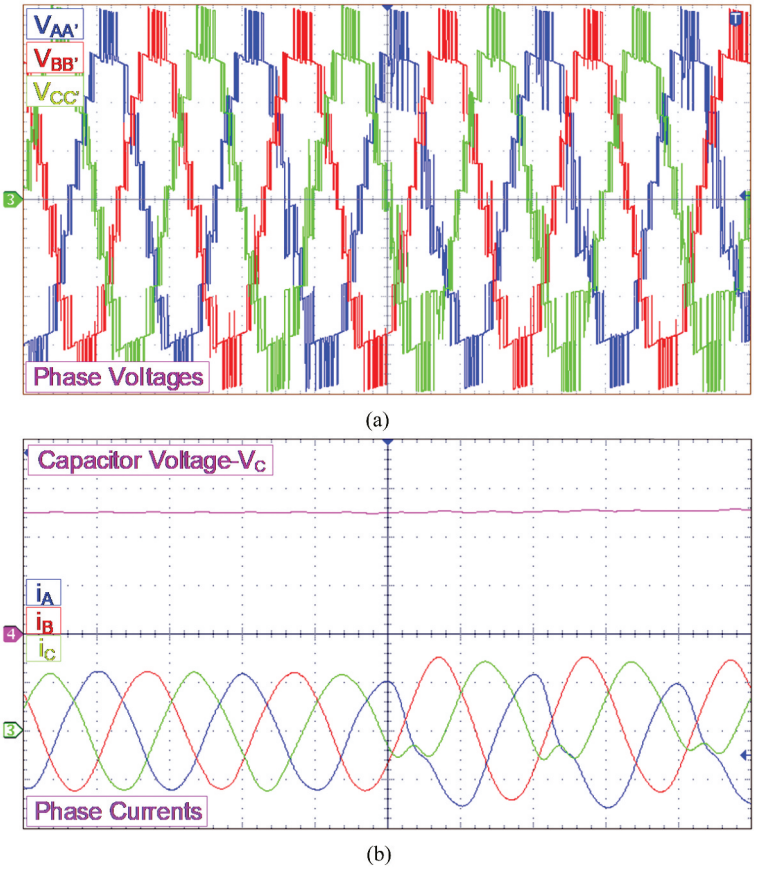

Figure 10. Waveforms of (X-axis:10 ms/div): A, three phase voltages (Y-axis: 50 V/div), B, FC voltage (Y-axis: 20 V/div) and three-phase no-load currents (Y-axis: 1A/div) with OC in switch S_{a7}.

harmonic distortion (THD) in the output phase voltage (VAA') and current (iA) in phase-A with MSL for OC fault in switch Sa1 are presented in Figure 11(e,f), respectively. Faults in switches in FC bridge i.e., S_{x7} and S_{x8} (where x ϵ a, b, c) will reduce the number of levels from nine to five in the output phase voltage with peak value twice the source voltage as illustrated in Figure 12a. With switch S_{a7} OC fault, the voltage across the FC is increased from 50 V to 75 V with greater than before voltage ripples. The rise in voltage is due to the fact that the FC gets charged from other two inverters, but the current path for phase windings of phase-A and phase-C during intermittent voltage levels is opened due to OC fault in S_{a7}.

This rise in FC voltage will also affect the other phase winding voltages as illustrated in Figure 12b. Whenever fault occurs in either switches S_{x7} or S_{x8} (where x ϵ a, b, c), then the top three switches (S_{a7}, S_{b7} and S_{c7}) or the bottom three switches (S_{a8}, S_{b8} and S_{c8}) of the FC bridge are turned on continuously throughout the operation. Subsequently, in the post fault operation with faults in switches S_{a7} or S_{a8}, the FC has no role to play and hence the voltage across the FC drops to zero over a period of time due to its internal impedance. The FFT analysis for THD in the phase voltage

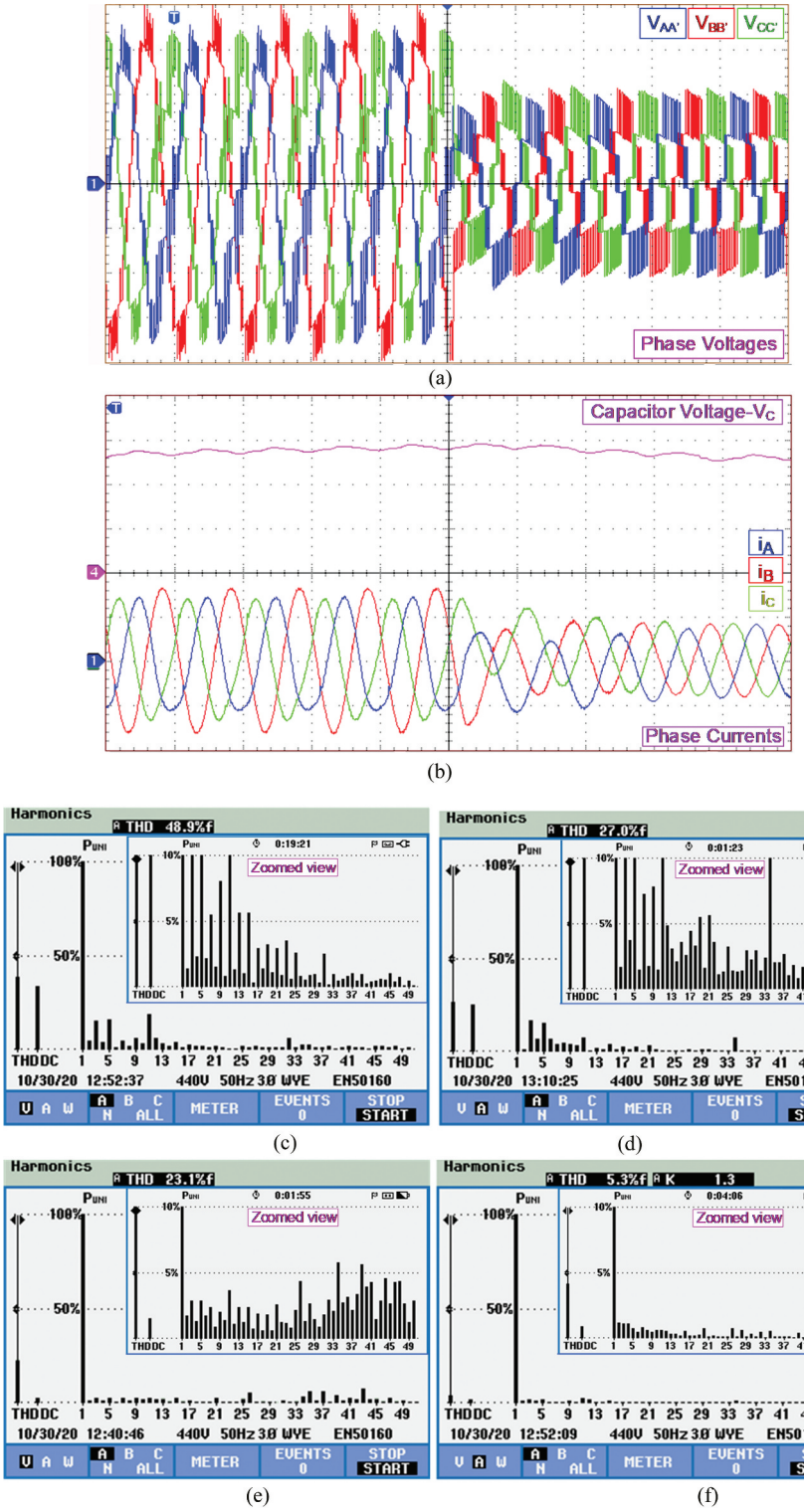

Figure 11. Waveforms of (X-axis:10 ms/div): A, Three phase output voltage (Y-axis: 50 V/div); B, FC voltage (Y-axis: 20 V/div) and three-phase no-load currents (Y-axis: 1A/div) with MSL for S_{a1} OC; C, THD for phase voltage during fault; D, THD of phase current during fault; E, THD for phase voltage after fault; F, THD of phase current after fault.

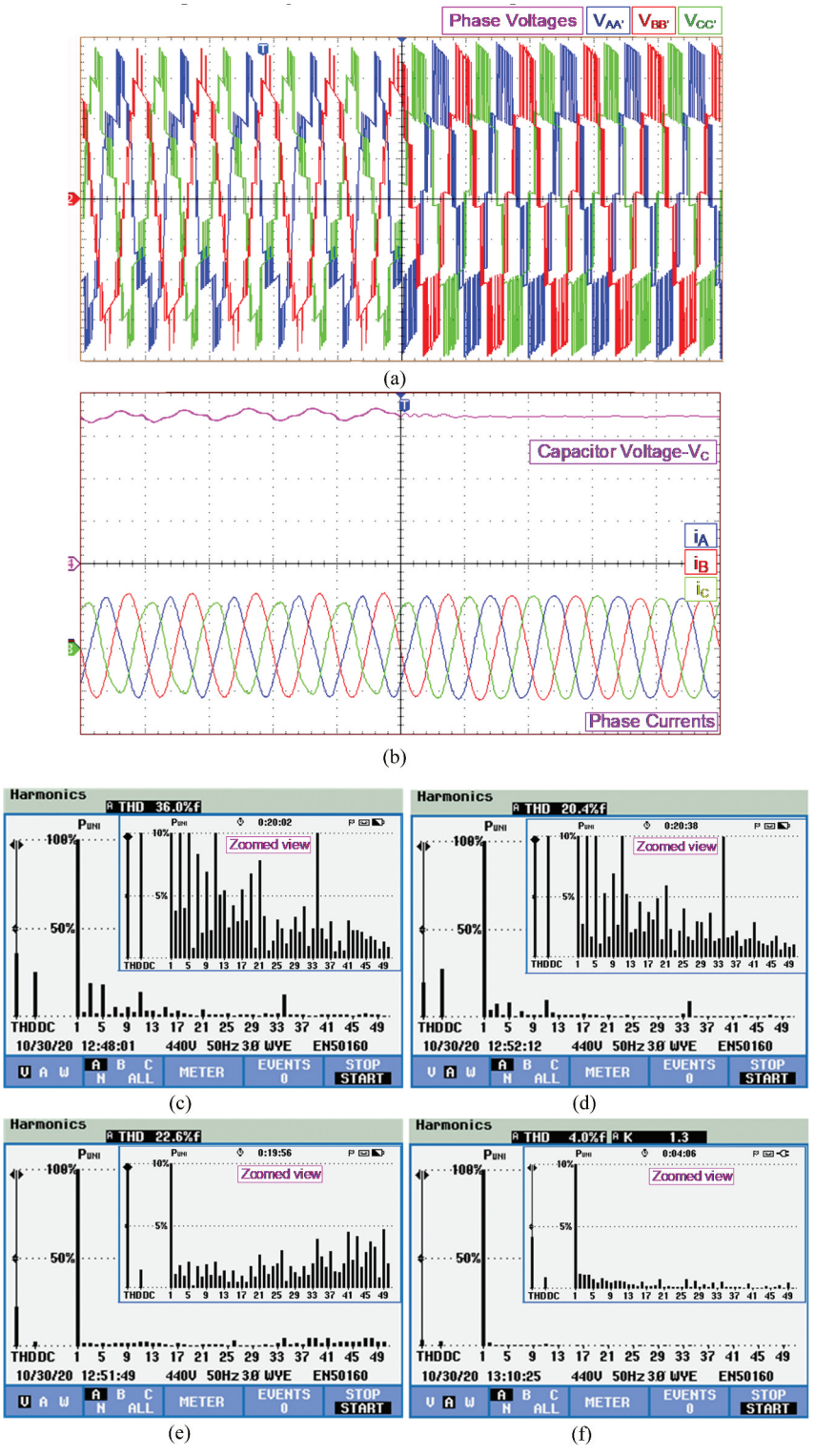

Figure 12. Waveforms of (X-axis:10 ms/div): A, Three-phase output voltage (Y-axis: 50 V/div); B, FC voltage (Y-axis: 20 V/div) and three-phase no-load currents (Y-axis: 1A/div) with MSL for S_{a7} OC; C, THD for phase voltage during fault; D, THD of phase current during fault; E, THD for phase voltage after fault; F, THD of phase current after fault.

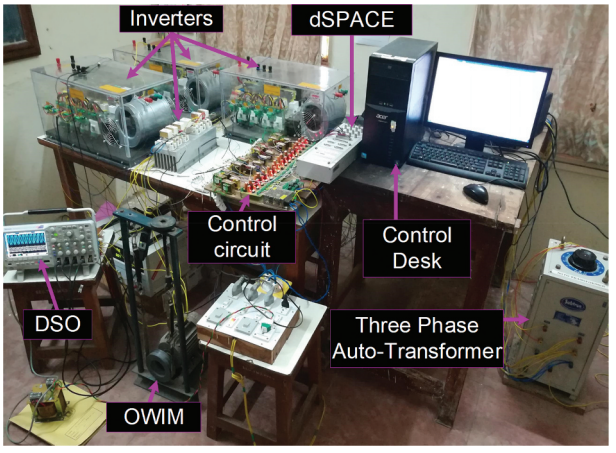

Figure 13. Experimental setup.

(VAA′) and current (iA) in phase A with OC fault in switch Sa7 are presented in Figures 12(c,d), respectively. The FFT analysis for THD in the phase voltage (VAA′) and current (iA) in phase A with MSL for OC fault in switch Sa7 are presented in Figures 12(e,f), respectively. Therefore, the presented results prove that the PMLIT works satisfactorily as five-level inverters with rated power even if the fault occurs in FC or the switches across the FC. Figure 13 presents the experimental setup of the PMLIT feeding 1-hp OWIM.

Based on the construction and area of application, every MLI topology exhibits certain merits and demerits. The PMLIT suffers from some demerits such as non-modular construction compared to conventional topologies and requires three isolated DC sources. However, integration of the PMLIT with renewable energy sources such as solar photovoltaics or fuel cells will overcome this demerit. The PMLIT also has certain advantages such as simple construction, requirement of less number of components, lower voltage rating source requirements and tolerance to switch faults. These merits make the PMLIT find applications in medium and high power traction, industrial and electric vehicular applications.

8. Conclusion

A nine-level inverter based on FC for OWIM drive is presented in this paper. The PMLIT employs three-phase VSIs, isolated dc sources and a FC. The FC is charged and discharged with load current from all the three-phases to realise nine-levels in the output voltage across the phase windings of the OWIM drive. Conventional SPWM techniques with modified reference wave and single carrier wave are employed for producing switch gate-pulses. The PMLIT is capable of producing balanced three phase voltage across the phase windings even under switch fault conditions. A MSL is proposed for the post-fault operation of PMLIT which ensures reliable operation without requirement of any redundant switching units. The effect of switch faults on three-phase output voltages, currents and capacitor voltage are presented. The dynamic behaviour of the PMLIT during fault and after application of the MSL is also presented.

A brief comparison of the PMLIT with similar existing topologies in terms of components count, control complexity and inverter cost is done which prove that the PMLIT is cost-effective with lower number of components and can be operated with reduced control complexity.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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Appendix

Inverter parameters
Make: SEMIKRON (Model:SKM-4M7-45A-3)
Semiconductor switches: IGBT (Model: SKM75GB063D)
Voltage rating: 600 V
Current Rating: 75A
DC Link Capacitors: 2 (each of 2200 uF)

Induction Motor Parameters

Parameter	Quantity
Stator Resistance (Rs)	8.45 Ω
Rotor Resistance (Rr)	7.2 Ω
Stator Inductance (Ls)	0.025 H
Rotor Inductance (Lr)	0.025 H
Mutual Inductance (Lm)	0.615 H
Poles (P)	4
Moment of Inertia (J)	0.06816 kg/m2
Motor Nominal Voltage	400 V (Line–Line)