Design and Development of High-Voltage High-Pulse Power Supply Using FPGA for Dynamic Impedance Matching

Krishna Kumar Rai, A. V. Giridhar, *Senior Member, IEEE*, D. R. Jahagirdhar, and Ashish Rai

***Abstract*— High-voltage high-pulse power supply (HVHPPS) is designed with the goal to match fixed load, so that precise pulse output can be achieved. Generally, the loads involve magnetron, klystron, and particle accelerators. The HVHPPS output pulse shape changes with load impedance variation due to various reasons. Due to the changes in impedance, the performance of pulse power supply degrades and reflects the power at the source end, which causes component failure and system shut down. To overcome such problems, a scale down high-voltage high-pulse power is designed and developed to match the dynamic impedance variations. In earlier days, all HVHPPS were designed using microcontrollers, where the problem of pulse to pulse monitoring and computational speed was compromised. The availability of variable and self-defined, field-programmable gate array (FPGA) controller, which provided flexibility to design the pulse to pulse shaping and various vital parameters monitoring, made it possible. This article presents the design and implementation of HVHPPS over an FPGA platform to meet the fast response requirement. This article provides a solution for impedance mismatch problems associated with such types of power supply and also presents specifications for major components in a high-voltage pulse power system for various types of load ranges. An experimental test hardware was designed and developed for HVHPPS to implement dynamic impedance algorithm and validate the results.**

***Index Terms*— Field-programmable gate array (FPGA), high-voltage high-pulse power supply (HVHPPS), impedance mismatch, klystron, pulse forming network (PFN), pulse shaping.**

I. Introduction and Background

THERE are a wide range of applications of high-voltage high-pulse power supply (HVHPPS) in commercial, industrial, and defense sectors. There are two domains of application, one at low-voltage low-pulse power level and another at high-voltage high-pulse power. Basically, low-voltage low-pulse power is used in commercial and some sectors in industry, whereas all military applications require HVHPPS. HVHPPS uses a range of load (impedance), such as magnetron, klystron, linear accelerator, and so on. Thus, efficient HVHPPS design and development is very essential [1]. The change in length of transmission line (impedance) is due to temperature effect on microwave oscillator cavity dimensions and dynamic impedance characteristics of amplifiers/oscillators. Impedance change in load will have an impact on the performance of HVHPPS, i.e., back reflection and power loss. HVHPPS design is based on voltage-fed series resonance pulse forming network (PFN), which contains five blocks, as illustrated in Fig. 1.

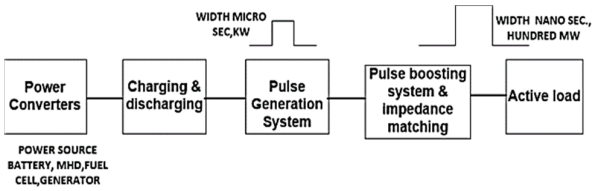

Fig. 1. Block diagram of HVHPPS.

The HVPPS begins with power converters and ends at the interface with the active load. There may be more blocks of pulse formation based on the requirement of pulsewidth amplitude. Pulse power system in a compact form is always desirable for defense, space, and commercial applications. High voltage high pulse power system generates peak power for very short duration as a single pulse at a particular pulse repetition frequency (PRF) [2], [3].

II. Design of High-Voltage High-Pulse Power System

All HVHPPS systems have the problem of impedance mismatch. Hardware was therefore designed and developed to simulate the impedance mismatch and implement dynamic impedance matching.

A. Transmission Line Type HVHPPS

For proper pulse definition i.e., pulsewidth, pulse shape, and PRF control, transmission line type of HVPPS is used and considered for design and development. As per the configuration shown in Fig. 2, the energy storage device is a lumped constant transmission line. These devices not only act as a

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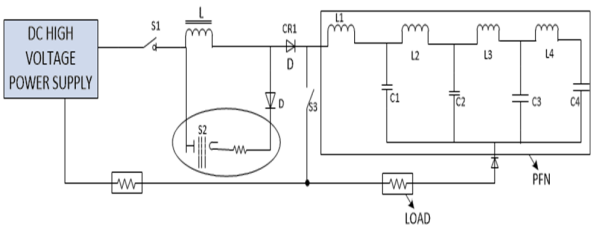

Fig. 2. Transmission line type HVHPPS.

TABLE I
SPECIFICATION OF HVHPPS

Parameter	Value
Pulse Output Voltage	15kV
Output Current	10A
Pulse width (Variable)	4-10µsec
Pulse width (nominal)	6 µsec
Repetition rate (Variable)	10-400Hz
Load impedance(R_L)	1500Ω
Turns Ratio	1:11

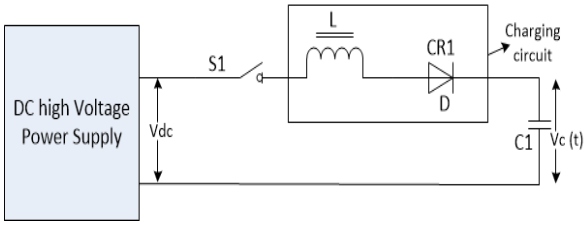

Fig. 3. Resonance charging circuit.

source of electrical energy but also work as pulse shaping element, i.e., PFN [4].

L—Charging inductance.
$L1$, $L2$, $L3$, $L4$—PFN inductor.
$C1$, $C2$, $C3$, $C4$—PFN capacitor.
$S1$—Controlled switch.
$S2$—Decrease quality factor (DeQ) switch.
$S3$—Main pulse discharging switch.
L—Controlled inductance.
$C1$—Capacitor.
CR1—Diode.
PFN—Pulse forming network.

Table I represents the specification for hardware designed and developed as to implement impedance matching algorithm on field-programmable gate array (FPGA).

B. Charging Circuit and Charging Inductor

As per Fig. 3, when switch S is closed, current flows through the inductor L to charge capacitor $C1$. Initially, the reactance of L limits the current resulting in voltage drop equal to battery voltage appearing across L.

Due to resonance, a damped oscillation of current flows between L and $C1$

Resonant time is $Tc = 2\pi\sqrt{L1C1}$.

Resonance charging transfers the stored energy in charging inductor through CR1 (which block the reverse flow of current back to through $L1$) to capacitor $C1$ at voltage equal to twice that of dc high-voltage supply [5].

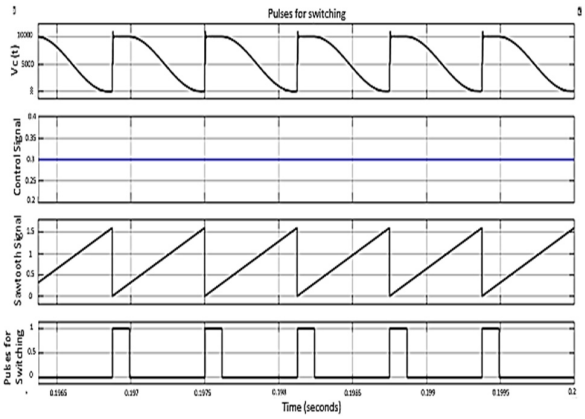

Fig. 4. Waveforms obtained from the controlling circuit.

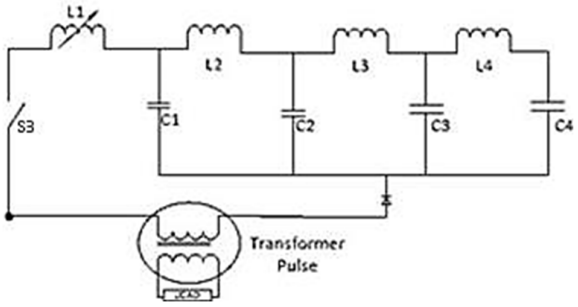

Fig. 5. Novel pulse forming network design.

The maximum PRF is the deciding factor for quiescent duration between two pulses. As per Fig. 4, once the charging inductor charges twice the input dc voltage, the main switches ON based on a comparison with sawtooth waveform and control signal. The main switch switches ON accordingly, and energy stored in capacitor discharges as pulse across the load

Charging time = period of resonance/2.

Charging time, $T = \pi\sqrt{LC}$, where L is the inductance of charging choke and C is the capacitance of PFN [6].

We consider a charging time = 1.5 ms and charging inductor = 0.808 H at 3 kV.

Higher inductance of the charging choke causes the slow rate of charging; thus, inductor charging time increases.

C. Charging Diode

The main purpose of charging diode is to block the reverse flow of current, which is connected in series, as shown in Fig. 3. The number of diodes will be decided based on the requirement of reverse blocking voltage.

In this case, six fast recovery diodes each having a 500-V reverse blocking voltage are considered to meet 3-kV reverse blocking voltage capacity.

D. Novel PFN

In PFN system architecture, as shown in Fig. 5, we have to make assumption about the load nature, i.e., whether it is static

TABLE II
CALCULATED VALUE OF NETWORK PARAMETERS

SN	Network Parameter	Calculated Value
1.	Network Capacitance (Cn)	0.24 μF
2.	C1 to C6	0.047 μF
3.	No. of capacitance	06 Nos
4.	Network Inductance	43.75 μH
5.	Mean diameter of the coil in inch (A)	2.75 Inch
6.	Length of the coil in inches (B)	24.5 Inch
7.	Number of turns (N)	82

or dynamic and the required pulse power generation voltage

$$(\text{Primary Impedance})Z_p = \frac{Z_s(\text{Seconday Load Impedance})}{N^2}$$

$$\text{Pulse current of pulse transformer} = \left(\frac{V}{R}\right).$$

Thus, the maximum transformer power is calculated by matching the pulse transmission line impedance to load impedance. The nature of pulse changes with the length of the transmission cable [7].

The novel requisite pulsewidth for load is the deciding factor for the calculation of PFN parameters. Thus, the total capacitance of PFN is, $C_n = (t_p/2Z_o)$, where tp is the pulsewidth; A, N, and B should meet L_n. Normally, $Z_o =$ load impedance, which is already known, and $Zo = \sqrt{(Ln/Cn)}$ is the characteristic impedance of PFN.

To achieve dynamic impedance variance compensation of transmission line, the value of PFN capacitance will always be 5%–10% higher than the calculated value.

The inductance required is

$$L_n = Z_0^2 \times C_n.$$

In case of air wound, inductance

$$L_n = \frac{0.2 \times A^2 \times N^2}{3A + 9B}$$

where L is the inductance in μH, A is the mean diameter of the coil in inches, B is the length of the coil in inches, and N is the number of turns.

As shown in Table II, for all the calculated value of network parameters, the total number of sections of L and C banks calculated on the basis of flatness percentage required for pulse shape is shown.

E. Modified Decreasing Quality Factor (DeQing)

Pulse to pulse regulation provides constant input so as to get constant output from RF. DeQing switch $S2$ in series with a resistance capacitor network is connected across the charging choke, as shown in Fig. 6.

DeQ switching operation takes place when charging inductor voltage crosses the set charging value (user defined). During switching operation, excess energy stored in the inductor is dissipated in DeQ resistor [8].

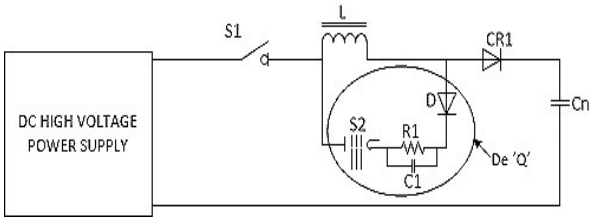

Fig. 6. DeQing switch circuit.

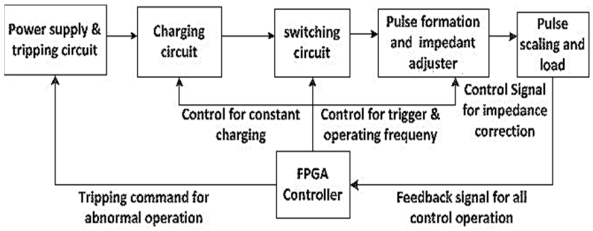

Fig. 7. Control architecture, power flow, and logical operation.

Decay time constant is

$$T_q = \frac{L_{\text{charging choke}}}{R_{\text{deq}}}.$$

Pulse charging average current is represented as $I_{\text{av}} = (\text{CV}/T)$. Hence, peak current I through charging choke is represented as $I_{\text{in}} = (\pi/2) \times I_{\text{av}}$.

DC current flowing through the choke is represented as $I_{\text{dc}} = I_{\text{av}} \times$ dutyratio.

FPGA-based controllers are always compact, more reliable, and simpler and are part of emerging technology. FPGA-based controller works in shielded environment for EMI and EMC protection. The block diagram of control architecture, power flow, and logical operation of high-voltage high-pulse power system is shown in Fig. 7. FPGA controls the charging requirement of the PFN and the main switch operation. Furthermore, it controls the impedance matching and logical flow of power.

To implement the control and impedance matching, pulse to pulse voltage is monitored through voltage compensation network and the same is used as a feedback for comparison with ideal pulse shape defined in [9]. When pulse shape deteriorates due to positive and negative impedance mismatch beyond 10% (acceptable limit defined by the user), a trip command is issued by the controller to stop output voltage generation.

F. Impedance Matching Algorithm Implementation

PFN has multiple sections of LC tank based on pulsewidth requirement. A novel technique is introduced to create an option for impedance matching at the source end. In this technique, more numbers of inductance coils are created to meet the impedance matching requirement. The source voltage is sensed with the help of voltage sensor circuit. The sensed source voltage is given as the analog input to ADC of Virtex 6 FPGA board of Xilinx.

FPGA controller is of importance because it is used to provide gate pulses for switching MOSFET. The gate pulse of required width, which is found from simulation, is developed using FPGA controller that is used for generating the gate pulses for switching on MOSFET at a high frequency. Here, the recurrence frequency used is of 1.6 kHz.

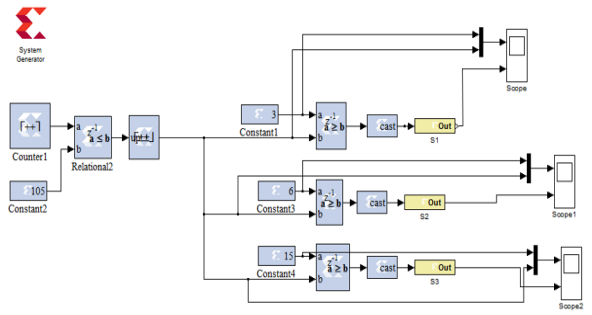

Fig. 8. Simulink model to generate required pulses using FPGA.

To develop the pulses of required width, the control scheme is developed in MATLAB simulation environment using Xilinx blocks shown in Fig. 8. The counter block generates either sawtooth or triangular waveforms by using up or up–down operational mode. The expression for selecting count value is shown in the following equation:

$$\text{Count value} = \frac{f_{\text{clcok}}}{f_{\text{desired}} \times \text{explicitperiod}} \tag{1}$$

but the count value is limited by the number of bits with the relation $2^{\text{nbits}} >$ count value. For example, if the count value is 210, then the minimum number of bits selected should be 8. The explicit period normally is very small. The count value for 1.6-kHz frequency of saw tooth waveform generation with an explicit value of approximately 10–6 is around 210. The clock frequency is made 1 when using system generator to match MATLAB simulation period. Saw tooth waveforms obtained from the upcounter block is of discrete type. Now, a constant value of half of the count value is compared to the saw tooth waveform so as to get 50% duty cycle of rectangular wave. Now, it is applied to up–down counter for which the signal increases linearly for high value and decreases linearly for low value. From the up–down counter block, a triangular signal was obtained. This was compared with a constant value selected based on the percentage of duty cycle needed to get the required gate pulse. The gateway out was used to assign proper I/O as per the pin assignment. The developed model was converted into VHDL code using system generator and further programmed into the FPGA board via SPI programmable interface, using ISE design suite.

The generated reference signal was compared with a set value of requirement. Finally, the switching signals were given to the devices through pulse amplification and isolation circuits. The flowchart in Fig. 9 indicates the working of algorithm implemented in FPGA.

FPGA gives a suitable trigger pulse to the main switch to deliver the requisite output pulse as indicated in the Simulink model. The control signal varies based on the level of faults and level of impedance mismatch.

III. Prototype Hardware of HVHPPS and Analysis

HVHPPS hardware created for 1.5-kΩ resistor was connected through three-shielded cables to match the transmission line impedance of 12.5 Ω. The system was fed from single-phase ac voltage source with a peak voltage of 220 V and 50-Hz frequency.

The detailed specifications of HVHPPS are given in Table I. A scale down proof of concept hardware model was developed

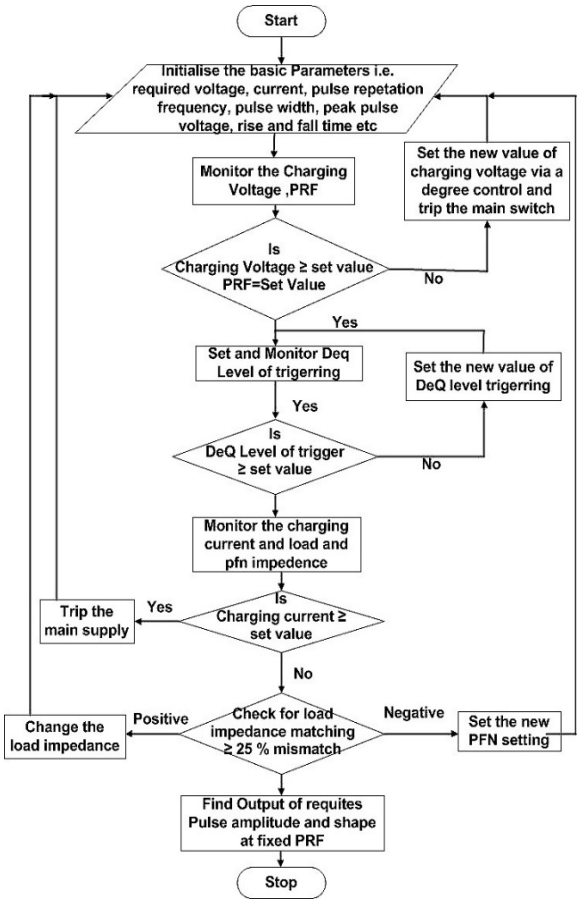

Fig. 9. Algorithm of FPGA programming.

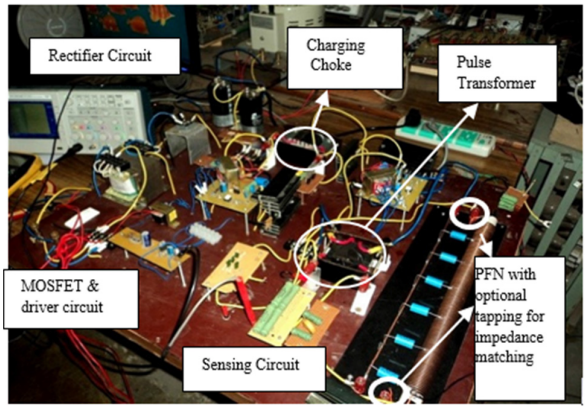

Fig. 10. Hardware of HVHPPS.

and control algorithm on FPGA implemented in high-voltage high-pulse power generation for impedance matching. The same experiment that has been proven on actual hardware was shown in Fig. 10, and the result was validated for establishing the functionality of the system.

Fig. 11 shows the charging voltage waveform, which shows series resonance charging phenomenon between charging choke and the capacitor (lumped) of PFN. In order to ensure proper charging, a fast *RC* compensation network (1:4) is developed.

DeQ trigger and choke voltage waveforms are shown in Fig. 12. Fast *RC* compensation network detects the extra

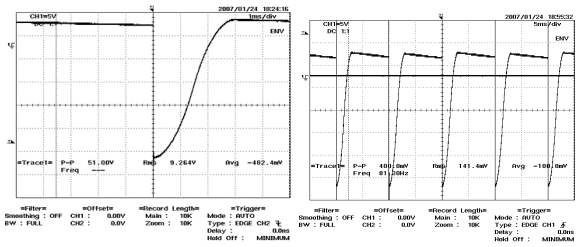

Fig. 11. Charging voltage waveform.

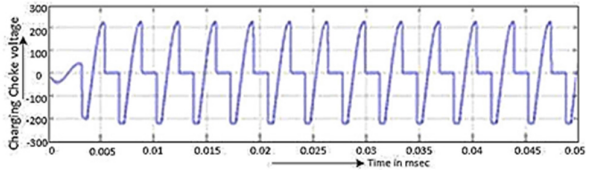

Fig. 12. DeQ trigger pulse and choke voltage.

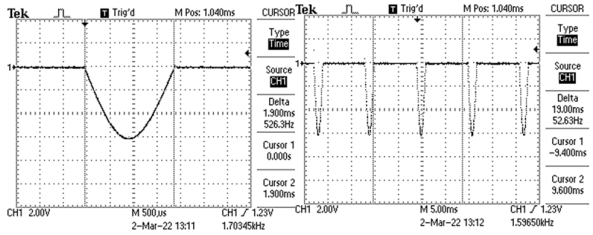

Fig. 13. Charging current and forward diode voltages.

charging voltage of choke. Then, the controller gives the trigger signal to DeQ switch to operate and dissipate excess power across resistor network for pulse to pulse regulation [10]. Setting is done in such a way that maximum power dissipation does not exceed more than 25% of total voltage.

If charging voltage is negative (between 5% and 10%), due to mismatch between the PFN and dynamic load, then reverse diode protection scheme reduces pulse repetition rate by 20%. The developed high-voltage high-pulse power system has high flexibility to reduce up to 50% of the output voltage with respect to pulsewidth, pulse PRF rate, and voltage magnitude during revere charging by more than 25%.

Fig. 13 shows the charging current and forward diode voltage. Charging current and time is sensed through 1-Ω resistor assembly. If output current rapidly increases due to arc, then overcurrent protection circuit turns off EHT supply.

The pulse transformer is conservatively designed with bifilar winding. Six pieces of ferrite core are used in the pulse transformer.

Fig. 14 shows the output voltage at load. To sense 15 kV, a fast compensation network was designed. For a load resistance of 1.5 kΩ and a charging voltage of 2.6 kV, the resulting output pulse voltage was 1.3 kV. The rise time of load voltage was approximately 100 ns (10%–90%). The initial peak of 5% was due to the first combination of L and C of PFN. The second and third overshoots were due to the mismatch of second and third combination of L and C PFN.

The initial few microseconds are required to settle down the initial mismatch of network and load. The rest of the pulse top is flat to make a total pulsewidth of 6 μs. It has been experimentally observed that the output voltage waveform

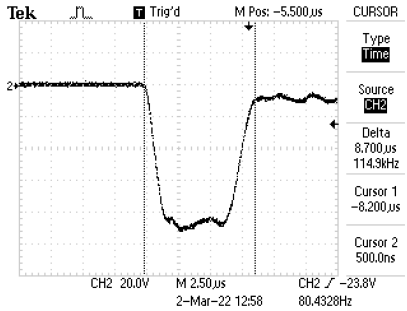

Fig. 14. Output voltage at load.

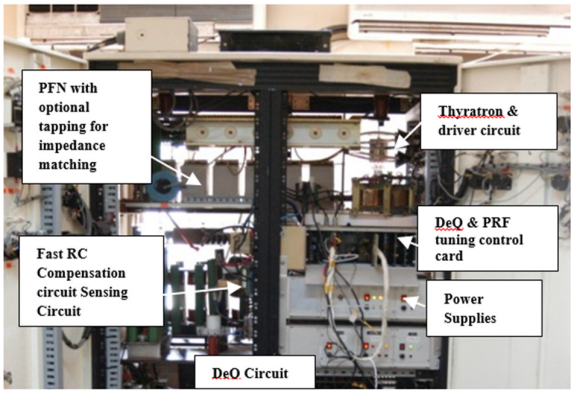

Fig. 15. Actual hardware of HVHPPS.

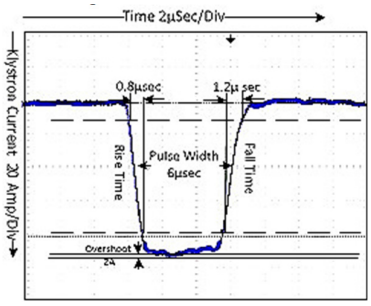

Fig. 16. Reference klystron current waveform observed in perfectly matched condition.

at load deteriorates with the increase of transmission line length. To compensate this deterioration of output waveform, a compensation circuit is designed and put across the primary side of pulse transformer.

IV. Experimental Results and Analysis

Fig. 15 shows the hardware of the HVHPPS developed for the implementation of impedance matching offline, which delivers 15 kV, 10–400-Hz (selectable) frequency, and approximately 10-A current (primary of pulse transformer) with 6-μs pulse duration for primary of pulse transformer, when the load is klystron microwave amplifier.

As shown in Fig. 16, a perfectly impedance matched klystron current waveform was observed during the experiment with manual taped change option created for impedance matching.

The rise time, pulsewidth, fall time, and overshoot of 8 μs, 6 μs, 1.2 μs, and 2 A are obtained, respectively.

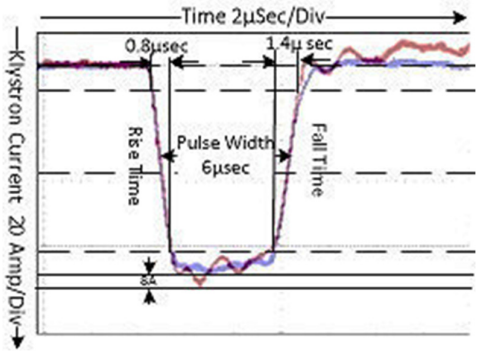

Fig. 17. Klystron current waveform with +ve mismatch.

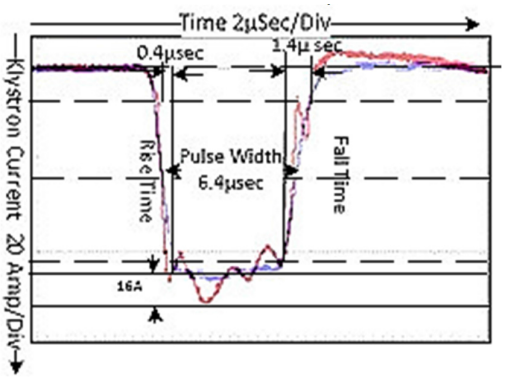

Fig. 18. Klystron current waveform with −ve mismatch.

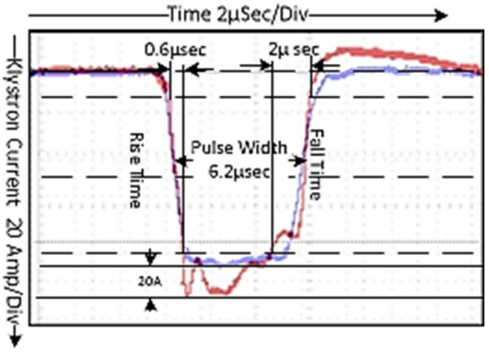

Fig. 19. Klystron current waveform with highly mismatch.

As per Fig. 17, the overshoot of 8 A was observed and 1.4 μs of fall time was obtained, which was due to positive mismatch ($Z_l > Z_o$) of PFN. The initial tapping of PFN increased, i.e., line inductance was enhanced to compensate positive mismatch by adding the number of turns (L_n) to obtain the reference waveform for klystron.

As per Fig. 18, klystron output current showed negative mismatch ($Z_l < Z_o$) of up to 18% of the reference value. This negative mismatch was detected and measured to give a suitable command for output voltage amplitude and frequency correction.

To compensate the overshoot, pulsewidth, fall time, and rise time, PFN tapping at the trailing edge was done in such a way that some of the air wound coils (L_n) were eliminated from the PFN.

Fig. 19 shows that when impedance mismatch is high, the controller will work in time domain and issue corrective command based on the deterioration of the output voltage pulse parameters.

After observation and comparative analysis with reference waveform, tripping command is issued by FPGA controller. Based on the mismatch condition, the developed hardware option for impedance matching correction is utilized offline, and impedance matching of PFN at the source end and finally ideal pulse, as shown in Fig. 16, is achieved, which is a perfectly impedance matched condition.

V. Conclusion

A concept hardware was developed for compact high-voltage high-pulse power system, which delivered 15-kV and 10-A pulse with a sharp fall and rise time in microseconds. Sharp fall and rise time are achieved by using MOSFET and ferrite core pulse transformer. With appropriate control using Virtex FPGA controller, the output pulse can vary PRF from 10 to 400 Hz and voltage can be achieved from 1 to 15 kV.

Impedance matching mechanism and algorithm were tested in scale down model. The same was implemented in actual hardware as klystron load (klystron amplifier of 6 MW, 6 μs, and 0.001 duty cycle) and impedance matching tested. Offline impedance matching tuning mechanism was achieved.

In future, dynamic impedance matching can be thought of using servo control mechanism for online PFN tuning and for use in power supply that needs wideband universal HVPPS.

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