# An Enhanced Fault-Tolerant and Autoreconfigurable BLDC Motor Drive for Electric Vehicle Applications

Patnana Hema Kumar and V. T. Somasekhar, *Member, IEEE*

***Abstract*—Semiconductor switching devices are susceptible to open-circuit (OC) and short-circuit (SC) faults, adversely affecting the reliability of power converters. This article proposes a multiple-switch fault-tolerant and autoreconfigurable brushless direct current (BLDC) motor drive configuration, suitable for electric vehicle applications, owing to its enhanced reliability. The proposed power circuit configuration, along with its fault diagnostic algorithm, is capable of achieving fault tolerance against multiple OC and SC faults. The proposed drive configuration is capable of delivering rated power to the BLDC motor even after the development of several faults in the power semiconductor switching devices. In this power converter, additional switching resources, provided to achieve fault tolerance, get connected only after the occurrence of faults. This feature avoids their unnecessary exposure before the occurrence of faults. Furthermore, the proposed topology requires fewer sensors to implement the fault diagnostic algorithm resulting in reduced cost and increased reliability. This article also presents an analysis that assesses the cost-effectiveness of the proposed drive configuration, which reveals that the additional cost to implement the proposed topology is not more than 6% of the total raw material cost of the conventional BLDC motor drive. Simulation and experimental studies validate the concept of the proposed drive configuration.**

***Index Terms*—Dynamic reconfiguration, electric vehicles (EVs), fault-isolation, inverters, multiple-switch fault-tolerant.**

## I. Introduction

CONTINUOUS emission of pollutants caused by internal-combustion engines (ICEs) propelled automobiles is one of the most important reasons for the deterioration of the environment. Globally, electric vehicles (EVs) are being promoted to mitigate the ill effects of the ICEs. It is predicted that by the end of the present decade, a major share of road transportation is borne by EVs. EVs typically employ electric motors as their propulsion units, which are controlled by voltage source inverters (VSIs). These VSIs are constituted by power semiconductor switching devices, such as IGBTs.

For electric propulsion, cage-type induction motors offer the advantages of lower maintenance, robustness, and lower costs. However, they are plagued with weaknesses, such as lower torque, higher starting currents, vibrations at starting conditions, moderate efficiencies, and moderate speeds. The shortcomings of the aforementioned motors forced designers around the globe to consider permanent magnet motors (PMMs) for EV applications. PMMs are capable of displaying the features of 1) lower size [due to the higher torque-to-weight ratio of brushless direct current (BLDC) motors], 2) higher efficiency (due to the absence of rotor winding and the corresponding ohmic losses), 3) lower maintenance, 4) low noise, 5) better P.F, and 6) good dynamic response [1]–[5]. The penetration of PMMs in EV applications is further hastened by the recent developments in supportive technologies, such as lightweight and high-energy-density batteries, efficient power semiconductor switching devices, high-energy permanent magnets, and high-speed digital control platforms. In the category of PMMs, two principal variants exist, namely, permanent magnet synchronous motors (PMSMs) and the BLDC motors. Propulsion systems based on BLDC motors are increasingly becoming popular in the low-power domain [34]. Popular EV designs based on BLDC motors include 1) wheelchairs, 2) bicycles, 3) golf-course vehicles, and 4) ambulances. In principle, there are no technical hindrances to extending the BLDC motor drives to higher power applications [4]. Owing to their higher efficiency due to the lack of secondary winding and magnetizing current, BLDC motors score over the induction motors for EV applications. Also, they can output 15% higher power compared to the PMSMs [1]. Though PMSMs result in lower torque ripples compared to the BLDC motors, they need more expensive sensors compared to BLDC motors, which only need inexpensive Hall sensors. The applicability and selection of the BLDC motor drives used in EV applications are presented in [4]–[9] and [34]. The major problem corresponding to the commutation torque ripple of the BLDC motors is addressed and corresponding minimization techniques are presented in the literature [10], [11].

However, in an EV, wherein the electric motor is the sole propulsion unit, reliability is of paramount interest. The reliability of EVs can be enhanced with the aid of fault-tolerant designs. A survey shows that power semiconductor devices account for about 38% of the total faults occurring in motor drive configurations. The faults in power semiconductor devices are of two types: 1) open-circuit (OC) and 2) short-circuit (SC) faults [12]–[15].

The research article reported in [16] describes the diagnosis of the OC/SC faults occurring in the switching devices of the VSI based on the behavior of the gate-to-emitter voltages of IGBTs within 3 $\mu$s. However, this method is applicable only

Manuscript received 25 April 2022; revised 4 July 2022 and 31 July 2022; accepted 1 August 2022. Date of publication 5 August 2022; date of current version 28 December 2022. *(Corresponding author: Patnana Hema Kumar.)*

The authors are with the National Institute of Technology Warangal, Warangal 506004, India (e-mail: hema1729@gmail.com; sekhar@nitw.ac.in).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JESTIE.2022.3196818.

Digital Object Identifier 10.1109/JESTIE.2022.3196818

to IGBT-based converters and requires auxiliary inductors for diagnosis.

Single-switch, as well as multiple-switch OC fault-diagnosis algorithms for conventional IM drives, are described in the literature [17]–[19]. However, the postfault reconfiguration of the drive to achieve fault-tolerant operation has not been described in these research articles. Single switch as well as multiple-switch OC/SC fault-tolerant capabilities of a multilevel inverter fed open-end winding IM-drive are presented in [20]–[22]. However, in these articles [20]–[22], the fault-diagnosis algorithms have not been presented. The research article presented in [23] describes a single switch OC fault-diagnosis algorithm for the fault-tolerant dual inverter fed open-end winding IM-drive configuration. Despite the availability of a rich repertoire of fault-diagnosis methods and postfault drive configuration strategies in the area of induction motor drives, they do not apply to BLDC motor drives due to the discontinuous current and trapezoidal back EMF of the BLDC motors. However, this literature forms the basis to develop fault-diagnosis and reconfiguration strategies for BLDC drives.

Fault-tolerant control strategies for multiphase open-end winding brushless dc motor (OEWBLDCM) drives, which are suitable for applications demanding high reliability, such as EVs, electric aircraft, processing industries, and transportation systems, are reported in [24]–[26]. These drives are capable of providing fault-tolerant operation against both single-switch and multiple-switch OC faults as well as motor phase OC faults. The work reported in the article [26] also describes the OC fault-diagnosis procedure for multiphase BLDC motor drive configuration.

The research article presented in [27] describes a detection strategy to identify a single OC fault and the corresponding fault-tolerant reconfiguration for a BLDC motor drive. Though elegantly formulated for OC fault, this research article has restricted applicability as it does not include the SC fault. A scheme, which is based on the employment of three additional triacs, to detect a single switch OC fault and the corresponding postfault reconnection for a BLDC drive, was proposed in [27]. It is worth noting that even this research article did not consider the diagnosis and the postfault reconfiguration of the drive in the eventuality of an SC fault.

In the research article presented in [28], a single-switch OC (or) SC fault-tolerant drive topology for EV applications is described, which uses six TRIACs and one actuator leg additionally. However, these triacs are constrained to conduct even during the normal (i.e., fault-free) operating conditions, making them vulnerable to the development of additional faults. The fault-diagnosis algorithms were not described in this literature.

Further, a single-sided-matrix converter fed OEWBLDCM drive topology is reported in [29]. Though this article describes the fault-tolerant operation against a single OC fault in the switch, it does not present the diagnosis algorithm, which asserts the occurrence of the OC fault.

A fault-tolerant BLDC motor drive for a magnetically suspended control (MSC) moment gyro for aerospace applications is presented in [30]. This drive configuration consists of a front-end buck dc–dc converter, which feeds a VSI that drives the BLDC motor. A fault-diagnosis algorithm has been described in this article, which is capable of detecting a single switch OC/SC fault in the overall power circuit. In this drive, the fault-tolerant operation is obtained by the placement of triacs in series and parallel to the converter leg. However, these triacs are constrained to conduct even during normal (i.e., fault-free) operating conditions, making them vulnerable to the development of additional faults. The fault-diagnosis algorithm presented in [30] does not address the faults developed in these additional triacs.

A dual-inverter fed OEWBLDCM drive for MSC moment gyro applications is proposed in [31], which can achieve fault tolerance to a single switch OC/SC fault. The diagnosis algorithm described in this article is capable of detecting an OC/SC fault in any one of the twelve semiconductor switching devices present in the drive. However, this fault-tolerant scheme requires that the motor phases carry double the rated current following either of these faults.

Another dual-inverter fed OEWBLDCM drive for low-power EV applications has been proposed in [32], which provides fault tolerance against single switch OC and SC faults. In this drive, each inverter is fed with a separate battery with half of the total battery voltage. This topology needs 12 semiconductor switching devices, wherein each switching device in this configuration is rated for half of the total battery voltage. Further, the fault diagnosis requires six voltage sensors and two current sensors. This article also proposes a postfault circuit reconfiguration strategy, wherein the healthy battery, which is connected to the faulty inverter, is reconnected in *parallel* to the battery feeding the healthy inverter with the aid of two double pole double throw (DPDT) relays. Also, a switched neutral point is created with the remaining healthy switching devices present in the faulty inverter. While such a reconnection succeeds in utilizing the charge available in the healthy battery connected to the faulty inverter, the maximum deliverable power (and consequently the maximum deliverable speed) is reduced by 50% compared to its prefault value.

This shortcoming is addressed in the OEWBLDCM drive proposed in [33], which employs the same number of sensors. In this variant, following the diagnosis of the fault, the healthy battery bank feeding the faulty inverter is reconnected in *series* to its counterpart feeding the healthy inverter. While this variant is capable of delivering rated torque (and rated power) even in the postfault scenario, achieving complete fault tolerance, it needs four single pole single throw (SPDT) relays. Furthermore, each power semiconductor switching device in this drive [33] should be rated to withstand the *total* battery voltage.

The power converter topologies described in [32] and [33] have a common feature in that, these topologies try to avoid the situation wherein the protecting semiconductor devices are utilized in the prefault condition as well. This would avoid the continuous power loss in triacs in the power circuit described in [30]. Further, the protective triacs [30] could be vulnerable to failures. The power converter configurations proposed in [32] and [33] demarcate the two tasks of 1) controlling power and 2) steering power. While the former task is delegated to the semiconductors (as VSIs are modulated at high switching

frequencies), the latter task is managed by slower but reliable switchgear, such as SPDT or DPDT relays. The power losses in the steering switchgear are considerably lower, as the voltage drop across the metallic contacts (such as NC or NO and the pole) are considerably lower compared to the drops encountered in their semiconductor counterparts.

The above prior art literature gives the motivation to develop a multiple-switch OC/SC fault-tolerant BLDC motor drive topology and its corresponding fault-diagnosis algorithm used for EV applications.

This article proposes a fault-tolerant BLDC motor drive topology, which can achieve full (i.e.,100%) fault tolerance against multiple-switch OC/SC faults. The proposed multiple-switch fault-tolerant topology requires three additional phase-legs to the VSI and three SPDT relays to achieve full fault tolerance. The proposed fault-tolerant BLDC motor drive topology is capable of developing the rated torque (and rated power) even after the occurrence of multiple-switch OC or SC faults, whereas the articles reported in the literature [27]–[33] are capable of handling only single-switch OC/SC fault conditions. This article also presents the algorithm for diagnosing the multiple-switch (two-switch and three-switch) OC fault conditions in the power semiconductor devices.

The additional switching resources of the proposed topology are pressed into service only after the occurrence of a fault, unlike the fault-tolerant drive topologies proposed in [30]–[33]. Hence, they are not vulnerable to the development of faults in the normal (i.e., prefault) mode of operation, which is a decisive advantage compared to the aforementioned drive topologies. Also, the proposed topology needs fewer sensors compared to the OEWBLDCM drives presented in [32], [33] for fault diagnosis. Only one Hall-current sensor and three voltage sensors are needed to implement the fault-diagnosis algorithm for the proposed drives. In contrast, the OEWBLDCM drives [32], [33] need two Hall-current sensors and six voltage sensors.

Thus, the proposed topology brings in a considerable improvement compared to the aforementioned fault-tolerant BLDC motor drives in terms of sensor requirement and the additional switchgear. This article also shows that even though the proposed power circuit configuration requires additional resources to implement the feature of fault tolerance (six additional power switching devices along with their driver circuits and three SPDT relays), it is still an affordable proposition as the escalated raw-material cost is appreciably compensated by the reduced requirement of voltage and current sensors, compared to the earlier designs reported in [32], [33]. This article also presents a feasibility analysis, which reveals that the proposed drive configuration is quite affordable despite the requirement of additional switching devices and switchgear. Owing to these advantages, it is envisaged that the proposed power converter configurations are suitable for low-power EVs.

The working principles of the proposed BLDC motor drive configuration is first verified with simulation studies. The simulation results are then experimentally validated on a laboratory prototype to demonstrate the effectiveness of the fault diagnosis algorithm and the circuit reconfiguration strategy following the detection of a fault.

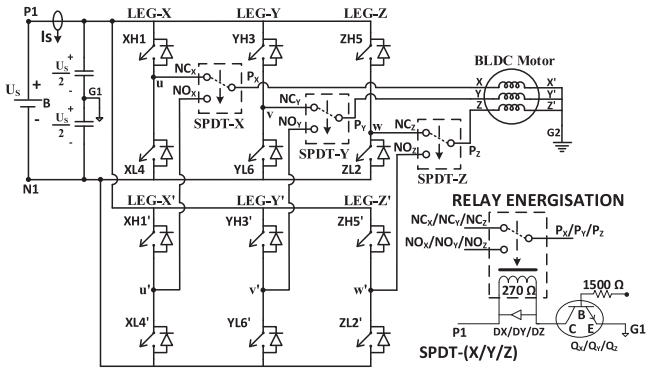


Fig. 1. Proposed multiple-switch OC/SC fault-tolerant drive configuration.

## II. Proposed Multiple-Switch Fault-Tolerant Configuration of the BLDC Motor Drive

Fig. 1 represents the proposed multiple-switch OC/SC fault-tolerant BLDC motor drive configuration. In the proposed topology, the conventional VSI (with power poles *X*, *Y,* and *Z*) is augmented with three additional power poles, namely, *X'*, *Y',* and *Z'* to obtain fault tolerance against multiple OC/SC faults.

The additional power poles in the topology are connected in parallel across the same dc input power supply "*Us*" (a battery bank in the case of EVs), avoiding the need for splitting the dc power supply into two halves as in the case of an open-stator connection presented in [32] and [33]. The terminals of a conventional star-connected BLDC motor are connected to the VSI through three SPDT relays ("*SPDT-X*," "*SPDT-Y*," and "*SPDT-Z*"). It may be noted that, in the normal (i.e., fault-free) mode of operation, the motor terminals (*X*, *Y*, *Z*) are connected to the output terminals of the VSI (*u* ,*v* ,*w*) through the poles of the SPDT relays ("$P_X$," "$P_Y$," and "$P_Z$") and the normally closed (NC) contacts ("$NC_X$," "$NC_Y$," and "$NC_Z$").

The notation of a semiconductor switching device of the VSI is based on the power pole it belongs to and its position in that power pole. As an example, the switch numbered "3" is denoted along with its position as YH3 (Fig. 1), wherein letters Y and H, respectively, denote the pertinent power pole and its position within that power pole (the letters "H" and "L," respectively, denote high-side and low-side switches). Similarly, the corresponding switch belonging to the backup power pole is denoted as YH3' (Fig. 1).

The rotor position is sensed using conventional Hall-sensor signals *Ha*, *Hb*, and *Hc*. Based on these signals, the position of the rotor is categorized into six symmetrical sectors, each spanning 60° (electrical), denoted as "Sector-1" to "Sector-6" as shown in Fig. 2. The gating signals of the inverter are based on the operating sector, which is identified from the Hall-sensor signals. Fig. 2 also shows the waveforms of the back-EMFs generated in the motor phases and the switching signals required in the steady-state conditions in the healthy as well as the postfault

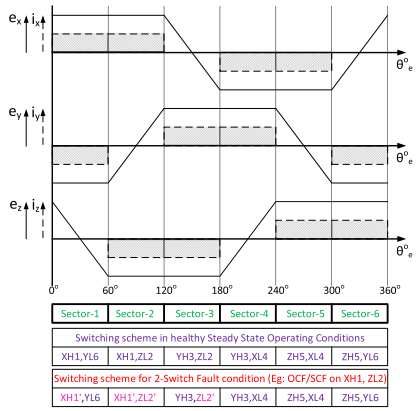


Fig. 2. Motor back-EMF, phase currents, and switching's during steady and faulty conditions.

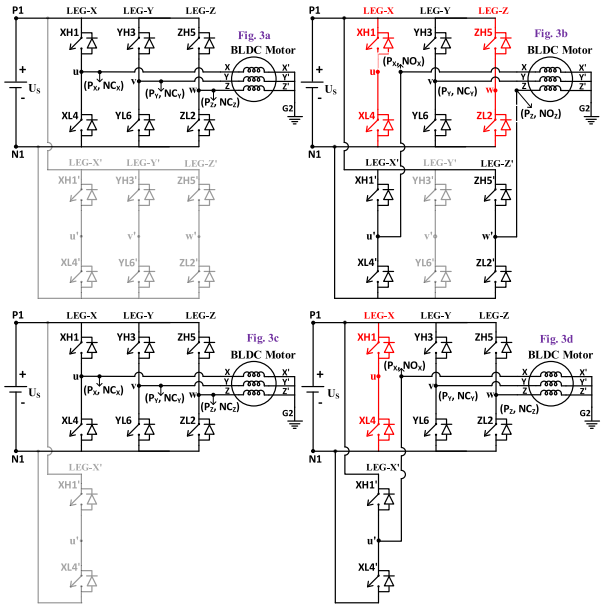


Fig. 3. Equivalent topology configuration of multiple-switch fault-tolerant topology during (a) steady drive operation; (b) multiple-switch OC/SC fault condition (in Leg-X and Z); derived single-switch fault-tolerant topology during (c) steady drive operation; (d) single-switch OC/SC fault condition (in Leg-X).

conditions. This figure also presents the details of the gating signals for the VSI as well as the additional legs after the processes of fault diagnosis and circuit reconfiguration under switch fault conditions.

One may obtain fault tolerance against multiple switch OC/SC faults, occurring in any of the phase-legs (*X*, *Y*, and *Z*), using the proposed fault-tolerant topology (Fig. 1). The only exception to the fault-tolerant operation of multiple-switch faults is the *simultaneous* occurrence of SC faults in the top and the bottom devices on a given phase-leg of the VSI, leading to the shoot-through fault. However, this exception can be handled by providing fast-acting semiconductor fuses in each leg of the VSI.

The grey-shaded portions of Fig. 3(a) indicate the inactive portions of the proposed multiple-switch fault-tolerant topology in the healthy operating conditions. As these portions are dormant

TABLE I
PARAMETERS OF THE BLDC MOTOR

| | |
|---|---|
| Voltage rated | 48 V |
| Torque rated | 0.6 (N-m) |
| Speed rated | 3200 (Rpm) |
| Per phase resistance | 0.295 Ω |
| Back-EMF constant | 11.8 (V/Krpm) |
| Power rated | 250 (W) |
| Pole pairs | 4 |

during the healthy condition of the proposed drive configuration, they are not susceptible to the occurrence of faults. The SPDT relays *X*, *Y*, and *Z* steer power to the BLDC motor either through the healthy legs (Legs-*X*, *Y*, and *Z*) of the VSI through their NC contacts, or from the additional phase legs (Legs-*X'*, *Y'*, and *Z'*) through their normally open (NO) contacts ("$NO_X$," "$NO_Y$," and "$NO_Z$"). This arrangement avoids the necessity of energizing the SPDT relays in the healthy condition of the drive.

Under faulty conditions, the relay coils of the pertinent SPDTs are energized through a transistor ($Q_X$/$Q_Y$/$Q_Z$ of Fig. 1) based circuitry, which is actuated based on the output of the fault diagnosis algorithm. Fig. 3(b) shows the postfault equivalent circuit of the drive, wherein the additional legs X and Z' substitutes the legs-X and Z of the VSI following the occurrence of multiple faults occurring in the legs-X and Z of the VSI.

For the conditions where the design requirement needs only single-switch OC/SC fault-tolerant operation, a circuit topology can be derived from the proposed multiple-switch fault-tolerant topology [shown in Fig. 3(c)], where one out of the three additional legs (say Leg-X') is sufficient and all the NO terminals ('$NO_X$', '$NO_Y$', and '$NO_Z$') of three SPDT relays ("*SPDT-X*," "*SPDT-Y*," and "*SPDT-Z*") are shorted and connected to the output terminal of the additional leg [as shown in Fig. 3(c)]. Fig. 3(c) and (d) presents the steady-state equivalent circuits of the derived single-switch fault-tolerant topology during healthy and faulty operating conditions (fault in Leg-X).

## III. Fault-Diagnosis Algorithm and Fault-Tolerant Control

### A. Multiple-Switch Open-Circuit Fault-Diagnosis Algorithm

This article presents a multiple-switch OC fault diagnosis, which is based on the measurement of the dc-source current with conventional Hall-position sensors. The fault-diagnosis algorithm utilizes these Hall-sensor signals to determine the sectors in which the dc-source current is absent. This information is pivotal to the identification of faulty switching devices [33].

The working principle of the multiple-switch OC fault diagnosis algorithm is demonstrated with the aid of simulations performed on the MATLAB/ SIMULINK platform. Table I enumerates the BLDC motor parameters used in these simulation studies, which are the same as those of the experimental prototype used.

To simulate an OC fault in a semiconductor device, its gating signal is withdrawn. Similarly, the occurrence of SC fault is

simulated by gating the pertinent device with a continuous gating signal [32].

As a case study for the detection of multiple-switch OC fault, failure of the switching devices XH1 and ZL2 is considered. Detection of all other cases pertaining to the two-switch failure is carried out using the same procedure as described in the following paragraphs.

A column matrix "***S***," with six elements is used in the detection of the multiple-OC fault. Each element in this matrix is called a flag, which denotes the current sector of operation. Each Flag is denoted with the symbol $S_n$, where the number "*n*" ($n = 1, 2 \ldots .6$) denotes the current sector of operation. It should be noted that this matrix is continuously updated based on the Hall-sensor signals

$$\begin{cases} S_n = 1, & \text{When sector} = n \\ S_n = 0, & \text{else condition} \end{cases} \quad (\text{where } (1 \le n \le 6) \quad (1)$$

$$[\boldsymbol{S}] = [S_1,\ S_2, S_3, S_4,\ S_5,\ S_6]^T. \quad (2)$$

The OC fault is identified whenever the dc-source current "*Is*" falls below a critical value "*Ith*." This critical current is a predetermined fraction "*Kf*" of the reference value "*Iref*." Generally, the reference dc-source current "*Iref*" is determined by the output of the speed controller (Fig. 8). However, for EV applications, wherein speed is controlled in an open loop, a suitable low value may be employed as the threshold current. Whenever an interruption is detected in the dc-source current, a flag named "*fi*" is set to "1"

$$Ith = Kf * Iref \quad (3)$$

$$\begin{cases} Is < Ith, & fi = 1\ (OC\ fault\ identified) \\ Is \ge Ith, & fi = 0\ (steady\ condition) \end{cases} \quad (4)$$

where the factor *"Kf"* lies between values 0 and 0.5. A value of *"Kf"* less than the mid-range value leads to reliable OC fault identification [27], [32]. In this article, the value of *"Kf"* is chosen as 0.1.

A single switch failure can occur in six different ways, while two-switch OC faults can occur in 15 (i.e., ${}^6c_2$) ways. From Fig. 2, it is evident that whenever a single-switch fault occurs, the dc-source current drops down to zero in two sectors. So far, as the two-switch OC faults are concerned, of the 15 combinations, 6 combinations would lose the dc-source current in 3 sectors and the remaining 9 lose the dc-source current in 4 sectors (Fig. 2).

To assert the loss of dc-source current in any given sector, the interruption in the dc-source current must persist for a time interval, which is higher than a critical time-period denoted as "*Tcri*." Dedicated accumulators are employed to determine the time for which the dc-source current falls below the threshold value. The time period of interruption in any given sector is denoted as "*Tint,n (n=12…6)*."

Whenever the current interruption flag "*fi*" is set to "1" in any given sector (where the sector number is positionally indicated in the ***S***-matrix), an accumulator corresponding to that particular sector is triggered. Based on a predetermined sampling time period "*Ts*" (70 $\mu$S) and the initial condition *Tint,n (−1)* = 0, it accumulates a count, which is a measure of the time of interruption of the dc-source current.

TABLE II
OC FAULT DIAGNOSIS INFORMATION

| Faulty switches | **Fs** | [ROCF1, ROCF2] | Nzts, Nzel | Relay-[X,Y,Z] | Backup legs |
|---|---|---|---|---|---|
| XH1 | [1 1 0 0 0 0] | [1,0] | 2,1 | [1,0,0] | Leg-X' |
| ZL2 | [0 1 1 0 0 0] | [2,0] | 2,1 | [0,0,1] | Leg-X' |
| YH3 | [0 0 1 1 0 0] | [3,0] | 2,1 | [0,1,0] | Leg-X' |
| XL4 | [0 0 0 1 1 0] | [4,0] | 2,1 | [1,0,0] | Leg-X' |
| ZH5 | [0 0 0 0 1 1] | [5,0] | 2,1 | [0,0,1] | Leg-X' |
| YL6 | [1 0 0 0 0 1] | [6,0] | 2,1 | [0,1,0] | Leg-X' |
| XH1, YH3 | [1 1 1 1 0 0] | [1,3] | 4,1 | [1,1,0] | Legs-X'&Y' |
| XH1, ZH5 | [1 1 0 0 1 1] | [1,5] | 4,1 | [1,0,1] | Legs-X'&Z' |
| XH1, XL4 | [1 1 0 1 1 0] | [1,4] | 2,2 | [1,0,0] | Leg-X' |
| XH1, YL6 | [1 1 0 0 0 1] | [1,6] | 3,1 | [1,1,0] | Legs-X'&Y' |
| XH1, ZL2 | [1 1 1 0 0 0] | [1,2] | 3,1 | [1,0,1] | Legs-X'&Z' |
| YH3, ZH5 | [0 0 1 1 1 1] | [3,5] | 4,1 | [0,1,1] | Legs-Y'&Z' |
| YH3, XL4 | [0 0 1 1 1 0] | [3,4] | 3,1 | [1,1,0] | Legs-X'&Y' |
| YH3, YL6 | [1 0 1 1 0 1] | [3,6] | 2,2 | [0,1,0] | Leg-Y' |
| YH3, ZL2 | [0 1 1 1 0 0] | [3,2] | 3,1 | [0,1,1] | Legs-Y'&Z' |
| ZH5, XL4 | [0 0 0 1 1 1] | [5,4] | 3,1 | [1,0,1] | Legs-X'&Z' |
| ZH5, YL6 | [1 0 0 0 1 1] | [5,6] | 3,1 | [0,1,1] | Legs-Y'&Z' |
| ZH5, ZL2 | [0 1 1 0 1 1] | [5,2] | 2,2 | [0,0,1] | Leg-Z' |
| XL4, YL6 | [1 0 0 1 1 1] | [4,6] | 4,1 | [1,1,0] | Legs-X'&Y' |
| YL6, ZL2 | [1 1 1 0 0 1] | [6,2] | 4,1 | [0,1,1] | Legs-Y'&Z' |
| ZL2, XL4 | [0 1 1 1 1 0] | [2,4] | 4,1 | [1,0,1] | Legs-X'&Z' |

All these accumulators are represented by the matrix "[***Tint***]," which is given by

$$[\boldsymbol{Tint}\,(\boldsymbol{i})]^T = (fi) * [S_n * (Tint, n\,(i-1) + Ts)]^T \quad (Wheren = 1to6)$$

$$[\boldsymbol{Tint}\,(\boldsymbol{i})]^T = \begin{bmatrix} Tint, 1\,(i) \\ Tint, 2\,(i) \\ \vdots \\ Tint, 6\,(i) \end{bmatrix} \quad (5)$$

$$[\boldsymbol{Tint}\,(\boldsymbol{i})]^T = (fi) * \begin{bmatrix} S_1 * (Tint, 1\,(i-1) + Ts) \\ S_2 * (Tint, 2\,(i-1) + Ts) \\ \vdots \\ S_6 * (Tint, 6\,(i-1) + Ts) \end{bmatrix}. \quad (6)$$

Whenever *"Tint,n (i)"* is greater than the critical time period "*Tcri*" in any given sector (see the following paragraphs for details), the OC fault is asserted. The affected sectors owing to these OC faults are set to "1" and are captured in the corresponding *fault-sector flags* denoted as "*Fs,n*" (where, $n = 12 \ldots 6$). Otherwise, the flag "*Fs,n*" is reset to "0." All these flags are collectively represented by the matrix "***Fs***" as shown in Table II

$$\begin{cases} Fs, n = 1, & Tint, n\,(i) \ge Tcri \\ Fs, n = 0, & Tint, n\,(i) < Tcri. \end{cases} \quad (where\ (1 \le n \le 6) \quad (7)$$

When an OC fault is diagnosed for the first time, the corresponding sector number is stored in another flag named *first-fault-sector* (*Ffs*). In the scenario of multiple-fault detection, the remaining sectors also need to be probed for a possible fault. This process of probing is carried out until the current sector of operation again equals the value of the flag "*Ffs*." Upon the completion of probing all remaining sectors, another flag

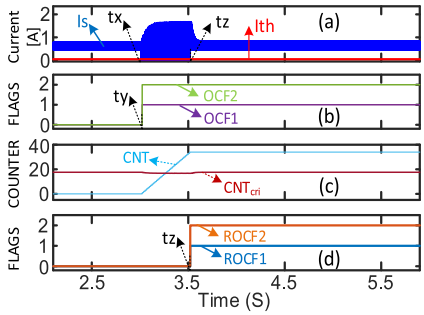


Fig. 4. Simulation results of multiple-switch OCF in switches XH1 and ZL2. (a) Is, Ith. (b) OCF1, OCF2. (c) CNT, $\mathrm{CNT_{cri}}$. (d) ROCF1, ROCF2.

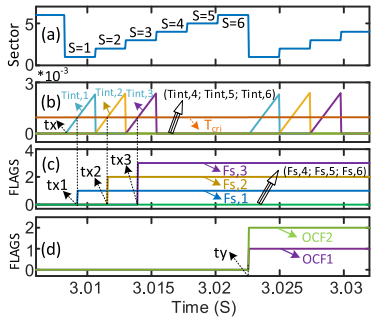


Fig. 5. Simulation results presenting the status of the flags for multiple-switch OC fault in switches XH1 and ZL2. (a) Sector of operation. (b) Tint,n, Tcri. (c) Fs,n. (d) OCF1, OCF2.

named *electric-fault-cycle* flag *(Tfc)* is set to "1." After this event, based on the information available in the matrix $\boldsymbol{Fs}$, the switch numbers corresponding to the faults are stored in two new flags called "*OCF1*" and "*OCF2*." (Table II). This procedure marks the completion of the stage called *"pilot-fault-affirmation."*

The symbol "*Tsect*" represents the time-period corresponding to the operation of the motor in any given sector, which depends on the speed of operation of the motor. It is determined as follows:

$$f_{\mathrm{ele}} = \frac{\omega_{\mathrm{ele}}}{2 * \pi} = \frac{p * \omega_{\mathrm{mec}}}{4 * \pi}\ ;\ t_{\mathrm{ele}} = \frac{1}{f_{\mathrm{ele}}} \tag{8}$$

$$Tsect = \frac{1}{6 * t_{\mathrm{ele}}} = \frac{4 * \pi}{P * \omega_{\mathrm{mec}} * 6} \tag{9}$$

where the quantities "$f_{\mathrm{ele}}$," "$\omega_{\mathrm{mec}}$," and "$\omega_{\mathrm{ele}}$," respectively, represent the electrical frequency, mechanical, and electrical angular speeds.

The critical-fault-time "*Tcri*" is the fraction of the time-period "*Tsect*"

$$Tcri = Gsf * Tsect \tag{10}$$

where the parameter "*Gsf*" denotes the sensitivity factor, which is a measure of the time period allocated to probe the zero-time periods of the dc-source current in a sector. A higher value of "*Gsf*" results in a higher accuracy [32]. As the critical-fault-time "*Tcri*" is a fraction of a sector time period, the value of "*Tcri*" is the same for both single-switch as well as multiple-switch OC fault conditions.

Figs. 4–7 show the simulation results used for explaining the diagnosis procedure of multiple-switch OC fault. As explained earlier, multiple-OC faults are enforced artificially on switches XH1 and ZL2. With the occurrence of multiple-switch OC fault (i.e., switches XH1 and ZL4) at instant "*tf2*" ( Fig. 6), the fall in the dc-source current is first identified at instant "*tx*" (Figs. 4–6). Consequently, the accumulators "*Tint,1*," "*Tint,2*," and "*Tint,3*" of sectors numbered 1, 2, and 3 are triggered, while the others remain inactive as shown in Fig. 5. When the values stored in the accumulators "*Tint,1*," "*Tint,2*," and "*Tint,3*" are greater than the critical value "*Tcri*," the fault-sector-flags "*Fs,1*," "*Fs,2*," and "*Fs,3*" are stored with corresponding sector information (at instant "*tx1*," "*tx2*," and "*tx3*," see Fig. 5), while the counts in the remaining flags ("*Fs,4*," "*Fs,5*," and "*Fs,6*") remains at "0." It

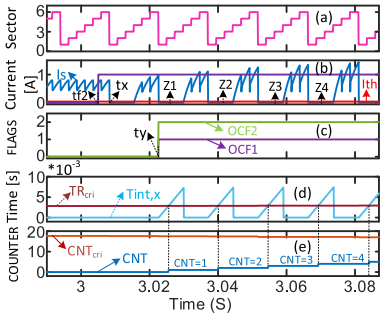


Fig. 6. Simulation results of multiple-switch OCF in switches XH1 and ZL2 (detailed diagnosis at instant "tx" of Fig. 4(a). (a) Sector of operation. (b) Is, Ith, Fault-initiation. (c) OCF1, OCF2. (d) Tint,x, TRcri. (e) CNT, $\mathrm{CNT_{cri}}$.

may be recalled that these flags constitute the matrix $\boldsymbol{F_s}$. Based on the information available in the $\boldsymbol{F_s}$ matrix, the faulty switch numbers are stored in flags "*OCF1*" and "*OCF2*" (at instant "*ty*," see Figs. 4–6; see Table II).

During dynamic conditions, the reference value of speed can cause a momentary dip in the dc-source current (which would eventually be restored to its previous value). This momentary dip could drop down to a value, which is below the threshold value "*Ith*" for a duration that is greater than the critical time-period "*Tcri*" and be misinterpreted as an interruption in the dc-source current leading to the false assertion of OC faults. Whereas, under genuine OC fault conditions, the dc-source current is absent in one or more operating sectors where the faulty switches are expected to conduct. These zero periods appear as periodic oscillations in the dc-source current. This fact is exploited to distinguish genuine OC faults from spuriously detected OC faults and the algorithm corresponding to it is presented in the following paragraphs.

As described earlier, at the end of the pilot-fault-affirmation stage, the faulty switch numbers are stored in the flags "*OCF1*" and "*OCF2*." To confirm the fault conclusively, the probation period of fault diagnosis is stretched to a time period of "Tre" (i.e., "$Tre = tz - ty$" in Fig. 4). During this period of probation, the number of zero-current time periods is counted, which are shown as "*Z1*," "*Z2*"... "*Zn−1*," "*Zn*" (Figs. 6 and 7). Each zero-current time period is validated only when its duration, denoted as "*Tint,x*" (11) is higher than the *recheck-critical-time* period given

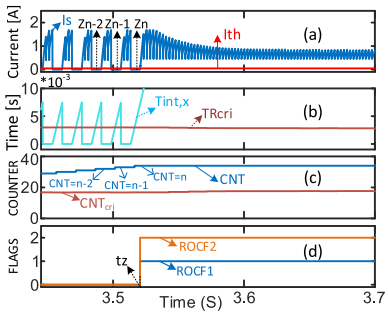


Fig. 7. Simulation results of multiple-switch OCF in switches XH1 and ZL2 (detailed diagnosis at instant "tz" of Fig. 4(a). (a) Is, Ith. (b) Tint,x, TRcri. (c) CNT, $\mathrm{CNT_{cri}}$. (d) ROCF1, ROCF2.

by "*TRcri*" (12). This "*TRcri*" is an integer multiple (*Nzts*) of the critical time period "*Tcri*" (10), where *"Nzts"* is determined by the number of sectors over which the OC fault is detected continuously (Table II), which depends on single-/multiple-switch OC fault conditions. Hence, the *recheck-critical-time* period "*TRcri*" depends on single-/multiple-switch OC faulty condition. The number of such validated zero-transition time periods is stored in a register, named "*CNT*," which is inspected at the end of the probation time period (Tre)

$$Tint,x\,(i) = (fi) * (Tfc) * (Tint,x\,(i-1) + Ts) \quad (11)$$

$$TRcri = Nzts * Tcri. \quad (12)$$

The suspected OC fault is confirmed, when the count value stored in "*CNT*" is more than the critical count value "$CNT_{cri}$" at the end of the "*Tre*" period (13) and (14). This confirmation sets a new flag, named "*ROCF*" (reliable OC fault diagnosis), to "1." The corresponding reliable OC fault switch numbers are stored in the flags "*ROCF1*" and "*ROCF2*" (15) and (16). Table II presents the values of these flags for all possible two-switch OC faults

$$CNT_{cri} = Nzel * Dsf * \frac{T_{re}}{t_{ele}} \quad (13)$$

$$CNT_{cri} = Nzel * Dsf * \frac{T_{re} * p * \omega_{mec}}{4\pi} \quad (14)$$

$$\begin{cases} ROCF = 1; & if\ CNT > CNT_{cri} \\ ROCF = 0; & otherwise \end{cases} \quad (15)$$

$$ROCFx = OCFx * ROCF; (x = 1, 2). \quad (16)$$

The value of critical-count "$CNT_{cri}$" depends on the probation time period "Tre" and the period of the electric cycle "$t_{ele}$" (which depends on the speed of the motor, "$\omega_{\mathrm{mec}}$"). In (13) and (14), the symbols "$D_{sf}$" and "$N_{zel}$," respectively, denote the factor of safety ($0 < D_{sf} < 1$, which is the designer's choice) and the number of zero transitions appearing in an electric cycle due to faulty switches. In this article, $D_{sf}$ is chosen to be 0.5. The values of "*Nzts*" and "*Nzel*" for all possible two-switch combinations are presented in Table II.

For the example considered (OC faults in XH1 and ZL2), when the value of count stored in the register "*CNT*" is greater than the critical value "$CNT_{cri}$" at the end of "*Tre*" (i.e., "*tz* − *ty*" in Figs. 4, 6, and 7), the flags "*ROCF1*" and "*ROCF2*" (see Figs. 4 and 7) are loaded with the faulty switch numbers (16).

Based on the information stored in the flags "*ROCF1*" and "*ROCF2*," which conclusively identify the faulty switches, the process of circuit reconfiguration is initiated. This process consists of energizing the pertinent SPDT relays corresponding to the faulty legs using the actuating signals *Relay-[X, Y, Z]* (presented in Table II). With this action, the motor phase windings, which are connected to the faulty legs of the VSI, are reconnected to the corresponding output terminals of the additional phase legs (*X'*, *Y'*, and *Z'*) resulting in the fault-tolerant operation of the drive. Table II presents the information regarding the backup phase legs, which are substituted for the corresponding phase legs of the VSI (*X*, *Y*, and *Z*).

If the value stored in the counter "*CNT*" is less than the "$CNT_{cri}$," the flag "*ROCF*" remains at the default value of "0" even after the probation period "*Tre*." This indicates that the pilot diagnosis of the OC fault is spurious and hence the process of subsequent circuit reconfiguration is not initiated. Consequently, the pilot-diagnostic system is reset by resetting all flags associated with it ("*Fs,n*," "*Tfc*," "*OCF1*," "*OCF2*," "*CNT*," "*ROCF1*," and "*ROCF2*") and is ready to detect future faults.

This procedure of fault diagnosis can also be extended for three-switch OC fault conditions. The three-switch faults can be subdivided into two categories; in the first case, the three faulty switches belong to three different inverter legs. In the second case, two out of the three faulty switches are from one phase-leg, while the other one is present in any one of the remaining two legs.

As an example, for the OC fault in switches XH1, YH3, and ZL2 (first case), the dc-source current shows a discontinuity in sectors—(1 to 4). Correspondingly, the flags "*Fs,1*" to "*Fs,4*" are set to "1." It may be verified that this situation is indistinguishable from the two-switch OC fault condition, wherein switches XH1 and YH3 develop OC faults. To resolve this issue, it is initially assumed that the developed fault is a two-switch fault (OC faults in XH1 and YH3) and the circuit is reconfigured accordingly. This action is termed pilot-reconfiguration. Obviously, this pilot reconfiguration is inadequate as the OC fault in the switch ZL2 is not covered, as it is not discovered yet. To discover the three-switch OC fault, the dc-source current is further probed. If the dc-source current reveals further oscillations (in sectors 2 and 3), it is a clear indication that the fault is indeed a three-switch OC fault and a new flag "*ROCF3*" is set to the number corresponding to the faulty switch (two in this example). Accordingly, *Relay-Z* is actuated to bring in the backup *leg-Z'* (Fig. 1), completing the process of postfault circuit reconfiguration.

In the second case, wherein switches XH1, XL4, and ZL2 develop the OC fault, the dc-source current would be absent in as many as five of the six sectors (sectors 1–5). It may be verified that this situation is indistinguishable from the one, wherein the switches XH1, XL4, and YH3 develop the OC fault. In this condition, first, switch numbers corresponding to XH1 and XL4 are stored in flags "*ROCF1*" and "*ROCF2*," based on which

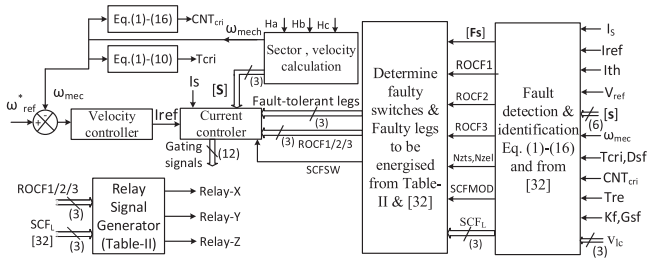


Fig. 8. Schematic overview of control scheme employed for fault-tolerant drive operation.

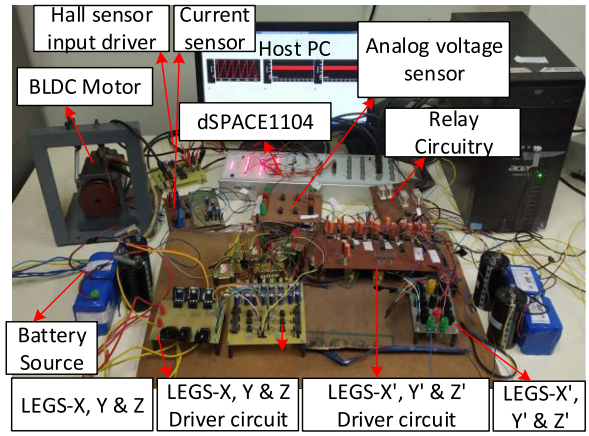


Fig. 9. Experimental setup of proposed fault-tolerant configuration.

the pilot-circuit reconfiguration is carried out. After this act, the dc-source current is further probed. Based on the sectors in which it is absent, the faulty switch is identified and the corresponding number is stored in the flag "*ROCF3*."

### *B. Single-Switch Short-Circuit Fault-Diagnosis Algorithm*

The SC fault is detected by extending the diagnosis algorithm presented in [32], which is applicable to a single-switch SC fault. In the single switch detection algorithm described in [32], six line–line voltages need to be sensed, which need to be electrically isolated from the power circuit. As Hall-voltage sensors are expensive, low-cost analog isolation amplifiers (based on ISO-124) are employed, which are capable of achieving the same bandwidth as that of a Hall sensor. The fault sensing algorithm exploits the nonconducting interval of 60° (electrical) between the top and bottom devices in any phase-leg of the VSI [32]. Unlike the case of the fault-tolerant BLDC motor drive proposed in [32], which needs six sensors, the proposed configuration requires only three line-voltage signals. This reduces the cost of sensors and increases reliability.

The overall performance of the proposed fault-tolerant BLDC motor drive system is assessed with experimental studies in open-loop as well as closed-loop operation. The closed-loop drive operation uses the traditional outer speed control loop and the inner current control loop. The schematic overview of the closed-loop control system for the proposed fault-tolerant drive is shown in Fig. 8.

## IV. Results and Discussion

An experimental prototype is built to verify the working principle of the proposed fault-tolerant BLDC motor drive, which is shown in Fig. 9. In this system, dSPACE-1104 is employed as the control platform. Ratings and parameters of the BLDC motor used for simulation as well as experimentation are presented in Table II, which is presented in Section III.

Experimental results pertaining to the performance of the proposed fault-tolerant drive topology against single as well as multiple-switch OC faults are presented in Figs. 10–16.

The procedure for diagnosing a two-switch OC fault and the subsequent fault-tolerant operation of the proposed multiple-switch fault-tolerant drive topology (Fig. 1) are shown in Figs. 10–12. When the drive is operated in an open-loop and OC faults are wilfully induced in switches XH1 and ZL2 (at instant

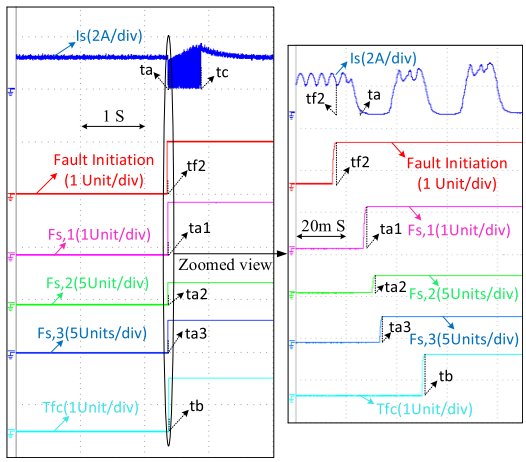


Fig. 10. Experimental results presenting the status of the flags during OC fault in switches XH1 and ZL2 (left-side: normal-view and right-side: zoomed view of the encircled figure portion).

"*tf2*," Fig. 10), the dc-source current falls below its threshold value in sectors 1, 2, and 3 (from instant "*ta*"), which pertain to the faulty devices as indicated in Fig. 2. Correspondingly, the fault-sector-flags "*Fs,1*," "*Fs,2*," and "*Fs,3*," described in Section III, are set at the instants "*ta1*," "*ta2*," and "*ta3*" as shown in Fig. 10. Furthermore, the *electric-fault-cycle* "*Tfc*" is set to "1" at the instant "*tb*." With the available *fault-sector-flag* matrix information "***Fs***" at the instant "*tb*," the faulty switches are identified (from Table II) and the corresponding faulty switch numbers are stored in flags "*ÓCF1*" and "*OCF2*" at instant "*tb*" as shown in Fig. 11. The periodic absence in the dc-source current "*Is*" is further examined till the end of the probation period as described earlier in Section III. When the number of oscillations in the dc-source current counted in the pertinent accumulators (denoted as "CNT") exceeds a critical value ("$CNT_{cri}$") as shown in Fig. 11(at instant "*tc*"), the multiple-switch fault is conclusively asserted and the numbers corresponding to the faulty switches are loaded in flags "*ROCF1*" and "*ROCF2*" (at instant "*tc*," Fig. 12). With the information available in

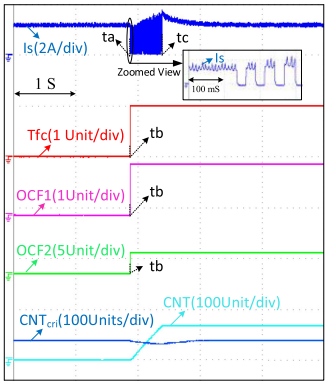


Fig. 11. Experimental results presenting the status of the counter and flags during OC fault in switches XH1 and ZL2.

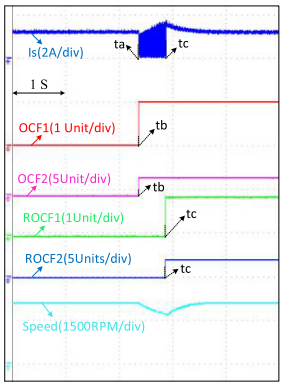


Fig. 12. Experimental results presenting the fault-tolerant drive operation during OC fault in switches XH1 and ZL2.

flags "*ROCF1*" and/or "ROCF2," the process of postfault circuit reconfiguration is triggered by energizing pertinent SPDTs (*SPDT-X* and *SPDT-Z*) in the present case (see Fig. 3 and Table II). From the bottom trace, which shows the speed of the BLDC motor, it is evident that the postfault speed (after the postfault circuit reconfiguration) is the same as the prefault speed. This conclusively proves that the proposed fault-tolerant BLDC motor drive is capable of delivering rated power at the rated speed (developing the rated torque), thus achieving the objective of obtaining 100% fault tolerance against two-switch faults.

Another example of OC multiple-switch fault-tolerant operation for the switches XH1 and XL4 under open-loop operation is shown in Figs. 13 and 14. Fig. 13 shows the status of the counter and other flag information loaded during the diagnosis procedure (Section III) of the multiple-switch OC fault condition in the switches XH1 and XL4. From Fig. 14, it can be noticed that the drive retains its capability of delivering the rated power after the detection of the OC fault and the subsequent process of circuit reconfiguration (Fig. 14). It should be noted that the fault-tolerant operation for a two-switch OC fault that occurred in the same inverter leg can be implemented using a derived single-switch fault-tolerant drive topology [Fig. 3(c)].

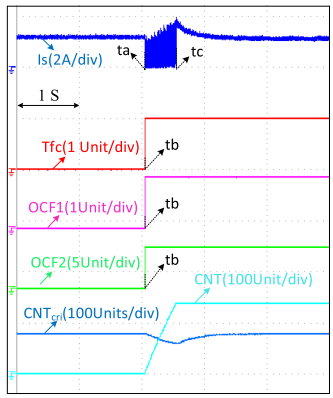


Fig. 13. Experimental results presenting the status of the counter and flags during OC fault in switches XH1 & XL4.

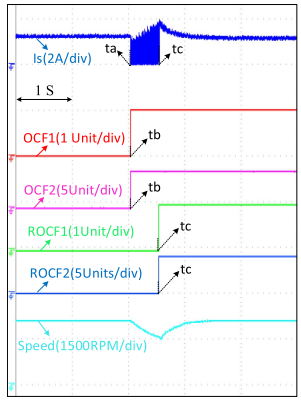


Fig. 14. Experimental results presenting the fault-tolerant drive operation during OC fault in switches XH1 & XL4.

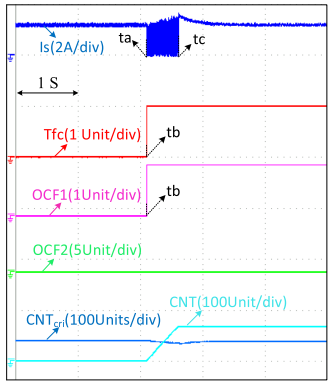


Fig. 15. Experimental results presenting the status of the counter and flags during OC fault in switches XH1.

Figs. 15 and 16 demonstrate the processes of fault diagnosis as well as fault-tolerant operation for a single-switch OC fault using the derived single-switch fault-tolerant topology [Fig. 3(c)]. In this experiment, an OC fault is enforced on the switch XH1 under open-loop drive operation. Fig. 16 validates the post-fault rated power (hence speed) delivering capability to the BLDC motor drive configuration.

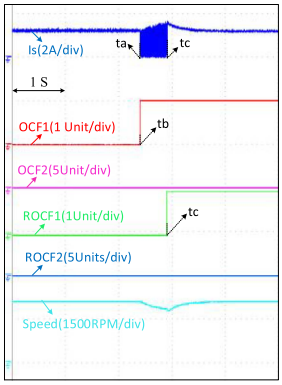


Fig. 16. Experimental results presenting the open-loop fault-tolerant drive operation during OC fault in switches XH1.

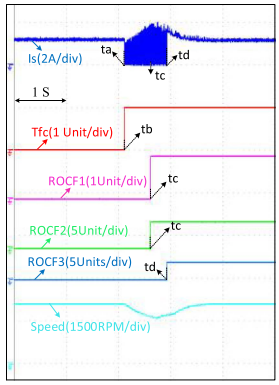


Fig. 18. Experimental results presenting the fault-tolerant drive operation during OC fault in switches XH1, YH3, and ZL2.

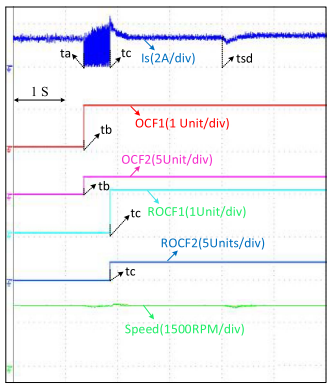


Fig. 17. Experimental results presenting the closed-loop fault-tolerant drive operation during OC fault in switches XH1 and ZL2.

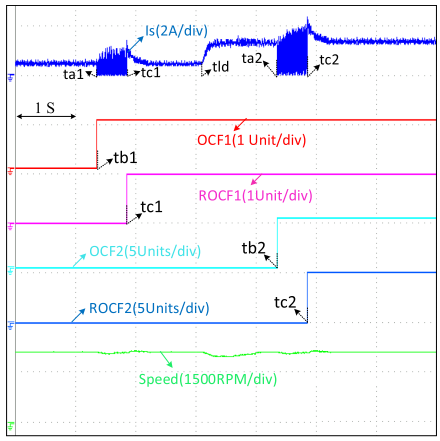


Fig. 19. Experimental results presenting the closed-loop fault-tolerant drive operation for sequential OC fault in switches XH1 and ZH5 under different loading conditions.

The suitability of the proposed multiple-fault tolerant BLDC motor drive for closed-loop speed control applications is demonstrated in the experimental results presented in Fig. 17. To demonstrate this capability, OC faults are created in the switching devices XH1 and ZL2 (Fig. 3). The closed-loop drive control system is implemented as shown in Fig. 8. With closed-loop speed control, it may be observed that the speed is restored to the reference value following the source disturbance created at the instant "*tsd*" (Fig. 17).

Fault-tolerant operation of the proposed drive against a three-switch OC fault is shown in Fig. 18. In this experiment, the switches XH1, YH3, and ZL2 are intentionally turned OFF. For this fault, the dc-source current drops to zero in sectors 1, 2, 3, and 4. The complication is that this fault is indistinguishable from the two-switch OC fault, wherein the switches XH1 and YH3 develop OC faults. Hence, this fault is initially treated as the two-switch fault (as if only XH1 and YH3 are faulty) and the flags "*ROCF1*" and "*ROCF2*" are set to the corresponding switch numbers at the instant "*tc*" (Fig. 18) to indicate the same. The dc-source current is probed after the circuit reconfiguration corresponding to the two-switch fault. If the dc-source current shows oscillations even after this manoeuvre, it is realized that it is indeed a three-switch fault. Consequently, the flag "*ROCF3*" is set to "2," and the corresponding circuit reconfiguration is initiated. When this process is completed, the drive regains the original speed (Fig. 18). Thus, the full fault tolerance is obtained by the proposed BLDC motor drive.

The fault-tolerant operation of the drive configuration operated under different load conditions is experimentally verified and the results are presented in Fig. 19. First, an OC fault is initiated in switch XH1, under closed-loop drive operation. As mentioned in Section III, after the successful fault diagnosis, the faulty switch number is stored in flag "ROCF1" (at instant "tc1," Fig. 19). Based on the diagnosis information, the SPDT-X relay is energized which replaces the faulty *leg-X* with *leg-X'* (Sections II and III). Once the drive attains its prefault speed, a different load condition is applied to the drive at instant "tld." Due to the closed-loop drive operation, the motor can attain its original speed. Finally, another OC fault is forced on the switch ZH5. In this case, the faulty *leg-z* of the VSI is substituted by the additional *leg-z'*. Thus, this experiment clearly shows the fault-tolerant operation of the drive under different loading conditions.

The experimental result shown in Fig. 20 shows the capability of the proposed drive configuration to handle sequential faults occurring in three different legs. In this experiment, first, the

TABLE III
COMPARISION OF PROPOSED TOPOLOGY WITH THE EXISTED TOPOLOGIES

| Features of the drive topology | Topology-[27] | Topology-[30] | Topology-[31] | Topology-[32] | Topology-[33] | Proposed topology |
|---|---|---|---|---|---|---|
| (1)-Requirement of isolated dc-sources | No | No | No | Yes | Yes | No |
| (2)-Number of switches in inverter | (6)-switches (conventional) and (3)-TRIACs | (6)-switches and (6)-TRIACs and (1)-additional leg | (12)-switches | (12)-switches | (12)-switches | (12)-switches |
| (3)-Ratings of the switches | Motor rated voltage and current | Motor rated voltage and current | Motor rated voltage and twice the motor rated current | Half the motor rated voltage and motor rated current | Motor rated voltage and current | Motor rated voltage and current |
| (4)-Rating of BLDC-motor | Designed for rated current and voltage | Designed for rated current and voltage | Designed for twice the rated value of current | Designed for rated current and voltage | Designed for rated current and voltage | Designed for rated current and voltage |
| (5)-Fault-tolerance | Only OC fault | OC and SC faults | OC and SC faults | OC and SC faults | OC and SC faults | Multiple-switch OC/SC faults |
| (6)-Diagnosis of faults in inverter extra-switches | Not susceptible for faults | No | Yes | Yes | Yes | Not susceptible for faults |
| (7)-Postfault maximum power and torque | Rated power and torque | Rated power and torque | Rated power and torque | Rated torque and half the rated power | Rated power and torque | Rated power and torque |
| (8)-Postfault maximum speed | Rated speed | Rated speed | Rated speed | Half the rated speed | Rated speed | Rated speed |
| (9)-Auxiliary components | No | Buck-converter and (3)-switches and (1) fault-protective-leg | Buck-converter and (1)-SPDT-switch and (1) fault-protective-leg | 2-DPDT relays | 4-DPDT relays | 3-SPDT relays |
| (10)-Suitability of fault-diagnosis for EV-applications | Yes | No | No | Yes | Yes | Yes |

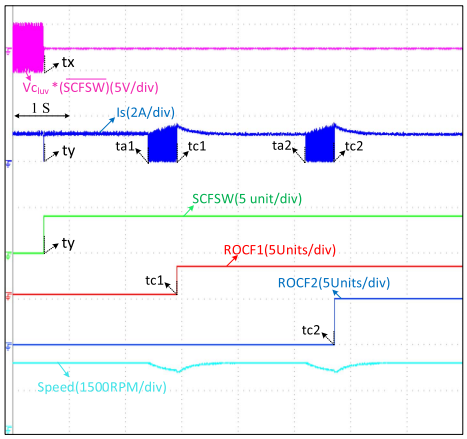


Fig. 20. Experimental results presenting the fault-tolerant drive operation for sequential SC faults in switch XL4, OC faults in switches YH3 and ZH5.

SC fault is inflicted on the switch XL4 by continuously gating it. The SC fault diagnosis algorithm proposed in [32] is used in the present article, which loads the number corresponding to the faulty switch into the flag "*SCFSW*" at the instant "*ty*" (Fig. 20). This event triggers the process of circuit reconfiguration by energizing the "*SPDT-X*," which connects the affected motor phase to the mid-point of the additional leg-X', achieving the required fault tolerance. Once the drive attains its prefault speed, an OC fault is initiated in switch "YH3." The proposed diagnosis algorithm identifies the number corresponding to the faulty switch and stores it in flag "*ROCF1*" at instant "*tc1*" (Fig. 20). This action triggers the *SPDT-Y* (Fig. 1) and the process of reconfiguration is initiated. At the end of the process, the *leg-Y* of the VSI is substituted by the additional *leg-Y'*, as explained in Section II. Finally, another OC fault is inflicted on the switch ZH5. In this case, the faulty *leg-z* of the VSI is substituted by the additional *leg-z'*. Thus, this experiment clearly demonstrates that the proposed drive configuration is capable of achieving multiple-switch fault tolerance against both OC and SC faults.

## V. FEASIBILITY STUDIES OF THE PROPOSED ELECTRIC DRIVE TOPOLOGY

Table III presents the comparative analysis of the proposed multiple-switch fault-tolerant BLDC motor drive topology vis-à-vis the other topologies reported in the earlier literature. The economic feasibility of the proposed drive is assessed, which is summarized in Table IV. The cost analysis carried out in this section shows that, though the proposed power converter needs three additional legs to achieve full fault tolerance, it is an affordable proposition, as its raw material cost (RMC) is principally determined by the cost of sensors. It may be noted that the proposed power converter brings in a significant reduction in the number of sensors and auxiliary component requirements when compared to the fault-tolerant converter topologies based on the open-end winding structure [32] and [33].

The analysis presented in Table IV estimates the cost of the additional raw materials to incorporate the feature of fault tolerance into the conventional BLDC motor drive. From Table IV, it can be observed that the proposed multiple-switch fault-tolerant topology requires 6% additional cost compared to its conventional counterpart. In contrast, the single-switch fault-tolerant topologies reported in [32] and [33] require additional costs of 9% and 11%, respectively. Thus, the additional cost required for the proposed multiple-switch fault-tolerant topology is lesser

TABLE IV
COST COMPARISON OF THE PROPOSED MULTIPLE-SWITCH FAULT-TOLERANT DRIVE TOPOLOGY (INDIAN RS.)

| Component name | | | Cost of each unit [Rs./-] | No. of components | Cost in total [Rs./-] |
|---|---|---|---|---|---|
| [a] BLDC motor 3KW; 96V | | | 31780 | 1 | 31780 |
| [b] Cost of battery (Lithium-ion) (12 V, 60 AH,720 WH) | | | 13620 | 8 | 108960 |
| [c] Inverter switches cost along with driver circuitry [Switch-safety-factor for current and voltage considered as 2] | | [$c_a$] Topology-[32] | (64+306) | 12 | 4440 |
| | | [$c_b$] Topology-[33] | (159+306) | 12 | 5580 |
| | | [$c_c$] Proposed topology | (159+306) | 12 | 5580 |
| | | [$c_d$] Traditional inverter | (159+306) | 6 | 2790 |
| [d] Sensors | Current sensors | [$d_a$] Top-[32] and [33] | 1,870 | 2 | 3740 |
| | | [$d_b$] Proposed topology | 1,870 | 1 | 1870 |
| | Analog voltage sensors required (ISO-124 and TL084CN)-[32] | [$d_c$] Top-[32] and [33] | (894+13) | ISO-124 - 6 TL084CN-2 | 5390 |
| | | [$d_d$] Proposed topology | (894+13) | ISO-124 - 3 TL084CN-1 | 2695 |
| [e] Auxiliary components [DPDT-Relays [32] & [33]; SPDT-Relays (Proposed topology)] | | [$e_a$] Topology-[32] | 806 | 2 | 1612 |
| | | [$e_b$] Topology-[33] | 806 | 4 | 3224 |
| | | [$e_c$] Proposed topology | 341 | 3 | 1023 |

Percentage (%) of additional cost used for single-switch OC/SC fault-tolerant topology-[32] with reference to the traditional BLDC motor drive

$$=\left[\frac{d_c+e_a+[c_a-c_e]+d_a}{a+b+c_d}\right]*100\% \quad =\left[\frac{5390+1612+1650+3740}{31781+108960+2790}\right]*100\% = 8.63\%.$$

Percentage (%) of additional cost used for single-switch OC/SC fault-tolerant topology-[33] with reference to the traditional BLDC motor drive

$$=\left[\frac{d_c+e_b+[c_b-c_e]+d_a}{a+b+c_d}\right]*100\% \quad =\left[\frac{5390+3224+2790+3740}{31781+108960+2790}\right]*100\% = 10.55\%.$$

Percentage (%) of additional cost used for the proposed multiple-switch OC/SC fault-tolerant topology with reference to the traditional BLDC motor drive

$$=\left[\frac{d_d+e_c+[c_c-c_e]+d_b}{a+b+c_d}\right]*100\% \quad =\left[\frac{2695+1023+2790+1870}{31781+108960+2790}\right]*100\% = 5.83\%.$$

compared to the single-switch fault-tolerant topologies reported in [32] and [33].

The additional cost to incorporate fault tolerance becomes further insignificant if costs incurred by the vehicle chassis, accessories, body, and aesthetics are considered. This feasibility analysis shows that the proposed fault-tolerant topology could find potential applications in the EV industry.

## VI. CONCLUSION

This article proposes a multiple-switch fault-tolerant BLDC motor drive system, which could find applications where reliability is of paramount interest. The proposed topology is autoreconfigurable and needs fewer additional components and sensors compared to the previously suggested topologies causing a reduction in the RMC and an enhancement of reliability. The proposed power circuit configuration is capable of handling multiple OC and SC switch faults occurring in the VSI. The proposed multiple-switch fault-tolerant topology is capable of delivering rated power to the BLDC motor even after the occurrence of faults. This article also presents algorithms, which diagnose multiple OC faults while avoiding spurious fault detection. The effectiveness of the presented multiple-switch OC fault diagnosis and the associated postfault circuit reconfiguration are experimentally verified. The cost analyses reveal that, compared to the conventional BLDC motor drives, the proposed fault-tolerant systems incur a meagre additional RMC of not more than 6%. Enhanced reliability with a low-cost overhead could make the proposed fault-tolerant BLDC motor drive system find applications for EVs.

## REFERENCES


[1] R. Krishnan, *Permanent Magnet Synchronous and Brushless DC Motor Drives*, 1st ed. Boca Raton, FL, USA: CRC Press, 2010, Ch. 1, pp. 50–51.

[2] C. C. Chan, "An overview of electric vehicle technology," *Proc. IEEE*, vol. 81, no. 9, pp. 1202–1213, Sep. 1993.

[3] C. C. Chan, K. T. Chau, J. Z. Jiang, W. Xia, M. Zhu, and R. Zhang, "Novel permanent magnet motor drives for electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 43, no. 2, pp. 331–339, Apr. 1996.

[4] B. Szadkowski, P. J. Chrzan, and D. Roye, "A study of energy requirements for electric and hybrid vehicles in cities," in *Proc. Int. Conf. Clean, Efficient Safe Urban Transp.*, Jun. 2003, pp. 4–6.

[5] A. M. Lulhe and T. N. Date, "A technology review paper for drives used in electrical vehicle (EV) & hybrid electrical vehicles (HEV)," in *Proc. Int. Conf. Control, Instrum., Commun. Comput. Technol., Kumaracoil*, Dec. 2015, pp. 632–636.

[6] A. E. Aliasand and F. T. Josh, "Selection of motor for an electric vehicle: A review," *Mater. Today: Proc.*, vol. 24, pp. 1804–1815, Jan. 2020.

[7] P. Bhatt, H. Mehar, and M. Sahajwani, "Electrical motors for electric vehicle—A comparative study," in *Proc. Recent Adv. Interdiscipl. Trends Eng. Appl.*, Apr. 2019, pp. 5–10.

[8] H.-X. Wu, S.-K. Cheng, and S.-M. Cui, "A controller of brushless DC motor for electric vehicle," *IEEE Trans. Magn.*, vol. 41, no. 1, pp. 509–513, Jan. 2005.

[9] J. Gan, K. T. Chau, C. C. Chan, and J. Z. Jiang, "A new surface-inset, permanent-magnet, brushless DC motor drive for electric vehicles," *IEEE Trans. Magn.*, vol. 36, no. 5, pp. 3810–3818, Sep. 2000.

[10] D. Nguyen and M. C. Ta, "New direct torque control scheme for BLdc motor drives suitable for EV applications," in *Proc. IEEE Veh. Power Propulsion Conf.*, Oct. 2014, pp. 1–5.

[11] C. Xia, Y. Xiao, W. Chen, and T. Shi, "Torque ripple reduction in brushless DC drives based on reference current optimization using integral variable structure control," *IEEE Trans. Ind. Electron.*, vol. 61, no. 2, pp. 738–752, Feb. 2014.
[12] F. W. Fuchs, "Some diagnosis methods for voltage source inverters in variable speed drives with induction machines—A survey," in *Proc. 29th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2003, pp. 1378–1385.
[13] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May/Jun. 2011.
[14] W.-S. Im, J.-S. Kim, J.-M. Kim, D.-C. Lee, and K.-B. Lee, "Diagnosis methods for IGBT open switch fault applied to 3-phase AC/DC PWM converter," *J. Power Electron.*, vol. 12, no. 1, pp. 120–127, 2012.
[15] B. Park, J. Lee, and D. Hyun, "A novel short-circuit detecting scheme using turn-on switching characteristic of IGBT," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, Oct. 2008, pp. 1–5.
[16] M. A. Rodríguez-Blanco et al., "A failure-detection strategy for IGBT based on gate-voltage behavior applied to a motor drive system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1625–1633, May 2011.
[17] J. O. Estima and A. J. Marques Cardoso, "A new algorithm for real-time multiple open-circuit fault diagnosis in voltage-fed PWM motor drives by the reference current errors," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3496–3505, Aug. 2013.
[18] F. Wu and J. Zhao, "A real-time multiple open-circuit fault diagnosis method in voltage-source-inverter fed vector controlled drives," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1425–1437, Feb. 2016.
[19] C.-J. Bae, D.-C. Lee, and T. H. Nguyen, "Detection and identification of multiple IGBT open-circuit faults in PWM inverters for AC machine drives," *IET Power Electron.*, vol. 12, pp. 923–931, Apr. 2019.
[20] K. K. Nallamekala and K. Sivakumar, "A fault-tolerant dual three-level inverter configuration for multipole induction motor drive with reduced torque ripple," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1450–1457, Mar. 2016.
[21] B. S. Umesh and K. Sivakumar, "Dual-inverter-fed pole-phase modulated nine-phase induction motor drive with improved performance," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5376–5383, Sep. 2016.
[22] B. P. Reddy, M. Rao A, M. Sahoo, and S. Keerthipati, "A fault-tolerant multilevel inverter for improving the performance of a pole–phase modulated nine-phase induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1107–1116, Feb. 2018.
[23] S. Yang, X. Sun, M. Ma, X. Zhang, and L. Chang, "Fault detection and identification scheme for dual-inverter fed OEWIM drive," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 6112–6123, Jul. 2020.
[24] T. Gopalarathnam, H. A. Toliyat, and J. C. Moreira, "Multi-phase fault-tolerant brushless DC motor drives," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 35th IAS Annu. Meeting World Conf. Ind. Appl. Elect. Energy*, Oct. 2000, pp. 1683–1688.
[25] M. Villani, M. Tursini, G. Fabri, and L. Castellini, "High reliability permanent magnet brushless motor drive for aircraft application," *IEEE Trans. Ind. Electron.*, vol. 59, no. 5, pp. 2073–2081, May 2012.
[26] Y. H. Kim, H. J. Heo, J. H. Park, and J. M. Kim, "Fault tolerant control methods for dual type independent multi-phase BLdc motor under the open-switch fault conditions," *J. Elect. Eng. Technol.*, vol. 13, no. 2, pp. 722–732, 2018.
[27] B. Park, K. Lee, R. Kim, T. Kim, J. Ryu, and D. Hyun, "Simple fault diagnosis based on operating characteristic of brushless direct-current motor drives," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1586–1593, May 2011.
[28] R. R. Errabelli and P. Mutschler, "Fault-tolerant voltage source inverter for permanent magnet drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 500–508, Feb. 2012.
[29] X. Huang, A. Goodman, C. Gerada, Y. Fang, and Q. Lu, "A single sided matrix converter drive for a brushless DC motor in aerospace applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3542–3552, Sep. 2012.
[30] H. Li, W. Li, and H. Ren, "Fault-tolerant inverter for high-speed low-inductance BLdc drives in aerospace applications," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2452–2463, Mar. 2017.
[31] J. Feng, K. Liu, and Q. Wang, "Scheme based on buck-converter with three-phase H-bridge combinations for high-speed BLdc motors in aerospace applications," *IET Elect. Power Appl.*, vol. 12, no. 3, pp. 405–414, Mar. 2018.
[32] P. H. Kumar, S. Lakhimsetty, and V. T. Somasekhar, "An open-end winding BLdc motor drive with fault diagnosis and auto reconfiguration," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3723–3735, Dec. 2020.
[33] H. K. Patnana and S. Veeramraju Tirumala, "A cost-effective and fault-tolerant brushless direct current drive with open-stator windings for low power electric vehicles," *Int. J. Circle Theor. Appl.*, vol. 49, no. 9, pp. 2885–2908, May 2021.
[34] [Online]. Available: https://www.goldenmotor.com/

**Patnana Hema Kumar** received the M.Tech. degree in power electronics and drives in 2017 from the National Institute of Technology Warangal, Warangal, India, where he is currently working toward the Ph.D. degree with the Department of Electrical Engineering.

His research interests include electric drives, multilevel inversion with open-end winding motors, and PWM strategies.

**V. T. Somasekhar** (Member, IEEE) received the bachelor's degree in electrical engineering from the Regional Engineering College Warangal (National Institute of Technology), Warangal, India, in 1988, the master's degree in power electronics from IIT Bombay, Bombay, India, in 1990, and the Ph.D. degree in control of open-end winding IM drives from the Indian Institute of Science, Bengaluru, India, in 2003.

He worked as an Research and Development Engineer with the Perpetual Power Technologies, Bengaluru, and as a Senior Engineer with the Kirloskar Electric Company Ltd., Mysore, India, during 1990–1993. He joined the Faculty of Electrical Engineering, National Institute of Technology, Warangal, in 1993, where he is currently serving as a Professor. His research interests are multilevel inversion with open-end winding induction motors, ac drives, and pulsewidth modulation (PWM) strategies.