A Single-Stage Quasi-Z-Source-Based 5-Level Grid-Tied PV Inverter With Reduced Leakage Current

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***Abstract*— This article presents a single-staged quasi-z-source (qZS)-based 5-level inverter topology for grid-tied photovoltaic applications. In this topology, two symmetrical qZS networks with a single dc source are fused with a 5-level hybrid inverter. When compared to the existing qZS-based 5-level inverters in the literature, the proposed power converter employs fewer semiconductor switching devices, enhancing its reliability. The objectives of boosting the voltage of the input PV source, as well as the synthesis of a 5-level output voltage are achieved with a modified level-shifted PWM scheme. Furthermore, closed-loop control schemes are implemented for the proposed power converter in both standalone and grid-tied modes of operation and its dynamic performance is assessed. The operability of the proposed power converter in the grid-tied mode of operation is demonstrated by injecting active power into the grid at the unity power factor (UPF). It is also shown that the proposed topology is capable of reducing the leakage current, which is one of the major safety concerns in transformerless PV systems. Experimental results obtained with a laboratory prototype, validate the operating principles of the power converter in both standalone and grid-tied modes of operation.**

***Index Terms*— Leakage current, multilevel inverter (MLI), quasi-Z-source (qZS) network, voltage boosting.**

I. Introduction

AFFORDABLE costs of semiconductor devices [1] and photovoltaic (PV) panels motivate researchers, manufacturers, and governments to promote PV-based electric power. Other advantages of PV-based generation include environmental friendliness, durability, and low maintenance. Solar PV systems are operated in standalone mode for water pumping, rural electrification, and street lighting applications. Also, grid-tied PV systems are gaining momentum due to the ever-increasing nature of electrical energy.

Conventionally, in grid-tied PV systems, the objectives of boosting the inadequate PV input voltage and the dc–ac conversion are achieved with a two-staged system, consisting of a boost converter and conventional VSI. In recent times, quasi-z-source (qZS)-based solar PV systems attract the attention of researchers [2]. Owing to their single-stage nature, these topologies can accomplish both of the aforementioned objectives with reduced switching resources, smaller sizes of passive components, lower cost, and enhanced efficiency [3], [4].

In the past two decades, multilevel inverters (MLIs) gained much attention as they are suitable for high power and high voltage applications [5], [6]. With an increased number of voltage levels, MLIs reduce the voltage stress across the power semiconductor switching devices and derive a superior harmonic performance compared to the conventional two-level VSIs. However, owing to their buck-typed nature, conventional MLIs require that the input dc voltage be higher than the desired peak value of the ac output voltage. Single-stage systems aim to overcome this disadvantage by fusing an MLI with a qZS network. Thus, single-stage MLIs are inherently regarded as boost-type inverters.

Initial investigations of single-stage systems were confined to qZS-based neutral point clamped (NPC) and cascaded H-bridge (CHB) topologies. A 3-level qZS-NPC topology was reported in [7], wherein two symmetrical qZS networks are interfaced with an NPC inverter. This topology suffers from the drawbacks associated with the conventional NPC, such as additional clamping diodes and neutral-point deviation [8], [9]. In qZS-CHB topologies [10], [11], [12], each unit of the H-bridge inverters is interfaced with a qZS network to boost the voltage of an isolated PV panel. However, the extension of CHB topologies to a higher number of voltage levels involves a corresponding increase in the number of qZS networks (and the associated passive components). Other complexities associated with the qZS-based CHB inverters are: 1) distributed MPPT control and 2) individual dc-link voltage regulation [13]. In [14], a 5-level inverter is proposed, which employs only one inductor and one capacitor in each qZS, halving the number of passive components, compared to the earlier topologies. However, two diodes and two switches are additionally needed in this topology to provide the boosting capability, increasing the switching power losses in the semiconductors. All of the aforementioned topologies [10], [11], [12], [13], [14] require more than one PV source. In an attempt to minimize the number of input sources and inductors, a modified power converter is proposed in [15]. With eight switching devices, this topology requires only two inductors and one PV source to produce a 5-level output voltage waveform. However, this

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topology results in increased voltage and current stresses in the devices when compared to the multiple-source qZS-CHB topologies. Moreover, the input current drawn from the dc source is discontinuous, which does not auger well for PV applications. The qZS-based 5-level topology presented in [16] employs eight switching devices and is a combination of NPC and T-type inverters. This topology suffers from the drawbacks of additional clamping diodes which are required for freewheeling operation.

Generally, in PV systems, a parasitic capacitor is formed between the grounded PV frame and the PV array. Common-mode voltage of the MLI results in high-frequency voltage transitions across this parasitic capacitor. In the absence of galvanic isolation, this capacitive coupling facilitates the flow of leakage current from the PV array to the ground. The shoot-through (ST) state which is essential for the operation of quasi-impedance (qZ) sources would result in additional high-frequency voltage transitions in CMV, further aggravating the problem of leakage current. To ensure the safety to the operating personnel, this leakage current should be limited to less than 300 mA as per the stipulation laid out by the standard VDE0126-1-1 [17].

In conventional single-phase inverters, the CMV is reduced either with modulation schemes of inverters or by devising newer topologies. In modulation methods, appropriate voltage vectors are employed to reduce the CMV [18], [19]. Alternatively, additional semiconductors are used to decouple ac and dc sides to eliminate the leakage current [20]. For three-phase qZSI topologies, the CMV is reduced by the modification of SVPWM [21], [22] and the addition of a fast recovery diode in the negative path of the PV panel [23]. To minimize the high-frequency voltage transitions in CMV for a single-phase qZSI, a modified PWM technique is suggested in [24], which chooses appropriate zero states. The power converter topology described in [25] employs two additional switches to create an alternative path between the negative dc terminal of the PV panel to the grid. These switches are operated at the grid frequency to clamp the parasitic voltage across the capacitor either to zero or to the grid voltage. The proposed power converter in [26] connects two extra switches and diodes across the grid terminals. These additional devices are switched during the zero states to isolate the PV source from the grid, paving the way to the minimization of voltage transitions in the CMV. However, the aforementioned literature [24], [25], [26] is limited to the minimization of leakage current in qZS-based single-phase 2-level inverter topologies.

The following limitations are found in single-phase single-stage systems: 1) multiple PV sources; 2) an increased number of switches, 3) discontinuous input current; and 4) leakage current. These shortcomings are the motivating factors for the proposal of a 5-level qZS-based MLI (5L-qZSI) in this manuscript. The proposed power converter operates with a dual-qZS network with a single dc source and a lower number of switching devices. A modified level-shifted PWM scheme is implemented to synthesize a 5-level output voltage waveform and to obtain the required voltage boosting of the PV sources. A symmetrical LCL filter is employed to minimize the high-frequency voltage transitions across the parasitic capacitor of the PV panel. It is shown that the leakage current is restricted to be well within the limit of the standard set by VDE0126-1-1 [17]. The experimentally obtained steady state and dynamic performances of the proposed power converter are presented in both the standalone and the grid-tied modes of operation.

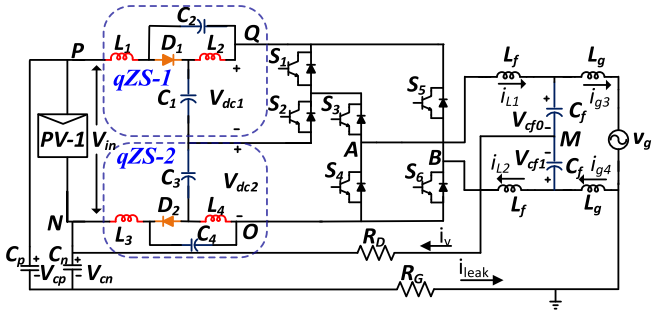

Fig. 1. Proposed 5L-qZSI.

TABLE I
DIFFERENT SWITCHING LOGIC TO OBTAIN 5-LEVEL OPERATION

State-type	Switching states (1-ON, 0-OFF)						Output Voltage 'V_{AB}'	V_{AB} for (V_{dc1}= V_{dc2}=0.5V_{dc})
	S_1	S_2	S_3	S_4	S_5	S_6		
NST-1	1	0	1	0	0	1	$V_{dc1}+V_{dc2}$	V_{dc}
NST-2	0	1	1	0	0	1	V_{dc2}	$0.5V_{dc}$
NST-3	0	1	0	1	0	1	0	0
NST-4	0	1	1	0	1	0	$-V_{dc1}$	$-0.5V_{dc}$
NST-5	0	1	0	1	1	0	$-(V_{dc1}+V_{dc2})$	$-V_{dc}$
ST-1	1	1	1	1	0	1	0	0

II. qZS-BASED 5-LEVEL HYBRID INVERTER

A. Power Converter

Fig. 1 shows the proposed single-stage PV-fed qZS-based 5-level hybrid inverter. This converter employs a single PV source, two qZS networks (qZS-1 and qZS-2), and a hybrid 5-level inverter. The output terminals of the PV source are input to the qZS networks, which boost the low voltage of the PV source. The hybrid 5-level inverter consists of three independent legs (S_1, S_2), (S_3, S_4), and (S_5, S_6). The switching legs (S_1, S_2) and (S_3, S_4) are connected in a cascade, which serves to provide a short circuit path to the qZS networks when they are operated in the ST mode. A separate switching leg (S_5, S_6) is connected across the positive terminal of the top qZS network (shown as "Q" in Fig. 1) and the negative terminal of the bottom qZS network (shown as "O" in Fig. 1). This facilitates five-level inversion across the output terminals "A" and "B." The 5-level inverter is interfaced with the grid through a symmetrical LCL filter. The role of the circuit components R_D, R_G, *Cp*, and *Cn* are discussed in detail in the section pertaining to the leakage current.

B. Switching States and Corresponding Output Voltage Levels of the Power Converter

The switching combinations of the proposed power converter, along with the corresponding voltage levels which reveals that it can achieve 5-level inversion are presented in Table I. Of the six switching states shown in Table I, five correspond to the non-ST (NST) states. These NST states

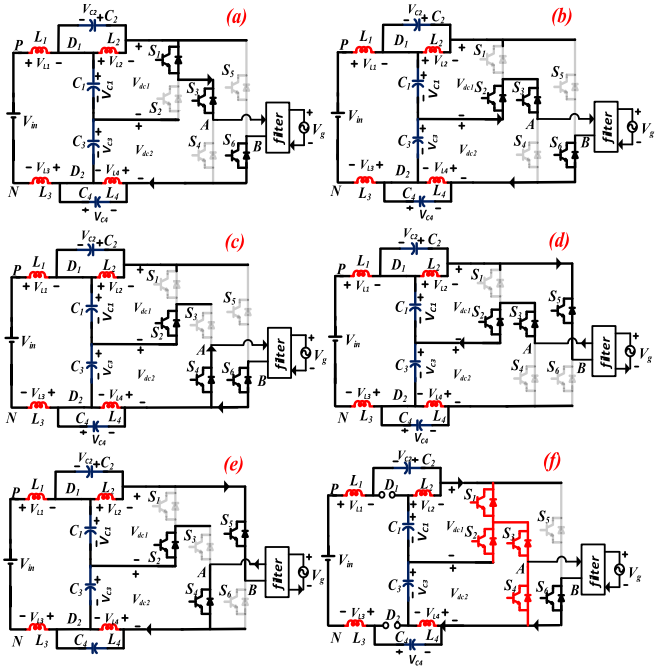

Fig. 2. Circuit diagram of (a)–(e) non-shoot-through states. (f) Shoot-through state.

synthesize the required voltage levels from the inverter. The remaining state, which is known as the ST state, is used to boost the voltage of the input PV source. Fig. 2 shows the operational modes (NST and ST) of the proposed power converter corresponding to the switching states shown in Table I. From Fig. 2(a), it may be observed that switches S_1, S_3, and S_6 are turned on to apply the total dc-link voltage of "$V_{dc1} + V_{dc2}$" across the load. When switches S_2, S_3, and S_6 are turned on, only half the total dc-link voltage "V_{dc2}" is applied across the load terminals as shown in Fig. 2(b). Fig. 2(c) demonstrates the zero state where only two switches S_4 and S_6 are turned on to produce the freewheeling path. Similarly, the corresponding operational modes, which produce the negative voltage levels in the output voltage across the load are shown in Fig. 2(d) and (e).

During the NST state, the voltages across the four inductors and the total dc-link voltage are expressed as

$$V_{L1} + V_{L3} = V_{\text{in}} - V_{C3} - V_{C1} \tag{1}$$

$$V_{L2} = -V_{C2} \tag{2}$$

$$V_{L4} = -V_{C4} \tag{3}$$

$$V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}} = (V_{C1} + V_{C2}) + (V_{C3} + V_{C4}). \tag{4}$$

It may be observed that during the zero state, there is no power transfer between the PV source and the load. A fraction of the zero-state [see Fig. 2(c)] is allocated to insert the ST state, which is pivotal to the implementation of the boosting operation, wherein all four switches S_1–S_4 are turned on to provide the short circuit path to qZS networks [see Fig. 2(f)].

The PWM scheme adopted in this work attaches a zero state to all of the NST states. As an ST state is inserted in every zero-state, the dc-link voltage falls periodically to a value of zero, making it appear as a pulsed waveform. The pulsation

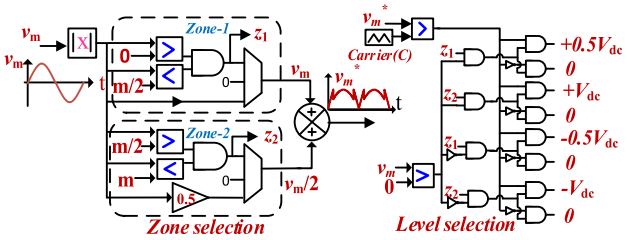

Fig. 3. Implementation of the modulation scheme for 5L-qZSI.

in the dc-link voltage causes a corresponding pulsation in the output voltage. Thus, the instantaneous value of the output voltage falls to a value of zero at all voltage levels.

During the ST state, the voltages across the inductors and the total dc-link voltage are expressed as

$$V_{L1} + V_{L3} = V_{\text{in}} + V_{C2} + V_{C4} \tag{5}$$

$$V_{L2} = V_{C1} \tag{6}$$

$$V_{L4} = -V_{C3} \tag{7}$$

$$V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}} = 0. \tag{8}$$

C. Boost Factor

Application of the volt-sec balance to all of the inductor voltages over one switching time period paves the way to the derivation of the boost factor obtained with the proposed power converter. Each switching time period consists of one of the NST modes (1)–(3) and the ST mode (5)–(7). It may be noted that the symmetry of the qZS networks results in $V_{C1} = V_{C3}$ and $V_{C2} = V_{C4}$.

The voltages across the capacitors are expressed as

$$V_{C1} = V_{C3} = \frac{(1-D)}{(1-2D)}\frac{V_{\text{in}}}{2} \tag{9}$$

$$V_{C2} = V_{C4} = \frac{(D)}{(1-2D)}\frac{V_{\text{in}}}{2} \tag{10}$$

where "D" is the ST duty ratio, defined as T_{sh}/T_s (where T_{sh} and T_s, respectively, denote the ST time and the time period of the switching cycle).

Hence, the total boosted dc-link voltage from (4) is expressed as

$$V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}} = \frac{1}{(1-2D)}V_{\text{in}}. \tag{11}$$

III. Modulation Scheme

A. Modulation Scheme for the Proposed Power Converter

The proposed power converter is modulated with a level-shifted PWM technique, which is capable of achieving the twin objectives of boosting the PV voltage as well as the generation of a 5-level output voltage waveform. Fig. 3 presents the schematic of the modulator, which generates the modulation signal v_m^* which is compared with the carrier C_1 to synthesize the gating signals for the power semiconductor switching devices. The modulator (see Fig. 3) performs two tasks namely: 1) zone selection and 2) level selection. In zone selection, the sinusoidal control signal "v_m" is divided into

two zones (z_1 and z_2) based on the value of the modulation index "m" as shown in Fig. 3. In zone-1 ($0 < v_m < m/2$), the modulating signal doesn't undergo any change. In zone-2 ($m/2 < v_m < m$), the modulating signal v_m is scaled down to $v_m/2$. The summation of the references generated in zone-1 and 2 synthesizes the modulation signal v_m^* as shown in Fig. 3.

In level selection, the required output level is selected based on the following factors: 1) polarity of the control signal "v_m;" 2) zone of operation (z_1 and z_2); and 3) comparison output of v_m^* and carrier signal "C." For example, if the control signal $v_m > 0$ and it is in zone-1 ($0 < v_m < m/2$) of operation, then the output voltage is switched to zero volts when $v_m^* <$ carrier (C) and switched to "0.5 V_{dc}" when $v_m^* >$ carrier (C). Furthermore, the required gating sequence of the selected level is chosen from Table I (NST-1 to NST-5).

To augment the functionality of ST to the level-generation described above, the power devices corresponding to the ST state should also be turned on (see the last row of Table I). The generation of the ST signal (S_T) is accomplished by the comparison of a dc reference signal (v_{sh}) with the carrier wave (C, Fig. 4). Thus, it is evident that the actual gating signals to the power devices S_1–S_4 are obtained by the logical OR operation of the level-generating gating signals (S_{11}–S_{44}, Fig. 4) with the ST-generating gating signals (S_T, Fig. 4). It should be noted that the switching devices S_5 and S_6 are low-frequency signal operated at grid frequency (see Fig. 4). These signals are generated based on the polarity of the control signal "v_m" (see Fig. 3).

IV. Proposed Control Strategy for Stand Alone and Grid Connected 5L-qZSI

A. Standalone Mode

The proposed power converter offers two degrees of freedom to regulate the output voltage to the desired rms value: 1) modulation index "m" and 2) shoot-thorough duty ratio "D." Generally, in the standalone mode of operation, the output voltage is regulated with exclusive control of the ST duty ratio "D" while keeping the modulation index "m" as a constant. By controlling the duty ratio "D" the dc-link voltage of the converter is regulated to a constant value, irrespective of the source and load disturbances.

In the proposed 5L-qZSI, the total dc-link voltage ($V_{dc1} + V_{dc2}$) drops to a value of zero whenever a shoot-thorough state is inserted in the zero-state [shown in Fig. 2(f)] and assumes the value of the boosted dc-link during the NST states. This results in a pulsating signal, which cannot be directly used as a feedback signal to the PI controller. Hence an indirect closed-loop control of the dc-link voltage of the proposed power converter is shown in Fig. 5.

From Fig. 5, it may be noted that the total dc-link voltage (V_{dc}) is estimated by sensing the capacitor voltages "V_{c1}," "V_{c3}," and "D." This estimated dc-link voltage (V_{dc}) is then compared with the reference dc-link voltage (V_{dc}^*) and the error generated is compensated by the PI controller. The duty ratio "D" is generated by comparing the output of the PI controller (the dc reference signal V_{sh} shown in Fig. 4) with the carrier C to introduce the ST state in the switches S_1–S_4.

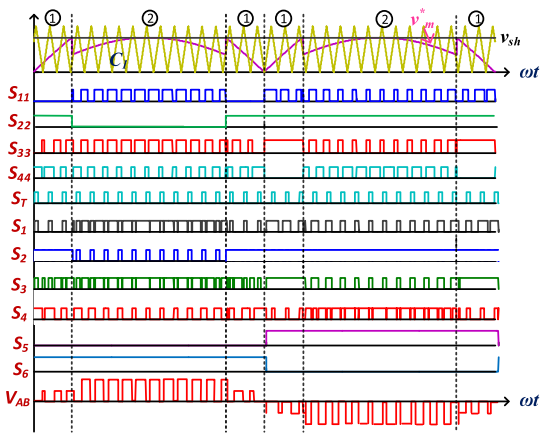

Fig. 4. Implementation of the modulation technique.

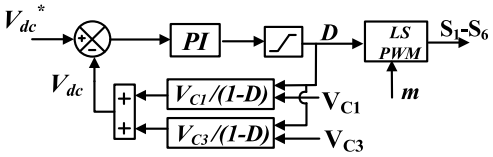

Fig. 5. Indirect dc-link voltage regulation of the proposed 5L-qZSI.

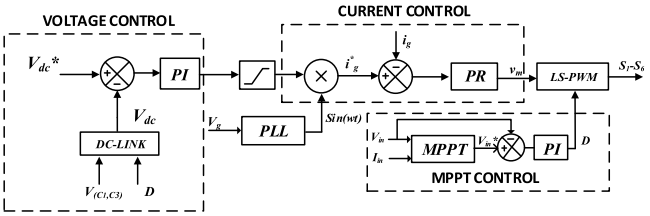

Fig. 6. Control scheme for grid-tied 5L-qZSI.

B. Grid-Connected Mode

Fig. 6 presents the control scheme for the proposed power converter to inject active power into the grid. This control scheme has an independent MPPT control (to extract the maximum power from the PV source), an outer voltage loop to regulate total dc-link voltage, and an inner current control loop to inject active power at unity power factor (UPF). As discussed earlier, the two degrees of freedom, namely the modulation index (m) and the ST duty factor (D) are utilized to achieve these objectives.

To track the maximum power point of the PV panel, a simple P&O algorithm is implemented. The voltage (V_{in}) and current (I_{in}) of the PV source are sensed and fed to the P&O algorithm. The MPPT tracks the maximum power, by generating the reference input voltage (V_{in}^*). Furthermore, the reference input voltage (V_{in}^*) is compared with the actual input voltage of the PV panel (V_{in}). The resultant error is compensated by the PI controller by controlling the ST duty ratio "D" of the power converter, which directly controls the total dc-link voltage (V_{dc}) of the proposed power converter.

As mentioned earlier, the dc-link voltage is indirectly estimated by the capacitor voltages (V_{C1}, V_{C3}) and the ST duty ratio (D). The outer voltage loop regulates the total dc-link voltage (V_{dc}) to its reference value (V_{dc}^*). The control

signal generated by the PI controller is multiplied by a unit-sine, which is synchronized to the grid using a single-phase SOGI-PLL. The synchronized reference current (i_g^*) is then compared with the grid current and the error is compensated by a PR controller. The output of the PR controller is a sinusoidal control signal (v_m), which is further modified to v_m^* as discussed in Section III. This modulation signal v_m^* is compared with the carrier "*C*" to produce the PWM for the switches S_1–S_6 thereby, controlling the active power injected into the grid [27], [28].

V. Reduction of Leakage Current

Leakage current is an issue of paramount interest in transformerless PV systems. The ill effects of leakage current are well researched and documented. It leads to the distortion of grid voltage, electromagnetic interference, and safety issues [32]. The VDE0126-1-1 standard stipulates that the maximum value of current be limited to 300 mA (rms) [17].

Additional ST pulses, which are inserted in qZS inverters to boost the input PV voltage, result in high-frequency voltage transitions across the parasitic capacitor formed between the PV array and the ground. This capacitive coupling induces leakage current when galvanic isolation is absent. Therefore, it is desirable to maintain a constant voltage across the parasitic capacitor to eliminate the leakage current. Nevertheless, in qZS-based MLIs, it is not possible to eliminate the leakage current owing to the insertion of ST in the zero state. Hence, in the proposed power converter, the leakage current is reduced by limiting the magnitude of the high-frequency voltage transition across the parasitic capacitor.

In the proposed power converter, these high-frequency voltage transitions are determined by the effective CMV ($v_{\rm ecm}$), which is defined as

$$v_{\rm ecm} = v_{\rm cmv} + v_{L3} - v_{C4} \tag{12}$$

where $v_{\rm cmv}$ is the common-mode voltage which is expressed as

$$v_{\rm cmv} = \frac{v_{\rm AO} + v_{\rm BO}}{2}. \tag{13}$$

The difference between inductor voltage "v_{L3}" and the capacitor voltage "v_{C4}" during ST and NST states are expressed as

$$v_{L3} - v_{C4} = 0.25V_{\rm dc}, \quad \text{for the ST state} \tag{14}$$

$$v_{L3} - v_{C4} = \frac{-(D)}{(1-2D)}\frac{V_{\rm dc}}{2}, \quad \text{for the NST state.} \tag{15}$$

Table II presents the pole voltages ($v_{\rm AO}$, $v_{\rm BO}$), CMV ($v_{\rm cmv}$), and the effective CMV ($v_{\rm ecm}$) of the power converter in the nonshoot through (NST) and the ST states. As an illustration, the effective CMV is calculated based on the (12) when the ST duty ratio "*D*" is equal to 0.25. It may be noted that the voltages across L_3 and C_4 of the qZS-2 network reduce the effective CMV in the range of 0–0.5 $V_{\rm dc}$ (12).

As mentioned above, the effective CMV ($v_{\rm ecm}$) of the power converter introduces current harmonics of higher order in the leakage current. To minimize these higher-order harmonics, a symmetrical LCL filter is connected across the

TABLE II
Effective CMV of the Power Converter for $D = 0.25$

State-type	Output voltage	v_{AO}	v_{BO}	v_{cmv}	v_{ecm}
NST-1	V_{dc}	V_{dc}	0	0.5 V_{dc}	0.25 V_{dc}
NST-2	0.5V_{dc}	0.5 V_{dc}	0	0.25 V_{dc}	0
NST-3	0	0	0	0	0.25 V_{dc}
NST-4	-0.5V_{dc}	0.5 V_{dc}	V_{dc}	0.75V_{dc}	0.5 V_{dc}
NST-5	-V_{dc}	0	V_{dc}	0.5V_{dc}	0.25 V_{dc}
ST-1	0	0	0	0	0.25 V_{dc}

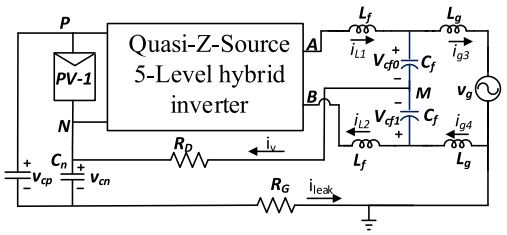

Fig. 7. 5L-qZSI with leakage current path.

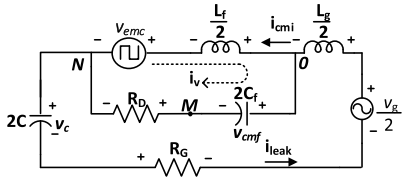

Fig. 8. Equivalent circuit of common-mode model.

output terminal of the inverter "*A*" and "*B*" as shown in Fig. 7. A damping resistor (R_D) is connected between the negative terminal of the PV source "*N*" and the midpoint of the filter capacitors "*M*" to dampen the oscillations in leakage current, which arise due to the ringing of the *LC* components. In Fig. 7, the symbols "R_G," "C_p," and "C_n," respectively, denote the ground resistance, the parasitic capacitances formed between the PV panel and the ground. Both of the parasitic capacitors of the PV panel are assumed to have the same capacitance value ($C_p = C_v = C$) [29].

The common-mode model of the power converter shown in Fig. 7 is assessed to evaluate the effect of the LCL filter on the leakage current.

The common-mode model equations are expressed as

$$\frac{L_f}{2}\hat{i}_{\rm cmi} = \frac{v_g}{2} - \frac{L_g}{2}\hat{i}_{\rm leak} - i_{\rm leak}R_G - v_c - v_{\rm ecm} \tag{16}$$

$$\frac{L_f}{2}\hat{i}_{\rm cmi} = v_{\rm cmf} - v_{\rm ecm} + i_v R_D \tag{17}$$

$$2C\hat{v}_c = i_{\rm leak} \tag{18}$$

$$2C_f\hat{v}_{\rm cmf} = i_{\rm leak} - i_{\rm cmi} \tag{19}$$

where $v_{\rm cmf}$ represents the common-mode filter voltage ($(v_{cf0} - v_{cf1})/2$) and $i_{\rm cmi}$ denotes the common-mode inverter current ($i_{L2} - i_{L1}$).

The equivalent circuit shown in Fig. 8 presents the pictorial representation of the common-mode equations (16)–(19). The simplified equivalent circuit of the common mode model of the filter is shown in Fig. 9. From the simplified equivalent circuit (see Fig. 9) the voltage "v_c" induced across the parasitic

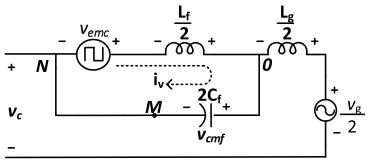

Fig. 9. Simplified equivalent circuit.

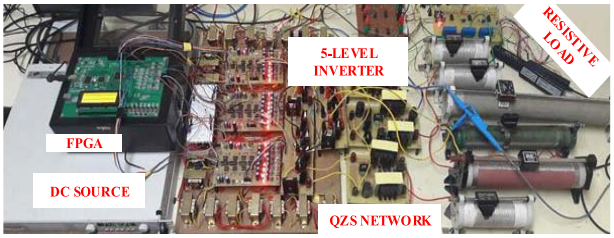

Fig. 10. Experimental prototype of the 5L-qZSI.

capacitor is expressed as follows:

$$v_c = \frac{-v_{\text{emc}}(\omega)}{1-\omega^2 L_f C_f} + \frac{v_g}{2} \tag{20}$$

$$v_c = \frac{-v_{\text{emc}}(\omega)}{1-\frac{\omega^2}{\omega_r^2}} + \frac{v_g}{2} \tag{21}$$

where "ω_r" is the resonance frequency of the filter $((L_f/2), 2C_f)$ and "ω" is the switching frequency of the inverter.

From (21), it may be observed that an extra term of $-1/(1-(\omega^2/\omega_r^2))$ is multiplied by the effective CMV(v_{emc}). Hence, the attenuation gain (dB) of 20 log $\left|1-(\omega^2/\omega_r^2)\right|$ is applied to v_{emc} which increases with lesser resonance frequency "ω_r." Thus, the main contribution of the high-frequency component in the parasitic capacitor "v_{emc}" is attenuated by 20 log $\left|1-(\omega^2/\omega_r^2)\right|$. This leaves only the grid frequency component to be present across the parasitic capacitor which reduces the leakage current to be within the grid standards. As the ac filter $((L_f/2), 2C_f)$ forms a closed path, a current i_v circulates in the closed loop as shown in Fig. 8. From Fig. 9, the current i_v is expressed as follows:

$$i_v = \frac{v_{\text{emc}}(\omega).\omega}{1-\frac{\omega^2}{\omega_r^2}}. \tag{22}$$

As the resonance frequency "ω_r" is far less than switching frequency "ω" the magnitude of the circulating current "i_v" in the *LC* filter is very small. Hence, there is no need for a damping resistor in the *LC* filter.

VI. Experimentation Results

The proposed power converter is experimentally validated with the laboratory prototype shown in Fig. 10. In this system, a programmable dc source is employed to emulate the CC–CV characteristics of the PV source. A SPARTAN-6 FPGA board is used as the digital control platform, which outputs the required gating signals to the power semiconductor switching devices S_1–S_6 (see Fig. 1). Table III presents the specifications of the parameters considered for hardware experimentation.

As shown in Fig. 1, the qZS networks are fed by the emulated PV source with an input voltage (V_{in}) of 105 V.

TABLE III
Experimental Specifications

Operational Parameters	Values	System Parameters	Values
Input voltage (V_{in})	105V	Inductors (EE65CORE)	3mH
Total DC-link voltage	210V	Capacitors (Electrolytic)	300V,1000μF
Output RMS voltage	110V	Ultra-Fast rectifier diode	MUR1560CT
Modulation-Index (m)	0.75	MOFFETs	IRFP460
Output Power (P_o)	400W	Parasitic capacitor (C_p)	100nF
Switching frequency(f_{sw})	20kHz	R_D,L_f, C_f, L_g	1ohm,1mH,6uf, 2.5mH

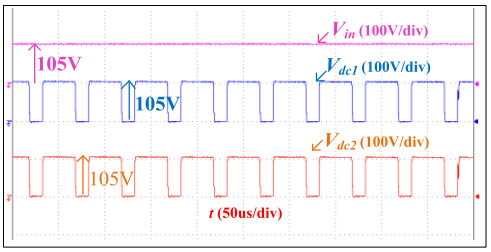

Fig. 11. Experimental results of input voltage (V_{in}) and dc-link voltages V_{dc1} and V_{dc2}.

As this voltage is inadequate to obtain the output voltage of the required magnitude [110 V (rms)], the input voltage is boosted to the required magnitude (which is twice that of the input voltage) by implementing an ST duty ratio of 0.25 (9).

The input voltage (V_{in}) and the dc-link voltages (V_{dc1} and V_{dc2}), i.e., the outputs of the qZS networks of the power converter, are shown in Fig. 11. It may be observed that the voltage of each dc-link is boosted to 105 V resulting in a total dc-link voltage of 210 V (i.e., $V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}}$). As shown in Fig. 11, the dc-link voltages "V_{dc1}, V_{dc2}" are pulsating waveforms, which drop to a value of zero whenever the ST mode is switched using the devices S_1–S_4 [see Fig. 2(f)]. voltage of each dc-link is boosted to 105 V resulting in a total dc-link voltage of 210 V (i.e., $V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}}$). As shown in Fig. 11, the dc-link voltages "V_{dc1}, V_{dc2}" are pulsating waveforms, which drop to a value of zero whenever the ST mode is switched using the devices S_1–S_4 [see Fig. 2(f)]. Fig. 12 presents the experimental waveforms of input voltage (V_{in}), dc-link voltage (V_{dc1}), inductor current (i_{L1}), and the capacitor voltages (V_{c1} and V_{c2}) of the power converter (see Fig. 1). It may be observed that, when the ST-mode (ST-mode) is inserted into the power converter, the dc-link voltage drops to a value of zero. During the ST-mode, the inductor current (i_{L1}) increases linearly and stores energy from the input source. In contrast, during the non-ST-mode (NST-mode), i.e., when the dc-link voltage assumes a value of 105 V as shown in Fig. 12, the inductor current (i_{L1}) decreases linearly while discharging its energy into the load. Theoretically, the capacitors "C_1" and "C_2" of the qZS network-1 should share the dc-link voltage (V_{dc1}) in the ratio of $(1-D)$: D. The traces of the capacitor voltages, presented in Fig. 12, confirm that the dc-link voltage output by the qZS network-1 (105 V) is

distributed in the ratio of 0.75:0.25 across these two capacitors (78 and 26 V, respectively).

The proposed power converter is operated with a modulation index of 0.75 and an ST duty ratio of 0.25 to obtain the required output voltage of 110 V (rms) at the output. The waveforms of the output voltage (V_{AB}) and the load current (i_{load}) are shown in Fig. 13. The experimental result of the output voltage clearly shows 5 distinct voltage levels namely, 0, ±105, and ±210 V. The magnified view clearly reveals that the output voltage pulsates between the values of zero and the current-voltage level output by the converter (see Fig. 13).

Fig. 14 provides the zoomed-in view of: 1) voltage across the parasitic capacitor "V_{cp};" 2) leakage current "i_{leak};" and 3) FFT spectrum of the leakage current. It may be noted that the high-frequency voltage transitions across the parasitic capacitor are effectively bypassed with the use of the LCL filter and the additional path "MN" (see Fig. 7). Consequently, the parasitic capacitor is exposed only to the low-frequency content in the voltage transitions, leading to an effective reduction in the leakage current. It may be noted that the leakage current with the proposed power converter is 10.15 mA (rms), which is well within the limits of 300 mA stipulated by VDE0126-1-1.

Figs. 15 and 16 demonstrate the experimental results pertaining to the regulation of the dc-link voltage for the proposed 5L-qZSI in the standalone mode of operation. The dynamic response of the proposed power converter (with the controller shown in Fig. 5) against the load disturbance is presented in Fig. 15. The top two traces in Fig. 15 present the dc-link voltages (V_{dc1} and V_{dc2}), while the bottom two traces show the output voltage and the load current waveforms. Initially, both the dc-link voltages are boosted to 105 V (peak) by maintaining a ST duty ratio (D) of 0.25, while delivering a load current of 1.76 A. Then, the load current is suddenly increased to 3.53 A and is then decreased back to 1.76 A. With this change in the load current, the disturbance in the dc-link voltage is sensed and the closed-loop dc-link controller automatically adjusts the ST duty ratio to maintain the dc-link voltage at 105 V. It may also be noticed that both dc-link voltages are regulated at 105 V despite the load disturbances (see Fig. 15). The settling time of the dc-link voltage after the load disturbance is less than two fundamental cycles. As the output voltage (V_{AB}) is solely dependent on the dc-link voltages of the power converter in the standalone mode of operation, it is regulated at the set value of the reference [i.e., 110 V (rms)] despite the load disturbances (see Fig. 15).

Fig. 16 shows the dynamic response of the proposed power converter against supply disturbances. In this experiment, the input voltage (V_{in}), which is initially maintained at 100 V is subjected to a quick disturbance of 30 V. It may be observed that the dc-link voltages (bottom two traces) are well regulated at a constant value of 105 V with a quick dynamic response. Thus, it may be concluded that the closed-loop controller (see Fig. 5) effectively regulates the dc-link voltages for both source and load variations.

Fig. 17 presents the behavior of the proposed power converter in the grid-tied mode of operation. With the controller shown in Fig. 6, the active power of 230 W is initially injected

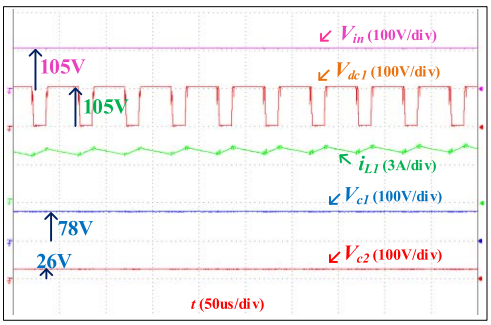

Fig. 12. Experimental results of the input voltage (V_{in1}), dc-link voltage (V_{dc1}), inductor current (i_{L1}), and capacitor voltages (V_{c1}, V_{c2}).

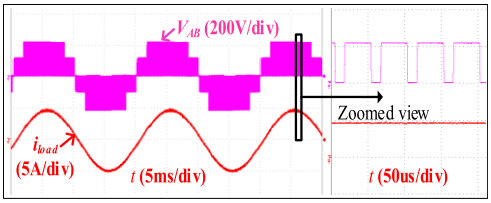

Fig. 13. Experimental waveforms of output voltage (V_{AB}) and load current (i_{load}).

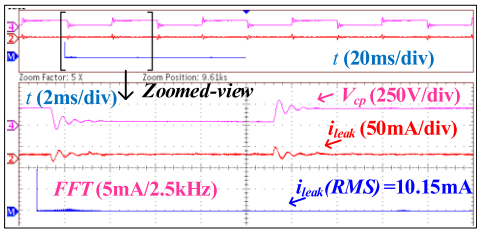

Fig. 14. Experimental results of parasitic capacitor voltage (V_{cp}), leakage current (i_{leak}) of the PV source, and harmonic spectrum of leakage current.

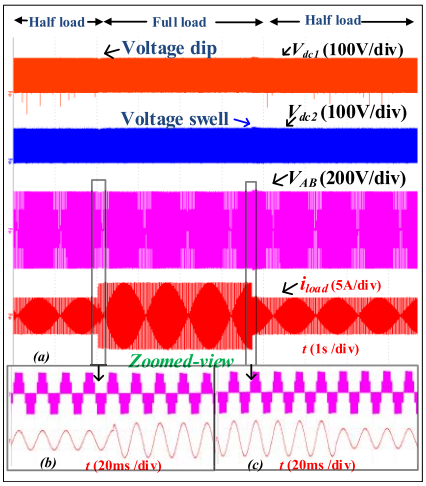

Fig. 15. Experimental results of (a) dc-link voltages (V_{dc1} and V_{dc2}), (b) output voltage (V_{AB}), and (c) load current (i_{load}).

into the grid. As mentioned earlier, the value of irradiation determines the value of the ST duty ratio "D." To emulate the behavior of the PV source, which increases the output power with an increase in the value of irradiation, a step change is introduced in the value of the ST duty ratio "D" (0.18–0.21). The corresponding increase in the input power can be noted

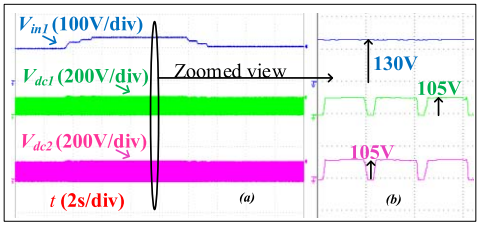

Fig. 16. Experimental results of (a) input voltages (V_{in1}) and dc-link voltages (V_{dc1} and V_{dc2}). (b) Zoomed-in view of the plot (a).

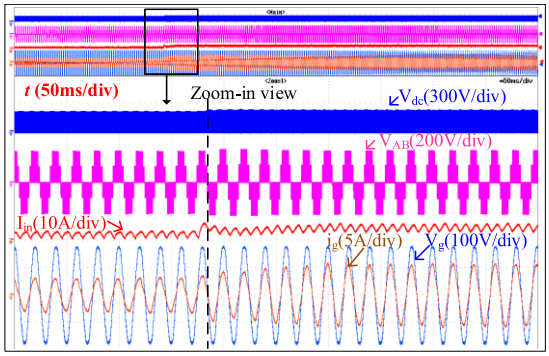

Fig. 17. Experimental results of the total dc link voltage, output voltage of the inverter (V_{AB}), grid voltage (V_g) and current (i_g).

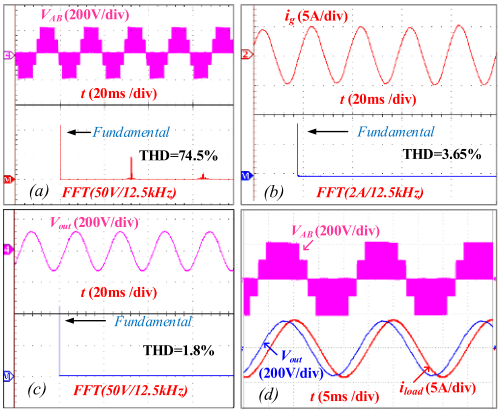

Fig. 18. (a) FFT of inverter output voltage "V_{AB}." (b) FFT of grid current "i_g." (c) FFT of output voltage "V_{out}." (d) Output voltage (V_{AB}), load voltage (V_{out}), and load current (i_{load}) for 0.8 lagging power factor.

from the change in the input current (I_{in}) from 2.4 to 3.8 A rms (third trace). This momentarily increases the dc-link voltage (second trace). However, the error between the reference and the actual (feedback) values of the dc-link voltage is compensated by the PI controller (see Fig. 6), which increases the reference value of the grid current. The PR controller, which is present in the inner current loop compensates for the current error by readjusting the modulation index "m" to increase the current injected into the grid. This automatically restores the value of the dc-link voltage (V_{dc}) and the output voltage (V_{AB}) of the inverter. Fig. 17 clearly shows the increase in the value of the grid current from 2.11 to 3.56 A (rms) at UPF.

Fig. 18(a) and (b) shows the harmonic spectrum of the inverter voltage "V_{AB}," and grid current "i_g" wherein the rms value of the fundamental component is 110 V (rms) and 3.6 A. The voltage THD and current THD obtained are 74.5% and 3.65%. The measured voltage THD of the power converter is on the higher side due to the insertion of a zero-state in each voltage level of operation to boost the input voltage. However, the inverter voltage "V_{AB}" is filtered by the LCL filter to provide sinusoidal output voltage "V_{out}" of THD 1.8% to load/grid [as shown in Fig. 18(c)].

To validate the reactive power capability, the power converter is tested for a 0.8 lagging ($R = 26\ \Omega$, $L = 61$ mH) power factor. Fig. 18(d) demonstrates the experimental waveforms of inverter output voltage "V_{AB}," load voltage "V_{out}," and load current "i_{load}." It may be observed that load current is lagging w.r.t to load voltage (V_{out}) which shows the reactive power capability of the power converter.

VII. Comparison With the Proposed 5L-qZSI

This section critically compares the proposed power converter vis-à-vis the previously available topologies in literature, which are based on the 5-level-qZS inverter. This comparison is based on the number of semiconductor switching devices and passive components and summarizes the voltage stress across devices for all of the five topologies From Table IV, it may be observed that the proposed topology (5L-qZSI) has a lower number of semiconductor switches, compared to other 5-level qZS inverters.

It may also be noted that, while the proposed power converter uses fewer power diodes when compared to the topologies [7], [15], [16]. The proposed topology 5L-qZSI is on par with the other qZS converters, in terms of the number of capacitors. While it appears that the MqZS-5LI [15] has an advantage w.r.t the proposed power converter in terms of inductors, it results in a discontinuous input current which is not favorable for PV applications. The rms value of the output voltage is the base value for the calculation of the per-unit voltage stress across the switching devices as well as the passive components. It may be observed that all the five topologies have equal voltage stress across the capacitor and diodes. Even though the voltage stresses on the diodes and active switches are comparable in all of the five topologies, the requirement of a higher number of diodes/switches in the compared topologies leads to lower reliability [7], [12], [15], [16]. As the number of switches and diodes are unequal across the compared topologies, the total standing voltage (TSV) (i.e., the sum of voltage stress of all the diodes and switches w.r.t the peak voltage value) of the power converters is calculated [30]. It may be noted that the proposed power converter (5L-qZSI) registers a lower TSV when compared to qZS-NPC [7], MqZS-5LI [15], and qZS-5L [16] topologies.

From Table IV, it may be observed that the proposed topology results in a lower leakage current of 210 mA (which is under the stipulated limit of 300 mA) when compared to topologies [7], [12], [15], and [16] even without the filter. This is because, the proposed modulation technique applies a zero-state in each level of operation.

Furthermore, with the employment of the "LCL" filter and with the additional path "MN," the leakage current of the proposed topology drops to 12 mA. It may be noted that the points "M" and "N" cannot be connected in a cascaded

TABLE IV
COMPARISON OF THE PROPOSED POWER CONVERTER WITH 5-LEVEL QZS TOPOLOGIES

		qZS-NPC[7]	qCHB-FLBI[12]	Mqzs- 5LI[15]	qZS-5L[16]	Proposed
Levels		5	5	5	5	5
Sources		1	2	1	1	1
Capacitors		4	2	4	4	4
Inductors		4	2	2	4	4
Active Switches		8	8	8	8	6
Diodes		6	4	3	4	2
Input current		continuous	continuous	discontinuous	continuous	continuous
Capacitor voltage stress		$1/\sqrt{2}$ C_1,C_2	$1/\sqrt{2}(1-D)$ C_1,	$1/\sqrt{2}$ C_1,C_2	$1/\sqrt{2}$ C_1,C_3	$1/\sqrt{2}$ C_1,C_3
		$D/\sqrt{2}(1-D)$ C_3,C_4	$1/\sqrt{2}(1-D)$ C_2	$D/\sqrt{2}(1-D)$ C_3,C_4	$D/\sqrt{2}(1-D)$ C_2,C_4	$D/\sqrt{2}(1-D)$ C_2,C_4
Diode voltage stress		$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$
Switch voltage stress		$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$ for S_1-S_4	$1/\sqrt{2}(1-D)$	$1/\sqrt{2}(1-D)$for S_1-S_3
				$\sqrt{2}/(1-D)$for S_5-S_8		$1/\sqrt{2}(1-D)$ for S_4-S_6
TSV		7	5	7.5	6	5.5
Voltage THD		76.4%	42.73%	38.2%	74.2%	74.5%
Leakage current	Without filter	720mA	1.1A	590mA	325mA	210mA
	With filter	520mA	Not applicable	70mA	22mA	12mA

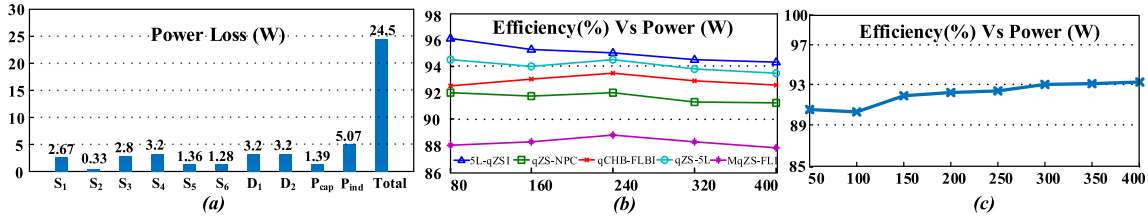

Fig. 19. (a) Power loss distribution in 5L-qZSI. (b) Efficiency comparison with the 5L-qZSI. (c) Experimental efficiency of the 5L-qZSI.

H-bridge topology with an LCL filter and isolated PV sources due to the lack of a common point (see Fig. 1) [12]. The proposed power converter has higher voltage THD when compared to [12] and [15] as zero level is inserted in each level of operation to boost the input voltage. However, the inverter output voltage is filtered by the LCL filter to provide a sinusoidal output voltage to the load/grid.

VIII. POWER LOSS FOR THE 5L-QZSI

The power loss of the proposed 5L-qZSI is assessed by evaluating it using the Powersim (PSIM) software, at 400 W. Thermal models of the MOSFET-IRFP460 and the power diode-ISL9R3060G2 are employed to evaluate power loss incurred in semiconductor switches (S_1–S_6), power diodes (D_1–D_2). Furthermore, conduction losses in the inductor (P_{ind}) and the ESR losses (P_{cap}) in the capacitors are estimated using the method described in [31]. These losses are evaluated with: 1) input voltage (V_{in}) of 105 V; 2) output voltage of 110 V (rms); 3) switching frequency (f_s) of 20 kHz; 4) ST duty ratio (D) of 0.25; and 5) the modulation index (m) of 0.75. Fig. 19(a) displays the power loss incurred in switching devices and passive components at 400 W.

Fig. 19(b) presents the efficiency curves of the topologies compared in Table IV. The efficiencies of the power converters are assessed by evaluating the power loss incurred in it using the Powersim (PSIM) software, in the output range of 0–400 W. Thermal models of the MOSFET-IRFP460 and the power diodeISL9R3060G2 are employed to evaluate the losses. It may be observed that the proposed power converter (5L-qZSI) registers a higher efficiency when compared to all of the compared topologies due to lower semiconductor switch and diode count. It may be noted that the average efficiency of the proposed power converter is about 95%.

The experimental efficiency of the power converter is validated by using a precision digital power meter (Yokogawa WT332E) to measure the input power and output power is measured by power analyzer (UNI-T UT283A). The experimentation is implemented for a step change of 50 W ranging from 50 to 400 W. The hardware efficiency curve of the 5L-qZSI is shown in Fig. 19(c). From Fig. 19(c), it may be noted that the experimental efficiency of the prototype achieves 93% at 400 W output. It may be observed that the hardware efficiency is in close approximation to the simulated efficiency [shown in Fig. 19(b)], which is about 95%. In addition to this, the CEC efficiency of the proposed power converter is also estimated using the method shown in [33]. The CEC efficiency is found to be 92%.

IX. CONCLUSION

This article proposes a single-stage, 5-level qZS-based hybrid inverter (5L-qZSI) for standalone, as well as grid-tied PV applications. The voltage boosting as well as 5-level inversion are simultaneously achieved with the proposed single-stage converter and the associated modulation technique. When compared to the existing qZS 5-level inverter topologies, the proposed power converter employs fewer switching devices to synthesize the 5-level output voltage waveform. It is shown that the use of an LCL filter reduces the leakage current. It is

also demonstrated that, due to the combined efforts of the filter and the PWM strategy, the leakage current is suppressed to 10 mA which is well within the stipulated limit of 300 mA by the VDE 0126-1-1 standard. The steady-state and dynamic performances of the power converter in the standalone mode and the grid-tied mode are experimentally demonstrated. It is shown that in the standalone mode of operation, the output voltage of the power converter is solely regulated with the control of the ST duty ratio against the source and load disturbances. Furthermore, the dynamic performance of the current controller in the grid-tied mode of operation is demonstrated experimentally. It is shown that the current control strategy achieves the injection of active power into the grid at UPF. The power loss analysis of the proposed power converter, evaluated using the PSIM software, reveals that the efficiency of the proposed power converter is around 95%.

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