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Single-Phase Five-level H5 and HERIC Transformerless Inverters for PV Applications

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***Abstract* — This work proposes an improved single-phase five-level H5 and Heric transformerless inverter topologies for grid-tied photovoltaic systems. The suggested topologies overcome issues associated with standard transformerless inverter topologies such as three-level operation, the influence of switch junction capacitances, and the lack of a bi-directional current path. Additional bi-directional clamping branches and modified modulation technique enables the inverter to operate under different power factor conditions of the grid without increasing the total harmonic distortion (THD) and common mode currents (CMC). Moreover, the proposed topologies generate five-levels in the output which will further reduce the THD and size of the passive components. Performance evolution between the traditional and proposed topologies was carried-out using 1 kW test setup implemented in PSIM simulation software using thermal module tool set.**

Keywords* — *Single – phase, transformerless inverter, grid-tied operation, Common mode currents, common mode voltage, switch junction capacitance, non-unity power factor, PWM scheme.

I. INTRODUCTION

Transformerless inverters are widely popular in grid-tied photovoltaic (PV) systems due to its high efficiency, improved power density, lower size, and cost [1]. However, due to the formation of direct connection between the grid and PV module there exist common mode currents (CMCs) in the case of transformerless operation as depicted in Fig. 1. The issues like low power quality, risk of operational safety and low life time of the PV panels arises due to the continuous flow of these CMCs. Voltage fluctuations across the common mode circuit due to inverter switching and the PV parasitic capacitance (C_{PV}) are the key factors for the generation of CMCs. Unfortunately, the value of PV parasitic capacitance is intermittent in nature due to changes in environmental and grounding conditions. Thus, the ultimate solution for eliminating the leakage current is of reducing and/or suppress the voltage fluctuations in common mode circuit [2].

In the common ground topologies like neutral point clamped (NPC), ANPC and HNPC topologies; PV parasitic capacitance is bypassed by connecting grid neutral to the negative terminal of the PV source and hence the issue of CMC is completely eliminated.

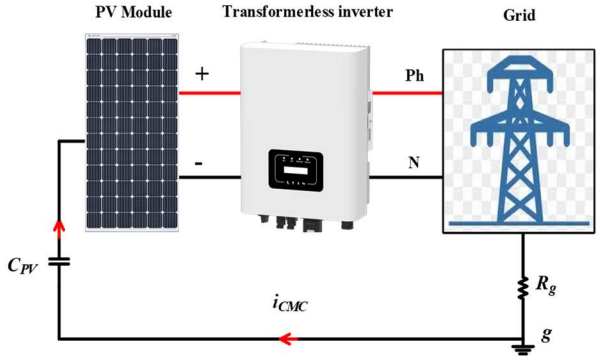

Fig. 1. Common mode current path in transformerless inverter operation.

However, these topologies require twice the input voltage and higher rating of power devices to obtain the grid peak voltage [3].

To overcome the afore-said drawbacks, H4 inverter is proposed with bi-polar PWM and uni-polar PWM schemes. In terms of CMC the bi-polar PWM is superior but it requires double the rated switches. Conversely, the uni-polar PWM requires low rated switches and superior in terms of THD, filter size. Main reason behind the CMCs with uni-polar PWM scheme is the non-availability of isolation between the grid and PV source during the freewheeling period. Thus, it is inevitable to replace or modify the inverter topology to achieve all-round features that are required for an efficient and reliable transformerless operation [4].

In this context, several topologies were proposed in the literature based on the elimination of voltage fluctuations in common mode circuit. Among those H5, Heric and H6 – Type topologies are quite popular and patented as highly efficient in its family as depicted in Fig. 2 (a), (b) and (c) respectively [5] – [6]. In all the above topologies, H4 inverter is upgraded with active elements to achieve decoupling (either AC side or DC side) between the PV source and grid during the freewheeling period. Thus, the high frequency oscillations across C_{PV} are eliminated. For example, in H5 configuration an additional switch S_5 is added in series with the H4 inverter to provide DC decoupling. Likewise, in Heric inverter two additional switches are connected in parallel with the grid to obtain AC side decoupling. Similarly, for H6 inverter both DC side and AC side decoupling circuits were proposed respectively.

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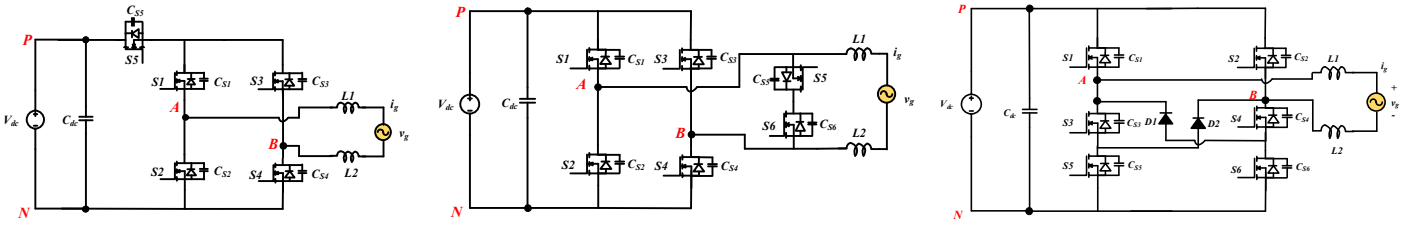
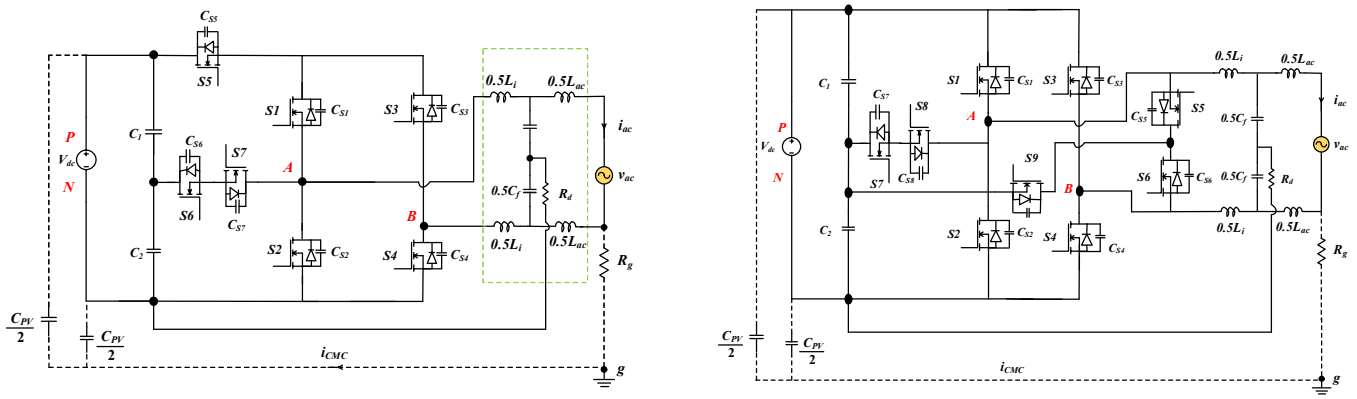


(a) (b) (c)

Fig. 2. Classical transformerless inverter topologies: (a) H5, (b) Heric, and (c) H6



(a) (b)

Fig. 3. Five-level transformerless inverter topologies: (a) I-H5, and (b) I-Heric.

Unfortunately, the effect of switch junction capacitances is not considered in all the upgraded H4 topologies. Generally, the value of switch junction capacitances (C_{SW_j}) varies from few picofarads to several nanofarads. While transmitting from active states to freewheeling state, the stored energy in C_{SW_j} creates voltage oscillations across $C_{PV,}$ and leads to generate CMCs. To reduce the effect of switch junction capacitances: an additional clamping branch is derived for the H4 based topologies. This additional clamping branch is activated during the freewheeling period to suppress the oscillations due to switch junction capacitances [7] – [8]. Thanks to additional clamping branch for maintaining constant voltage across C_{PV}. Thus, the CMC's are suppressed at great extent below the grid standards (VDE01260-1-1) and not causing any serious issues to the system.

Contemporarily, as per the revised grid standards (VDE-AR-N4105) the transformerless inverter should support the fault ride through (FRT) capability up to certain amount of time without compromising on THD. However, several of the resultant H4 topologies have been examined for grid unity power factor operation. Furthermore, the PWM method and setup are missing a bi-directional current path. As a result, the power quality of the output waveforms was considerably influenced by non-unity power factor grid situations or the FRT state. In addition to that, output levels of all the topologies are limited to three-level which will increase the THD, filter size, and cost of passive components. Recently, five-level output is widely accepted by the industry even in single-phase low/medium voltage applications to enhance the performance of the inverter for the same range of frequency [9] – [10]. Therefore, the quality of output waveforms are ensured at reduced filter size and cost. To meet all the above stated merits, in this paper an improved single-phase five-level H5 and Heric transformerless inverter topologies were proposed. Moreover, the common drawbacks of conventional H5 and Heric topologies such as: three-level operation, effect of CMC's and bi-directional current paths is well addressed in the proposed topologies. Additional clamping branch and bi-directional switches enables the inverter to produce lower CMC's and five-level output respectively. In addition to that, modified sinusoidal PWM is employed to get lower common mode voltage oscillations. Further, the simulation results of both traditional and improved H5 and Heric topologies were presented and compared by using MATLAB simulink toolbox.

II. Improved H5 and Heric Topologies

In this section, improved five-level H5 and Heric topologies are presented with bi-directional current capabilities. Various modes of operation for generating five-level output are explained for both improved H5 and Heric topologies. In both the topologies, PV source is emulated as an equivalent DC source to realize the operation of an inverter. Moreover, the bi-directional current path in each stage is drawn individually to show the non-unity power factor operation of the grid.

A. Opearting Stages

Fig. 3(a) and (b) illustrates the improved H5 (I-H5) and improved Heric (I-Heric) topologies respectively. In both the topologies: bi-directional switch (BDS) enables five-level operation without effecting the balancing of DC-link

capacitors in all the modes of operation. And the clamping branch de-couples the inverter from grid during freewheeling period. Moreover, the control pulse applied to BDS is same and hence the driver requirement is reduced. In all the stages of operation red arrows indicate the current path from source to grid and the blue arrow indicates current path from grid to source. Operation of the improved inverter topologies are explained in five-stages as follows:

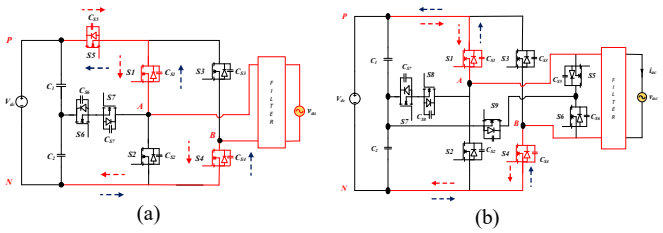
I. Stage A: In this stage, $V_{AB} = V_{PN}$, switches *S1, S4 and S5* in I-H5 and switches *S1 and S4* in I-Heric are triggered on and the remaining switches are triggered off as shown in Fig. 4(a) and (b) respectively. The current path from DC source to grid and vice-versa is also shown in Fig. 4(a) and (b) with black and red arrows respectively.

II. Stage B: The simplified circuit for both I-H5 and I-Heric topologies related to this stage is illustrated in Fig. 5(a) and (b) respectively. Where, $V_{AB} = 0.5V_{PN}$ and switches *S4, S6 and S7* in I-H5 and switches *S4, S7 and S8* in I-Heric are triggered on and the remaining switches are triggered off. Switches in BDS branch are triggered on/off simultaneously for providing current path from PV source to grid and vice-versa.

III. Stage C: In this stage, $V_{AB} = 0$, switches *S1, S3, S6 and S7* in I-H5 and switches *S5, S6 and S9* in I-Heric are triggered on as shown in Fig. 6(a) and (b) respectively and the remaining switches are triggered off. During this mode the inverter isolated from the PV source grid by means of conventional method which is present in the H5 and Heric topologies. Along with that clamping is also achieved by triggering BDS alone in I-H5 and clamping branch in I-Heric topologies. Thus, the amplitude of high-frequency oscillations is reduced even under the five-level generation. Furthermore, active clamping minimized the influence of switch junction capacitances. Furthermore, the level shifted PWM set permits the current flow from PV source to grid and vice versa. Therefore, the power quality of output waveforms is guaranteed under different modes of grid conditions. (Either positive power mode or negative power mode based on the demand).

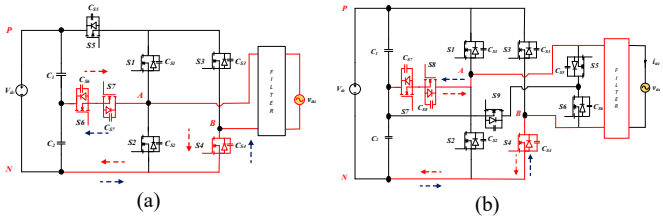
IV. Stage D: The simplified circuit for both I-H5 and I-Heric topologies related to this stage is illustrated in Fig. 7(a) and (b) respectively. Where, $V_{AB} = -0.5V_{PN}$ and switches *S3, S5, S6 and S7* in I-H5 and switches *S3, S7 and S8* in I-Heric are triggered on and the remaining switches are triggered off. Switches in BDS branch are triggered on/off simultaneously for providing current path from PV source to grid and vice-versa.

V. Stage E: In this stage, $V_{AB} = -V_{PN}$, switches *S2, S3 and S5* in I-H5 and switches *S2 and S3* in I-Heric are triggered on and the remaining switches are triggered off as shown in Fig. 8(a) and (b) respectively. It is noted that the bi-directional current path is presented in all the operating stages of the proposed five-level H5 and Heric topologies. Hence, the quality of output waveforms is not affected even under the non-unity operation of the grid when comparing with the traditional topologies.



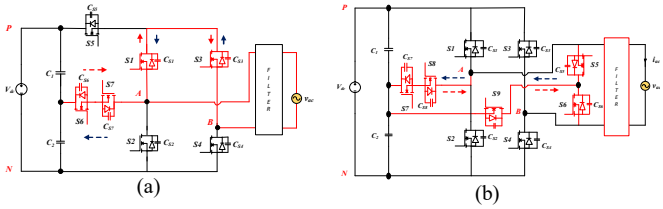
(a) (b)

Fig. 4.Stage A: (a) I-H5, and (b) I-Heric.



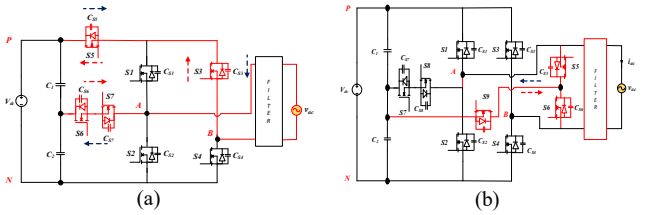
(a) (b)

Fig. 5.Stage B: (a) I-H5, and (b) I-Heric.



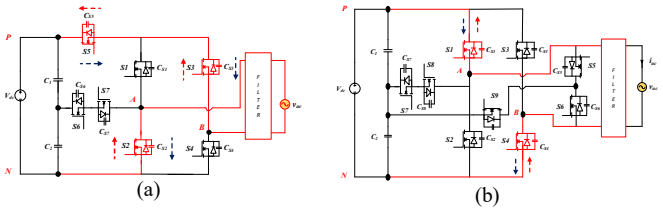
(a) (b)

Fig. 6.Stage C: (a) I-H5, and (b) I-Heric.



(a) (b)

Fig. 7.Stage D: (a) I-H5, and (b) I-Heric.



(a) (b)

Fig. 8.Stage E: (a) I-H5, and (b) I-Heric.

Gate pulse generation for the traditional H5 topology is illustrated in Fig. 9 by using unipolar PWM scheme. Fig.10 illustrates the gate pulses for the I-H5 topology by using unipolar PWM scheme. Switches S6 and S7 are additional in the improved topology to realize the five-level voltage along with decoupling and clamping during freewheeling period. Moreover, the switches S1 and S2 are turned on during freewheeling period for both positive and negative current directions to enhance the quality of output waveform other than unity power factor operation. Thus, the modified PWM scheme enhances the quality of output waveforms irrespective of the power factor and capable of generating five-level output voltage. Moreover, it is similar for the I-Heric topology for generating the gate pulses.

III. CMC REDUCTION

The main reason for CMC is the formation of resonant circuit between PV source and grid due to parasitic elements. Resonant circuit includes the PV parasitic capacitance, switch junction capacitances, capacitance due to heat sink and wires. Voltage oscillations across the resonant circuit are generated due to switching operation of an inverter from one level to other. Sometimes, the CMC may exceed the safety standards and causes several reliability issues. Further, it may lead to poor quality of output waveforms and operational insecurity. The ultimate solution to reduce the CMC is to suppress voltage oscillations across the resonant circuit.

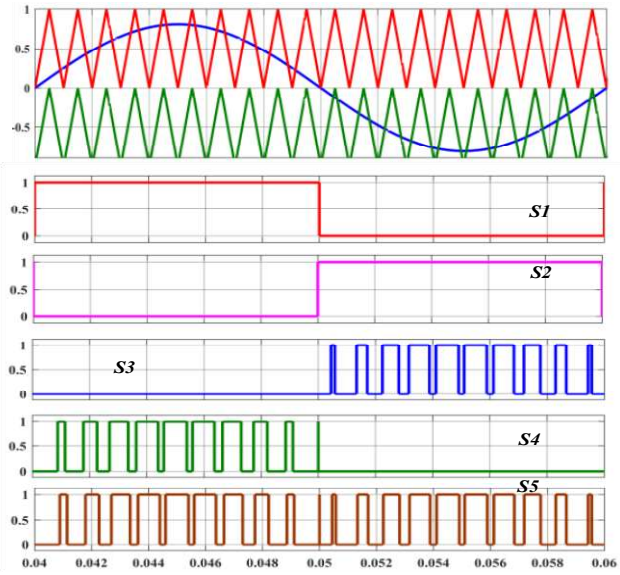


Fig. 9. UPWM and gate pulses traditional H5 topology

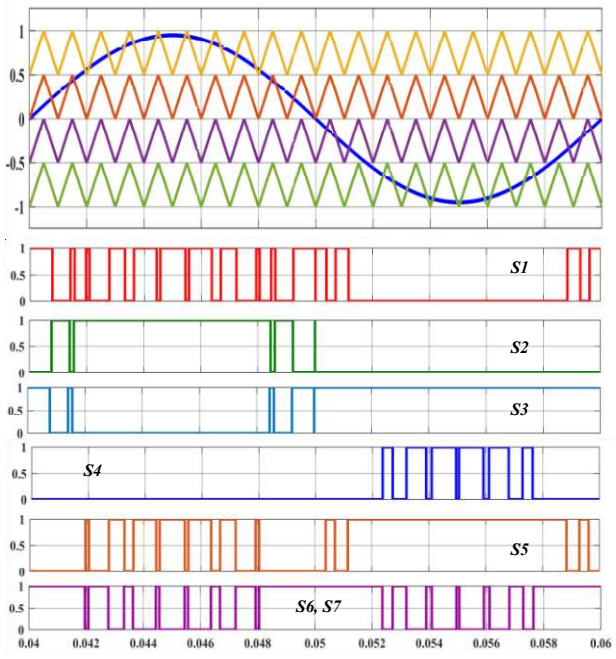


Fig. 10. UPWM and gate pulses I-H5 topology

Both the design and the PWM scheme in this study simplify the decrease of voltage oscillations and their elimination by the issue of CMC as follows; the extra bi-directional branch clamps the inverter to half of the DC link voltage during the freewheeling period. Simultaneously, the employed SPWM scheme decouples grid and PV source by switching the inverter as explained Stage C. Thus, the total voltage oscillations across common mode circuit are restricted to $0.25V_{dc}$ to $0.75V_{dc}$ as shown in Fig. 11 and it is the average of both the terminal voltages as expressed in Eq. (1).

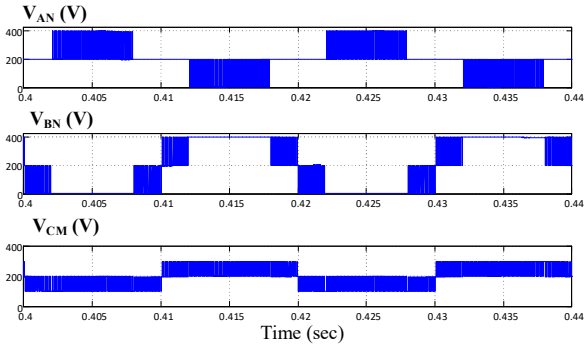


Fig. 11. Common-mode characteristics V_{AN}, V_{BN} and V_{CM}.

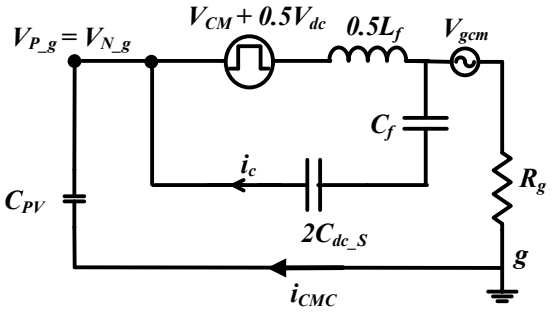


Fig. 12. Simplified equivalent circuit.

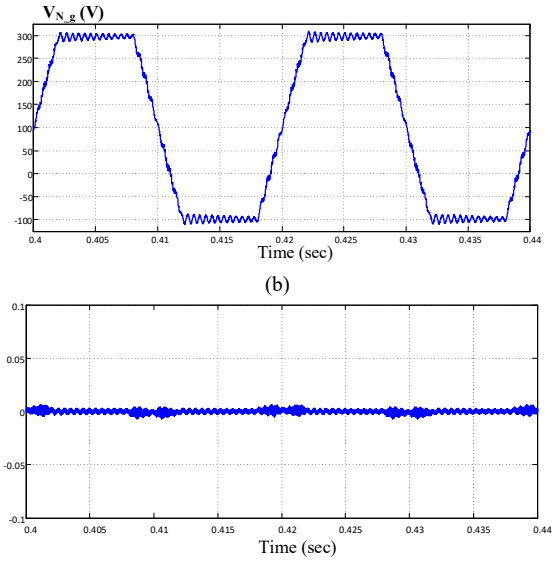


Fig. 13. (a) Voltage across parasitic capacitance $V_{N\text{-}g}$, (b) CMC

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

Further to maintain oscillation free CMV, an LCL filter connection is rearranged and connected to negative of the PV source as illustrated in Fig. 12. Because of this connection a low pass filter is formed and it attenuates the high frequency low amplitude oscillations and produces low frequency signal across the resonant circuit. Hence, the issue of leakage current is eliminated in the proposed topologies irrespective of parasitic elements as shown in Fig. 13.

IV. Simulation Results

A 1 kW test setup has been built in Matlab/simulink software for the validation of proposed topologies. Table I, illustrates the system parameters used in the simulation and it is same for both topologies [11]. Moreover, performance characteristics of both the topologies are similar and hence H5 topology alone shown in different operating conditions of the grid. A proportional – resonant (PR) based closed loop controller is used to regulate the inverter output voltage and injected grid current irrespective of the irradiance or temperature conditions of PV source [12]. A typical boost converter is used to measure maximum power while also increasing the low PV voltage. The simulation results of the proposed five-level H5 inverter are presented below in two separate cases:

Table I. System Parameters

S. No	*Parameters*	*Specification*
1	DC voltage	400 V
2	Inductor L_i, L_{ac}	4 mH, 2 mH
3	Capacitors *C1, C2,* C_f	1 mF, 1 mF, 4 µF
4	AC output voltage	230V, 50 Hz
5	Switching frequency f_s	10 kHz
6	Output power	1000 W
7	C_P and R_g	20 nF, 10Ω
8	Modulation index (M_a)	0.94

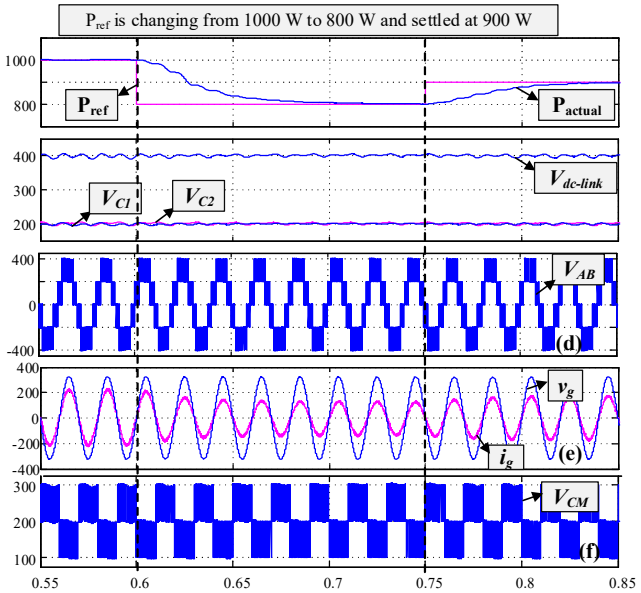


Fig. 14. Simulation results of the five-level H5 inverter topology at different real power conditions.

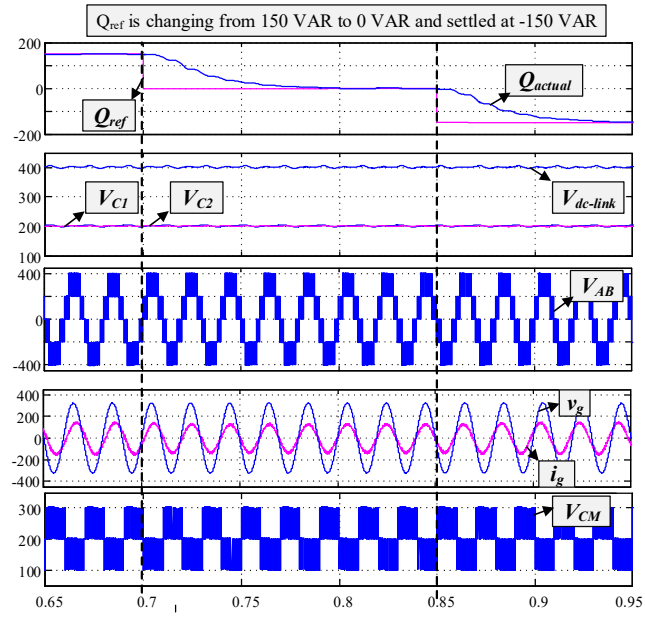
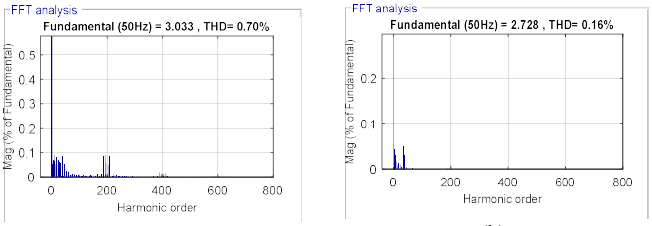


Fig. 15. Simulation results of the five-level H5 inverter topology at different reactive power conditions.



(a) (b)

Fig. 16. FFT spectrum under (a) unity power factor, and (b) 0.42 Lagging.

Case I illustrates under different active powers such as 1000 W to 800 W and settled at 900 W (as shown in Fig. 14).Conversely, case II illustrates under different reactive powers such as 200 kVAR to 0 kVAR and settled at -200 kVAR (as shown in Fig. 15). Each result consists of power waveform, capacitor voltages, five-level voltage, grid voltage and current, and CMV. Further, total harmonic distortion under unity power factor and lagging power factor conditions as illustrated in Fig. 16 respectively. From the simulation studies, it is evident that the proposed topology preserves the quality of output waveform well below the IEEE 1547 international standard at different operating conditions of the power factor (i.e., THD less than 5%). Moreover, the additional leakage current due to parasitic elements is reduced to 8 mA (RMS) which is well below the safety standards imposed by DINVDE0126-1-1.

V. Comparitive Analysis

In this section, comparison between traditional H5 and Heric and the proposed five-level H5 and Heric topologies are illustrated in terms of no.of levels, switch count, blocking voltage, THD, CMCs and efficiency for the same power level. All the performance parameters are obtained from the PSIM thermal module box with IRFP460N real-time switch characteristics.

TABLE II. COMPARITIVE ANALYSIS

Parameter	H5	Heric	5L-H5	5L-Heric
No.of levels	3 level	3 level	5 level	5 level
Switch count	five	six	seven	Nine
Blocking voltage	$4.5*V_{dc}$	$6*V_{dc}$	$5.5*V_{dc}$	$8*V_{dc}$
THD @ U.P.F	1.43 %	1.45 %	0.70 %	0.71 %
CMC (RMS) in mA	18.4	17.92	8.2	7.9
BDC path	No	No	Yes	Yes
Size of the filter	Large	Large	Low	Low
Efficiency	96.7 %	97.8%	96.1 %	97.1 %

*BDC – Bi-directional current path

From Table II, it is observed that the proposed topologies are producing better results than traditional topologies in terms of both common mode and differential mode characteristics. Also, they are capable to operate under different operating conditions of the grid without losing the quality of output waveforms and it is very much essential to operate under fault-ride through conditions of the grid (FRT). Moreover, five-level operation at the output reduces size of the filter under same operating frequency. However, all the above benefits are attained at the cost of little drop in efficiency.

VI. CONCLUSION

In this paper, five-level H5 and Heric inverter topologies are proposed to abolish the drawbacks of traditional topologies. Operating modes in different stages of level generation were explained in detail without losing the quality of output waveforms. Also, the effect of parasitic elements on leakage current is well addressed by deriving low pass filter across resonant circuit. Moreover, the performance of the proposed five-level H5 topology is validated through Matlab simulink under various conditions of the grid. A brief summary of the conventional and new topologies is provided as well to demonstrate the benefits. The experimental findings with fault-ride through capabilities are being worked on and will be included in the expanded edition of the publication.

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