An Asymmetrical Dual Quasi-Z-Source Based 7-Level Inverter for PV Applications

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***Abstract*—This paper presents a new single-stage quasi-z-source (qZS) based power converter for Photovoltaic (PV) applications. This seamless topology is obtained by the fusion of two quasi-z-source networks with a 7-level cascaded multilevel inverter (MLI). The proposed converter requires fewer passive components and power switching devices compared to the seven-level topologies with impedance and quasi-impedance sources, reported in the literature. The proposed modulation technique achieves the required level of voltage boosting using the qZS networks while synthesizing seven levels in the output voltage waveform. While the proposed power converter can regulate the output voltage in the standalone mode, it can inject active power into the grid at Unity power factor (UPF) in the grid-connected mode of operation. This paper also aims to mitigate the leakage current, which is one of the major issues in transformerless PV inverters, by reducing the magnitude of voltage transitions in the parasitic capacitor and the suppression of higher-order harmonics in the ground leakage current. The steady-state and the dynamic performances of the proposed power converter during grid-connected mode of operation is assessed with simulation studies and are validated with experimental results.**

***Index Terms*—Qquasi-Z-source (qZS) network, leakage current, voltage boosting, 7-level cascaded MLI.**

I. Introduction

PHOTOVOLTAIC generation of electrical energy has steadily grown in the last couple of decades owing to its cleanliness and reliability. Lower maintenance, durability, and falling costs are likely to cause an increased generation of solar energy in the foreseeable future. However, the solar PV systems output DC voltage which requires a power converter to convert it to AC form, either to be utilized in standalone systems or inject power into the grid [1]. In solar PV systems, the low output voltage of PV panels is boosted to a higher voltage using a separate DC-DC boost converter. The boosted DC-link voltage is then fed to an inverter to generate the AC voltage of the required magnitude and frequency. This two-stage conversion achieves its objectives at the expense of efficiency at an increased cost [2], [3]. To overcome these disadvantages, a single-stage Z-source inverter (ZSI) topology is proposed. This monolithic structure, while boosting the PV voltage, can produce an AC output voltage of the required voltage and magnitude. Additionally, this system offers an inherent shoot-through (ST) protection of power semiconductor switching devices [4], [5]. The Z-source is a symmetrically configured LC network consisting of a DC source and a series diode, which displays an inherent ability to boost the input voltage. However, switching of the series power diode in Z-source results in a discontinuous input current, which is not favorable for PV applications. This disadvantage is overcome with a variant of the Z-source, which is known as the quasi-z-source (qZS) [6]. While resulting in a continuous input current, the qZS reduces the voltage rating of one of the capacitors significantly.

In recent years, multilevel inverters (MLI) [7], [8] are extensively used in high power applications over the conventional 2-level inverters due to the following advantages: (i) reduced harmonic contamination in the output (ii) reduced voltage stress on semiconductor devices (iii) smaller filter sizes and (iv) lower EMI. Despite these advantages, conventional multilevel inverters (being buck type DC-AC power converters) produce an output voltage with a peak value that is less than the input DC voltage. This limitation is successfully overcome by integrating a ZS / qZS with an MLI, making it a buck-boost inverter [9], [10].

Initially, Z-sources are integrated with MLIs of Neutral point clamped (NPC) and Cascaded-H-bridge (CHB) types. A three-level NPC is integrated with two isolated ZS networks to boost the input voltage to produce a 5-level phase voltage waveform [11], [12]. In the work reported in [13], a three-level NPC topology is integrated with a single Z-source and two DC sources. Despite this attempt to optimize the topology, the cost of the system could not be brought down as a consequence of the increased rating of passive elements. Furthermore, both of these topologies demand additional clamping diodes, which increases the cost and lowers the reliability. Further, a seven-level inverter topology is reported in [14], wherein a cascaded Z-source network with two switches is connected to an H-bridge inverter. This power converter requires fewer semiconductor switches compared to the other ZS-NPC topologies. However, this topology needs three isolated Z-source networks, which increase the number of passive components. The drawback of discontinuous input current associated with the Z-source-MLIs is overcome by fusing the NPC and CHB topologies with a quasi-z-source.

The research work presented in [15] describes an integrated system, wherein two symmetrical qZS networks are integrated with a 3-level NPC converter. Apart from the requirement of clamping diodes, this topology suffers from the drawback of neutral point deviations, which are typically found in all NPC-

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based power circuits. In qZS-based CHB topologies [16], [17], [18], each H-bridge inverter requires an exclusive qZS. This increases the number of passive elements as well as switching devices. In addition, all the isolated PV sources require independent Maximum power point tracking (MPPT) and DC-link voltage control, thereby increasing the complexity of control [19]. In [20], a five-level quasi switched boost MLI (qSB-MLI) is proposed, which avoids two inductors and two capacitors compared to qZS-CHB. However, the qSB-MLI requires two additional switches and diodes to boost the input DC voltage. In all of these topologies [15], [16], [17], [18], [19], [20], the number of passive components and switching devices increases with an increase in the number of voltage levels. A modified qZS-based hybrid 3-level inverter is proposed in [21], which needs fewer inductors and semiconductor devices with a single DC source. However, in [21], the device current and voltage stress are increased when compared to qZS-CHB and qSB-MLI topologies. In addition to this the power converter results in a discontinuous input current which is not favorable for PV applications. Further in [22], an NPC-based qZS inverter is proposed which employs 8 switching devices to synthesize a 5-level output voltage waveform. However, in addition to the switching devices, additional clamping diodes are also required for freewheeling operation.

Leakage current is another major issue in PV-fed grid-connected transformerless inverter [23], [24]. High-frequency transitions in the Common mode voltage (CMV) of the MLI charge the parasitic capacitance of the PV panel, facilitating the flow of leakage current. If this leakage current is not restricted to be within the prescribed limits, the safety of the PV system could be compromised. Apart from the regular switching transitions, the shoot-through states (which are deliberately introduced in ZS / qZS-based MLIs to achieve the required voltage boosting) also contribute to the high-frequency transitions in CMV.

The research work reported in [25] minimizes high-frequency transitions in CMV with the employment of a modified PWM scheme, which selects appropriate zero-states in a switching cycle. The qZS inverter described in [26] employs two additional switches to connect the grid neutral to the negative DC bus of the input source. When switched at grid frequency, these devices show a path to the leakage current while limiting high-frequency transitions in common-mode voltage. In contrast to [26], the power converter proposed in [27] connects two switches and two diodes across the grid, which conduct during the freewheeling conditions, effectively decoupling the PV source from the grid. As far as the issue of leakage current is concerned, the aforementioned literature [25], [26], [27] is confined to two-level, single-phase qZS-based inverters.

The aforementioned literature on single-phase, qZS-MLI reveals the following limitations in the present state-of-the-art: (i) requirement of a higher number of power semiconductor switching devices, (ii) leakage current, and (iii) discontinuous input current. These shortcomings are the impetus for the development of the single-stage dual quasi-z-source 7-level inverter (DqZS-7LI) topology proposed in this manuscript. This power converter configuration, which utilizes a lower number of devices, is obtained by combining two antiparallel qZS networks with a cascaded 7-level H-bridge circuit. This paper also proposes a modified level-shifted PWM scheme, which achieves the twin objectives of input voltage boosting and generation of 7-levels in the output voltage. Along with the proposed PWM technique, an LCL filter is used to reduce the high-frequency voltage transitions across the parasitic capacitance. This restricts the leakage current within the safety standards stipulated by the VDE0126-1-1 [28]. Steady-state and dynamic performances of the power converter are evaluated both in standalone and the grid-connected modes with the aid of simulation studies and are experimentally verified with a hardware prototype.

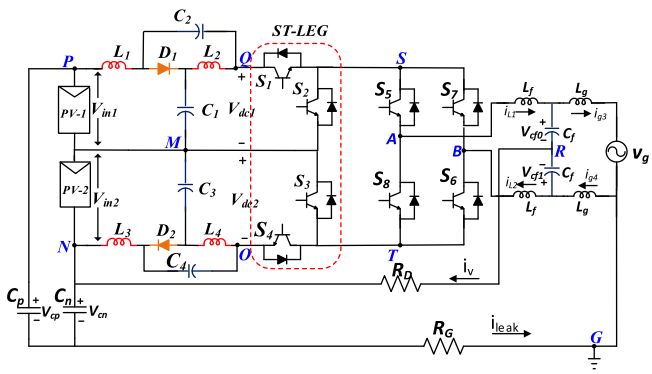

Fig. 1. Proposed DqZS-7LI.

II. The Proposed DQZS-7LI

A. Proposed Power Converter

The proposed PV fed dual- quasi-z-source 7-level inverter (DqZS-7LI) topology is shown in Fig. 1. This configuration employs two PV sources, PV-1 and PV-2, with an unequal voltage ratio of 1:2 respectively. Also, this topology consists of two quasi-z-source networks and a cascaded 7-level H-bridge inverter. The outputs of the PV sources are input to the quasi-z-source networks as shown in Fig. 1. The qZS networks boost the input PV voltage to suit the requirements of the 7-level inverter. The top qZS network (qZS-1) employs switches S_1 and S_2 to obtain the required shoot-through. Similarly, the switches S_3 and S_4 are used to obtain the shoot-through for the bottom qZS network (qZS-2). As shown in Fig. 1, the midpoints of the switches S_1, S_2, and S_3, S_4 respectively serve as the positive and negative DC rails for the output H-bridge inverter, which is constituted by the switches S_5-S_8. The midpoints A and B of the H-bridge are interfaced to the grid with a symmetrical LCL filter. The detailed description of the parameters C_p, C_n, R_D, and R_G are explained in section V.

B. Output Voltage Levels and Corresponding Switching States of the Power Converter

The proposed configuration is capable of generating seven levels in the output phase voltage waveform V_{AB} (see Column-2, Table I). In Table I, the 'on' and the 'off' states of the semiconductor devices are indicated as logic '1' and '0' respectively. These switching states are classified into two types namely, the non-shoot-through states (NST), and the shoot-through states (ST). The NST states are further sub-divided into six active states and two zero states. These active -states generate six

TABLE I
SWITCHING COMBINATIONS TO ACHIEVE 7-LEVEL OPERATION

State type	Voltage (V_{AB}) for *Vin1 = V & Vin2 =2V*	Switching states (1-ON, 0-OFF)							
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
NST	$3V$	1	0	0	1	1	1	0	0
NST	$2V$	0	1	0	1	1	1	0	0
NST	V	1	0	1	0	1	1	0	0
NST	0	0	0	0	0	1	0	1	0
NST	0	0	0	0	0	0	1	0	1
NST	$-V$	1	0	1	0	0	0	1	1
NST	$-2V$	0	1	0	1	0	0	1	1
NST	$-3V$	1	0	0	1	0	0	1	1
ST	0	1	1	0	0	1	0	1	0
ST	0	0	0	1	1	1	0	1	0
ST	0	1	1	1	1	1	0	1	0

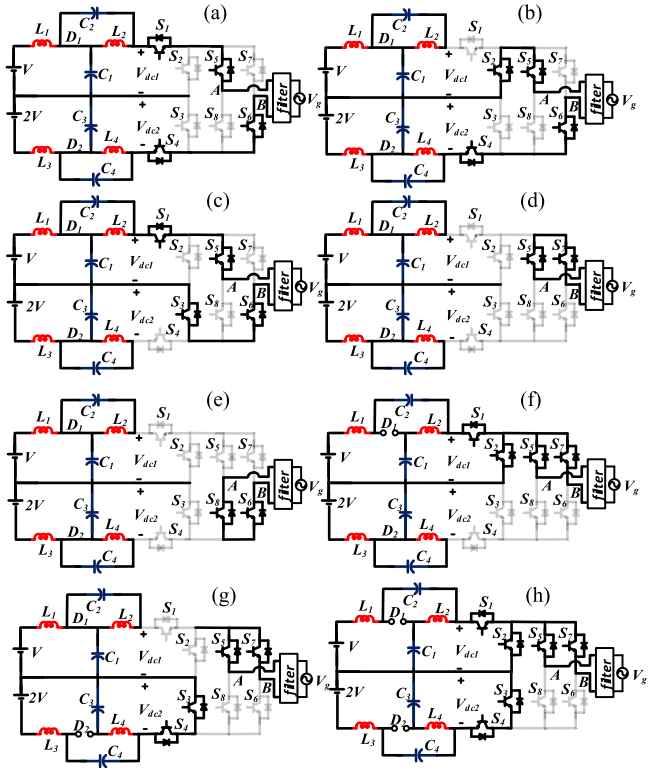

Fig. 2. Circuit diagrams for NST and ST states of the power converter.

distinct voltage levels ±V, ± 2V, and ±3V in the output voltage waveform (considering Vin = V).

Fig. 2 presents the operating modes of the proposed converter during the NST and the ST states. While Fig. 2(a)–(e) represent the NST modes of the power converter, Fig. 2(f)–(h) represents the ST mode. From Fig. 2(a), it may be noticed that by turning on S_1 and S_4, the combined DC-link voltage (V_{dc1}+V_{dc2}, Fig. 1) is equal to +3V, which is applied to the H- bridge inverter terminals. Fig. 2(b) shows the operating mode to synthesize the voltage level of +2V, wherein the switches S_2 and S_4 are turned on. The operating mode to generate the level of +V is demonstrated in Fig. 2(c), wherein the switches S_1 and S_3 are turned on (Table I and Fig. 2(c)). It may be noted that the switches S_5 and S_8 are turned on in all these three modes to connect the rails of the H-bridge to the outputs of the qZS networks. The method of synthesizing the three negative levels (-V, -2V, and -3V) can readily be deduced with the aid of Table I. In the zero states, the H-bridge is completely isolated from the qZS networks by turning off all the four switches S_1 - S_4 as shown in Fig. 2(d) and (e). During these two states, there is no power transfer between the PV source and the load. Thus, it is evident that the shoot-through (ST) mode of operation can be inserted in the zero-state.

In the proposed power converter, the shoot-through mode of operation can be implemented in three different ways. These are: (i) qZS-1 shoot-through (Fig. 2(f)) (ii) qZS-2 shoot-through (Fig. 2(g)) (iii) both qZS-1 and qZS-2 shoot-through (Fig. 2(h)). In (i) and (ii) shoot-through modes of operation the respective DC-link voltages (V_{dc1}, V_{dc2}) of the qZS networks drop to zero, and in (iii) the total DC-link voltage (V_{dc1}+V_{dc2}) of the power converter drop to zero. In this configuration, the zero-state (which includes the ST state) is inserted in all the 7 levels of operation to obtain the required boosting of the DC-link voltage. Consequently, the output voltage displays pulsation (from zero to the synthesized voltage level) in any given time period.

III. CONTROL SCHEME FOR THE PROPOSED DUAL QZS 7-LEVEL INVERTER

A. *Implementation of the MLS-PWM Scheme*

Generally, two control techniques are commonly employed to obtain a multilevel output waveform: (i) level-shifted PWM (LSPWM) and, (ii) phase-shifted PWM. In this work, a modified level-shifted PWM (MLSPWM) is implemented to synthesize the desired 7-level phase voltage waveform with input voltage boosting. To synthesize the required 7-level output voltage waveform despite the asymmetry in the input voltages, the sinusoidal modulating signal ($v_m = m\ sin(\omega t)$) should be modified to v_m^* as shown in Fig. 3. The PWM scheme is implemented by comparing a modified reference signal (v_m^*) with a single carrier signal. Initially, the modulated sine wave (v_m) is divided into three regions of operation Z_{n1}, Z_{n2}, and Z_{n3} (shown in Fig. 3) based on the value of modulation index (m) and 'R_1', 'R_2', where 'R_1' and 'R_2' are defined as the multiplication factors which are taken into consideration for asymmetry of the input voltages. The multiplication factors 'R_1' and 'R_2' are expressed as:

$$R_1 = {V_{in1}}/{V_{in1} + V_{in2}}\ , R_2 = {V_{in2}}/{V_{in1} + V_{in2}} \qquad (1)$$

In region-1, wherein $0 < v_m < (R_1.m)$, the modulated sine wave (v_m) is not modified. In region-2 ($R_1.m < v_m < R_2\ .m$), the sine wave (v_m) is scaled down to $v_m/2$ and in region-3 ($R_2\ .m < v_m < m$), it is scaled down to $v_m/3$. The summation of the references in regions 1, 2 & 3 synthesizes the modified reference wave (v_m^*) as shown in Fig 3. The modified reference wave (v_m^*), shown in Fig. 3, is plotted considering the voltage ratio of the input PV sources (1:2). Hence R_1 and R_2 are selected as 1/3 and 2/3.

The modified reference wave (v_m^*) is compared with the carrier wave (C) in the three regions mentioned above, for both positive and negative half-cycles. The voltage level in the

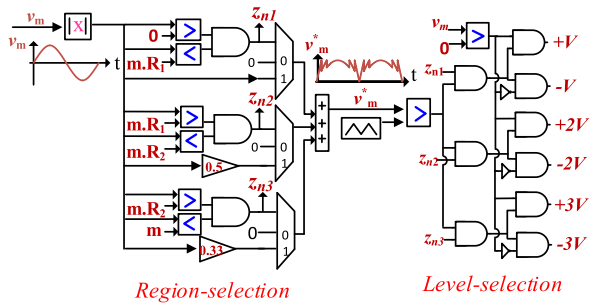

Fig. 3. Implementation of modified reference wave (v_m^*) for DqZS-7LI.

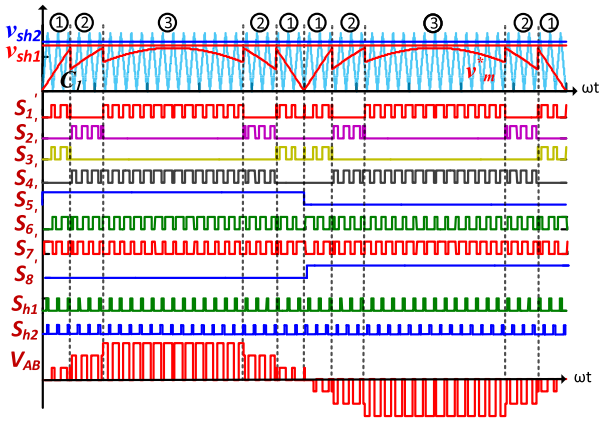

Fig. 4. Implementation of modified reference wave (v_m^*) for DqZS-7LI.

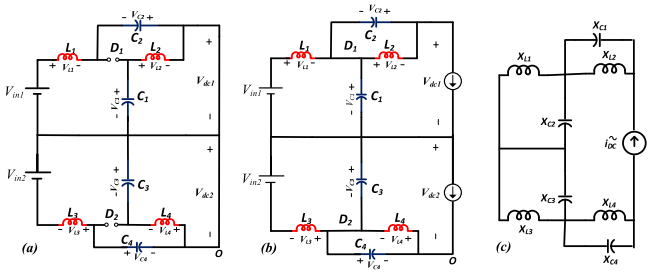

Fig. 5. Equivalent circuit of DqZS-7LI during (a) Shoot-through state (ST) (b) Non-shoot-through (NST) state. (c) Simplified equivalent circuit.

output is determined by the output of the comparator and the region of operation (Z_{n1}, Z_{n2}, and Z_{n3}) as shown in Fig. 3. Table I shows the generation of gating signals for the power devices to synthesize various voltage levels. Fig. 4 presents the PWM pulses (S_1'-S_8') required to synthesize the 7-level output voltage waveform. Further, to implement voltage boosting in qZS networks, two shoot-through pulses S_{h1} and S_{h2} are generated by comparing the DC references v_{sh1}, v_{sh2} with the carrier signal (C). Tofacilitate the boosting operation with qZS-1 and qZS-2, logical 'OR' operations are respectively performed between the shoot-through pulse train (S_{h1}) and the signals (S_1'-S_2'), and the shoot-through pulse train (S_{h2}) and the signals (S_3'-S_4'). The signals obtained after these logical 'OR' operations are employed to gate the switches S_1-S_4. It may be noted that the gating signals (S_5'-S_8') are directly used to gate the switches S_5-S_8 to generate polarity in the output voltage.

B. Boost-Factor of the Proposed DqZS-7LI

Fig. 5 shows the equivalent circuit for the proposed DqZS-7LI during shoot-through (ST) and non-shoot-through (NST) states of operation.

During the ST, the inductor voltages (V_{L1}, V_{L2}) and DC-link voltages are presented in (2), (3) & (4):

$$V_{L1} = V_{in1} + V_{c2}\,,\ V_{L2} = V_{c1} \tag{2}$$

$$V_{L3} = V_{in2} + V_{c4}\,,\ V_{L4} = V_{c3} \tag{3}$$

$$V_{dc1} = 0\,,\quad V_{dc2} = 0 \tag{4}$$

Similarly, in the NST state these are given by:

$$V_{L1} = V_{in1} - V_{c1}\,,\quad V_{dc2} = 0 \tag{5}$$

$$V_{L3} = V_{in2} - V_{c3}\,,\ V_{L4} = -V_{c4} \tag{6}$$

$$V_{dc1} = V_{c1} + V_{c2}\,,\quad V_{dc2} = V_{c3} + V_{c4} \tag{7}$$

Applying the volt-sec balance to the inductors (2), (5), (3) & (6) over one switching time-period (T_s) the following equations are derived:

$$V_{C1} = \frac{1-D_1}{1-2D_1}\,V_{in1}\,,\ V_{C2} = \frac{D_2}{1-2D_2}\,V_{in1} \tag{8}$$

$$V_{C3} = \frac{1-D_1}{1-2D_1}\,V_{in2}\,,\ V_{C2} = \frac{D_2}{1-2D_2}\,V_{in1} \tag{9}$$

where 'D_1 & D_2' are the shoot-through (ST) duty ratios, which are expressed as T_{sh}/T_s; where T_{sh} is the ST time.

From (7), (8) & (9), the boosted DC-link voltages are expressed as:

$$V_{dc1} = \frac{1}{1-2D_1}\,V_{in1}\,,\ V_{dc2} = \frac{1}{1-2D_2}\,V_{in2} \tag{10}$$

C. Design of qZS Network of Proposed DqZS-7LI

In the proposed power converter the design of the quasi-z-source inductors and capacitors are derived based on the allowable low frequency current ripple of the inductor and DC-link voltage ripple of the inverter. This low-frequency ripple is caused by the second harmonic component of the output power. Further, to simplify the design equations only the low-frequency ripple component is considered neglecting the switching frequency ripple of the inductor current. The simplified equivalent circuit of the power converter is shown in Fig. 5(c). The current source $\tilde{i_{DC}}$ shown in Fig. 5(c), represents the fundamental component of the DC-link current and $X_{l(1-4)}$ to $X_{c(1-4)}$ represent the reactive components of the quasi-z-source network.

From the equivalent circuit, the low-frequency component of i_{L1} is derived as:

$$\tilde{i_{L1}} = \frac{4\sqrt{2}}{3\pi}\cdot\frac{k\,(P_{OUT})}{V_{OUT}}\cdot\sin\left(\frac{4.\pi.t}{T}-\frac{\pi}{2}\right)\cdot\frac{x_{C2}}{x_{L1}+x_{C2}} \tag{11}$$

Where the variable 'k' represents the percentage of the power delivered by the PV-1. From (11) and the power balance of the power converter the low-frequency inductor ripple 'x' is

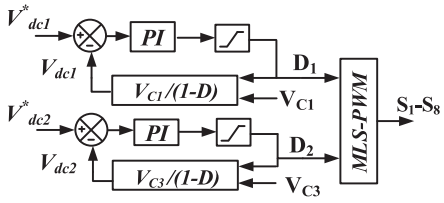

Fig. 6. Closed-loop DC-link voltage control for the proposed DqZS-7LI.

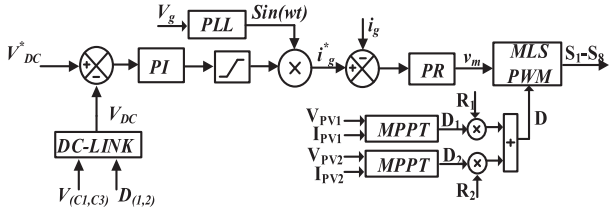

Fig. 7. The grid control scheme for DqZS-7LI.

expressed as

$$x = \frac{4\sqrt{2}}{3\pi}\frac{\mathrm{V}_{in1}}{V_{OUT}}\frac{T^2}{(16\pi^2 L_1 C_2 - T^2)} \tag{12}$$

Similarly, the low frequency voltage across the capacitor 'C_1' is given by

$$v_{C1}^{\sim} = \frac{4\sqrt{2}}{3\pi}\frac{k\,(P_{OUT})}{V_{OUT}}\sin\left(\frac{4.\pi.t}{T} - \frac{\pi}{2}\right).\frac{\mathrm{x}_{L2}.\mathrm{x}_{C1}}{\mathrm{x}_{L2} + \mathrm{x}_{C1}} \tag{13}$$

From (13) the low frequency voltage ripple 'y' across the capacitor 'C_1' is expressed as:

$$y = \frac{4\sqrt{2}}{3\pi}\frac{k\,(P_{OUT})\,.\,(D)}{V_{OUT}.\,(1-2D)\,\mathrm{V}_{in1}}\frac{4\pi T L_2}{(16\pi^2 L_2 C_1 - T^2)} \tag{14}$$

Solving the (12) and (14) and considering $\mathrm{L}_1 = \mathrm{L}_2$ and $\mathrm{C}_1 = \mathrm{C}_2$ the inductor and capacitor values of qZS-1 are obtained. A similar analysis is applied to the inductor and capacitor of qZS-2 to derive L_3, L_4 and C_3, C_4 parameters.

IV. Standalone and Grid Connected Control Strategy of DQZS-7LI

A. Stand-Alone Mode

It is well known that the output voltage of the quasi-z-source MLI is determined by the gain, which is the product of the boost factor 'B' and modulation index 'm' and obtained by the qZS network. In the standalone mode of operation, the modulation index (m) is held constant while controlling the output voltage. In such a situation, the gain of the power converter is solely determined by the boosting factor (B), which needs to be controlled to regulate the output voltage against the load and source disturbances.

In the proposed topology, a pulsating DC-link is produced across the qZS-1 and qZS-2 networks, when shoot-through (ST) is inserted in the shoot-through leg constituted by S_1, S_2, S_3, and S_4 (Fig. 1). An indirect measurement of the DC-link voltage is required as the pulsating DC voltage cannot be measured directly or it can be used as a feedback signal.

In the present work, the DC-link voltage $\mathrm{V}_{\mathrm{dc1}}$ and $\mathrm{V}_{\mathrm{dc2}}$ of the 7-level inverter are estimated using shoot-through duty ratios (D_1, D_2) and the capacitor voltages (V_{c1}, V_{c3}) (8) & (9). Fig. 6 presents the closed-loop control scheme to control the DC-link voltages ($\mathrm{V}_{\mathrm{dc1}}$ and $\mathrm{V}_{\mathrm{dc2}}$) of the proposed converter. The estimated DC-link voltages $\mathrm{V}_{\mathrm{dc1}}$, $\mathrm{V}_{\mathrm{dc2}}$ are then compared with the reference voltages $V^*_{\mathrm{dc1}}, V^*_{\mathrm{dc2}}$ respectively and the error generated is compensated by the PI controllers. The outputs of the PI controllers determine the required shoot-through duty ratios ($\mathrm{D}_1, \mathrm{D}_2$). These duty ratios are translated into the reference signals 'V_{sh1} and V_{sh2}' (Fig. 4), which are compared with the carrier signal to implement the shoot-through mode as discussed in Section III. Thus, the output voltage of the DqZS-7LI is regulated solely with the closed-loop feedback control of DC-link voltages ($\mathrm{V}_{\mathrm{dc1}}$, $\mathrm{V}_{\mathrm{dc2}}$).

B. Grid-Connected Mode

The grid-connected mode of operation requires the fulfillment of three objectives: (i) DC-link voltage regulation (ii) Injection of power into the grid at unity power factor (iii) Independent MPPT control of the two quasi-z-source networks. The two degrees of freedom offered by the qZS converter namely, the shoot-through duty ratio 'D' and the modulation index 'm' and are utilized to control these three objectives. Fig. 7 shows the control scheme for the closed-loop control of the proposed DqZS-7LI in the grid connection mode.

Perturb & Observe MPPT algorithm is employed to extract the maximum power from the PV panels. The currents ($\mathrm{I}_{\mathrm{PV1}}$, $\mathrm{I}_{\mathrm{PV2}}$) and voltages ($\mathrm{V}_{\mathrm{PV1}}$, $\mathrm{V}_{\mathrm{PV2}}$) of the PV panels are sensed and fed to the respective MPPT controllers. These controllers generate the required duty ratios (D_1 and D_2), which are multiplied by R_1 and R_2 (1) to generate the shoot-through duty ratio (D) [33]. Further, the duty ratio is fed to the MLS-PWM to implement the ST mode with the help of the shoot-through leg.

As stated in the previous section, the total DC-link voltage is assessed by sensing the voltages across capacitors and the duty ratios of the qZS-1 and qZS-2 networks. The error between the reference DC-link voltage (V^*_{DC}) and the estimated value ($\mathrm{V}_{\mathrm{dc1}}$+$\mathrm{V}_{\mathrm{dc2}}$) is compensated by the PI controller that is present in the outer voltage loop. The control signal generated by the PI controller is multiplied with a unit-sine signal $(\sin\omega t)$ to generate the reference value for the inner current loop (i^*_{g}) which is synchronized to the grid using a PLL. The reference grid current (i^*_{g}) is then compared to the actual grid current (i_{g}) and the resultant error is compensated by a PR controller. The output of the PR controller then generates the required modulation signal v_m, which is employed by the MLS-PWM control scheme to control the magnitude of the active power injected into the grid. [30].

V. Reduction of Leakage Current

In transformerless PV systems, due to the absence of galvanic isolation, the leakage current flows through the path that is formed by the frame of the PV panel, the parasitic capacitance, and the common ground. The VDE0126-1-1 standard [23] specifies that the maximum leakage current is limited to 300mA. As mentioned earlier, quasi-z-source multilevel inverters boost the input voltage with the insertion of the shoot-through mode in the zero states of the switching period. Although PV sources

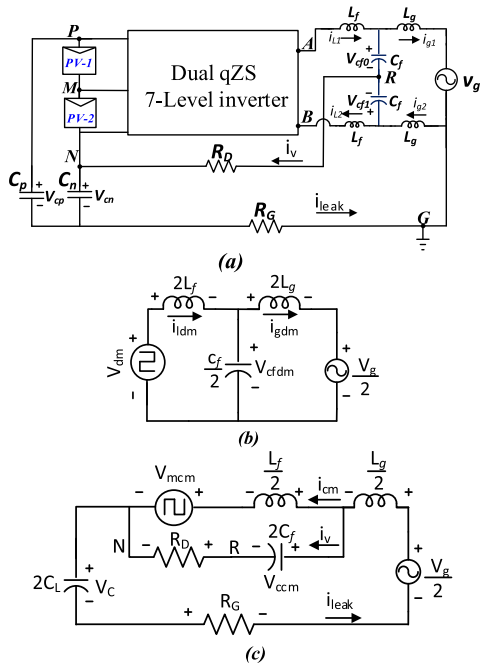

Fig. 8. (a) DqZS-7LI with leakage ground current path (b)Equivalent circuit of the differential-mode model (c) Equivalent circuit of the common-mode model.

are isolated from the grid during the zero-states (Fig. 2(d) and (e)), the addition of the shoot-through state introduces high-frequency transitions in the voltage impressed across the parasitic capacitor. These high-frequency transitions generate the leakage current, which flows from the PV source to the ground. Thus, it stands to reason that maintenance of a constant voltage across the parasitic capacitance eliminates the leakage current. Though it is generally desirable to eliminate the leakage current, it is not possible in qZS-based multilevel inverters owing to the insertion of the shoot-through in the zero-states. In such a scenario, the leakage current is reduced by reducing the magnitude of high-frequency transitions in the voltage, which is impressed across the parasitic capacitor. It is well known that the magnitude of these high-frequency transitions is determined by the common-mode voltage (CMV), which is defined as follows:

$$V_{cm} = \frac{V_{AO} + V_{BO}}{2} \tag{15}$$

As shown in Fig. 1 the qZS-2 network is connected with a reversed orientation compared to the qZS-1 network (Fig. 1). This facilitates the inclusion of inductor L_3 and the capacitor C_4 between inverter negative terminal 'O' and negative terminal of PV panels 'N' throughout the shoot-through (ST) as well as the non-shoot-through (NST) states. Hence, the effective CMV (V_{mcm}) is represented as:

$$V_{mcm} = V_{cm} + V_{L3} - V_{C4} \tag{16}$$

Furthermore, an LCL filter is connected across the inverter output terminals (AB), as shown in Fig. 8(a), to achieve the dual objectives of (i) reducing higher-order current harmonic components in the leakage current induced by the effective CMV (V_{mcm}) and (ii) filtering the output voltage of the inverter. To damp out the oscillations in the leakage current, a damping resistor (R_D) is connected between the midpoint of the filter capacitor and the negative terminal of the PV source (N) as shown in Fig. 8(a). In Fig. 8(a), C_p and C_n respectively represent the parasitic capacitance formed between the PV cells and their metallic frame, while R_G represents the ground resistance [29].

The mathematical model of the system shown in Fig. 8(a) may be resolved into the differential-mode and the common-mode models.

The equations corresponding to the differential-mode model are given by:

$$2L_f \ \hat{i}_{ldm} = V_{dm} - V_{cfdm} \tag{17}$$

$$2L_g \ \hat{i}_{gdm} = V_{cfdm} - V_g \tag{18}$$

$$\frac{C_f}{2} \ \hat{V}_{cfdm} = i_{ldm} - i_{gdm} \tag{19}$$

where the symbols i_{ldm}, i_{gdm}, V_{dm} and V_{cfdm} respectively denote the differential-mode inverter current ($(i_{l1}+i_{l2})/2$), differential-mode grid current ($(i_{g1}+i_{g2})/2$), differential-mode inverter voltage (V_{AN}-V_{BN}) and the differential-mode filter voltage (V_{cf0} +V_{cf1}). A pictorial representation of (17)–(19) results in the differential-mode equivalent circuit presented in Fig. 8(b).

On the other hand, the equations corresponding to the common-mode model are given by:

$$\frac{L_f}{2} \ \hat{i}_{lcm} = \frac{V_g}{2} - i_{leak}R_G - V_c - V_{mcm} - \frac{L_g}{2}\hat{i}_{leak} \tag{20}$$

$$\frac{L_f}{2} \ \hat{i}_{lcm} = V_{mcm} - V_{cfcm} + i_v R_D \tag{21}$$

$$2C_L \ \hat{V}_c = i_{leak} \tag{22}$$

$$2C_f \ \hat{V}_{cfcm} = i_{leak} - i_{lcm} \tag{23}$$

where the symbols i_{lcm} and V_{cfcm} respectively denote the common-mode inverter current ($(i_{l2}$-$i_{l1})$) and the common-mode voltage of the filter ($(V_{cf0}$ -$V_{cf1})/2$).

A pictorial representation of (20)–(23) results in the common-mode equivalent circuit presented in Fig. 8(c). In this analysis, it is assumed that both PV parasitic capacitors have the same value of capacitance (i.e., $C_P = C_N = C_L$).

From Fig. 8(c), it may be noted that the leakage current (i_{leak}) is split into two components i_{lcm} and i_v (the high-frequency current flowing through the midpoint of capacitors 'R' and the 'N' terminal, Fig. 8(a)). This mid-point connection creates an alternate path to the current produced by the high-frequency voltage transitions in V_{mcm}. This branch bypasses higher-order components of leakage current (on account of the presence of the capacitor $2C_f$) and allows only lower-order components of currents to flow through the ground path. From this analysis, it is evident that the LCL filter reduces the leakage current significantly.

VI. Simulation Results

MATLAB-Simulink is utilized to validate the proposed single-phase DqZS-7LI. Fig. 9 presents the grid-connected operation of the proposed power converter with time-varying insolation for the PV sources. The following three cases are

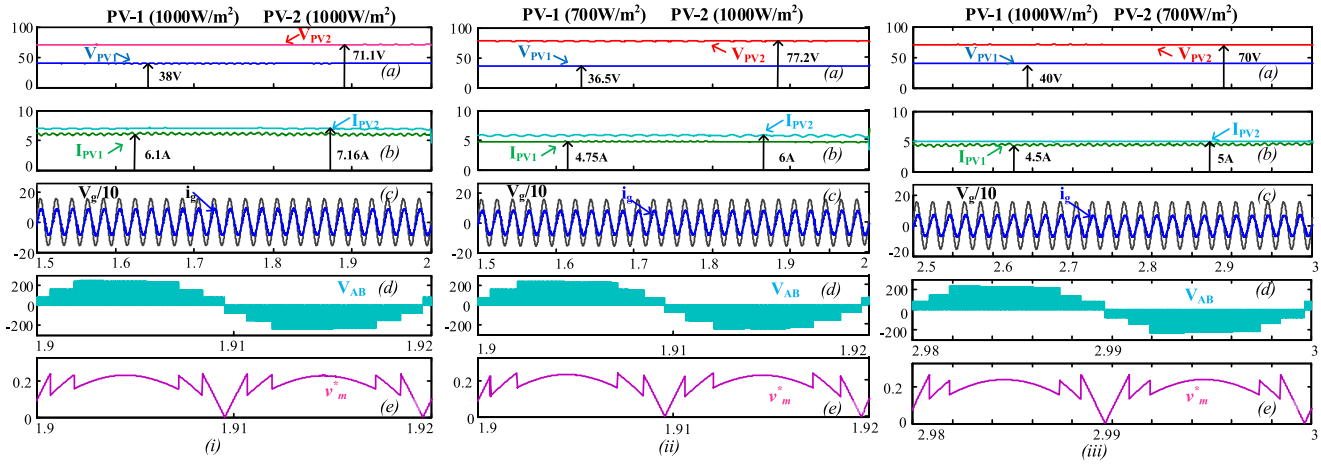

Fig. 9. Simulation results of grid control of the power converter for (i) PV-1 = PV-2 = 1000W/m^2 (ii) PV-1 = 700 W/m^2, PV-2 = 1000W/m^2 (iii) PV-1 = 1000 W/m^2, PV-2 = 700W/m^2. The subplots give the waveforms of :(a) PV voltages (V_{PV1}, V_{PV2}) (b) PV currents (I_{PV1}, I_{PV2}) (c) Grid voltage (V_g) and currents (i_g) (d) Output voltage (V_{AB}) (e) Modified modulation index (v_m^*) voltage.

simulated to study the behavior of MPPT and the grid current control for the changes in insolation levels: (i) both PV-1 and PV-2 operate at 1000W/m^2 (ii) PV-1 operates at 700 W/m^2 and PV-2 operates at 1000 W/m^2 (iii) PV-1 operate at 1000 W/m^2 and PV-2 operate at 700 W/m^2. A solar panel of open-circuit voltage 21.05V and a short circuit current of 3.74A is considered for simulation. Series and parallel combinations of the solar panels are used to form PV-1 ($V_{oc1} = 42.1$, $I_{sc1} = 7.48$) and PV-2 ($V_{oc2} = 84.2$, $I_{sc2} = 7.48$) sources. In Fig. 9. subplots (a) and (b) presents the PV voltages (V_{PV1}, V_{PV2}) and PV currents (I_{PV1}, I_{PV2}) during changes in the insolation of PV sources with a constant temperature. The maximum power point control tracks the power by adjusting the shoot-through duty ratios (D_1 and D_2, Fig. 7) to obtain the maximum power from the PV sources. Further, these shoot-through duty ratios are multiplied with the multiplication factors R_1 and R_2 to account for the asymmetry of the PV voltages. The resultant shoot-through duty ratio 'D' is fed to MLSPWM to generate shoot-through in the qZS network. It may be noted that in case I, the maximum voltage and the maximum current generated by the sources PV-1 and PV-2 (Fig. 1) at 1000W/m^2 are (38V, 6.1A) and (71.1, 7.16A) respectively.

In case II, as the source PV-1 operates at an insolation level of 700 W/m^2, the maximum currents of PV-1 and PV-2 are reduced to 4.75A and 6A respectively by the MPPT algorithm by re-adjusting the shoot-through duty ratio 'D'. In case III, while the source PV-2 operates at a maximum voltage of 70V and a reduced peak current of 5A (due to the lower insolation level of 700 W/m^2), the source PV-1 operates at a non-MPPT point at (40V, 4.5A) to facilitate the 7-level operation. These results clearly show that the MPPT control (in Fig. 7) tracks the changes in insolation with effective control of the shoot-through duty ratio. The subplot (c) in Fig. 9 presents the grid voltage and grid current in all three cases of operation. It may be observed that a sinusoidal current of varying magnitude, which depends on the level of insolation, is injected into the grid at UPF.This shows the effective control of modulation index 'm' by the current controller shown in Fig. (7). The subplots (d) and (e) present the output voltage (V_{AB}) and the modified modulation wave (v_m^*)

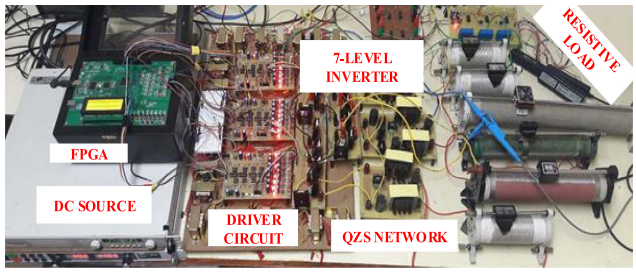

Fig. 10. Hardware prototype of the power converter.

of the proposed power converter (Fig. 9). Both the modulation wave (v_m^*) and phase voltage are modified based on the voltage asymmetry of the PV sources. The change in the modulation signal (v_m^*) can be observed by comparing the subplots (e) of case-I, II, and III.

VII. Experimental Results

A low-scale hardware prototype of the proposed DqZS-7LI is fabricated to verify the MATLAB-Simulink results. Fig. 10 shows the fabricated hardware prototype.

To emulate the PV source two programmable DC power supplies with CC-CV characteristics are employed. The PWM scheme is implemented with a Spartan-6 FPGA board, which outputs gating pulses which are employed to drive the switches S_1-S_8 (power MOSFETs). A Yokogawa DL850 power oscilloscope is utilized to capture the experimental waveforms. Table II presents the details of the component and the specifications of the hardware prototype.

Fig. 11 demonstrates the applied input voltages (V_{in1}, V_{in2}) and boosted DC-link voltages (V_{dc1}, V_{dc2}) of the 7-level inverter. As shown in the figure the input voltages of 35 V (V_{in1}) and 70V (V_{in2}) are input to the top and bottom qZS networks respectively. As stated in the earlier sections, the proposed converter utilizes the dual-quasi-Z source networks to achieve the required voltage boosting. In the present experimental studies, a shoot-through duty ratio (D) of 0.25 to achieve a boosting factor of 2 (10). A modulation index (m) of 0.75 is chosen to obtain the

TABLE II
HARDWARE PROTOTYPE SPECIFICATIONS

Parameters	Values
Input DC voltage(V_{DC})	105V
Total boosted voltage	210V
output voltage	110V (RMS)-50Hz
Switching-frequency(fs)	20kHz
Modulation-Index (m)	0.75
Inductors	EE65CORE, 3-mH
Capacitors (Electrolytic)	1400μF,300V
Ultra-Fast rectifier diode	MUR1560CT
Parasitic capacitor C_p	100nF
R_D,L_f, C_f,, L_g	1ohm,1mH, 6uf, 2.5mH
Power	300W

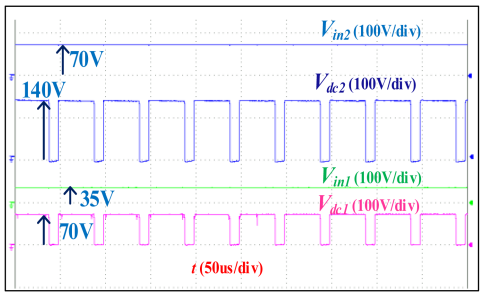

Fig. 11. Experimental results of DC-input voltages (V_{in1}, V_{in2}) and DC-link voltages (V_{dc1}, V_{dc2}) of DqZS-7LI.

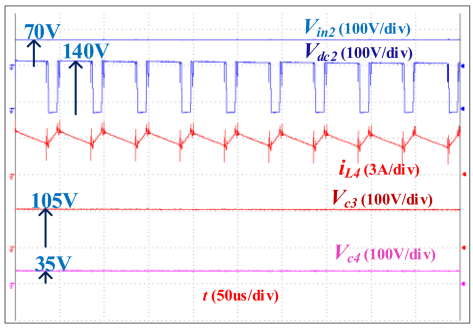

Fig. 12. Experimental results of the DC input voltage (V_{in2}), DC-link voltage (V_{dc2}) and inductor current (i_{L4}) and capacitor voltages (V_{c3}, V_{c4}) of the qZS-1 network.

required output voltage (110 V). From Fig. 11 it may be observed that the input voltages are boosted to 70 and 140V as indicated by the traces of V_{dc1} and V_{dc2}. It may also be noted that the waveforms of the DC-link voltages are typically pulsating, as they drop to a value of zero whenever a shoot-through mode is inserted.

The experimental waveforms of inductor current (i_{L4}) and the capacitor voltages (V_{c3}) and (V_{c4}) of the qZS-2 are shown in Fig. 12. For a shoot-through (ST) duty ratio (D) of 0.25, the input voltage (top trace) of 70V is boosted to 140V DC-link (second trace). From the figure it is evident that the boosted DC-link voltage of 140V is distributed across the capacitors C_3 and C_4 in the ratio of (1-D): (D). Fig. 12 also shows that the voltages across the capacitors (C_3, C_4) attain steady-state values of 105 and 35V respectively. It may be observed that whenever the DC-link voltage drops to a value of zero (during the ST time period), the inductor current (i_{L4}) (third trace) increases linearly.

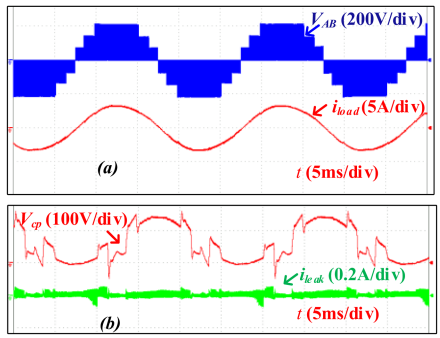

Fig. 13. Experimental results of (a) Output voltage waveform (V_{AB}), Load voltage (i_{Load}) (b) Parasitic capacitor voltage (V_{cp}) and Leakage current (i_{leak}) of DqZS-7LI.

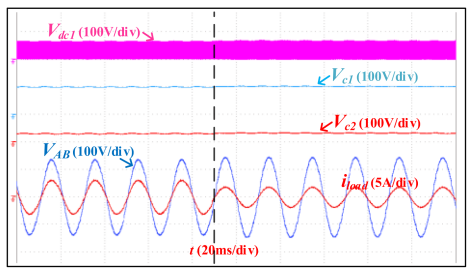

Fig. 14. Experimental results of DC-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), output voltage (V_{AB}), and the load current (i_{load}).

During the non-shoot-through time period, the inductor current decreases linearly.

Fig. 13(a) presents the output voltage and the load current of the proposed DqZS-7LI in the stand-alone mode of operation. The output voltage displays seven distinct levels between its negative and positive peak values (-210V to +210V). It may be noted that the phase voltage is a pulsating waveform that drops to a value of zero during the shoot-through period. The terminal voltage of the PV parasitic capacitor (V_{cp}) and leakage current (i_{leak}) are shown in Fig. 13(b). It may be observed that all high-frequency voltage transitions in the terminal voltage of the parasitic capacitor (V_{cp}) are filtered out, resulting in a low leakage current (i_{leak}) of 11.97mA (RMS). This leakage current, which flows between the PV source and the ground, is well within the limits of 300mA stipulated by VDE0126-1-1.

The dynamic performance of the power converter with closed-loop control in the standalone mode of operation is shown in Fig. 14. The control scheme shown in Fig. 6, which regulates the DC-link voltage, is employed for experimentation. The top three traces of this figure show the DC-link voltage of the top qZS (V_{dc1}) and the capacitor voltages (V_{C1}, V_{C2}) of the corresponding qZS network. The bottom two traces show the output voltage (V_{AB}) and the load current (i_{load}) of the power converter. The load on the proposed converter is suddenly reduced (2.2 A to 1.4A) to evaluate its dynamic response against load disturbances. Fig. 14 reveals that neither the DC-link voltage (V_{dc1}) nor the capacitor voltages (which add up to the DC-link voltage) show any noticeable change despite a sudden change in the load. It may also be noted that the output voltage (V_{AB}) remains unperturbed as its magnitude is solely determined by the DC-link voltage in the standalone mode of operation.

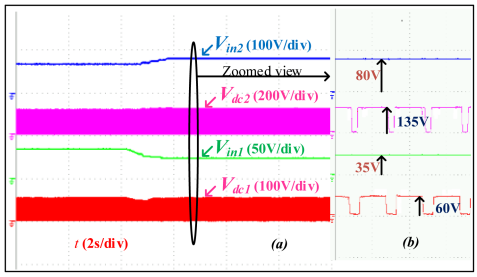

Fig. 15. Experimental results of (a) DC input voltages (V_{in1}, V_{in2}) and DC-link voltages waveforms of DqZS-7LI in the course of source disturbance (b) Zoomed view of the DC-link and DC input voltages of the DqZS-7L.

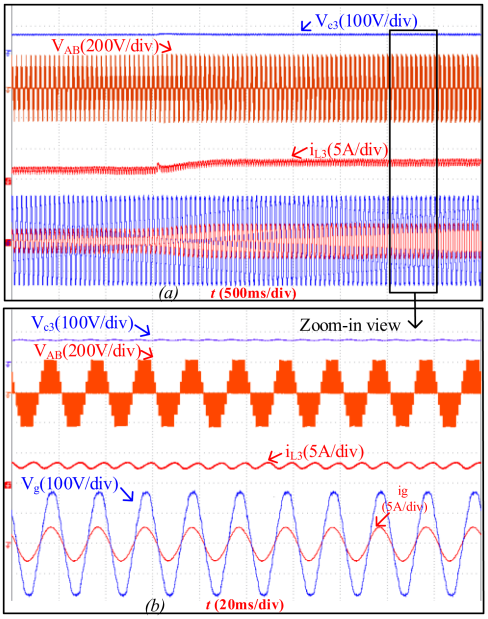

Fig. 16. Experimental results (a) Capacitor voltage (V_{c3}), Phase voltage (V_{AB}), Inductor current (i_{L3}) Grid voltage (V_g), and Grid current (i_g) (b) Zoom-in view at 300W.

Further, the dynamic response of the power converter against the source disturbance is assessed. In this experiment (Fig. 15), V_{in1} and V_{in2}, which are initially are maintained at 70V and 45 V respectively, are suddenly changed to 80V and 35 V. It may be noted that the second and the last traces of Fig. 15, which respectively show the two DC-link voltages, do not show any appreciable transients following the source disturbance.

Fig. 16 demonstrates the dynamic behavior of the proposed power converter while it feeds the grid. In this experiment, the active power of 135 W is fed into the grid initially. The shoot-through duty factor (D), which is automatically adjusted by the controller (Fig. 7) based on the insolation, is then increased to inject higher power into the grid. This action momentarily disturbs the DC-link voltage, which is quickly regulated by the action of the outer loop PI controller. This increases the reference grid current, which determines the magnitude of the current which should be fed into the grid to maintain the DC-link voltage and the output voltage. The PR regulator injects the required current into the grid by adjusting the modulation index. Fig. 16 clearly shows the action of the controller, which automatically adjusts the modulation index. The adjustment of the modulation

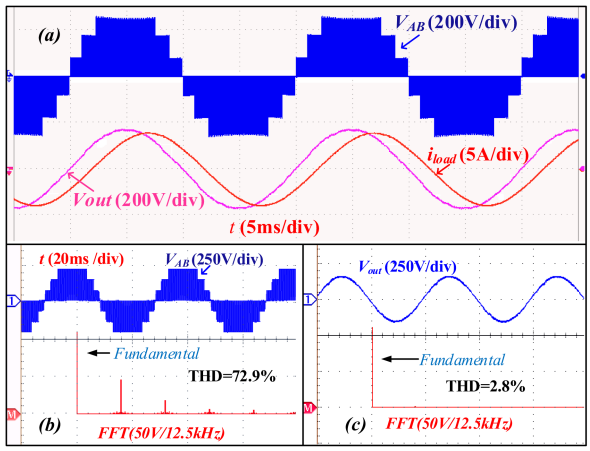

Fig. 17 (a) Output voltage (V_{AB}), load voltage (V_{out}), and load current (i_{load}) for 0.8 lagging power factor (b) FFT of inverter output voltage 'V_{AB}' (c) FFT of output voltage 'V_{out}'.

index results in (a) restoration of the DC-link voltage, which is evident from the first and second traces (b) increase in the source current iL3 (from 1.3 A to 3 A, third trace), and (c) increase in the power injected into the grid (fourth trace, wherein the grid current increases from 1.23 to 2.2 A, RMS). The zoomed picture of the aforementioned quantities and waveforms clearly shows the power injection into the grid at UPF.

Fig. 17(a) demonstrates the reactive power capability of the power converter. The power converter is tested for a 0.8 lagging ($R = 40\Omega$, $L = 95$mH) power factor. From Fig. 17(a) it may be noted that, load current 'i_{load}' is lagging w.r.t to load voltage 'V_{out}' which displays the reactive power capability of the proposed power converter.

VIII. Comparison With the Proposed DQZS-7LI

This section summarizes the merits of the proposed topology over the other impedance-source-based topologies, which have been reported so far in the literature. As qZS-based 7-level inverters available in the literature are scanty, a comparison with recent 5-level inverters is also considered. Table III presents the comparison of the number of components required, boost, and voltage stress across the devices in these topologies.

The proposed power converter (DqZS-7LI) requires a lesser number of capacitors, inductors, and switches when compared to the seven-level topologies presented in [14] and [18]. It may be noted that the proposed power converter requires an equal number of passive components and switches when compared to the 5-level topologies described in [15], [22]. Further, it is seen that the proposed power converter requires a lesser number of power diodes compared to all of these topologies. It may be noted that the voltage stress in [18] is lower when compared to all other topologies.

However, this advantage is overshadowed by the increased number of switches, diodes, and passive components needed in this topology. As seen from the Table, it may be noted that all these power converters have the same boost factors for a given shoot-thorough duty ratio 'D' except [21]. The voltage stresses on the capacitors, diodes, and switches in all these topologies are calculated on a per-unit basis, taking the output voltage (RMS)

TABLE III
COMPARISON OF THE PROPOSED POWER CONVERTER WITH QZS TOPOLOGIES

Parameters	ZS- 7L[14]	qZS-NPC[15]	qZS-CHB[18]	MqZS[21]	qZS-5L [22]	Proposed
Levels(N_L)	7	5	7	5	5	7
Sources	3	1	3	1	1	2
Capacitors	6	4	6	4	4	4
Inductors	6	4	6	2	4	4
N_{SW}	10	8	12	8	8	8
Diodes	3	6	3	3	4	2
Input current	discontinuous	continuous	continuous	discontinuous	continuous	continuous
Boost	$1/(1-2D)$	$1/(1-2D)$	$1/(1-2D)$	$2/(1-2D)$	$1/(1-2D)$	$1/(1-2D)$
Switch voltage stress	$(x\sqrt{2})/3$ $(x/\sqrt{2})$	$(x/\sqrt{2})$	$(x\sqrt{2})/3$	$(x/\sqrt{2})$	$(x/\sqrt{2})$	$x\sqrt{2}\ for\ S_1, S_2$ $(x\sqrt{2})/3\ for\ S_3, S_4$ $(x, 2\sqrt{2})/3\ for\ S_5 to S_8$
Capacitor voltage stress	$\sqrt{2}/3$	$1/\sqrt{2}\ for\ C_1$	$\sqrt{2}/3\ for\ C_1$	$1/\sqrt{2}\ for\ C_1$	$1/\sqrt{2}\ for\ C_1, C_3$	$\sqrt{2}/3\ for\ C_1$ $(x, D, \sqrt{2})/3\ for\ C_2$
		$(x.D)/\sqrt{2}\ for\ C_2$	$(x, D, \sqrt{2})/3\ for\ C_2$	$(x.D)/\sqrt{2}\ for\ C_2$	$(x.D)/\sqrt{2}\ for\ C_2, C_4$	$(2\sqrt{2})/3\ for\ C_3$ $(x, D, 2\sqrt{2})/3\ for\ C_4$
Diode voltage stress	$(x\sqrt{2})/3$	$(x/\sqrt{2})$	$(x\sqrt{2})/3$	$(x/\sqrt{2})$	$(x/\sqrt{2})$	$(x\sqrt{2})/3\ for\ D_1$ $(x, 2\sqrt{2})/3\ for\ D_2$
TSV/N_L	1	1.4	0.71	1.5	1.2	1
Voltage THD	24.3%	76.4%	29.3%	38.2%	74.2%	72.9%
Nsw* cost of high side driver	10*263= Rs.2630/-	8*263= Rs.2104/-	6*263= Rs.1578/- 6*117= Rs.702/- Total = 2280/-	8*263= Rs.2104/-	8*263= Rs.2104/-	8*263= Rs.2104/-

*x=1(1−D) where D is shoot−through duty ratio; cost of high side driver(1EDF5673K)=Rs.263 ;/cost of low side driver(IED44173NO1B3K)=Rs.117.

value as the base value. As the numbers of diodes, switches, and the voltage levels of the compared topologies are unequal, the Total Standing Voltage (TSV) (the sum of blocking voltages of all the switches and diodes w.r.t the peak voltage value) per number of voltage levels (N_L) is calculated [27]. It may be noted that the proposed power converter registers a lower (TSV/N_L) ratio when compared to the topologies [14], [15], [21], and [22].

The proposed power converter has higher voltage THD when compared to [14], [18], and [21] as the zero-level is inserted in each level of operation to boost the input voltage, achieve 7-level operation, and minimize the leakage current. However, the inverter output voltage is filtered by the LCL filter to provide a sinusoidal output voltage with a THD of 2.8% (as shown in Fig. 17(c)) to load/grid.

All the topologies compared in Table III except [18], requires high side drivers for multilevel operation. All the topologies, are evaluated for $M = 0.75$, $P_o = 1$kW, Vo (RMS) $= 230$V. The minimum available high side gate driver is rated for 600V, hence cost of the 600V high side gate driver is considered for all the topologies. As the number of switches is equal in the topologies presented in [15], [21], [22], and the proposed power converter, the cost (w.r.t high side driver) is also equal. Further, the proposed power converter incurs a lower cost (w.r.t to high side gate driver) when compared to topologies [14], as the number of switches is less. The power converter [18] has 6 low-side drivers, however, this advantage is offset by an equal number of high-side switches.

IX. LOSS ANALYSIS FOR THE DQZS-7LI

The efficiency of the proposed power converter is assessed by evaluating the following losses (i) switching loss (P_{sw}) and conduction power losses (P_{con}) occurring in the semiconductor switches $S_1 - S_8$ (ii) switching loss (P_{sd}) and conduction losses (P_{cd}) in anti-parallel and quasi-z-source diodes (Fig. 1). To

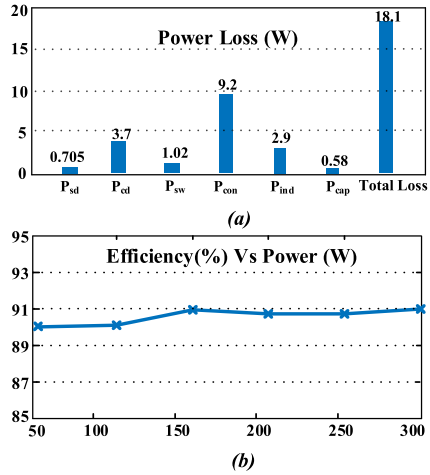

Fig. 18. (a).Power Loss distribution in DqZS-7LI at 300W. (b)Experimental efficiency of the proposed DqZS-7LI.

this end, the Powersim (PSIM) software is employed, which possesses thermal models of several popular switching devices. These simulation studies are carried out by employing MOSFET IRFP460 and the power diode 150EBU04 to construct the power converter. Further, the ESR losses (P_{cap}) in the capacitors and the conduction losses (P_{ind}) in the inductors are calculated using the method described in [31]. The loss distribution for the proposed converter for 300W power output is shown in Fig. 18(a). From Fig. 18(a) it may be noted that simulated efficiency of the converter is around 94% at 300W output power. These losses have been evaluated assuming $V_{in1} = 35$V, $V_{in2} = 70$V, $f_s = 20$ kHz, $M = 0.75$, $D = 0.25$, Vo (ph-RMS) $= 110$V, $PF = 1$.

Fig. 18(b) shows the experimental efficiency of the power converter for a step change of power ranging from 50W to 300W. To validate the efficiency of the power converter, a power analyser (UNI-T UT283A) is employed to measure the output

power. The input power is measured by a digital power meter (Yokogawa WT332E). From Fig. 18(b), it may be observed that the efficiency of the prototype reaches 91% at 300W output. It may be noticed that the efficiency achieved in experimental proptotype is less in comparison with simulation studies as the ripple due to high frequency and 2ω component in the DC-link voltage and inductor current are neglected.

X. Conclusion

This manuscript proposes a single-phase, single-stage dual-quasi-z-source 7-level inverter (DqZS-7LI), which is suitable for standalone as well as grid-connected PV applications. In this single-stage power converter, a modified LSPWM achieves the twin objectives of boosting the input PV voltages (using dual-qZS networks) and synthesizing the 7-level output voltage waveform (using the 7-level output inverter). Being a seamless structure, this power converter requires fewer semiconductor switching devices, compared to the other qZS and ZS-based seven-level topologies reported in earlier literature. Experimental studies are carried out to assess the steady-state and dynamic performances of the proposed power converter in the standalone mode as well as the grid-connected modes of operation. It is also shown that the leakage current is minimized by the combined effort of the modulation technique and the symmetrical LCL filter. Experimentation results demonstrate that the leakage current is well within the limits of the standards set by the *VDE 0126-1-1*. Based on the simulation and experimental results, it can be concluded that the proposed power converter could be effective for solar PV applications.

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