A Dual Quasi Z-Source Based T-Type Five-Level Inverter With Improved HERIC Structure for Photovoltaic Applications

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***Abstract*—A new single-stage, T-type five-level inverter, which is based on a dual quasi Z-source, and an improved HERIC structure has been proposed in this paper. It is envisaged that the proposed power converter could find applications in the area of grid-connected PV generation. The conventional topologies, which are based on two-stage conversion are bulky and expensive. The proposed single-stage system overcomes these disadvantages. Furthermore, the issue of leakage current, which is of paramount interest in PV systems is addressed by the adaptation of a PWM scheme along with the employment of passive filters. It is shown that the leakage current is effectively suppressed by the elimination of the high-frequency transitions across the parasitic capacitance due to the combined effort of the PWM scheme and the filter. The proposed power converter also displays the capability of supporting reactive power, which is one of the essential requirements for the present-day PV inverters. The steady-state and the dynamic performances of the proposed power converter are assessed with simulation studies and are then experimentally validated. A comparative study of the proposed power converter with the existing quasi-Z-source-based power converters is also undertaken, which reveals the advantages of the proposed configuration.**

***Index Terms*—Heric structure, level shifted PWM, quasi Z-source, T-type inverter, voltage boosting.**

I. Introduction

EVER increasing energy demands and the deterioration of the environment are the primary causes for the promotion of renewable energy sources (RES) like solar PV, wind, and fuel cells. Of these, solar photovoltaic (SPV) systems are poised to be the most dominant sources due to their abundance, zero-carbon emission, reduced cost of panels, absence of moving parts, and advancements in power semiconductor switching device technology and inverter topologies [1]. SPV is widely employed in distributed power generating systems either in stand-alone or grid-connected modes. The objectives of an SPV inverter include the realization of high-quality ac output, maximum power point tracking (MPPT), and minimization of losses. In general, SPV-based inverter topologies are classified into two categories based on their connection to loads namely: (i) isolated topologies and (ii) non-isolated topologies [2].

Isolated topologies provide galvanic isolation between the source and the grid, protection from the injection of DC, and low leakage current [3]. However, the disadvantages of isolated topologies are lower efficiency, bulkiness, and higher cost. Research focus has shifted to the development of transformerless non-isolated topologies, as they overcome the drawbacks of isolated topologies with increased efficiency. However, the transformerless topologies are plagued with a serious disadvantage of leakage current, which flows from PV panels to the grid [4]. The value of leakage current is primarily depends on the value of the parasitic capacitance and the voltage fluctuations present across the common mode circuit. Leakage current is undesirable on account of (i) increased EMI (ii) lower physical safety (iii) distortion of grid current (iv) high noise level during installation and (v) lowered life span of PV panels due to potential-induced degradation [5]. Thus, suppression of leakage current is essential in transformerless PV inverters and this aspect has received a lot of research attention in recent times. From the inverter side, this can be achieved by (i) Restructured topology which provides decoupling between the inverter AC side to the DC side during freewheeling period. Examples: HERIC and H5 topology [6]. (ii) Connecting neutral of the inverter to negative terminal of the DC source which creates short circuit for the common mode circuit of the inverter. Example: Neutral point clamped converter [7]. (iii) Employing an additional common mode choke to supress the oscillations [8]. (iv). Finally, a modified modulation scheme which can eliminates the oscillations due to inverter switching [9]. Traditionally two-stage systems were employed to interface PV and grid; wherein first a voltage boosting circuit was employed later inverter was employed to interface with grid. In the past, two-stage topologies [10], [11], [12], [14] have

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been suggested to circumvent this problem of leakage current. However, they still require an additional boosting stage to handle large input voltage variations which lower overall efficiency and increases control complexity.

Therefore, to address the above issues, Quasi Z-source inverters (qZSI) are extensively being researched for PV power systems, as they are capable of single-stage power conversion [15]. They have the potential to handle large variations in PV power, which is due to environmental conditions. Moreover, the lattice structure of the qZSI offers advantages such as low component rating and continuous input current compared to the Z-source inverter (ZSI) [16]. Its shoot-though capability does not only eliminate the issue of dead-time but also improves its anti-electromagnetic interference capabilities.

Topology-based solutions for single-phase transformerless ZSI and qZSI are suggested in [17], [18], [19], [20], which rearrange the switching devices to obtain the suppression of CMV. It has been suggested to connect two additional switching devices between the ac side and the negative rail of the dc side to suppress the variation of CMV in 1-ph qZS-based systems [17]. It has also been shown that decoupling of ac and dc sides in a ZS/qZS-based HERIC topology would result in a constant CMV. Freewheeling of grid current, as well as isolation of source and load sides, can be accomplished with additional switches, which are connected in parallel to the grid [18], [20]. An active power filter-based topology along with a modified modulation scheme is proposed for a 1-ph qZSI in, which is capable of reducing the CMV while eliminating the 2nd harmonic content in dc-link voltage [19]. Despite the availability of various ZS/qZS-based 1-ph solutions, that suppress leakage current and they provide only a 3-level output. Consequently, the output voltage has higher THD, EMI noise, and higher filter size. Although ZS/qZS-based multilevel inverters are available in the literature [21], [22], [23], [24], which achieves higher boosting [22], improved switching scheme [21], and high reliability [23], [24] the study for CMV and leakage current was not explored.

To overcome the aforementioned limitations, the authors selected an improved HERIC structure [12], [13]. The improved HERIC converter had attracted the industry and researchers' interest due to its higher efficiency in the family of single-phase three-level transformerless inverter topologies. A dual qZSI-based T-type structure is integrated into the improved HERIC structure to obtain the following merits:

a) Multilevel operation
b) Decoupling and clamping from the AC side to the mid-point of DC capacitors which guarantee the reduction in leakage current under various conditions of parasitic capacitance and grounding conditions
c) Bi-directional current path
d) Voltage gain
e) Enhance the shoot-through immunity

Therefore, a modified switching scheme with level-shift PWM (LSPWM) method is implemented to provide a five-level output with single-stage boosting. The proposed power converter is capable of sourcing reactive power in varying load conditions is an added advantage in the present scenario for grid-connected PV applications. Moreover, a detailed comparison is presented with the existing single-stage quasi-z-source-based inverters available in the literature to highlight the merit of the proposed configuration.

II. Proposed Topology and its Operation

A. Proposed Topology

A single-phase dual-qZS-T-type inverter with an improved HERIC structure is proposed in this paper. This converter outputs a five-level output voltage waveform and is applicable for photovoltaic applications. The proposed power converter appears as a continuous structure consisting of a dual qZS network and a T-type five-level inverter with an improved HERIC arm as shown in Fig. 1. The boosting network comprises two conventional qZS networks in a sequential manner, which are connected across the PV terminals. With the orientations of the qZS networks as shown in Fig. 1, it is possible to create a DC neutral point (the point 'O' in Fig. 1). Owing to the structural symmetry of the proposed topology, the neutral point 'O' is balanced naturally. The proposed topology is an amalgamation of a T-type arm, the HERIC structure, and a switch that helps in clamping the mid-point 'O'. Bidirectional switches (S_5, S_6), which constitute the T-type arm facilitate the generation of the voltage level $\pm V_{DC}/2$. Further, bidirectional switches (S_7, S_8) form the HERIC structure, which offers a freewheeling path for the grid current, while isolating the AC side and the DC side. In the improved HERIC structure, the switch S_9 is utilized to clamp the mid-point 'O' to the mid-point of the bidirectional switches (S_7, S_8) during this freewheeling period, which pushes the CMV to attain a value of zero. This topology uses a modified modulation scheme, which generates gating signals for driving the switches to obtain the suppression of CMV while synthesizing the five-level voltage waveform across the load. The working modes and the control structure are explained in the following sections.

B. Operating Modes

The operating modes of the inverter as shown in Fig. 2. These operating modes are broadly classified into 2 categories, namely the non-shoot-though modes and the shoot-through modes. The non-shoot-through mode consists of 5 states of which 4 states correspond to the active mode and the remaining state corresponds to the zero-mode. The shoot-though mode consists of 2 states namely, the Upper-Shoot-Through mode (UST) and the Lower-Shoot-Through mode (LST). Table I enumerates the voltage levels and the switching scheme to realize these levels along with the auxiliary information.

As stated earlier, the implementation of shoot-though modes (UST and the LST) is pivotal to the attainment of the required voltage boosting. In this context, the UST mode is employed to realize the objective of voltage boosting during the positive half cycle using the top-qZS. Similarly, the LST mode is applied during the negative half-cycle of the output voltage to short-circuit the bottom qZS. The non-shoot through zero-vector mode, which is shown in Fig. 2(g), clamps the mid-point 'O' to the junction of the bidirectional switches while forcing the CMV to zero. Also, this mode offers an additional advantage

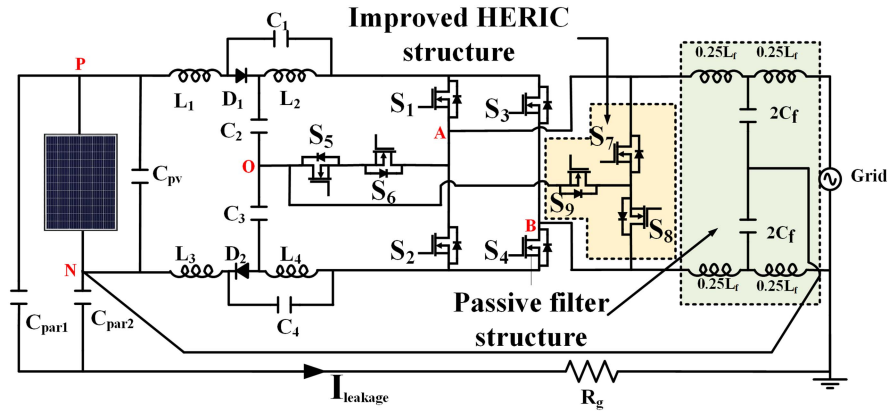

Fig. 1. Circuit diagram of proposed qZS based improved HERIC topology.

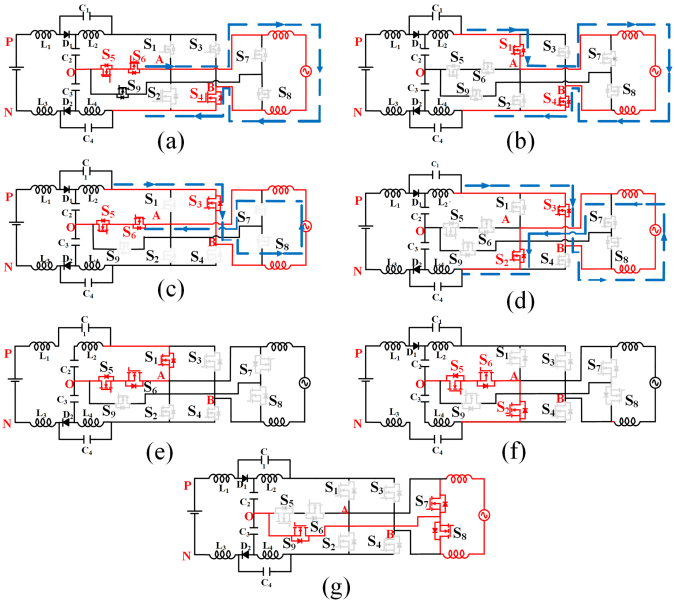

Fig. 2. Modes of operation of the proposed inverter that include active states ((a)–(d)), shoot-through states ((e)–(f)), and the zero-state (g).

TABLE I
SWITCHING TABLE

Voltage level obtained	Turned-on Switches	Nature of the switching state	Reference to figure
+V_{DC}/2	S_4, S_5 and S_6	Active, Non-shoot-through	2(a)
+V_{DC}	S_1 and S_4	Active, Non-shoot-through	2(b)
-V_{DC}/2	S_3, S_5 and S_6	Active, Non-shoot-through	2(c)
-V_{DC}	S_2 and S_3	Active, Non-shoot-through	2(d)
0	S_1, S_5 and S_6	Upper Shoot-through	2(e)
0	S_2, S_5 and S_6	Lower shoot-through	2(f)
0	S_7, S_8 and S_9	Zero-state	2(g)

of improving the reliability of the converter, as it facilitates the freewheeling of the grid current without utilizing the level-generating switching devices.

Modulation index (m) is defined as the ratio of the amplitudes of the carrier wave and the modulating (reference) wave; it determines the amplitude of the fundamental component of the output voltage. Condition to apply the shoot though-duty (D_S) is related to the peak modulation index (m) by:

$$D_S + m \leq 1 \tag{1}$$

Applying volt-sec balance to the inductors over one switching cycle, the boost factor and various capacitor voltage values are obtained which are as follows:

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{(2 - 4D_S)} \tag{2}$$

$$V_{C2} = V_{C3} = \frac{(1 - D_S)\, V_{IN}}{(2 - 4D_S)} \tag{3}$$

$$B = \frac{\hat{V}_{DC}}{V_{IN}} = \frac{1}{1 - 2D_S} \tag{4}$$

$$V_{\text{out}} = mBV_{\text{in}} \tag{5}$$

In (4) and (5), The boost factor is represented by the symbol 'B' which is identical to the conventional qZS system. The terms V_{IN} and V_{DC} respectively denote the input voltage to the converter (PV source in the present case) and the peak value of dc-link voltage. Similarly, the average capacitor voltages for the qZS system are represented by the terms $V_{C1}, V_{C2}, V_{C3}, V_{C4}$. The peak dc-link voltage output by the dual-qZS is obtained by adding up the average voltages across all four capacitors ($V_{C1}, V_{C2}, V_{C3}, V_{C4}$):

$$\hat{V}_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{6}$$

C. Modified Modulation Scheme

The Level-Shifted PWM (LSPWM) scheme is deployed in this work for the generation of gating signals to drive the switching devices of the proposed power converter. Four level-shifted carrier waveforms (Fig. 3(a)) are compared with a sinusoidal modulating signal to produce the signals *A-D*. Two DC references are compared with the upper as well as the lower triangular carrier waves and are combined through an 'OR' gate to produce the shoot-through pulse trains *ST*. Also, the signal '*G*' is obtained when the modulating wave is compared with a value of zero. By processing these signals through the combinational logic

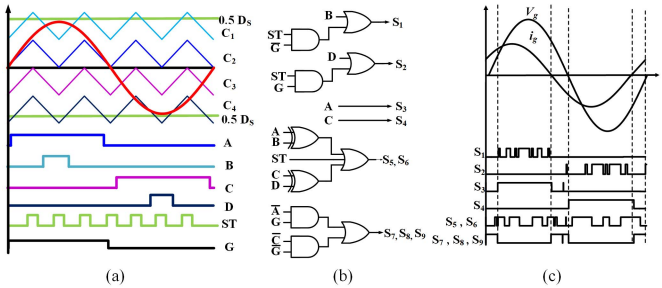

Fig. 3. Modified PWM Scheme implementation; (a) LSPWM scheme and corresponding signals. (b) The logic for the generation of switching signals for S_1-S_8. (c) Switching signals during reactive loads.

scheme, shown in Fig. 3(b), the gating signals are generated for all of the switching devices. Fig. 3(c) shows the gating signals generated when the load is reactive. It may be noted from Fig. 3(c) that, during negative output power, the modulation scheme provides the free-wheeling path by activating the switches S_7, S_8, and S_9.

III. Design of Passive Components

A. qZS Passive Components Calculation

From Fig. 1, it is evident that the proposed converter requires 8 passive components, *viz.* four inductors, and four capacitors. Due to the symmetrical nature of the top and bottom qZS networks, it is obvious the parametric values of all inductors (L_1-L_4) and capacitors (C_1, C_4, and C_2, C_3) should be the same. The values of these components can be found using two parameters: operating frequency and ripple content. Assuming a lossless system, the input power (P_{IN}) and output power (P_{OUT}) are equal, i.e.,:

$$P_{IN} = P_{OUT} = 500\,\text{W} \tag{7}$$

and,

$$I_{IN} = \frac{P_{OUT}}{V_{IN}} = \frac{500}{100} = 5\,\text{A} \tag{8}$$

In (8), I_{IN} denotes the average input current, which is the same as the average current flowing through the inductor L_1 ($I_{IN} = I_{L1}$). The ripple in the inductor current is primarily due to the employment of the shoot-through (ST) and the non-shoot-through (NST) modes of operation in a switching cycle. The ripple content in the inductor current can be found by:

$$\Delta I_{L1} = \int_0^{TD_s} \frac{dI_{L1}}{dt}\,dt = \frac{V_{IN}+V_{C1}}{2L}\,TD_S = \left(\frac{1-D_s}{1-2D_s}\right)\frac{V_{in}TD_s}{2L} \tag{9}$$

wherefrom the minimum value of the inductor current to obtain the continuous conduction mode (CCM) is given by:

$$L = \frac{V_O^2\,(1-2D_S)\,TD_S}{2\,(1-D_S)\,K_L P_{OUT}} \tag{10}$$

where the term K_L represents the allowable ripple content through the inductor and V_O is the output voltage.

Similarly, the values of the outer capacitors (C_1, C_4) and the inner capacitors (C_2, C_3) are calculated as:

$$\Delta V_{C1} = \frac{1}{C_1}\int_0^{TD_s} i_C dt = \frac{1}{C_1}\int_0^{TD_s} i_L dt = \frac{1}{C_1} I_{in} TD_s$$

Substituting (2)–(7) we get:

$$C_1 = C_4 = \frac{TP_{OUT}(1-D_S)^2}{4k_{C1}V_O^2\,(1-2D_S)} \tag{11}$$

$$C_2 = C_3 = \frac{TP_O\,(1-D_S)\,D_S}{4k_{C2}V_O^2\,(1-2D_S)} \tag{12}$$

Where K_{C1} and K_{C2} respectively denote the allowable ripple content in these capacitors.

B. Input Filter Calculations

It is a well-known fact that 1-Ph inverters cause a ripple in the source current. This ripple corresponds to a frequency that is twice that of the output frequency. In conventional 1-Ph inverters, a capacitor, which is provided at the dc input terminals facilitates the circulation of this ripple current by providing a path of low impedance to it. Generally, a PV source is also equipped with such a capacitor to circulate the ripple current. The value of this capacitor (denoted as C_{PV}) is given by:

$$C_{PV} = \frac{P_{PV}}{2\omega_g V_{PV}\Delta V_{PV}} \tag{13}$$

Where P_{PV} is the power rating of the PV panel, ΔV_{PV} is the allowable ripple content in the PV voltage and ω_g is the fundamental value of the grid frequency.

C. Output Filter Calculations

The primary function of the output filter (Fig. 1) is to eliminate the harmonics from the output voltage (V_{AB}). The ST and the NST modes cause high-frequency transitions in the V_{AB} as well as the CMV. The modulation scheme explained in the earlier section, clamps the CMV to a value of zero during the zero period. However, CMV still contains high-frequency transitions due to the ST mode of operation. The output filter, apart from providing a purely sinusoidal output voltage, is instrumental in attenuating the high-frequency transition across the parasitic capacitor (which is the root cause of leakage current). As seen in Fig. 1 the filter structure is a modified form of the conventional LC filter, wherein the filter inductor is split into 4 parts. Similarly, the filter capacitor is split into two halves with their mid-point connected to the point 'N'. The lumped value of the LC-filter is given by:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{14}$$

IV. Control Structure

As discussed above, the proposed configuration is tested for two different modes such as standalone and grid-connected operations. Fig. 4(a) shows the detailed schematic diagram of the control system, which is used in the standalone mode. This

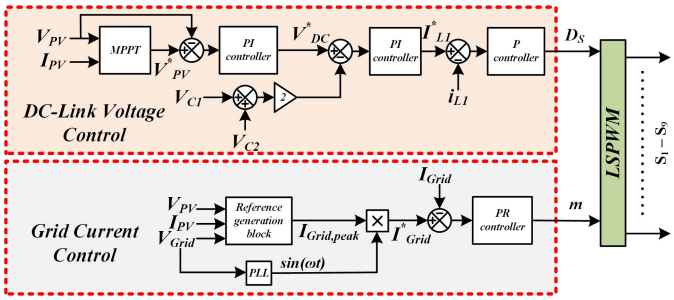

Fig. 4. Control schematic for the proposed power converter. (a) DC link control, (b) grid current control.

control system employs a two-loop control structure to obtain a fast dynamic response. It monitors the dc-link voltage with its outer loop, while the inner current loop controls the inductor current (i_{L1}). The regulation of the dc-link voltage ($\hat{V}_{DC}$) is achieved by adjusting the ST duty ratio (D_s). For the proposed PV converter, the MPPT is obtained with the well-known perturb and observe (P&O) method. Based on the voltage (V_{PV}) and current (I_{PV}) of the PV panels, the MPPT algorithm provides the reference (required) value of the input voltage V^*_{PV}.

The error between the required and the actual values of the input voltage is compensated by a PI controller, which outputs the reference value for the peak dc-link voltage (V^*_{DC}). This reference is then compared with the dc-link voltage ($\hat{V}_{DC}$), which is measured by exploiting the symmetrical nature of the qZS networks (Fig. 1).

Exploiting the symmetrical nature of the qZS networks, (6) becomes:

$$\hat{V}_{DC} = 2\,(V_{C1} + V_{C2}) \tag{15}$$

The measured and the reference values of the peak dc-link voltages are then compared and their difference is compensated with the aid of another PI controller. The output of this PI controller provides the reference value of the input current i^*_{L1}. The error between the reference and actual values of the input current (i.e. $i^*_{L1} - i_{L1}$) is compensated by a Proportional (P) controller, which outputs the signal that controls the ST duty ratio (D_s). It should be noted that the dc-link voltage is affected by both source and load disturbances. As the modulation index is held constant, the regulation of the dc-link voltage paves the way to the regulation of the output voltage as well.

In the grid-connected mode of operation, both the ST duty ratio and the modulation index are controlled. Thus, the controller shown in Fig. 4(a) is augmented with the one shown in Fig. 4(b), which determines the modulation index. Apart from the regulation of the dc-link voltage, this control system tries to inject active power into the grid at UPF. These objectives are fulfilled by processing the PV voltage (VPV), PV current (IPV), and the grid voltage (Vg) with a reference *generation block* that generates the reference signal for the peak value of the grid current (denoted as $I_{grid,peak}$ in Fig. 4(b)), which is given by:

$$I_{Grid,peak} = \frac{\sqrt{2}\,V_{PV} I_{PV}}{V_{grid}} \tag{16}$$

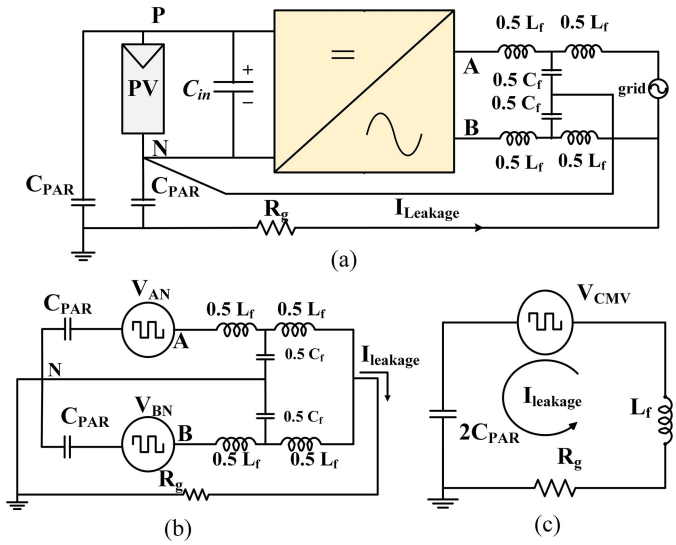

Fig. 5. Representation of circuit with parasitic elements; (a) entire system with parasitic elements. (b) Equivalent circuit of the proposed converter in terms of terminal voltage V_{AN} and V_{BN}. (c) Common mode equivalent circuit.

The reference value of the peak grid current is then multiplied with a unit-sine wave, which is synchronized to the mains by using a PLL. This signal serves as the instantaneous reference waveform for the grid current. The error between the instantaneous reference and the actual grid currents is then compensated with a PR controller, which outputs a signal that determines the modulation index (m). This modulation signal is employed to generate the gating signals as described in the earlier section.

V. CMV Analysis

The leakage current that flows between PV panels and load is mainly due to the CMV and interaction between various components such as junction capacitance of power semiconductor switching devices, parasitic elements of the filter, parasitic elements in the leakage path, and passive components of the quasi-Z-sources [28] (Fig. 5(a)). The CMV of the proposed power converter (Fig. 1) is given by:

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} \tag{17}$$

The terms V_{AN}, $V_{BN,}$ and V_{CMV} can be represented in terms of the switching functions by

$$V_{AN} = [0.5\,\{S_3S_5S_6\} + \{S_1S_3\} + 0.5]\,V_{DC} \tag{18}$$

$$V_{BN} = [0.5\,\{S_4S_5S_6\} + \{S_2S_4\} + 0.5]\,V_{DC} \tag{19}$$

$$V_{CMV} = 0.25\,V_{DC}\,[\{S_5S_6S_3\} + 2\{\,S_1S_3\} + \{S_5S_6S_4\} + 2\{\,S_2S_4\} + 2] \tag{20}$$

The equivalent circuit of the proposed converter w.r.t the sources V_{AN} and V_{BN} is shown in Fig 5(b), from which it is evident that the leakage current is caused by the potential difference between point A and B w.r.t the point N Fig. 5(c)

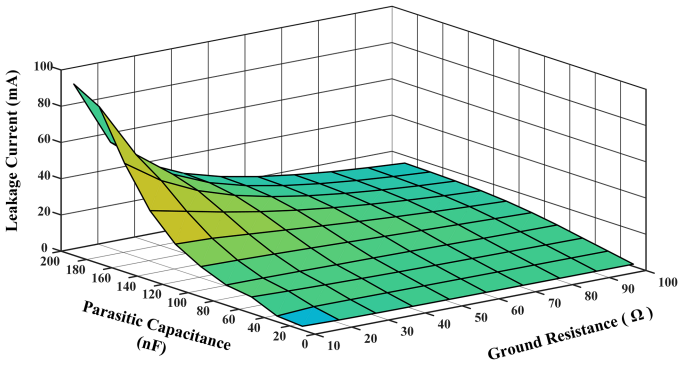

Fig. 6. Variance of the leakage current with respect to the parasitic capacitance and ground resistance.

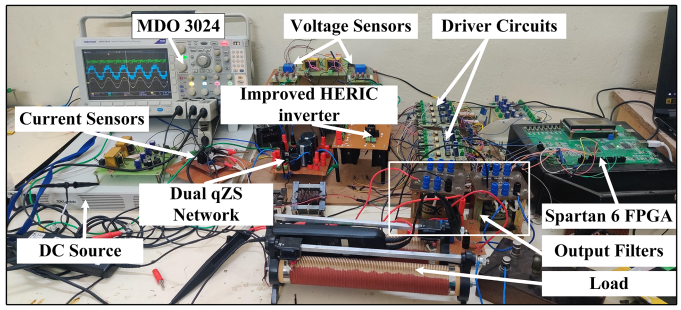

Fig. 7. Experimental prototype of the proposed converter.

TABLE II
PARAMETERS USED FOR SIMULATION AND EXPERIMENT

Parameters		Values
P_O		500 W
V_{in}		100 V
V_{out} (rms)		110 V
Inductors	L_1 - L_4	1 mH
	L_f	4 mH
Capacitors	C_1-C_4	1000 µF
	C_f	2 µF
	C_{PAR1}, C_{PAR2}	100 nF
Frequency	F_s, f_o	10 kHz, 50 Hz
R_g		10 Ω

shows the common-mode equivalent circuit which shows that the common-mode voltage (V_{CMV}) causes the leakage current.

The magnitude of the leakage current is principally determined by the values of the ground resistance (R_g) and the parasitic capacitance (C_{PAR}). From Fig. 5(c) the leakage current (i_{LEAK}) is given by

$$i_{LEAK} = C_{PAR}\frac{dV_{PAR}}{dt} + \frac{V_{CMV}}{R_g} \tag{21}$$

where V_{PAR} represents the voltage across the parasitic capacitance. From (21), it is evident that the leakage current is directly proportional to the value of the parasitic capacitance (C_{PAR}) and is inversely proportional to the ground resistance (R_g). As stated earlier, the value of the parasitic capacitance varies in the range of (7 nF–220 nF) /kW depending upon numerous factors such as the type of panels, distance between frame and ground, weather, and aging conditions.

Fig. 6 shows the relationship between the estimated leakage current for the proposed converter w.r.t the values of C_{PAR} and R_g, assuming that the average value of CMV is 50 V. This plot reveals that the leakage current is reduced at low values of parasitic capacitance and high values of ground impedance.

VI. RESULTS AND DISCUSSION

The performance of the proposed power converter is assessed with simulation studies using the MATLAB/Simulink platform. Table II provides the values of various components, which are used for both simulation studies and experimental verification. An input PV voltage (V_{in}) of 100 V, output voltage ($V_{o,rms}$) of 110 V (RMS) and modulation index (m) of 0.7 are employed in both simulation and experimentation. With the selected ST duty ratio of 0.27, a boost factor of 2.2 is achieved (4) and (5). Fig. 7 shows the picture of the 500 W laboratory prototype, which is developed to validate the simulation studies. The prototype is built with power MOSFETs (IRFP460) and fast recovery diodes (MURS1560). The proposed modulation scheme is implemented with the Spartan 6 FPGA digital control platform.

Fig. 8 shows the steady-state performance of the converter in the standalone mode. This figure shows the plots of dc-link voltage, the output voltage of the inverter, filtered output voltage, and the load current respectively which clearly demonstrates the voltage boosting capability of the qZS network by a factor of 2.2 (100 V to 220 V). The output of the inverter clearly shows the five voltage levels ($\pm V_{DC}/2, \pm V_{DC}$ and zero, Fig. 2). Fig. 8(c) and (d) shows the FFT spectrum of both simulation and experimental results. The waveforms pertaining to common mode parameters can be seen in Fig. 9. The first and second traces of this figure respectively present the terminal voltages V_{AN} and V_{BN}. The CMV (third trace) is shown in the figure (both simulation and experiment), which is calculated using (17). It can be observed that the shoot-through period, introduced in the zero-period of *every switching cycle*, contributes to the high-frequency transitions present in CMV.

As stated earlier, the combined effort of the modulation scheme and the output filter suppresses these high-frequency transitions. Consequently, the voltage across the parasitic capacitor (V_{PAR}), (trapezoidal waveform lacks sudden spikes) is rid of high-frequency transitions. This causes a reduced leakage current, which is shown in the bottom trace of Fig. 9. The measured RMS value of this current is 15 mA, which is significantly lower than 300 mA, which is the stipulated value as per the German standard *VDE 0126-1-1*.

Apart from reducing the leakage current, the modulation scheme achieves the capability of supporting the reactive power, which is demonstrated in Fig. 10. As shown in Fig. 2(g), the modified PWM scheme turns on the switches S_7 and S_8 during the zero-state, providing a path for the circulation of the load current, which manifests as the reactive power supporting capability of the converter. This experiment clearly shows that

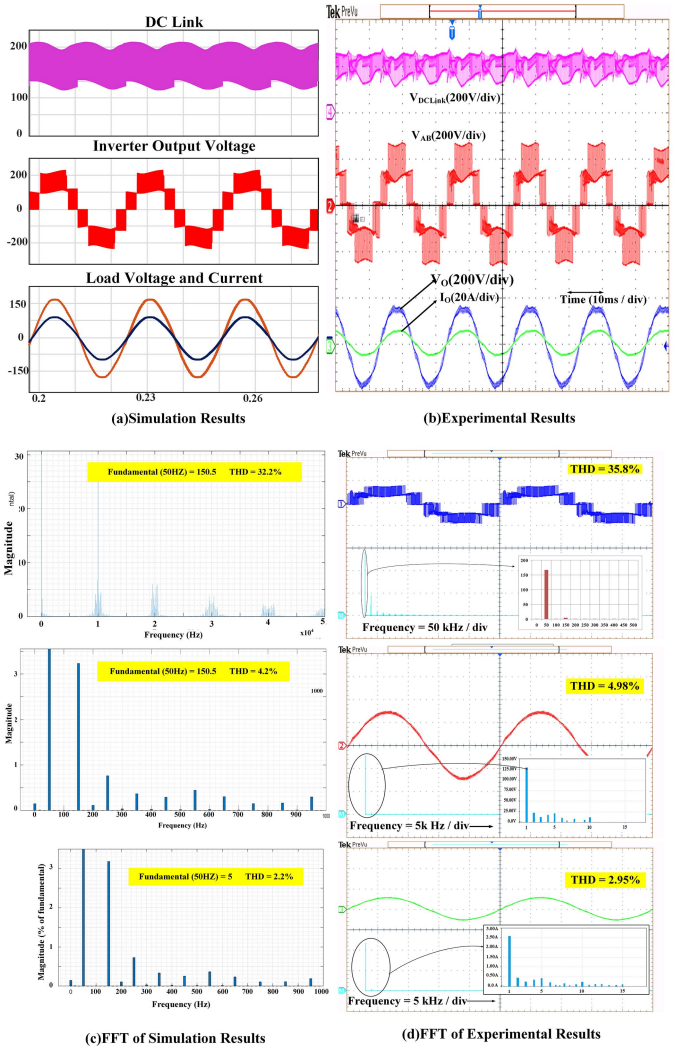

Fig. 8. (a) Simulation and (b) experimental waveform of the proposed converter in steady state showing DC-link voltage, level voltage, output voltage and output current. (c) And (d) shows the FFT results.

the proposed power converter comfortably negotiates a sudden changeover from an initial UPF load to a 0.9 PF (lagging) load.

The control scheme shown in Fig. 4(a) readjusts the ST duty ratio to restore the dc-link voltage. This experimental result clearly demonstrates the capability of the controller to regulate the dc-link voltage against source disturbances (90 V to 105 V and vice versa, Fig. 11) and the load disturbance (2.5 A–4 A, Fig. 12).

Fig. 13 shows the behaviour of the proposed system for grid-tied applications. As stated earlier, the controller (shown in Fig. 4(a) and (b)) regulates both the ST duty factor and the modulation index in this operating mode while realizing UPF. Results presented on the right side of Fig. 13 show the performance of the proposed power converter during the grid-tied mode of operation, which is assessed using the real-time simulator Opal-RT (OP4510) [25].

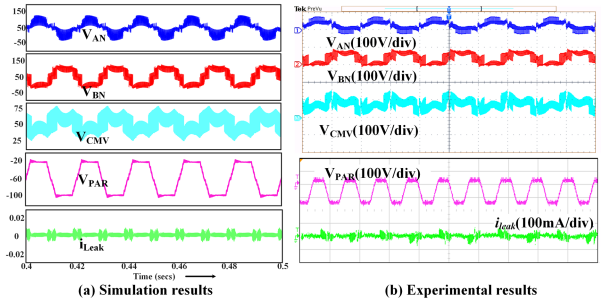

Fig. 9. Results of common mode parameters. (a) Simulation and (b) experimental waveform of V_{AN}, V_{BN}, and V_{CMV}, voltage across parasitic capacitor (V_{PAR}) and leakage current ($i_{Leakage}$) respectively (*from top to bottom*).

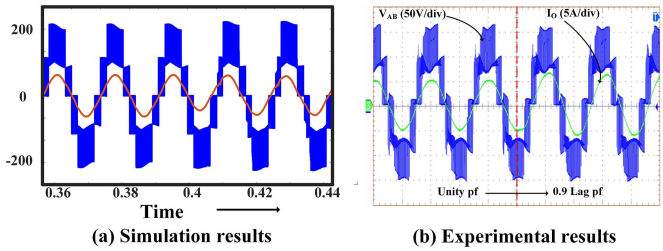

Fig. 10. Simulation and experimental results for reactive power capability from unity pf to 0.9pf lag.

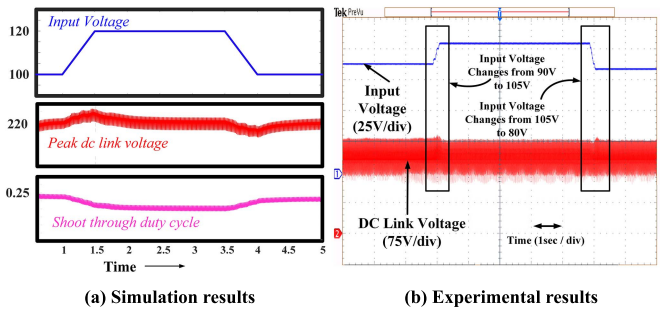

Fig. 11. Results for dynamic performance of converter subjected to input voltage change (a) simulation and (b) experimental.

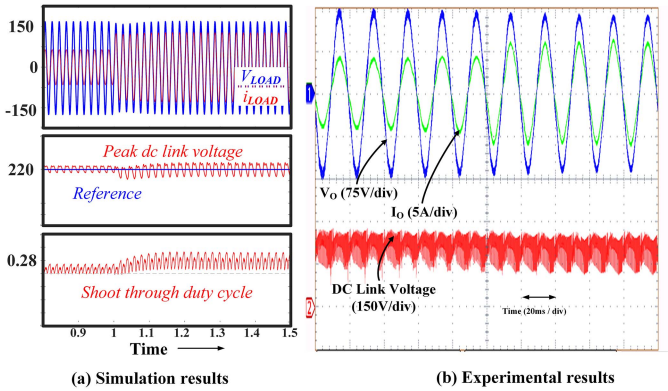

Fig. 12. (a) Simulation and (b) experimental waveform for dynamic response of the system for load changes from 2.5 A to 4 A.

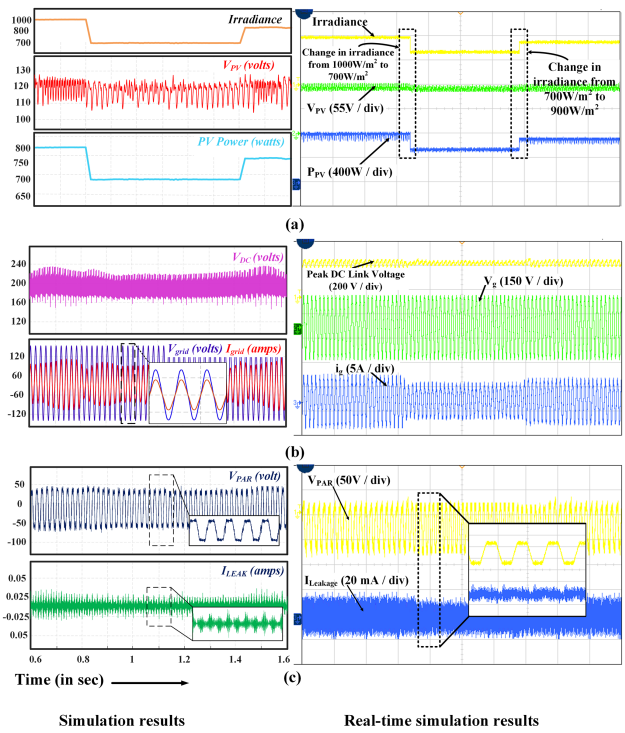

Fig. 13. Simulation and real-time simulation results during the grid-tied mode. (a) Solar irradiance, PV voltage, and PV power. (b) Peak dc-link voltage, grid voltage, and grid current. (c) The voltage across PV parasitic capacitor and leakage current.

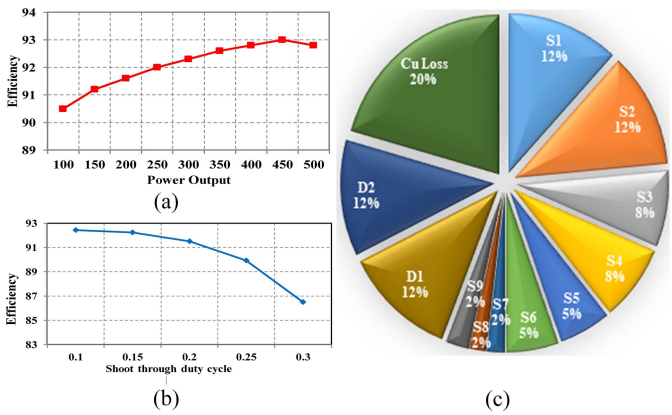

Fig. 14. Efficiency curves of the proposed converter. (a) Power output vs. efficiency curve. (b) ST duty ratio vs. efficiency curve. (c) Loss distribution chart.

In this study, the irradiance is changed; firstly from 1000 W/m^2 to 700 W/m^2, and then to 900 W/m^2 (top trace, Fig. 13(a)). Following the first change, a drop occurs in the PV power (bottom trace) with an associated drop in the PV voltage (second trace). However, the MPPT algorithm restores the PV voltage to its original value. The corresponding changes of this disturbance in the output (peak dc-link voltage, grid voltage, and grid current) are shown in Fig. 13(b). Due to the change in the PV power, a slight disturbance appears across the dc-link voltage (top-trace of Fig. 13(b)), which is eventually regulated by the controller (Fig 4(a)). The fluctuations in the irradiance (and therefore the PV power) cause the corresponding fluctuations in the grid current as shown in the bottom trace of Fig. 13(b). However, the controller (Fig. 4(b)) ensures that the power converter injects active power into the grid at UPF, despite disturbances in irradiance.

The waveforms pertaining to the leakage current and the voltage across the parasitic capacitor (V_{PAR}) in the grid-tied operation are shown in Fig. 13(c). It is observed that the RMS value of the leakage current in the grid-tied operation is 15mA, which is very much lower than the value stipulated by the *VDE-0126-1-1*. These experimental and real-time simulation results (Figs. 8–13) adequately validate the simulation results, for the proposed power converter.

VII. Efficiency and Loss Analysis

Efficiency curves of the proposed converter at various values of output power and ST duty factors are provided in Fig. 14. Fig. 14(a) shows the efficiency obtained with the PSIM simulator, which is capable of importing actual characteristics of various active devices and passive components to the power converter that is simulated [26]. It may be noted that the proposed converter obtains a maximum efficiency of 93% at an output power of 400 W (app.). Fig. 14(b) shows the dependence of efficiency on the ST duty ratio. This plot shows that the efficiency decreases when the ST duty ratio is increased. This phenomenon is attributed to the increased conduction loss in the ST devices (S_1, S_2, S_5, and S_6) and the qZS inductors.

Fig. 14(c) presents the loss distribution chart, which shows the percentage division of power loss in various active and passive elements. The copper loss incurred in the inductors is about 21% while the losses in diodes (D_1 and D_2) sum up to 24% of the total loss. Out of the nine-power semiconductor switching devices, most of the loss occurs in 6 switches (S_1-S_6) while the other three switches (S_7-S_9) incur relatively lower power loss. Though the proposed topology uses one more switching device compared to most of the other topologies reported in the literature, the incurrence of negligible power loss in 3 switches offsets this drawback.

VIII. Comparison With Existing Topologies

Table III presents the comparison of various factors like total component count, number of DC sources, total blocking voltage, maximum conducting switches in a cycle, and various stresses amongst the components of the existing single phase five-level inverters. Due to the symmetrical structure of the proposed inverter, the total number of inductors and capacitors is the same as in the case of most existing five-level topologies in literature except [22]. Although [22] has the lowest number of inductors amongst the known topologies, it incurs a higher number of losses as it uses a higher number of switches. From Table III, it can be observed that topologies like [23], and [24] use a higher number of input PV sources, which have the demerit of strengthening the parasitic capacitance and decreasing the overall reliability of the system. Due to the higher count of power semiconductor devices, the proposed topology suffers from a higher total blocking voltage (TBV) which can be defined as the

TABLE III
COMPARISON OF PROPOSED TOPOLOGY WITH EXISTING FIVE-LEVEL TOPOLOGIES

Type of converter	Components count				Total Blocking Voltage	Sources required	Maximum conducting switches	Reactive power support	Leakage current	Switch stress	Capacitor stress	Diode stress
	S	D	L	C								
[21]	8	6	4	4	$6*V_{DC}$	1	4	No	NA	$\frac{1}{\sqrt{2}(1-D)}$	$\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2}(1-D)}$
[22]	8	3	2	4	$6*V_{DC}$	1	4	No	NA	$\frac{1}{\sqrt{2}(1-D)}, \frac{\sqrt{2}}{(1-D)}$	$\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2}(1-D)}$
[23]	8	2	4	4	$4*V_{DC}$	2	4	No	NA	$\frac{1}{\sqrt{2}(1-D)}$	$\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2}(1-D)}$
[24]	8	2	4	4	$6*V_{DC}$	2	3	No	NA	$\frac{1}{\sqrt{2}(1-D)}, \frac{\sqrt{2}}{(1-D)}$	$\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2}(1-D)}$
[29]	12	0	0	4	$6*V_{DC}$	1	6	Yes	Low	0.25,1	0.5, 0.25	--
[30]	6	2	4	4	$5*V_{DC}$	1	4	Yes	Low	$\frac{1}{\sqrt{2}(1-D)}, \frac{\sqrt{2}}{(1-D)}$	$\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2}(1-D)}$
[31]	6	1	0	3	$5.5*V_{DC}$	1	3	Yes	Zero	0.5, 1	0.5, 1	1
[32]	8	0	0	2	$7*V_{DC}$	1	3	Yes	Low	0.5, 1	0.5	--
Proposed	9	2	4	4	$7.5*V_{DC}$	1	3	Yes	Low	$\frac{1}{\sqrt{2}(1-D)}, \frac{\sqrt{2}}{(1-D)}$	$\frac{1}{\sqrt{2}}, \frac{1}{\sqrt{2}}\frac{D}{1-D}$	$\frac{1}{\sqrt{2}(1-D)}$

S=Switch, D=Diode, L=Inductor, C=Capacitor

TABLE IV
COMPARISON WITH EXISTING QZS BASED TLI

Type of converter	Maximum conducting switches	Reactive power support	Leakage current	Strategy utilized
[17]	3	Yes	Low	CMV clamping
[18]	5	Yes	Low	AC based decoupling
[19]	4	Yes	Low	Modulation strategy based
[20]	6	Yes	Low	AC based decoupling
proposed	3	Yes	Low	AC based decoupling + CMV clamping

sum of the voltages blocked by individual switches. It can be observed that [29] proposed an interesting topology that clamps the CMV to $0.5V_{dc}$ but has higher number of power semiconductor devices amongst the compared topology. A similar voltage boost and reduced leakage current is achieved by [30] on the cost of higher conducting devices. Leakage current is completely eliminated by [31] by employing minimum number of switches but the flying capacitor makes the system more complex than the proposed topology. Although [32] achieves a low leakage current employing 8 devices, this system still needs a larger input voltage to feed the grid. However, the proposed qZS-based five-level inverter proves to be more efficient and reliable due to the lower number of conducting switches to provide the necessary operation while providing reactive power support which is an essential condition for grid-connected transformerless inverters.

According to IEEE's grid code, the RMS value of the leakage current is considered low when it is less than 120 mA; it is assumed to be very low when a value is below 10 mA [27]. The comparison of the proposed topology with the existing qZS-based inverters [17], [18], [19], [20], which result in a reduced leakage current is shown in Table IV. It can be seen that the proposed qZS inverter utilizes the lowest number of power semiconductor devices to produce a higher voltage level than the reported solutions. Thus, the employed strategy namely, the *AC-based decoupling and CMV clamping* makes the proposed qZS inverter suitable for PV-based grid-connected systems.

IX. CONCLUSION

This paper introduces a new dual-quasi-Z-source-based T-type five-level inverter with an improved HERIC structure for PV applications. The proposed configuration results in the following benefits: (i) freewheeling of load current is accomplished without the aid of the level generating switches (ii) isolation of AC and DC sides and, (iii) achieving a CMV of zero by clamping the neutral point during the zero-state. The proposed modulation scheme achieves the twin objectives of deriving a five-level boosted output and reactive power capability. Moreover, the proposed modified filter structure attenuates high-frequency transitions in CMV and keeps the leakage current well below the standards specified by *VDE 0126-1-1*. In addition, the dynamic response of the proposed configuration is verified extensively through simulation and experimentation. Furthermore, the proposed converter is compared with various qZS-based five-level inverter topologies in terms of the number of active switches and passive components, voltage stresses, and the TVB. This comparison reveals that the proposed converter incurs the lowest power loss. With these features and advantages, it is envisaged that the proposed single-stage power converter could be useful for PV generation.

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