A Quasi-Switched Capacitor Based Grid-Connected PV Inverter With Minimum Leakage Current

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***Abstract*— This article proposes a single-stage quasi-switched capacitor based five-level inverter (qSB-5LI) for photovoltaic (PV) systems. The proposed topology comprises dual quasi-Z-source (qZS) networks and switched capacitor based five-level inverter with a single PV source. A modified modulation technique based on level-shifted PWM (LSPWM) is implemented to achieve voltage boosting and five-level inversion. Furthermore, the proposed topology achieves a higher boost factor in comparison to the existing qZS-fed five-level topologies in the literature. The steady-state and dynamic performances of the qSB-5LI with closed-loop control schemes in both stand-alone mode and grid-connection mode of operation are demonstrated. In addition, the proposed topology results in a reduced leakage current complying with the VDE0126-1-1 standard. Moreover, the proposed topology eliminates the requirement of any external LCL filter to reduce the leakage current. The principle of the power converter is verified with an experimental prototype in both stand-alone and grid-connection modes of operation.**

***Index Terms*— Leakage current, level-shifted PWM (LSPWM), quasi-switched boost (qSB) inverter, voltage boosting.**

I. Introduction

IN RECENT years, photovoltaic (PV) power has graduated to the level of being an alternative to fossil-fuel-based power generation. Lack of pollution declined the costs of PV panels, and lower maintenance requirements contributed to this advancement. Generally, solar PV systems are interfaced with the load/grid via a power converter to meet the requirement of ever-increasing power demand. In general, the power converter is a two-stage system wherein the input PV voltage is boosted to the required dc voltage using a dc–dc converter and is then inverted to ac using a dc–ac converter. However, the main shortcoming of the two-stage conversion is the increased switching resources, cost, and decrease in efficiency [1]. In this context, quasi-Z-source (qZS)-based inverters drew the focus of researchers because of their capability of single-stage power conversion [2]. Furthermore, qZS power converters accomplish dc–ac inversion with lower cost, reduced switch count, and higher efficiency [3] and [4].

Owing to lower switching voltage stress, superior harmonic performance, and lower filter size, multilevel inverters (MLIs) are increasingly used in renewable applications [5], [6]. As conventional voltage source inverters (VSIs) are essentially buck-type converters, separate boost converters are required to boost low PV voltage to obtain the desired ac output voltage. This disadvantage is minimized by the amalgamation of qZS networks with MLI to obtain single-stage operation.

Initially, investigations are carried out on conventional MLI topologies, namely: 1) neutral point clamped (NPC) and 2) cascaded H-bridge (CHB) inverters. In [7], a qZS-fed NPC inverter is proposed that combines a three-level NPC inverter with two qZS networks. Even though this topology achieves single-stage operation, it is plagued with drawbacks such as: 1) neutral point deviation and 2) additional clamping diodes [8], [9]. Each isolated PV source is interfaced with the qZS network in qZS-based CHB topologies [10], [11], [12] to obtain the necessary voltage boosting. Therefore, the number of qZS networks increases with an increase in isolated sources. This increases the passive device count and further increases the complexity of control with respect to dc-link voltage regulation and MPPT control [13].

Further topological modifications are brought into the qZS-based CHB inverter to reduce the passive device count. In [14], a quasi-switched boost MLI is proposed wherein one capacitor and one inductor in each qZS network are reduced. However, to obtain the required voltage-boosting capability, two additional switches and diodes are required. This increases the switching losses of the power converter. In the power converter configurations described in [7], [8], [9], [10], [11], [12], [13], and [14], the shoot-through (ST) is implemented only in the zero-states of the switching cycle thereby limiting the practical boost factor in qZS inverters. A modified qZS-based MLI is proposed in [15], which derives a higher boost factor when compared with other qZS-NPC and qZS-CHB topologies. Furthermore, the power converter [15] uses two inductors with only one PV source to synthesize a five-level waveform. To obtain a higher boost factor, this converter is operated with a discontinuous input current which does not bode well with PV applications. Moreover, this topology results in higher voltage stress across the switches and current stress in the inductors when compared with qZS-NPC and qZS-CHB topologies. A dual qZS-based five-level inverter is proposed in [16], which is a combination of a T-type and an NPC inverter. This power converter uses eight semiconductor devices and additional freewheeling diodes to produce a five-level output voltage. When compared with the power converter described in [15], the dual qZS-based five-level inverter results in less voltage stress across the switching devices. However, the power converter [16] produces zero

Manuscript received 17 April 2023; revised 3 July 2023 and 24 July 2023; accepted 31 August 2023. Date of publication 11 September 2023; date of current version 1 December 2023. Recommended for publication by Associate Editor Jeehoon Jung. *(Corresponding author: P. Manoj.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JESTPE.2023.3313625.

Digital Object Identifier 10.1109/JESTPE.2023.3313625

switched five-level output voltage which results in a voltage waveform with a higher THD.

In transformerless PV inverters, one of the major issues is the flow of leakage current from the PV panel to the grid. This leakage current is the result of the high-frequency voltage variations across the stray capacitance formed due to the grounded frame of the PV panel. The high-frequency voltage variations arise owing to the common-mode voltage (CMV) of the MLI. In qZS inverters, the ST state is inserted in every zero-state of the switching cycle to boost the low-voltage PV source. These ST states create additional high-frequency voltage variations across the stray capacitance, further increasing the leakage current. The safety standard VDE0126-1-1 [17] specifies that the leakage current should be restricted to less than 300 mA.

To minimize the leakage current, a few modulation techniques and topological modifications are suggested for qZS inverters. In single-phase qZS inverters, the CMV is minimized by selecting appropriate zero switching states which minimize the high-frequency transitions [18]. In the power converter stated in [19], two extra switches are used to interface the grid to the negative dc bus of the PV panel. Owing to this, the parasitic voltage is clamped to either zero or grid voltage thereby reducing leakage current. Moreover, the topology presented in [20] decouples the grid from the power converter in the zero-state using two extra switches and diodes. This results in minimizing the voltage transitions across the parasitic capacitor. However, these strategies for minimizing leakage current are effective only for the two-level qZS inverters [18], [19], [20]. Furthermore, a qZS-based 5LI reported in [16] uses an additional LCL filter to reduce leakage current. However, the extra passive components incur additional power loss decreasing the efficiency.

Other prominent power converters used for voltage boosting when compared with qZS inverters are switched capacitor based MLIs. The SC-based MLI topologies display advantages such as voltage boosting capability, higher voltage levels, and low requirement of switching resources. Research on SC-based MLI is primarily focused on single-phase topologies using cascading switched capacitor dc–dc converters and an H-bridge inverter [21], [22]. Other SC topologies use two half-bridge inverters to provide inverting ac polarity [23], [24]. However, SC-based MLIs exhibit a major drawback of high inrush charging current of the capacitor, which increases the switching losses of the power converter and may even damage the devices. Furthermore, the boosting capability of the SC-MLI is entirely dependent on SC networks, and therefore, the voltage gain is mostly constant and cannot be varied in a larger range by controlling the switching devices [25], [26]. Consequently, the input voltage can only be permitted to narrow voltage fluctuations, thereby limiting their applications.

From the aforementioned literature survey, the limitations, namely: 1) multiple PV sources; 2) discontinuous input current; 3) conventional boosting of qZS network; 4) higher inrush current in switched capacitors; and 5) leakage current, are identified. To overcome these limitations, a quasi-switched capacitor based five-level inverter (qSC-5LI) is proposed in this article. The proposed topology operates with a single dc source and draws continuous current from the input supply.

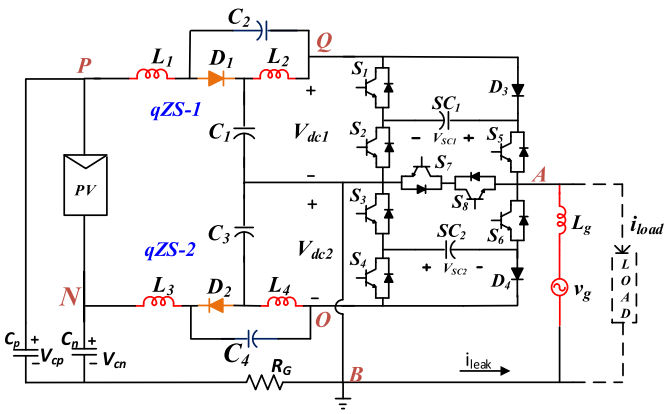

Fig. 1. Proposed qSC-5LI.

Furthermore, the power converter simultaneously achieves higher voltage boosting capability and five-level voltage inversion with the aid of a modified level-shifted PWM (LSPWM) scheme. In addition, the power converter minimizes the high-frequency voltage variations across the stray capacitance thereby minimizing the leakage current. The measured leakage current is determined to be substantially within the VDE0126-1-1-specified limit [17]. In addition, the experimental results pertaining to the dynamic performance of the five-level inverter in both the stand-alone and grid-connection operations are presented.

II. Quasi-Switched Capacitor Based Five-Level Inverter

A. Proposed Topology

The proposed qSB-5LI is shown in Fig. 1. The power converter comprises two qZS networks (qZS-1 and qZS-2) with a single PV source and a switched capacitor based five-level inverter. To boost the input voltage to the desired dc-link voltage, the output terminals of the qZS networks "Q" and "O" are short-circuited by turning on the switches (S_1–S_4). Furthermore, two switched capacitor units "S_1, D_3, S_{C1}" and "S_4, S_{C2}, D_4" are used to synthesize five levels in output voltage waveform. The load/grid is interfaced to the inverter to the mid-points of switches S_5, S_6, and the ground.

B. Switching Logic of the QSC-5LI

The voltage levels obtained with the proposed qSC-5LI, along with their corresponding switching logics, are shown in Table I. Among the eight states presented in Table I, states NST-1–NST-5 are the non-ST states which synthesize five output levels and states ST-1–ST-3 represent different ST states to obtain boosting in qZS networks. Fig. 2 displays the circuit diagram of the power converter during the non-ST mode of operation. From Fig. 2(a), it may be noted that both the qZS diodes (D_1 and D_2) are forward biased to provide a total dc-link voltage of "$V_{dc1} + V_{dc2}$" across the inverter input terminals (Q, O).

Furthermore, Fig. 2(b)–(e) shows the non-ST states NST-1–NST-5 shown in Table I to generate $\pm V_{dc}$, $\pm 0.5 V_{dc}$, 0 voltage levels. During the NST states, it may be observed that the charging currents of the switched capacitor (S_{C1}, S_{C2}) are

TABLE I
DIFFERENT SWITCHING STATES TO ACHIEVE A FIVE-LEVEL INVERSION

State-type	Switching logic (0-OFF, 1-ON)								Output Voltage 'V_{AB}' (V_{dc1}= V_{dc2}= V_{sc1}= V_{sc2}=0.5V_{dc})	
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8		
NST-1	1	0	1	0	1	0	0	0	(V_{dc1}+ V_{SC1})	V_{dc}
NST-2	0	1	1	0	1	0	0	0	V_{dc1}	0.5V_{dc}
NST-3	0	1	1	0	0	0	1	1	0	0
NST-4	0	1	1	0	0	1	0	0	-V_{dc2}	-0.5V_{dc}
NST-5	0	1	0	1	0	1	0	0	-(V_{dc2} +V_{SC2})	-V_{dc}
ST-1	1	1	1	1	1	0	0	0	V_{SC1}	0.5V_{dc}
ST-2	1	1	1	1	0	1	0	0	-V_{SC2}	-0.5V_{dc}
ST-3	1	1	1	1	0	0	1	1	0	0

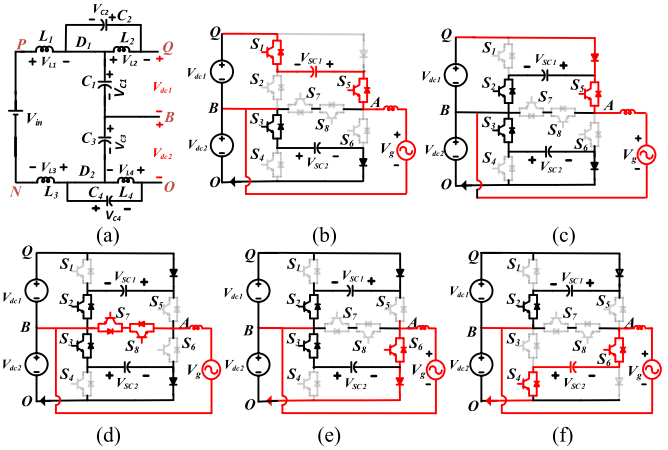

Fig. 2. (a) Schematic of qZS network during NST states. (b)–(f) Schematic of MLI during NST-1–NST-5.

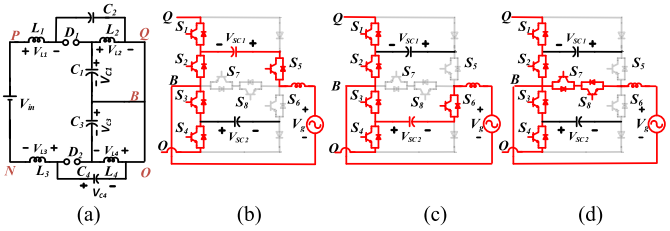

Fig. 3. (a) Schematic of qZS network during ST states. (b)–(d) Schematic of MLI during ST-1 to ST-3.

provided by the inductors of the qZS network. Therefore, the inrush charging currents of the switched capacitors are reduced to a lower value.

During the non-ST state, the inductor voltages (V_{L1}–V_{L4}) and the total dc-link voltage (V_{dc}) are stated as

$$V_{L1} + V_{L3} = V_{in} - V_{C3} - V_{C1} \quad (1)$$
$$V_{L2} = -V_{C2} \quad (2)$$
$$V_{L4} = -V_{C4} \quad (3)$$
$$V_{dc} = V_{dc1} + V_{dc2} = (V_{C1} + V_{C2}) + (V_{C3} + V_{C3}). \quad (4)$$

Fig. 3 presents the different ST states (ST-1–ST-3) of the qSC-5LI shown in Table I. From Fig. 3(a), it may be noted that the terminals "Q and O" of the power converter are short-circuited by turning on the switches "S_1–S_4" thereby

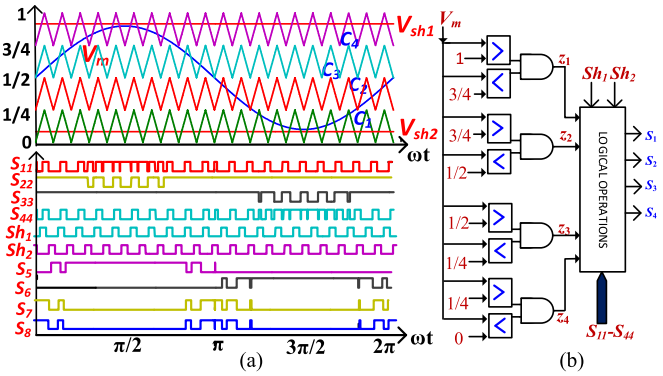

Fig. 4. (a) Implementation of modulation technique. (b) Zone selection logic.

storing energy in the qZS inductors. This ST can be implemented in three different ways in the proposed topology as shown in Fig. 3(b)–(d). During ST-1 and ST-2, the power converter outputs $+0.5V_{dc}$ and $-0.5V_{dc}$ across the grid, as shown in Fig. 3(b) and (c). Furthermore, during ST-3 the switches S_7 and S_8 are turned on to output 0 V across the grid as shown in Fig. 3(c).

During the ST state, the inductor voltages (V_{L1}–V_{L4}) and the total dc-link voltage (V_{dc}) are stated as

$$V_{L1} + V_{L3} = V_{in} + V_{C2} + V_{C4} \quad (5)$$
$$V_{L2} = V_{C1} \quad (6)$$
$$V_{L4} = -V_{C3} \quad (7)$$
$$V_{dc} = V_{dc1} + V_{dc2} = 0. \quad (8)$$

III. MODULATION TECHNIQUE

A. Proposed Modulation Technique for QSB-5LI

For the proposed topology, the LSPWM technique is implemented to perform the following operations: 1) boost the input PV voltage and 2) five-level output voltage inversion. From Fig. 4(a), it may be noted that the modulating signal "V_m" is compared with the carriers C_1–C_4 to produce the auxiliary signals S_{11}–S_{44} and level generating signals S_5–S_8. Furthermore, to generate ST pulses "Sh$_1$–Sh$_2$," two dc reference signals "V_{sh1} and V_{sh2}" are compared with carriers "C_4" and "C_1."

Further from Fig. 4(a), it may be observed that the modulation signal "V_m" is divided into four zones of operation, namely, "z_1, z_2, z_3, and z_4." These zones of operation are selected based on the magnitude of modulation signal "V_m" as shown in Fig. 4(b). Moreover, logical operations are performed between the auxiliary signals "S_{11}–S_{44}," ST pulses "Sh$_1$–Sh$_2$," and zones of operation "z_1, z_2, z_3, and z_4" to obtain the desired PWM signals "S_1–S_4." The logical operations are stated by (9)–(12). Finally, the PWM signals "S_1–S_4" and "S_5–S_8" are fed to the power converter to implement boosting and voltage inversion

$$S_1 = [S_{11} + (\text{Sh}_1 \cdot (Z_1 + Z_2))] + [S_{11} + (\text{Sh}_2 \cdot (Z_3 + Z_4))] \oplus S_{11} \quad (9)$$
$$S_2 = S_{22} \quad (10)$$
$$S_3 = S_{33} \quad (11)$$
$$S_4 = [[S_{44} + (\text{Sh}_2 \cdot (Z_1 + Z_2))] \oplus S_{44}] + [S_{44} + (\text{Sh}_2 \cdot (Z_3 + Z_4))]. \quad (12)$$

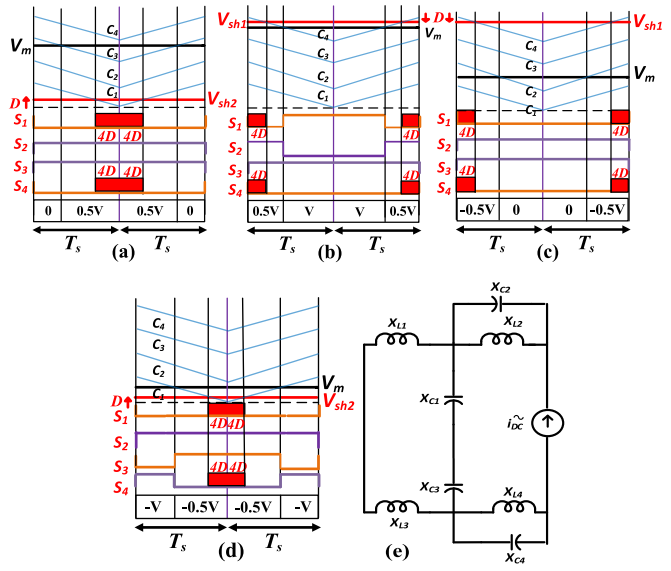

Fig. 5. (a)–(d) Generation of switching states in positive and negative half cycles. (e) Equivalent circuit.

Fig. 5 presents the switching states of the qSC-5LI during the positive and negative half-cycles of the output voltage waveform. As shown in Fig. 5(a), the modulation signal "V_m" is compared with carrier "C_3" to generate voltage levels 0 and 0.5 V. It may be observed that the dc reference signal (V_{sh2}) is incremented by "D" (where "D" is defined as the ratio of ST time and sample time) and is compared with carrier "C_1" to insert an ST pulse in "S_1" and "S_4." From Fig. 5(a), it is evident that the ST duty ratio "D" is scaled up by a factor of 4 (shown in red color) by the LSPWM. The implementation of ST in voltage level 0.5 to V is shown in Fig. 5(b).

In contrast to Fig. 5(a), the ST is generated by a decrement of the dc-reference (V_{sh1}) by D. The dc-reference signal (V_{sh1}) is compared with carrier "C_4" to insert ST pulse in "S_1" and "S_4." A similar conclusion can be drawn from Fig. 5(c) and (d), where V_{sh1} and V_{sh2} are used to insert ST in voltage levels from (0 to −0.5 V) and (−0.5 to −V).

B. Boost Factor

To derive the boost factor of the power converter, volt-second balance is applied to inductor voltage equations during non-ST [(1)–(3)] and ST states [(5)–(7)].

From the volt-second balance, the voltage across the qZS capacitors is expressed as

$$V_{C1} = V_{C3} = V_{\text{in}} \tag{13}$$

$$V_{C2} = V_{C4} = \frac{(4D)}{(1-4D)} V_{\text{in}} \tag{14}$$

where the ST duty ratio (D) is defined as the ratio of ST time (T_{sh}) and sample time (T_s).

The total dc-link voltage (V_{dc}) of the power configuration during the NST state is expressed as

$$V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}} = V_{c1} + V_{c2} + V_{c3} + V_{c4} = \frac{2}{(1-4D)} V_{\text{in}}. \tag{15}$$

C. Design of Switched Capacitor and qZS Inductor and Capacitor

The design of switched capacitors mainly depends on the modulation wave, discharge time, and load current. As both the switched capacitor have equal voltage ripple, the design of SC_1 is only shown below.

To determine the voltage ripple, the maximum time duration during which the voltage oscillates between 0.5 V_{dc} and V_{dc} is selected. The voltage ripple of SC_1 is estimated as

$$\Delta V_{\text{SC1}} = \frac{\Delta Q}{C_{\text{SC1}}} = \frac{\int_{t_1}^{t_2} I_m \sin\omega t\, dt}{C_{\text{SC1}}}. \tag{16}$$

Substituting $t_1 = [\sin^{-1}(0.5/m)]/\omega$ and $t_2 = (\pi/\omega) - t_1$

$$\Delta V_{\text{SC1}} = \frac{\Delta Q}{C_{\text{SC1}}} = \frac{2I_m}{\omega C_{\text{SC1}} m}\sqrt{m^2 - 0.25}. \tag{17}$$

The switched capacitor is given by the following expression:

$$C_{\text{SC1}} = \frac{2I_m}{\omega \Delta V_{\text{SC1}} m}\sqrt{m^2 - 0.25} \tag{18}$$

where "I_m" and "m" represent the peak value of load current and modulation index, respectively.

The permitted dc-link voltage ripple and low-frequency current ripple of the inductor serve as the design guidelines for the qZS inductors and capacitors in the proposed qSC-5LI. This low-frequency ripple is produced by the double-frequency component of the output power. In addition, the switching frequency ripple in inductor current is ignored, to simplify the design calculations. Fig. 5(e) shows the equivalent circuit of qSC-5LI. In Fig. 5(e), $X_{l(1-4)}$ to $X_{c(1-4)}$ denote the passive components of the qZS network, and $i_{\text{dc}}^{\sim}$ represents a current source which signifies the fundamental component of the dc-link current.

From Fig. 5(e), the double-frequency component of i_{L2} is expressed as

$$i_{L2}^{\sim} = \frac{4\sqrt{2}}{3\pi} \cdot \frac{P_{\text{OUT}}}{V_{\text{OUT}}} \cdot \sin\left(\frac{4 \cdot \pi \cdot t}{T} - \frac{\pi}{2}\right) \cdot \frac{x_{C2}}{x_{L2} + x_{C2}}. \tag{19}$$

Furthermore, the double-frequency inductor current ripple "x" is estimated from (19) as

$$x = \frac{4\sqrt{2}}{3\pi} \frac{V_{\text{in}}}{V_{\text{OUT}}} \frac{T^2}{\left(16\pi^2 L_2 C_2 - T^2\right)}. \tag{20}$$

Correspondingly, the double-frequency voltage across the capacitor "C_2" is expressed as

$$v_{C2}^{\sim} = \frac{4\sqrt{2}}{3\pi} \frac{P_{\text{OUT}}}{V_{\text{OUT}}} \sin\left(\frac{4 \cdot \pi \cdot t}{T} - \frac{\pi}{2}\right) \cdot \frac{x_{L2} \cdot x_{C2}}{x_{L2} + x_{C2}}. \tag{21}$$

From (21), the double-frequency voltage ripple "y" across the capacitor "C_2" is estimated as

$$y = \frac{4\sqrt{2}}{3\pi} \frac{(P_{\text{OUT}}) \cdot (1-4D)}{V_{\text{OUT}} \cdot (4D) V_{\text{in}}} \frac{4\pi T L_2}{\left(16\pi^2 L_2 C_2 - T^2\right)}. \tag{22}$$

The inductor and capacitor values of qZS-1 are acquired by solving (20) and (22) and considering $L_1 = L_2$ and $C_1 = C_2$. A similar study is performed to determine the qZS-2 inductors (L_3, L_4) and capacitors (C_3, C_4).

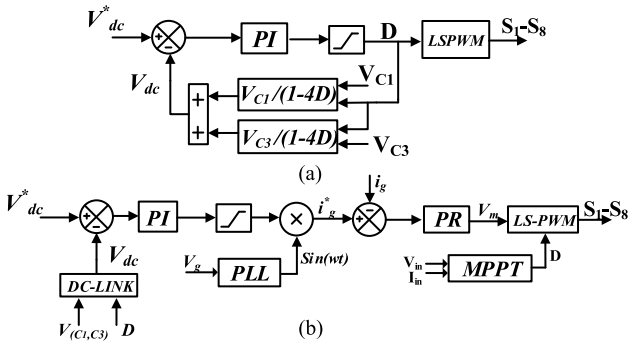

Fig. 6. (a) Control scheme for a stand-alone mode and (b) control scheme for a grid-connection mode of operation.

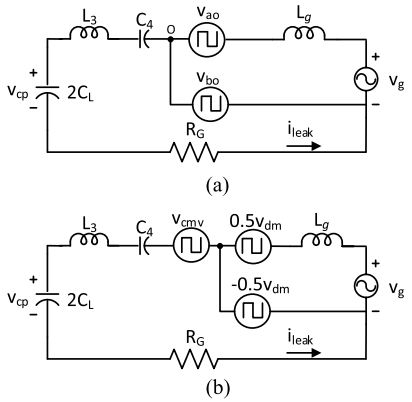

Fig. 7. (a) Common-mode model of qSC-5LI. (b) Simplified common-mode model.

IV. Proposed Closed-Loop Control Schemes For QSB-5LI

A. Stand-Alone Mode

The primary goal of the power configuration in the stand-alone mode is to maintain the output voltage at its rated value against load and source disturbances. To this end, the closed-loop control scheme [shown in Fig. 6(a)] is implemented to regulate the output voltage at the desired rms value. In general, the output voltage of the inverter ($m.V_{\rm dc}$) is controlled by regulating the total dc-link voltage ($V_{\rm dc} = V_{\rm dc1} + V_{\rm dc2}$) at a constant value of the modulation index. It may be noted that the dc-link voltage pulsates from a value of zero to the boosted dc voltage as a consequence of inserting the ST mode of operation using the inverter switches (S_1–S_4). As the direct measurement of dc-link voltage is not feasible, it is estimated with an indirect measurement as shown in Fig. 6(a). Furthermore, the total dc-link voltage "$V_{\rm dc}$" is assessed by the capacitor voltages "V_{c1}, V_{c3}" and ST duty ratio "D." The error generated by the comparison of $V^*_{\rm dc}$ and $V_{\rm dc}$ is compensated by the PI controller. The PI controller generates a dc signal, corresponding to the duty ratio "D," which in turn determines the ST dc-reference signals "$V_{\rm sh1}$, $V_{\rm sh2}$," which are needed to implement the LSPWM. These dc-reference signals are compared with carrier signals "C_1, C_4" to generate the ST signals "$\rm Sh_1$ and $\rm Sh_2$" [as discussed in Section III-A].

B. Grid-Connection Mode

The closed-loop control scheme for the grid-connection mode of operation is presented in Fig. 6(b). This scheme enables the controller to inject power into the grid at the unity power factor (UPF). In this control scheme, an outer voltage loop is used to control the dc-link voltage, while an inner current loop injects current into the grid. Furthermore, an independent MPPT control is implemented to extract the peak power from the PV source.

The perturb and observe (P&O) MPPT algorithm is used to track the peak power of the PV source. Both PV voltage ($V_{\rm in}$) and current ($I_{\rm in}$) are fed as input to the P&O algorithm. The algorithm generates the required duty ratio "D" to track the maximum power point of the PV panel. The change in duty ratio "D" results in the change in the total dc-link voltage "$V_{\rm dc}$" of the five-level inverter. The assessed dc-link voltage "$V_{\rm dc}$" is compared with the reference dc-link voltage ($V^*_{\rm dc}$) and the produced error is compensated by the output loop PI controller. The PI controller generates the current reference (i^*_g), which is in sync with the grid using a PLL. The difference in the current reference (i^*_g) and the actual grid current is compensated by a PR controller by varying the modulation signal (V_m). The change in modulation signal (V_m) results in a change in the current injected into the grid [27], [28]. Thus, in the grid-connection mode, the two degrees of freedom provided by the qSC-5LI, namely, the ST duty ratio (D) and the modulation index (m), are efficiently used to achieve the goals of MPPT and current injection into the grid.

V. Minimization of Leakage Current

Transformerless inverter configurations are widely reported in the literature for grid-connection applications. They offer advantages such as higher power density and higher efficiency. However, the elimination of the transformer results in the flow of leakage current, which is highly undesirable. In general, high-frequency voltage variations across the stray capacitance formed due to the grounded frame of the PV panel pave the way to the genesis of the leakage current.

The harmful effects of the leakage current in terms of performance and safety are well-documented [29]. In view of this, the standard VDE0126-1-1 [17] limits the maximum leakage current to 300 mA (rms). The most popular strategies to minimize/restrict the leakage current include clamping the voltage across the stray capacitance to a constant value or reducing the high-frequency voltage content across it. This high-frequency voltage content is caused by the common-mode voltage of the MLI. This calls for the assessment of high-frequency voltage content applied across the stray capacitance.

To realize this objective, a common-mode model of the power converter is developed, which is shown in Fig. 7(a). Furthermore, the common-mode voltage is resolved into the common mode and the differential mode components as shown in Fig. 7(b).

From Fig. 7(b), the parasitic voltage (V_{cp}) across the PV capacitor is determined by the following expression:

$$V_{cp} = V_{L3} + V_{C4} + V_{tcmv} \tag{23}$$

where the effective common-mode voltage is defined as $V_{tcmv} = V_{cmv} - 0.5V_{dm}$.

TABLE II
PARASITIC VOLTAGE OF QSC-5LI FOR $D = 0.1$

State-type	V_{AB}	V_{AO}	V_{BO}	V_{tcmv}	$V_{L3} + V_{C4}$	V_{cp}
NST-1	V_{dc}	$3V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-2	$V_{dc}/2$	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-3	0	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-4	$-V_{dc}/2$	0	$V_{dc}/2$	$V_{dc}/2$	$-0.35V_{dc}$	$0.15V_{dc}$
NST-5	$-V_{dc}$	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$-0.35V_{dc}$	$0.15V_{dc}$
ST-1	$V_{dc}/2$	$V_{dc}/2$	0	0	$0.15V_{dc}$	$0.15V_{dc}$
ST-2	$-V_{dc}/2$	$-V_{dc}/2$	0	0	$0.15V_{dc}$	$0.15V_{dc}$
ST-3	0	0	0	0	$0.15V_{dc}$	$0.15V_{dc}$

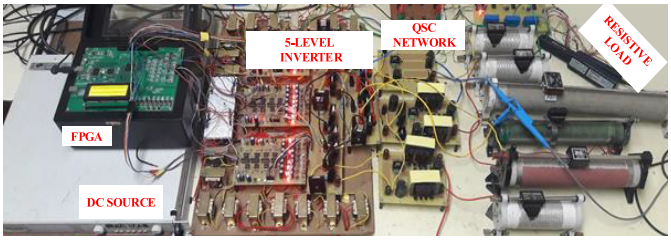

Fig. 8. Hardware low-scale prototype of qSC-5LI.

The sum of inductor and capacitor voltages "$V_{L3} + V_{C4}$" during the NST and ST states is stated as

$$V_{L3} + V_{C4} = \frac{-(1+4D)}{4} V_{\text{dc}} \quad \text{for the NST state} \tag{24}$$

$$V_{L3} + V_{C4} = \frac{(1-4D)}{4} V_{\text{dc}} \quad \text{for the ST state.} \tag{25}$$

The pole voltages (V_{AO}, V_{BO}), effective common-mode voltage (V_{tcmv}), the sum of voltages $V_{L3} + V_{C4}$, and the parasitic voltage across the PV capacitor (V_{cp}) during ST and NST states are shown in Table II. For example, "V_{cp}" is calculated for a "D" of 0.1. It may be observed that "V_{cp}" remains to be constant at a value of 0.15 V_{dc} for both ST and NST states. As the parasitic voltage "V_{cp}" across the PV capacitor remains constant, the leakage current from the PV panel to the grid is minimized.

VI. EXPERIMENTATION RESULTS

The operating principles of the proposed qSC-5LI are validated with a scaled-down prototype which is shown in Fig. 8. A programmable dc power supply is used to replicate the constant current and constant voltage behavior of the PV panel, and FPGA (Spartan-6) is used to output the gating pulses for the power converter. Table III displays the hardware specifications and the experiment's operational settings.

In this experimental setup, an input voltage (V_{in}) of 68 V is applied across the qZS networks to acquire the output voltage of 110 V (rms). However, this input voltage (68 V) is not adequate to achieve 110 V (rms). Therefore, the input voltage (V_{in}) is boosted to obtain the required magnitude, by inserting an ST duty ratio of 0.08, which realizes a boost factor of 2.94 (11). The experimental waveforms of the input voltage (V_{in}) and the boosted dc-link voltages (V_{dc1} and V_{dc2}) of qSC-5LI are shown in Fig. 9.

TABLE III
OPERATING PARAMETERS OF HARDWARE PROTOTYPE

Operational conditions	Values	Components	Values
Input voltage (V_{in})	68V	EE65CORE Inductors	2.5mH
Total DC-link voltage	200V	Capacitors (C_1-C_4)	300V,1300μF
Switching frequency	20kHz	Switched capacitors (SC_1, SC_2)	200V,400 μF
Output voltage(RMS)	110V	Fast recovery diode	MUR1560CT
Modulation Index (m)	0.8	MOSFETs	IRFP460
Output Power (P_o)	400W	PV capacitor (C_p)	100nF

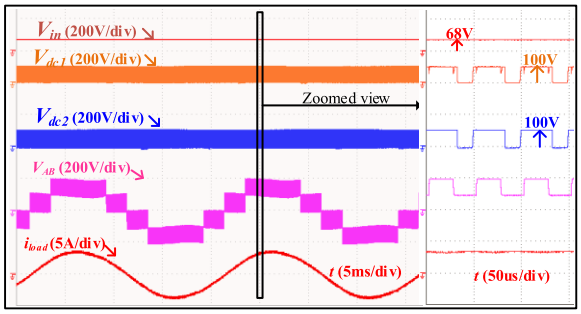

Fig. 9. Input voltage (V_{in}), dc-link voltages (V_{dc1} and V_{dc2}), output voltage (V_{AB}), and load current (i_{load}) of qSC-5LI.

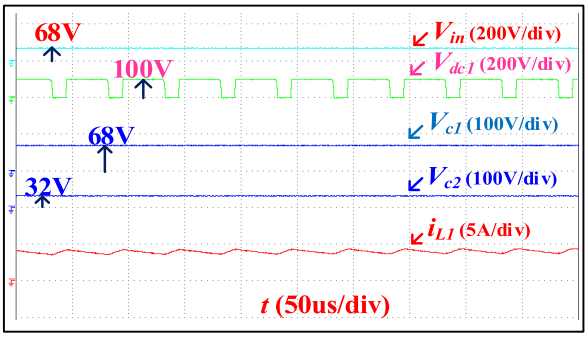

Fig. 10. Input voltage (V_{in}), dc-link voltage (V_{dc1}), capacitor voltages (V_{c1}, V_{c2}), and inductor current (i_{L1}) of qSC-5LI.

It may be noted that the dc-link voltage (V_{dc1} and V_{dc2}), are pulsating waveforms which switch between the voltage levels of 100 V during the NST state and 0 V during the ST state. Thus, the total dc-link is boosted to 200 V (i.e., $V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}}$) indicating that a boost factor of 2.94 is obtained. Furthermore, the last two traces of Fig. 9 present the output voltage (V_{AB}) and the load current (i_{load}). It may be noted that the output voltage has five different voltage levels, namely, 0, ±100, and ±200 V. The zoomed-in view of Fig. 9 clearly shows the voltage transitions in the dc-link voltages and output voltage of qSC-5LI.

Fig. 10 presents the inductor current (i_{L1}) and capacitor voltages (V_{c1} and V_{c2}) of the top qZS network-1 of the power converter (Fig. 1). Theoretically, in qZS-1 the boosted dc-link voltage (V_{dc1}) is distributed in the ratio (1–4D:4D) across the qZS capacitors "C_1" and "C_2." It may be noted from Fig. 10 that the capacitors "C_1" and "C_2," respectively, support

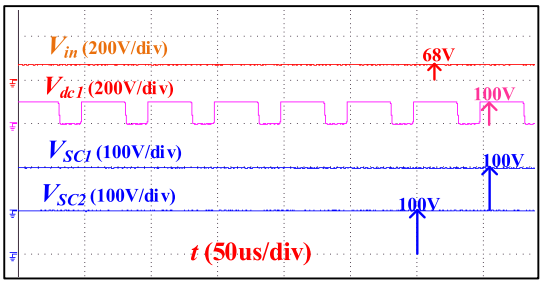

Fig. 11. Input voltage (V_{in1}), dc-link voltage (V_{dc1}), and switched capacitor voltages (V_{SC1}, V_{SC2}) of qSC-5LI.

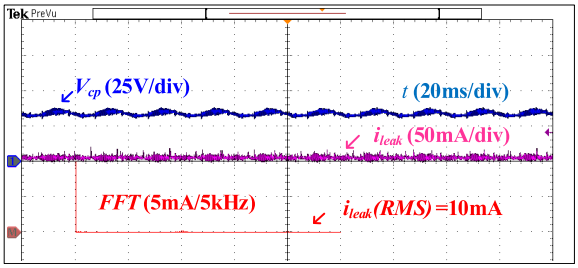

Fig. 12. PV capacitor voltage (V_{cp}) and leakage current (i_{leak}) of qSB-5LI.

the voltages 68 and 32 V, which add up to the total dc-link voltage (V_{dc1}) of 100 V. Furthermore, the last trace shows the rise and fall of the inductor current (i_{L1}) during the ST and NST modes of operation.

The input voltage (V_{in1}), the dc-link voltage V_{dc1}, and the voltage across the switched capacitors (V_{SC1} and V_{SC2}) are presented in Fig. 11. In the proposed power converter, both the switched capacitors (SC_1 and SC_2) are charged to half the total dc-link voltage to obtain the five-level output voltage waveform. It may be observed that the switched capacitors are charged to 100 V each of which is half of the total dc-link voltage of 200 V.

The experimentally obtained parasitic voltage (V_{cp}) and the leakage current (i_{leak}) are shown in Fig. 12. It may be observed that the mean value of the parasitic voltage is 34 V with only the switching frequency ripple present in it. It is evident that the induced leakage current is minimized due to the absence of high-frequency voltage transitions in "V_{cp}." The experimentally measured leakage current is 10 mA (rms), which falls within the standard VDE0126-1-1 limit of 300 mA (rms) [17].

In the stand-alone mode, the dynamic response of the proposed qSC-5LI is validated for load disturbance in Fig. 13. In this experiment, both the dc-link voltages (V_{dc1} and V_{dc2}) of the power converter are regulated at 100 V (peak) to generate an output voltage of 110 V (rms). Initially, the power converter is loaded to 1.4 A, which is half of its full-load value. When the converter is suddenly loaded to its rated value of load current (2.82 A), the dc-link voltages (V_{dc1} and V_{dc2}) remain practically unperturbed (Fig. 13) due to the control action exerted by the closed-loop controller shown in Fig. 6(a). This regulatory action also manifests at the output, as the output voltage of the proposed topology is exclusively dependent on the dc-link voltages (V_{dc1} and V_{dc2}).

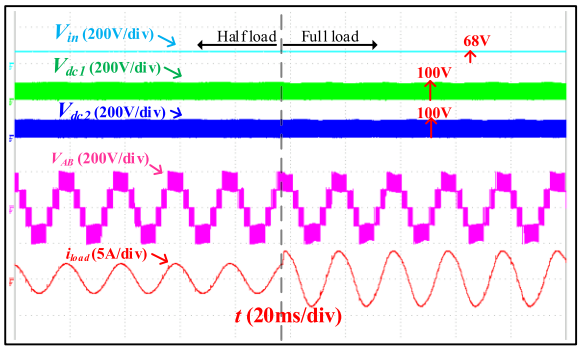

Fig. 13. Input voltage (V_{in}), dc-link voltages (V_{dc1} and V_{dc2}), output voltage (V_{AB}) and load current (i_{load}) during load disturbance.

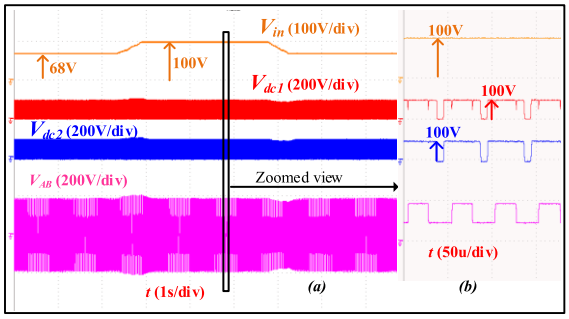

Fig. 14. Input voltages (V_{in1}) and dc-link voltages (V_{dc1} and V_{dc2}) and output voltage (V_{AB}). (b) Zoomed-in view of the plot (a).

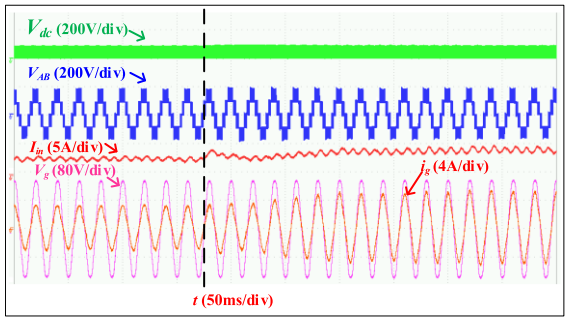

Fig. 15. Total dc-link voltage (V_{dc}), inverter output voltage (V_{AB}), input voltage (V_{in}), grid voltage (V_g), and grid current (i_g).

The proposed qSC-5LI is also validated for source disturbance as shown in Fig. 14. In the experimental result presented in Fig. 14, the input voltage (V_{in}) is initially maintained at 68 V with a total dc-link voltage of 200 V (i.e., 100 V per each qZS) and a quick disturbance of 32 V is created in the supply voltage. From Fig. 14, it may be noted that both the dc-links (V_{dc1} and V_{dc2}) are maintained at 100 V irrespective of the changes in the supply voltage. Thus, it is experimentally verified that the closed-loop controller shown in Fig. 6(a) is capable of regulating the dc-link voltages against the supply disturbances as well.

Fig. 15 presents the experimental result pertaining to the grid-connection operation of qSC-5LI. In this mode, the control scheme presented in Fig. 6(b) is used. Initially, the active power of 250 W is injected into the grid by the controller. As stated in Section V, the controller dynamically adjusts the value of the "D" based on the insolation level on PV panels.

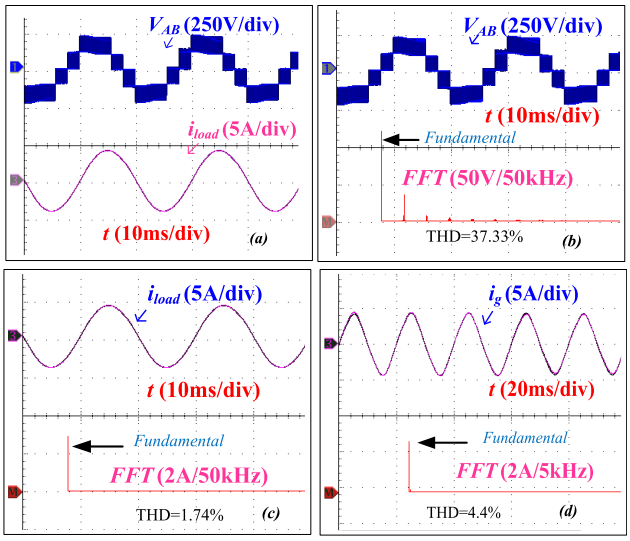

Fig. 16. (a) Experimental output voltage "V_{AB}" and load current (i_{load}) at 0.8 pf. (b) Harmonic spectrum of inverter output voltage "V_{AB}." (c) Harmonic spectrum of load current "i_{load}." (d) Harmonic spectrum of grid current "i_g."

As the insolation of the PV panel increases, the output power injected into the grid also increases. When a quick increase in the duty ratio "D" is introduced (which follows an increase in the insolation level), the input current (I_{in}, third trace) is correspondingly increased from 2.7 to 4 A (rms), in turn increasing the dc-link voltages. The outer loop PI controller [Fig. 6(b)] responds to this disturbance by increasing the reference value of the grid current. The inner current loop's PR controller compensates for the difference between the reference and actual grid current values by increasing the modulation index "m." This increases the grid current thereby increasing the active power pumped into the grid. In consequence, the dc-link voltage automatically returns to its actual value. The corresponding increase of grid current (i_g) is clearly visible in Fig. 15 (from 2.26 to 3.39 A rms at UPF).

The proposed qSC-5LI is evaluated for a 0.8 lagging power factor to validate its nonunity power factor capability. The experimental waveforms of inverter output voltage "V_{AB}" and load current "i_{load}" are shown in Fig. 16(a). It may be observed that load current lags behind inverter output voltage "V_{AB}" indicating the power converter's capability to support non-UPF loads.

Fig. 16(b) and (c) shows the FFT of the inverter output voltage "V_{AB}" and load current "i_{load}." It may be observed that the voltage THD is 37.5% and the current THD is 1.74%. Furthermore, the grid current (i_g) THD of qSC-5LI is shown in Fig. 16(d). It may be noted that the grid current THD is 4.4% which is within the grid standards IEEE 1547 [30] of 5%.

VII. Comparison Between Proposed QSC-5LI and QZS-Five-Level Inverter Topologies

A brief comparison between the proposed power converter and the existing qZS-five-level topologies is presented in this section. In Table IV, all the power converters are compared in terms of device count, boost factor, voltage stress, voltage THD, and leakage current. It may be noted that the proposed topology uses an equal number of switches but requires two additional capacitors when compared with the other qZS five-level inverters. The topology reported in [15] needs fewer inductors when compared with the proposed power converter. However, the input current drawn by this power converter is discontinuous which is not ideal for PV applications. In addition, it may also be observed that the proposed qSC-5LI exceeds the other five-level qZS topologies in terms of boost factor. The voltage stress across the switches, diode, and capacitors is calculated on a per-unit (p.u.) basis. For these computations, the base value is considered as the output voltage (rms). It may be observed that all the five topologies have equal voltage stress across the switches and diodes. It may be noted that the qZS capacitors of the proposed topology are subject to higher voltage stress when compared with the other qZS based five-level topologies. However, this may not be a disadvantage as the proposed qSC-5LI provides a higher boost factor. As the total switching device count is unequal in the topologies presented in Table IV, the total standing voltage (TSV) is calculated [31]. In comparison to topologies [7] and [15], the proposed converter has a minimum TSV value as shown in Table IV. Furthermore, all the topologies are simulated at an equal output voltage of 110 V rms and a power level of 400 W in MATLAB to obtain output voltage THD. It may be observed that the qSC-5LI registers lower voltage THD when compared with power converters [7], [12], and [16]. The topologies presented in [7], [12], and [15] do not address the issue of leakage current. Furthermore, the topology [16] uses an additional LCL filter to minimize the leakage current. Hence, to compare the leakage current, these topologies are simulated with the parasitic capacitor "C_p" of value 100 nF and without any LCL filters. It may be noted that in comparison to the other four power converters, the proposed qSC-5LI has a lower leakage current (10.02 mA) which is less than 300 mA according to standard VDE0126-1-1 [17].

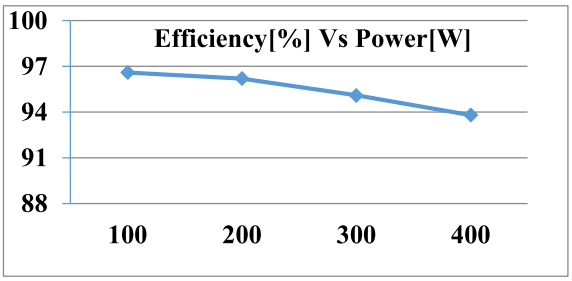

Fig. 17. Efficiency curve of qSC-5LI.

VIII. Loss Distribution in QSC-5LI.

To estimate the efficiency of qSC-5LI, the loss analysis is implemented in Powersim (PSIM) software. The qSC-5LI is simulated using the thermal models of the power diode (MUR1560CT) and semiconductor switch (MOSFET-IRFP460). The switching losses (P_{sd}, P_{sw}) and conduction (P_{cd}, P_{con}) losses incurred in the diodes and the switches (S_1–S_8) are evaluated for output power in the range of 0–400 W. Furthermore, the ESR losses in the capacitors (P_{cap}) and conduction losses in the inductors (P_{ind}) are

TABLE IV
COMPARISON OF QSC-5LI WITH FIVE-LEVEL QZS MLIS

	qZS-NPC[7]	qCHB-FLBI[12]	Mqzs- 5LI[15]	qZS-5L[16]	qSC-5LI (proposed)
N_{Levels}	Five	Five	Five	Five	Five
$N_{sources}$	One	Two	One	One	One
$N_{inductors}$	Four	Four	Two	Four	Four
$N_{capacitors}$	Four	Four	Four	Four	Six
N_{diodes}	Six	Two	Three	Four	Four
$N_{switches}$	Eight	Eight	Eight	Eight	Eight
Boost	$1/(1-2D)$	$1/(1-2D)$	$2/(1-2D)$	$1/(1-2D)$	$2/(1-4D)$
Gain	$(1-D)/(1-2D)$	$(1-D)/(1-2D)$	2(1-D)/(1-2D)	$(1-D)/(1-2D)$	$2(1-D)/(1-4D)$
Continuous input current	Yes	Yes	No	Yes	Yes
Voltage stress across the capacitor	$1/\sqrt{2}$ ($C_{1,2}$)	$1/\sqrt{2}$ ($C_{1,2}$)	$1/\sqrt{2}$ ($C_{1,2}$)	$1/\sqrt{2}$ ($C_{1,3}$)	(1 − 4D). x ($C_{1,3}$)
	D. x ($C_{3,4}$)	D. x($C_{3,4}$)	D. x ($C_{3,4}$)	D. x ($C_{2,4}$)	(4D). x ($C_{2,4}$)
					x ($SC_{1,2}$)
Voltage stress across Diode	x	x	x	x	x
Voltage stress across the switch	x	x	x for S_1-S_4	x	x
			2x for S_5-S_8		
TSV	7	5	7.5	6	6
THD (Voltage)	76.4%	42.73%	38.2%	74.2%	38.2%
Simulated leakage current without filter	720mA	1.1A	590mA	325mA	10.02mA

* $x = 1/\sqrt{2}(1-D)$

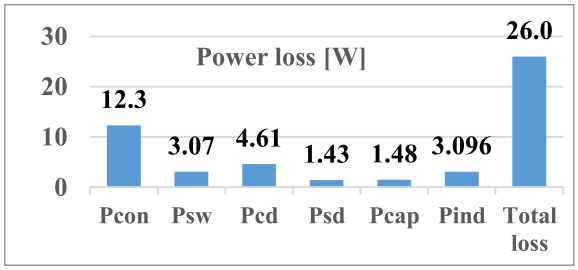

Fig. 18. Distribution of power loss in switches, diodes, inductors, and capacitors at 400 W in qSC-5LI.

estimated using equations given in [32]. The power converter displays an average efficiency of 95% as shown in Fig. 17. Furthermore, at 400 W, the power loss in switches (S_1–S_8) and passive components is depicted in Fig. 18.

Furthermore, to measure the CEC efficiency of the power converter, the experimental efficiencies at six different power levels (10%, 20%, 30%, 50%, 75%, and 100%) of the rated output power are determined [33]. The CEC efficiency of the proposed power converter is estimated to be 91.5%.

IX. CONCLUSION

In this article, a single-stage qSB-5LI is investigated for PV applications. The proposed topology, along with its modulation scheme, simultaneously achieves voltage boosting and five-level operation. The power converter offers a higher boost factor when compared with other qZS based five-level topologies in the literature. In addition, the proposed topology reduces the leakage current to 10 mA, which is far lower than the specified limit set by the VDE 0126-1-1 standard (300 mA rms) [17]. In the stand-alone mode, a closed-loop dc-link control system is used to regulate the output voltage by controlling the ST duty ratio "D." It is also shown that in the grid-connection mode of operation, the control is decoupled in that the objective of MPPT is addressed with the ST duty factor while the control of grid current requires that the modulation index be controlled. Finally, experimentation is carried out to evaluate the dynamic performance of the proposed system in both the stand-alone and grid-connected modes.

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