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A cross connected cell based modular multilevel converter for HVDC system with DC short-circuit fault ride-through capability

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Summary

The non-permanent dc short-circuit fault is a crucial issue in overhead high voltage dc transmission (HVDC) lines. In this paper, a cross connected (CC) cell also known as hexagonal switch cell (HSC) based modular multilevel converter (MMC) with dc short-circuit fault ride through feature is addressed for an HVDC system. During normal operation, the CC cell-MMC is capable of producing an identical number of levels while using fewer power devices than full-bridge (FB) and clamp double sub-module (CDSM)-based MMCs. Similarly to the FB-MMC and CDSM-MMC, the provided CC cell-MMC not only blocks the dc fault current but can also function as a static synchronous compensator (STATCOM) during a DC-Bus fault. The Proposed control technique uses MMC as a STATCOM to inject reactive power during a pole-to-pole DC-Bus fault to keep the grid stable. The control approach comprises injecting zero-sequence voltage into each phase to balance the mean voltage of capacitors and arm currents. The fundamental zero-sequence voltage is obtained by a simple stationary reference frame-based controller. The control strategy's efficacy is evaluated in MATLAB and confirmed in the Opal-RT environment.

KEYWORDS

cross connected (CC) cell, high voltage DC transmission (HVDC), modular multilevel converter (MMC), pole-to-pole fault, static synchronous compensator (STATCOM), zero-sequence voltage injection (ZSVI)

1 | INTRODUCTION

Voltage source converter (VSC)-based HVDC transmission systems are attracting researchers because of the numerous advantages they provide over conventional line-commutated thyristor-based HVDC systems, such as decoupled control of real power, imaginary power, and power reversal with constant dc voltage polarity, high-quality output voltage and current with very low harmonic distortion, and so on.[1] A Two-Level VSC, voltage blocking capability is extended by connecting series of switches became a feasible solution till 1999. Moreover, Three-Level VSC in 2000 generated voltage and current with less harmonic content compared to former VSC. The two VSC topologies are not modular in nature and ends in lack of fault tolerant operation. MMC has emerged as a potential architecture for high/medium power applications due to its modular construction, level scaling, and submodule redundancy functioning.[2–4]

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Conventional MMC comprises of half-bridge (HB) or chopper cells that can able to generate two levels, that is, 0 and V_c (magnitude of capacitor voltage).[5–7] In HB-MMC, when pole to pole voltage collapse to zero, the gating pulses for the switching devices are seized and MMC behaves as a grid connected uncontrolled rectifier. This leads to the flow of large current through the MMC contributed by the grid and may damage the semiconductor devices. To address this issue, two anti-parallel thyristors are used across the bottom IGBT of each HB cell and are activated during the fault, preventing damage to freewheeling diodes. Perhaps, this is not a promising solution as the fault current flowing is supplied by the grid rather than DC-Bus.[8] On the other hand, full-bridge (FB) cell can produce three-levels, that is, 0, $+V_c$, and $-V_c$. When pole to pole voltage collapse to zero, unlike HB-MMC, the additional voltage level ($-V_c$) generated by FB cell can block the fault current. Furthermore, FB-MMC may be used as a STATCOM to deliver reactive power to the grid, improving grid stability during faults.[9]

To further improve fault-tolerant capability of MMC, a Clamped Double Sub-module (CDSM) was introduced. A CDSM cell consist of an ancillary IGBT, which is used to connect two H-bridges in series to form a single cell. Depending on the direction of current flow, CDSM generates 0, V_c, $2V_c$, and $-V_c$ levels. During fault, CDSM in addition to blocking of fault current it can operate as STATCOM. During STATCOM operation, ac voltage is generated only when the arm current is negative, this will result one arm in conduction mode and other arm in blocking mode. Perhaps only half the rated reactive power will be injected into the grid.[10] In the Z packed U-cell (ZPUC) topology proposed in Arazm and Haddad,[11] when a DC-Bus fault occurs, the converter is unable to restrain the fault current if the gating signals are interrupted. A new SM topology proposed in Gen et al.,[12] additional power switches and a bypass switches are utilized to operate MMC successfully during SM failure and the converter cannot be operated as STATCOM during DC-Bus fault. A hybrid MMC is proposed to reduce the arm voltage to half compared to conventional MMC. This advantage will be ruled out during the DC-Bus fault.[13] The authors proposed a new topology having self-voltage balancing capability using additional components.[14] This topology lacks the capability of injecting reactive power during DC-Bus fault.

As a result, the following are the primary contributions of this paper:

1. In Nami et al.,[15] a mixed cell based MMC that combines cross connected and half-bridge cells in the ratio of 1:3 has been proposed that has the potential to block fault current during DC-Bus fault. The aforementioned work does not address how MMC functions as a STATCOM during a DC-Bus fault. This paper presents only CC cell-based MMC,[16,17] which requires fewer power devices than FB-MMC.
2. A voltage sorting technique that is frequently used to balance the capacitor voltages of MMC was combined with a carrier rotation PWM[18] in order to accomplish uniform conduction of switches and equalizing the power sharing among CC cell units. Compared to PI-based voltage balancing control,[19,20] sorting method is easier to put into practice.
3. The proposed CC cell-MMC based HVDC system is demonstrated for normal and as well as pole-to-pole short-circuit fault. During normal operation, a Circulating Current Suppression Control (CCSC) is implemented in this paper to avoid additional heating of components due to second order harmonic circulating current.[21,22]
4. During pole-to-pole short-circuit fault, the gating signals to all IGBTs are deactivated then the negative voltage level ($-2V_c$) generated by CC cell will oppose the fault current as shown in Figure 2F,G. Moreover, CC cell-MMC can be operated as STATCOM to inject two-fold reactive power into the grid compared to one-fold in CDSM-MMC.
5. During STATCOM operation, the mean voltage of capacitors in one phase will deviate from the mean voltage of capacitors in other phases without proper control. Therefore, to minimize the deviation in capacitor voltages of three phases a fundamental zero-sequence voltage component is injected into the three phase MMC modulating signals. There are various methods to compute the amplitude and phase-angle of ZSVI.[23] But in this paper, a simple alpha-beta reference frame-based control strategy is adopted[24] and extended to MMC structure to calculate the fundamental zero-sequence voltage. The suggested approach computes the active power current component in real-time to offset MMC losses during a fault, rather than nullifying it.[25] The proposed method is simple and less complex than the control strategy used in the literature.[26,27]

The paper is structured as follows. Section 2 depicts the CC cell-MMC topology and operating principle of MMC. Section 3 explains about the control of grid connected converter during normal and pole-to-pole short circuit operation. Satisfactory results of MMC operation during normal and fault are exhibited in Section 4. Section 5 presents the real time validation results of the proposed converter during normal and fault operation.

2 | CC CELL-BASED MODULAR MULTILEVEL CONVERTER TOPOLOGY

The traditional three-phase MMC consists of two arms per phase, named as upper arm and lower arm. Each arm consists of sub-modules connected in cascade and a series arm inductor to limit the circulating current under normal operation and the fault current during DC-Bus fault as shown in Figure 1. In general, each sub module of MMC consists of a half-bridge, full-bridge or CDSM cell. However, in this paper, N number of sub modules is considered and each sub module is replaced with a CC cell unit. The six switches and two capacitors that make up each CC cell unit along with the various switching states of the CC cell are depicted in Figure 2.

To understand the operating principle of MMC as shown in Figure 1, let V_{dc} is the dc-link voltage and I_{dc} is the DC-Bus current. Upper arm and lower arm currents be i_{ux} and i_{lx} (here, $x = a$, b, and c), i_x be the load current. v_{ux} and v_{lx} be the upper and lower arm sub-module voltage and v_x be the ac output voltage. R_0 and L_0 be the resistance and inductance of arm inductor. In order to generate ac output voltage across the output terminals of the converter, the upper and lower arm sub modules need to be switched as given by Equations (1) and (2), assuming the voltage drop across the arm inductors are negligible.[28]

$$v_{ux} = \frac{V_{dc}}{2} - v_x \tag{1}$$

$$v_{lx} = \frac{V_{dc}}{2} + v_x \tag{2}$$

where $v_x = \frac{mV_{dc}}{2}\sin(\omega t + \theta_x)$; $\theta_x = 0, 120^\circ, 240^\circ$ and m is the modulation index.

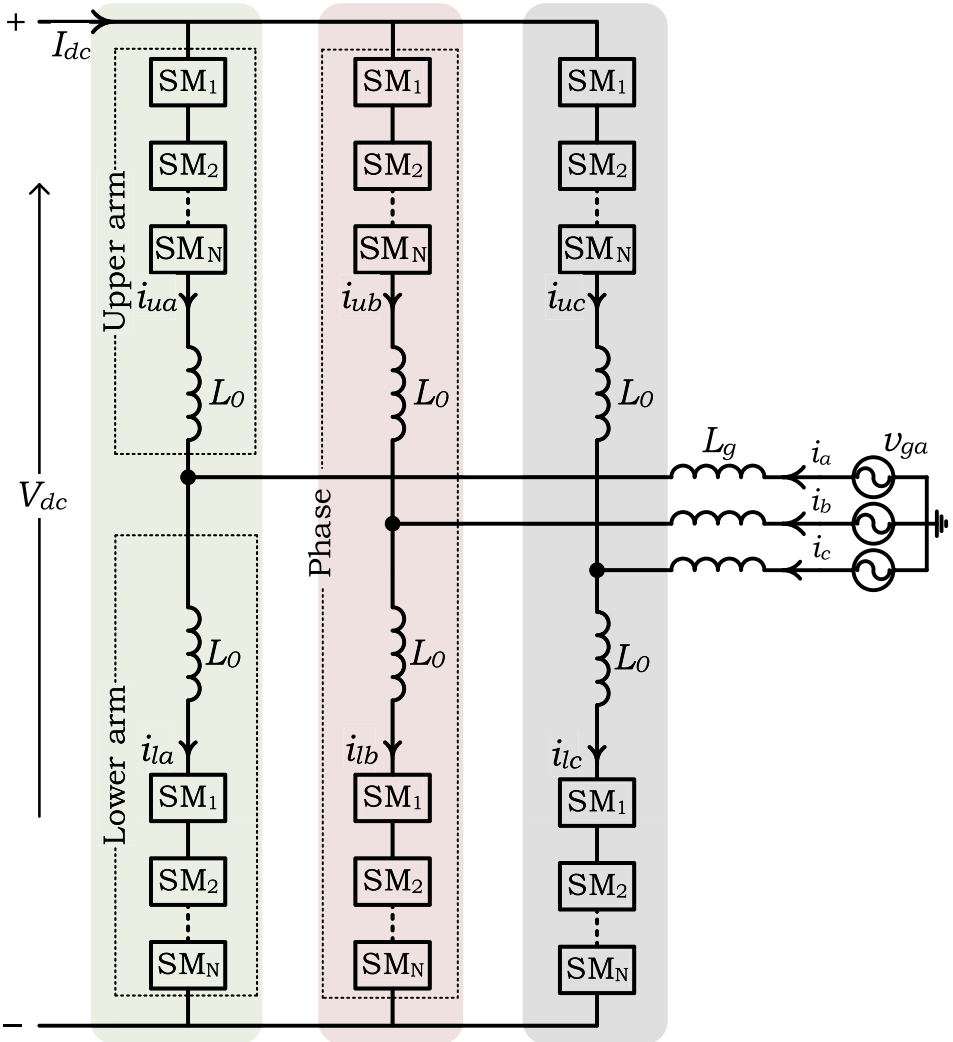

FIGURE 1 Three phase circuit diagram of CC cell-MMC.

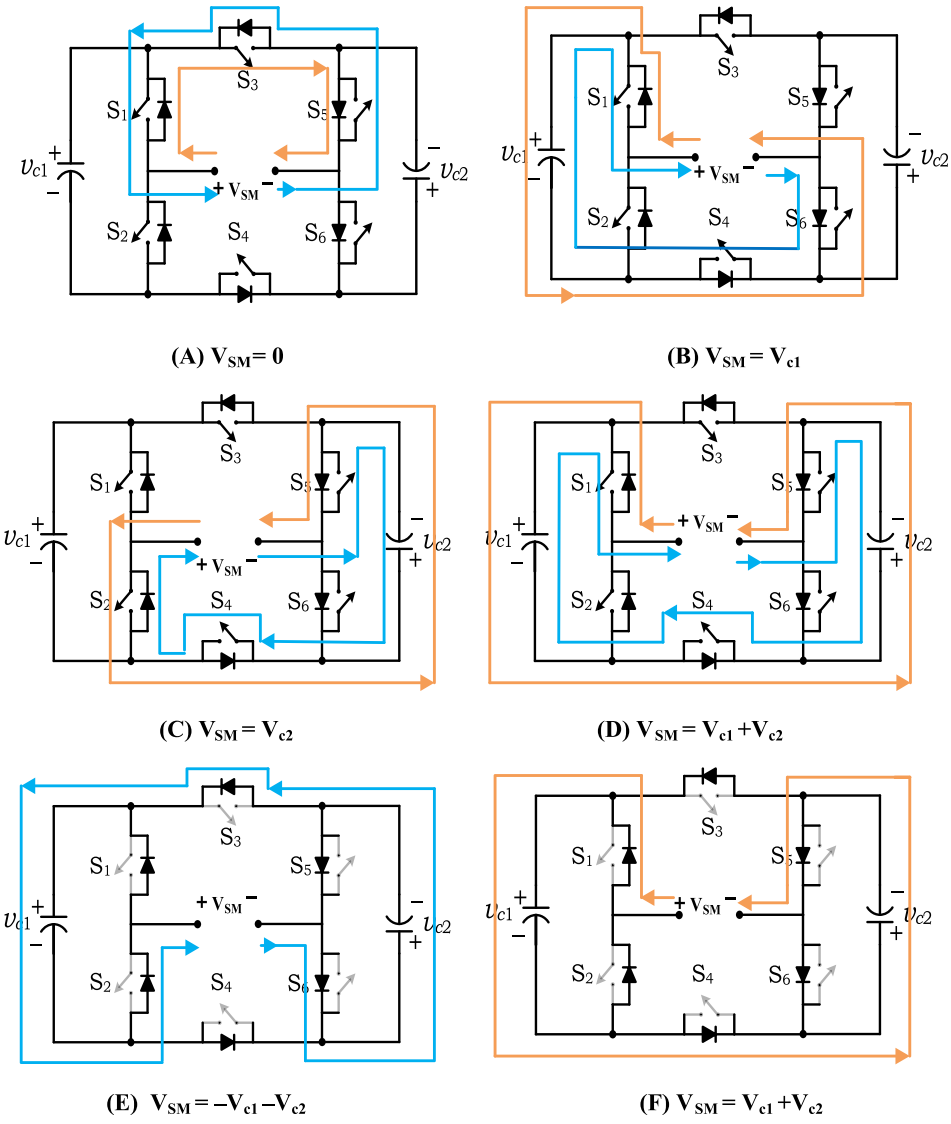

FIGURE 2 CC cell switching states: (A–D) During normal operation, depending on the direction of arm currents, the capacitors will be charged or discharged. (E–F) Gating signals are seized during DC-Bus fault then the current flows through the free-wheeling diodes and capacitors.

2.1 | Capacitor voltage balancing using sorting algorithm

In HVDC application, the capacitor voltages in each CC cell need to be regulated at their desired voltage level. In order to achieve this, the redundant states of the converter need to be used according to the voltage magnitude of capacitors and current direction through each cell. If the current flowing through the arm is positive, then capacitor with lowest magnitude is to be switched to charge the capacitor. If the current is in negative direction then capacitor with highest magnitude is to be switched to discharge. The sorting methodology for CC cell-based MMC is shown in Figure 3 to balance the magnitude of capacitors to desired level.[29]

2.2 | Circulating current control

Each CC cell consists of two capacitors and for successful operation of converter, the capacitor voltages must be regulated at specified voltage. The capacitor ripple voltages, on the other hand, change continually, resulting in a voltage disparity between the DC-Bus voltage and the phase-legs. Because of the voltage difference, a prominent second harmonic circulating current (SHCC) will flow through the phase-legs.[30] Circulating current cannot be directly measured; however, the mathematical equation is provided by

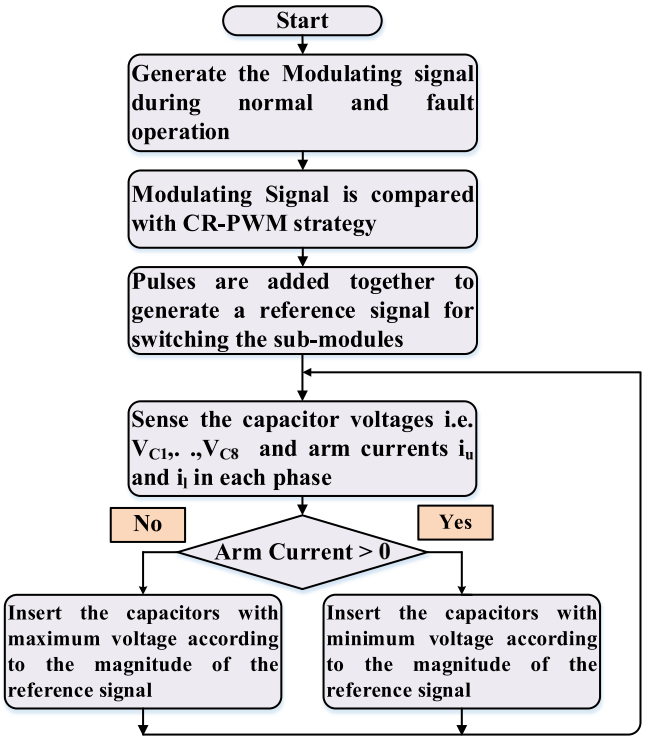

FIGURE 3 A sorting approach for regulating the capacitor voltages in CC cell modules of MMC.

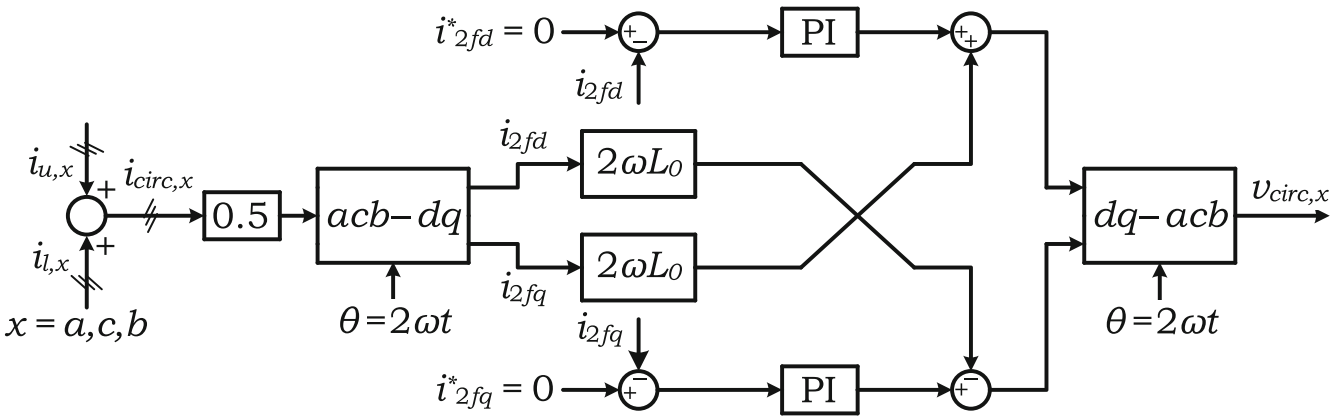

FIGURE 4 Circulating current control block diagram.

$$i_{circ,\,x} = \frac{i_{u,x} + i_{l,x}}{2} \tag{3}$$

The circulating current will result in excessive converter losses, but will not affect the ac-side waveforms. In this paper, a negative-sequence synchronous reference frame control is used to reduce or completely eliminate the SHCC. The equation involving the circulating current control dynamics is given by

$$v_{circ,x} = \frac{V_{dc}}{2} - \left(\frac{v_{ux} + v_{lx}}{2}\right) = R_0 i_{circ,x} + L_0 \frac{di_{circ,x}}{dt} \tag{4}$$

The circulating current $i_{circ,x}$ can be controlled by modulating the unbalance voltage $v_{circ,x}$ using negative sequence rotational reference frame. The block diagram of *d-q* reference frame based circulating current eliminator is shown in Figure 4.

3 | CONTROL OF GRID CONNECTED-MMC

In this paper, a five-level CC cell-MMC is used to independently inject the active and reactive power into the grid by using synchronous reference frame. The operation of MMC during normal and faulty conditions are described as follows.

3.1 | During normal operation

To control active and reactive power independently, d-axis component is aligned with grid voltage vector and q-axis component becomes zero.[31] Where v_{gd}, v_{gq} are d- and q-axis components of grid and v_{id}, v_{iq} are components of MMC. i_d and i_q are the components of current flowing through MMC. The active and reactive power are given by

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_{gd} & v_{gq} \\ -v_{gq} & v_{gd} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{5}$$

When the d-axis component is aligned with the v_{gd}, then $v_{gq} = 0$. If the reference active and reactive powers are p^* and q^*, respectively, then the d- and q-axes reference currents are given by

$$i_d^* = \frac{p^*}{v_{gd}} \tag{6}$$

$$i_q^* = \frac{q^*}{v_{gd}} \tag{7}$$

The overall block diagram of grid connected MMC is shown in Figure 5. Under normal operation of MMC, the reference reactive power is set to zero for operating the MMC at unity power factor.

The reference signals for switching upper and lower sub-modules given by Equations (1) and (2) are modified to eliminate SHCC are given by Equations (8) and (9) and the whole control of CC cell-MMC along with current control reference signals is shown in Figure 6.

$$v_{ux\_ref} = \frac{V_{dc}}{2} - v_{ix}^* - v_{circ,x} \tag{8}$$

$$v_{lx\_ref} = \frac{V_{dc}}{2} + v_{ix}^* - v_{circ,x} \tag{9}$$

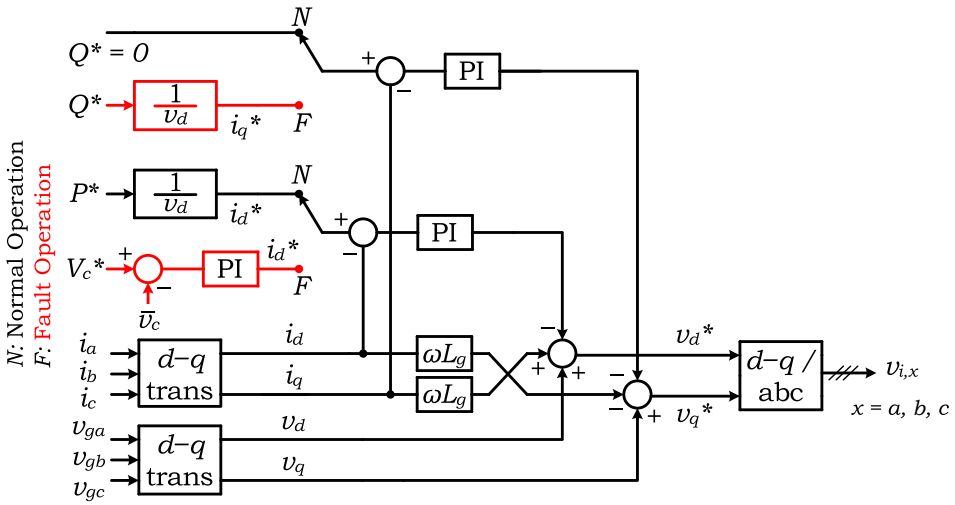

FIGURE 5 Current control block diagram of grid connected converter.

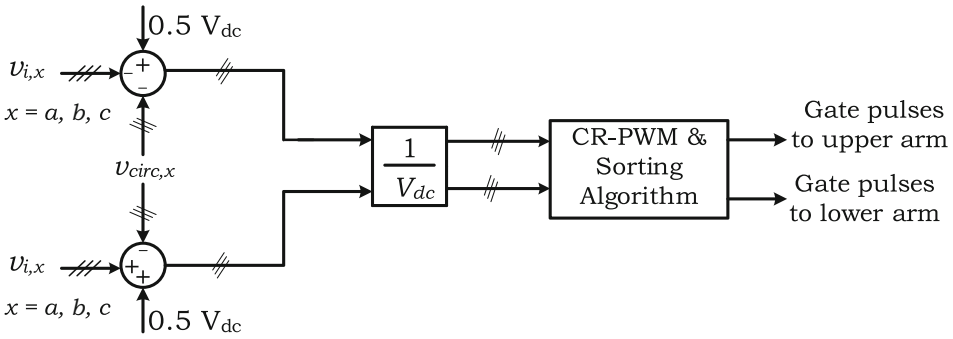

FIGURE 6 The control block diagram of CC cell-MMC during normal operation for gating pulse generation.

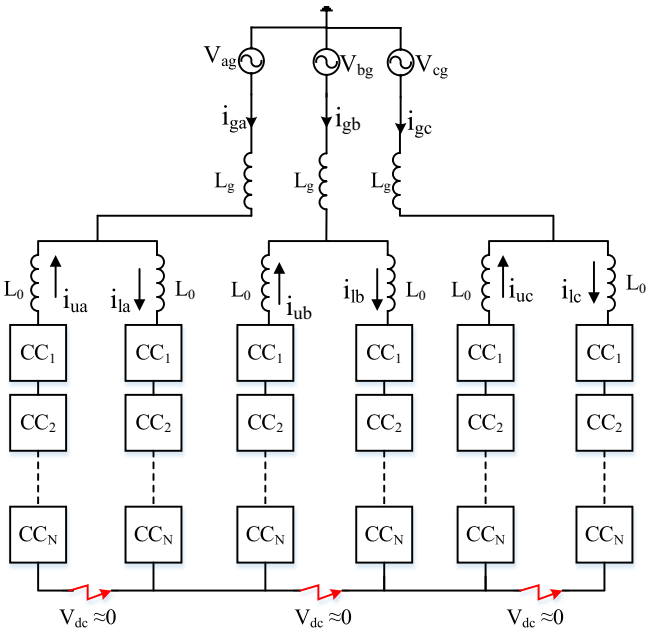

FIGURE 7 CC cell-MMC restructured to CMC during DC-Bus fault.

3.2 | During the occurrence of DC-Bus fault

When the DC fault occurs the dc voltage collapse to zero that reflects to short circuit. This short circuit restructures the CC cell-MMC configuration to cascaded multilevel converter (CMC) configuration with upper and lower arm as parallel units in single phase as shown in Figure 7. If parallel units of upper and lower arms are not controlled properly, the circulating currents flow between the parallel and phase units. To avoid circulating currents carrier rotation (CR) pulse width modulation is adopted. For satisfactory operation of the CMC, the mean voltage of capacitors in three phases need to be balanced. To achieve this condition, a zero-sequence voltage injection (ZSVI) using a simple control strategy is employed to exchange energy between the three phases.

In this paper, α-β reference frame is used to compute the accurate amplitude and phase of ZSV to be injected into three phases. The mathematical equations involving ZSVI are as follows:

The mean voltage of capacitors in each phase is given by

$$\overline{v}_{cx} = \frac{1}{8}(v_{cx1} + v_{cx2} + v_{cx3} + v_{cx4} + v_{cx5} + v_{cx6} + v_{cx7} + v_{cx8}) \; ; \mathrm{x} = \mathrm{a}, \mathrm{b}, \mathrm{c} \tag{10}$$

The overall mean voltage of capacitors of three phases is given by

$$\overline{v}_c = \frac{1}{3}(\overline{v}_{ca} + \overline{v}_{cb} + \overline{v}_{cc}) \tag{11}$$

The mean voltage of capacitors in each phase includes a DC component and a second harmonic component; a notch filter is employed to eliminate the second harmonic component, and the bode plot of the notch filter is shown in Figure 8.

The difference between overall average voltage of capacitors and average voltage of capacitors in individual phases are converted into α-β reference frame to compute the amplitude and phase angle of ZSVI is given by

$$\begin{bmatrix} \Delta\overline{v}_{C\alpha} \\ \Delta\overline{v}_{C\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} \overline{v}_c - \overline{v}_{ca} \\ \overline{v}_c - \overline{v}_{cb} \\ \overline{v}_c - \overline{v}_{cc} \end{bmatrix} \tag{12}$$

The resultant amplitude and phase angle of ZSVI is given by

$$\Delta\overline{v}_c = \sqrt{\Delta\overline{v}_{C\alpha}^2 + \Delta\overline{v}_{C\beta}^2} \tag{13}$$

$$\phi_o^* = \tan^{-1}\frac{i_q}{i_d} - \tan^{-1}\frac{\Delta\overline{v}_{C\beta}}{\Delta\overline{v}_{C\alpha}} \tag{14}$$

The zero-sequence voltage to be injected into each phase is obtained by Equation (15), and the complete control structure of ZSVI is shown in Figure 9.

$$v_0^* = \sqrt{2} * K_0 * \Delta\overline{v}_C * \sin\left(\omega t + \phi_0^*\right) \tag{15}$$

The reference signal for upper arm and lower arm sub-modules during fault is given by Equations (16) and (17). The control block diagram illustrating the overall operation of the CC cell-MMC during a DC-Bus fault is shown in Figure 10.

$$v_{ux\_ref} = -v_{ix}^* - v_0^* \tag{16}$$

$$v_{lx\_ref} = v_{ix}^* + v_0^* \tag{17}$$

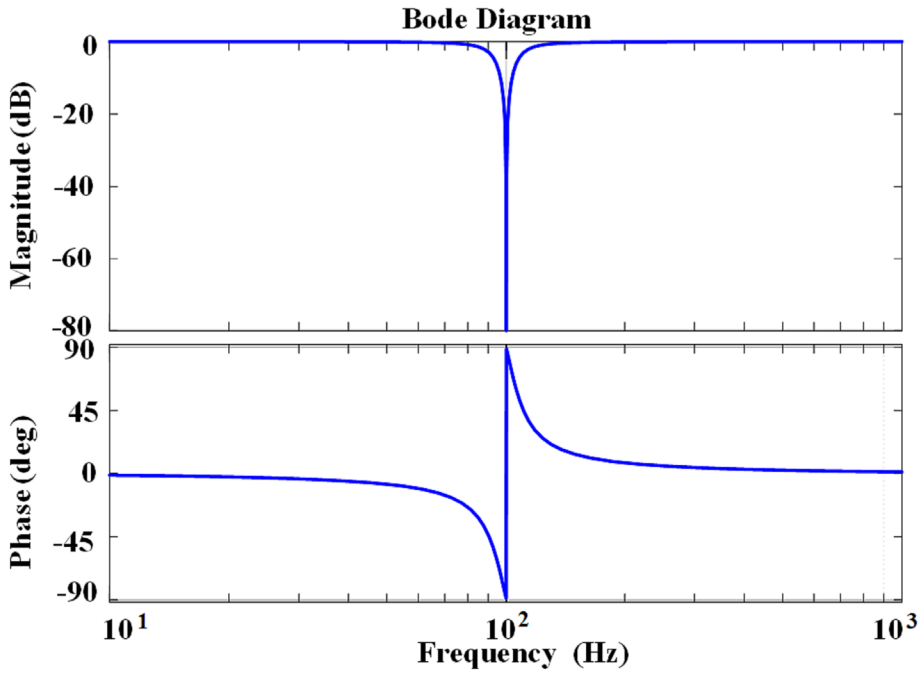

FIGURE 8 Bode plot of notch filter.

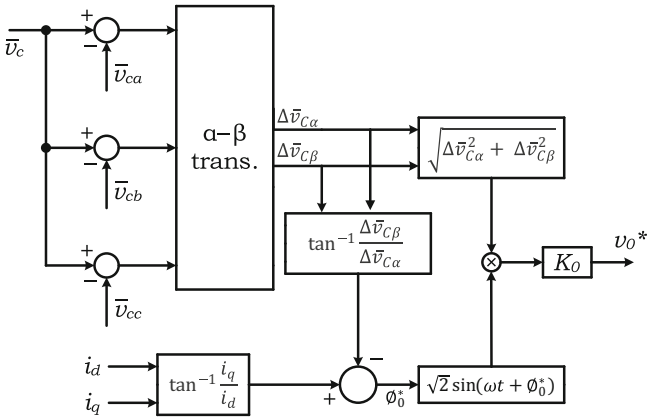

FIGURE 9 Control block illustration of zero sequence voltage infusion.

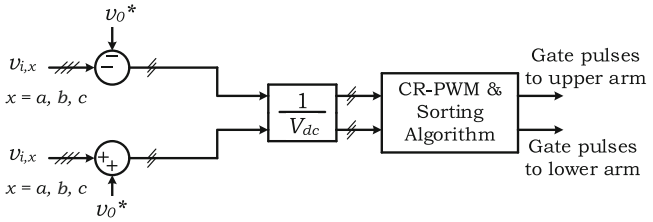

FIGURE 10 The control block diagram of CC cell-MMC during DC-Bus fault for gating pulse generation.

TABLE 1 Description of parameters used in test system.

Parameter	Value
Grid line to line RMS voltage (V_g)	6.6 kV
Grid interfacing inductance (R_g,L_g)	0.4 Ω, 10 mH
DC-Bus voltage (V_{dc})	12 kV
Number of sub modules per arm (N)	2
Arm inductance (R_0,L_0)	0.35 Ω, 5 mH
Sub module capacitance (C)	4700 μF
Carrier frequency (f_c)	1 kHz

4 | GRID-CONNECTED CC CELL-MMC SIMULATION STUDIES

To validate the performance of CC cell-MMC with circulating current control during normal operation and ZSVI during fault, two CC cell sub-modules per arm are considered. The carrier-rotation strategy PWM scheme is used between upper and lower arm sub-modules during normal and fault operation. The voltage balancing of capacitors is implemented using sorting algorithm to suit HVDC application. The parameters with it values considered in simulation are shown in Table 1.

4.1 | During normal operation

To validate the independent control of active and reactive power of grid connected MMC, a PI controller based closed loop control is adopted to control active power reference $(p^*) = -1.5\,\text{MW}\, to - 3\,\text{MW}$ and reactive power reference $(q^*) = 0$ to ensure unity power factor during inverter mode.

The simulation results of the active and reactive power shows that actual power is tracking the reference power and as shown in Figure 11A,B. Prior to activating CCSC, the arm currents in the three phases encompass DC, fundamental, and second harmonic current components. In an ideal scenario, the currents in the arms should be composed of DC and fundamental current components. A PI-based control is employed to regulate the second harmonic current circulating between the phase legs, and this control is initiated at 0.5 s. Beyond this time point, the phase-a upper and lower arm currents comprise DC and the fundamental component as shown in Figure 11C. Before CCSC activation, the three-phase circulating current comprises a DC component and a second harmonic current component. Upon the initiation of CCSC at 0.5 s, the three-phase circulating currents showcase a DC component with minimal ripple, ensuring the effective operation of CCSC, as depicted in Figure 11D. To demonstrate the dynamic behaviour of the CCSC and grid current controllers, the active power reference is altered at 0.8 s, and the obtained results confirms the satisfactory performance of the controllers in response to rapid changes. Upon activating CCSC, adjustments should be confined to the arm currents and circulating currents, without impacting the AC side quantities. This is attributed to the absence of interconnection between the grid current controller and CCSC. As depicted in Figure 11E,F, the voltages and currents of the MMC, as well as the grid voltages and currents, remain unaffected upon CCSC activation. A marginal decrease in the ripple of the capacitor voltages across all three phases is expected, attributed to the regulation of the second harmonic current. The capacitor voltages of the phase-a upper and lower arms are shown in Figure 11G,H.

4.2 | During the occurrence of DC-Bus fault

The occurrence of a DC-Bus fault in HVDC system results in the collapse of the DC voltage source to zero, rendering the MMC unable to supply active power to the grid. To anticipate this, the active power reference is pre-emptively adjusted from $(p^*) = -3$ MW to Zero MW before the fault is initiated. During the fault, the converter operates as a STATCOM to enhance grid stability. To align with this operation, the reactive power reference is altered from$(q^*) =$ Zero MVar to -3 MVAR. Simultaneously, the online calculation of the active power current component (i_d^*) necessary to compensate for converter losses, is conducted as illustrated in Figure 5. Simulation results confirm that the actual active and reactive powers closely follow the references, as depicted in Figure 12A,B. While in STATCOM operation, the voltages of capacitors within each phase exhibit deviations from those in the other two phases. For instance, the deviations among the first capacitors in all three phases, as illustrated in Figure 12C, show an average difference of 10 V among them. The average difference among the capacitors increases with prolonged operation of the converter, posing a risk of instability. Given the zero DC-Bus condition, it is imperative to implement proper control measures to minimize the average difference in dc voltage among the three phases. To address this challenge, a control structure is employed, as illustrated in Figure 10, injecting fundamental frequency zero sequence voltage into the three phases. The results indicate that the deviation between corresponding capacitors in the three phases is significantly reduced through Zero Sequence Voltage Injection (ZSVI), and this deviation is virtually eliminated in approximately two cycles of the fundamental frequency upon activating the ZSVI controller, as demonstrated in Figure 12D. The three-phase voltage and current waveforms of CMC and grid are shown in Figure 12E,F. The zoomed version of phase-a voltage and current of CMC validate that CMC is operated in capacitive mode as the current waveform is leading the voltage by 90° and results are displayed in Figure 12G.

5 | REAL-TIME VALIDATION USING OPAL-RT

The OPAL-RT systems are employed to validate intricate systems. The Real-Time validation of the proposed CC cell-MMC is conducted using the OP4510 RCP/HIL FPGA-BASED REAL-TIME SIMULATOR. The presented results encompass both normal and fault operation within a single plot. At 1.2 s, active power undergoes a linear decrease and reaches zero at 1.3 s, marking the intentional initiation of a fault. During a fault, the active power does not become zero, as the converter draws an active power current component to compensate for its losses. In normal operation, the initial reference for reactive power is set at zero MVAR, gradually increasing to -3 MVAR at 1.3 s. The results demonstrate that both the actual active and reactive powers injected into the grid closely follow the reference active and reactive powers with a scale of (x-axis $= 0.1$ s/div and y-axis $= -2$ MW/div and y-axis $= -2$ MVAR/div), as depicted in Figure 13A. To eradicate the second harmonic circulating current, CCSC is initiated at 0.5 s, resulting in upper and lower arm currents comprising DC and fundamental components during only normal operation. During fault

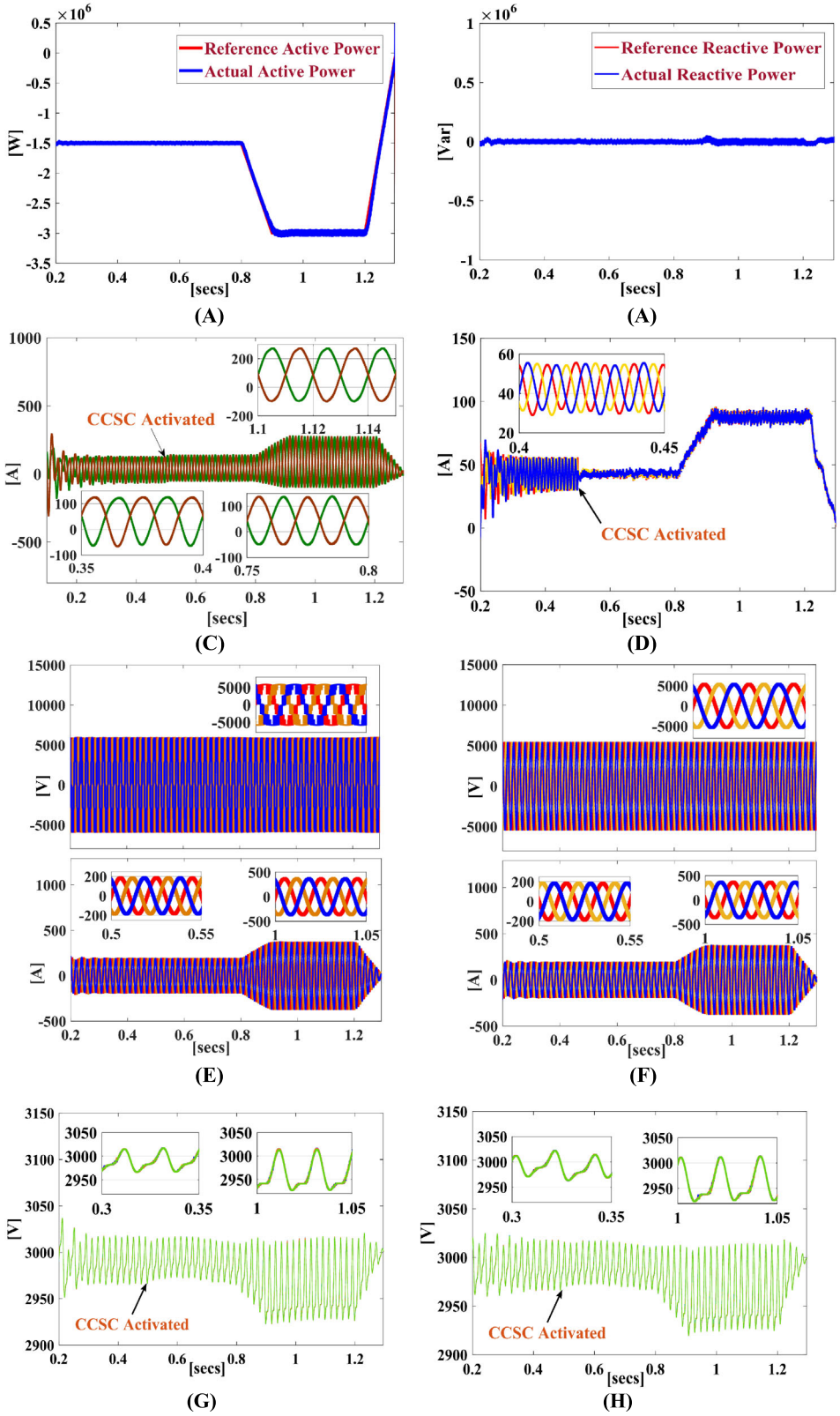

FIGURE 11 During normal operation. (A) Active power injected into grid. (B) Reactive power injected into grid. (C) Phase-a upper and lower arm currents. (D) Three phase circulating currents. (E) Three phase CC cell-MMC voltages and currents. (F) Three phase grid voltages and currents. (G) Phase-a upper arm capacitor voltages. (H) Phase-a lower arm capacitor voltages.

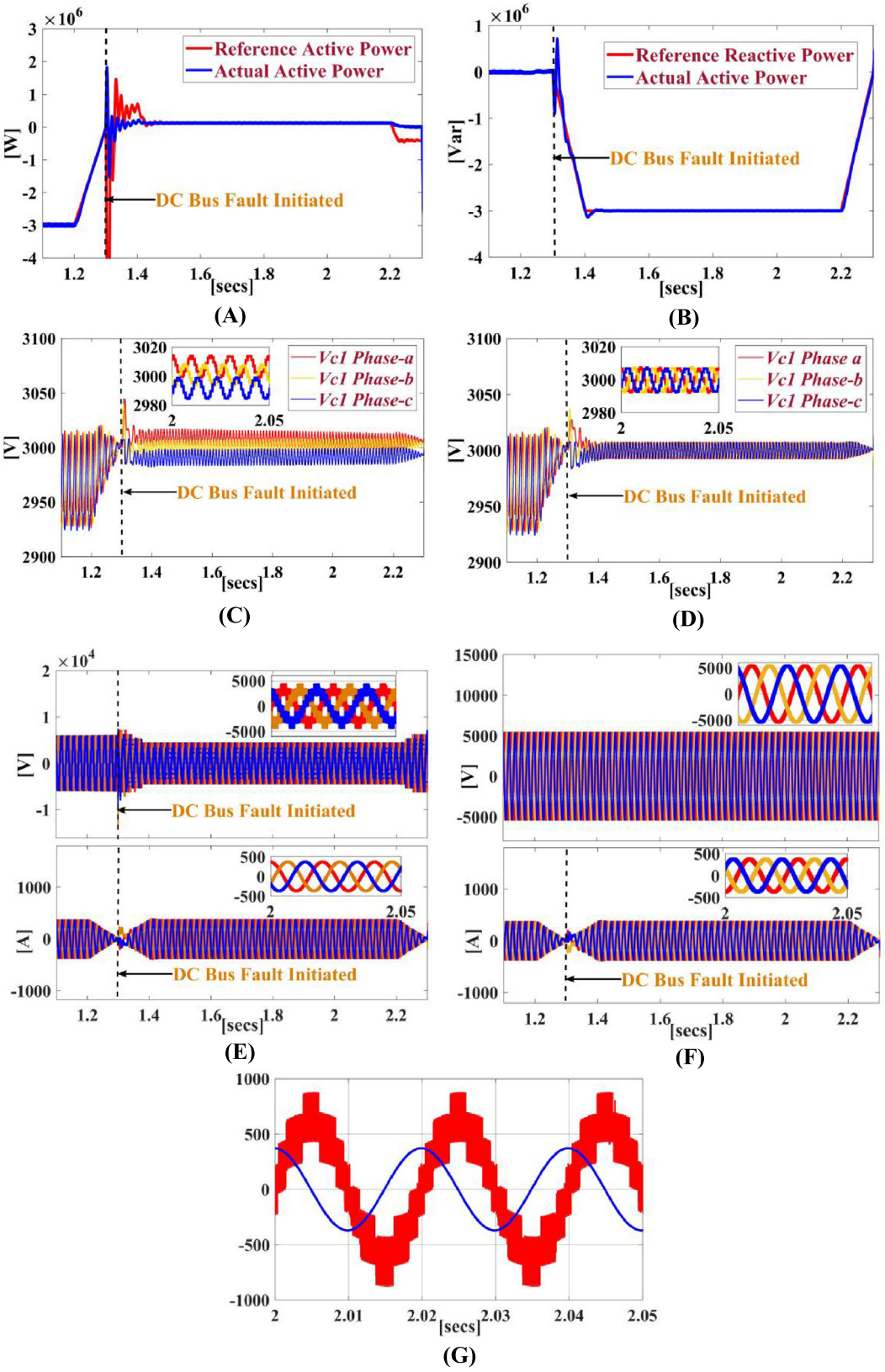

FIGURE 12 During fault operation: (A) Active power. (B) Reactive power. (C) First capacitor voltage in three phases without ZSVI. (D) First capacitor voltage in three phases with ZSVI. (E) Three-phase CMC voltages and currents. (F) Three-phase grid voltages currents. (G) Phase-a voltage (magnitude reduced by 5 times) and current of CMC operated in capacitive mode of operation.

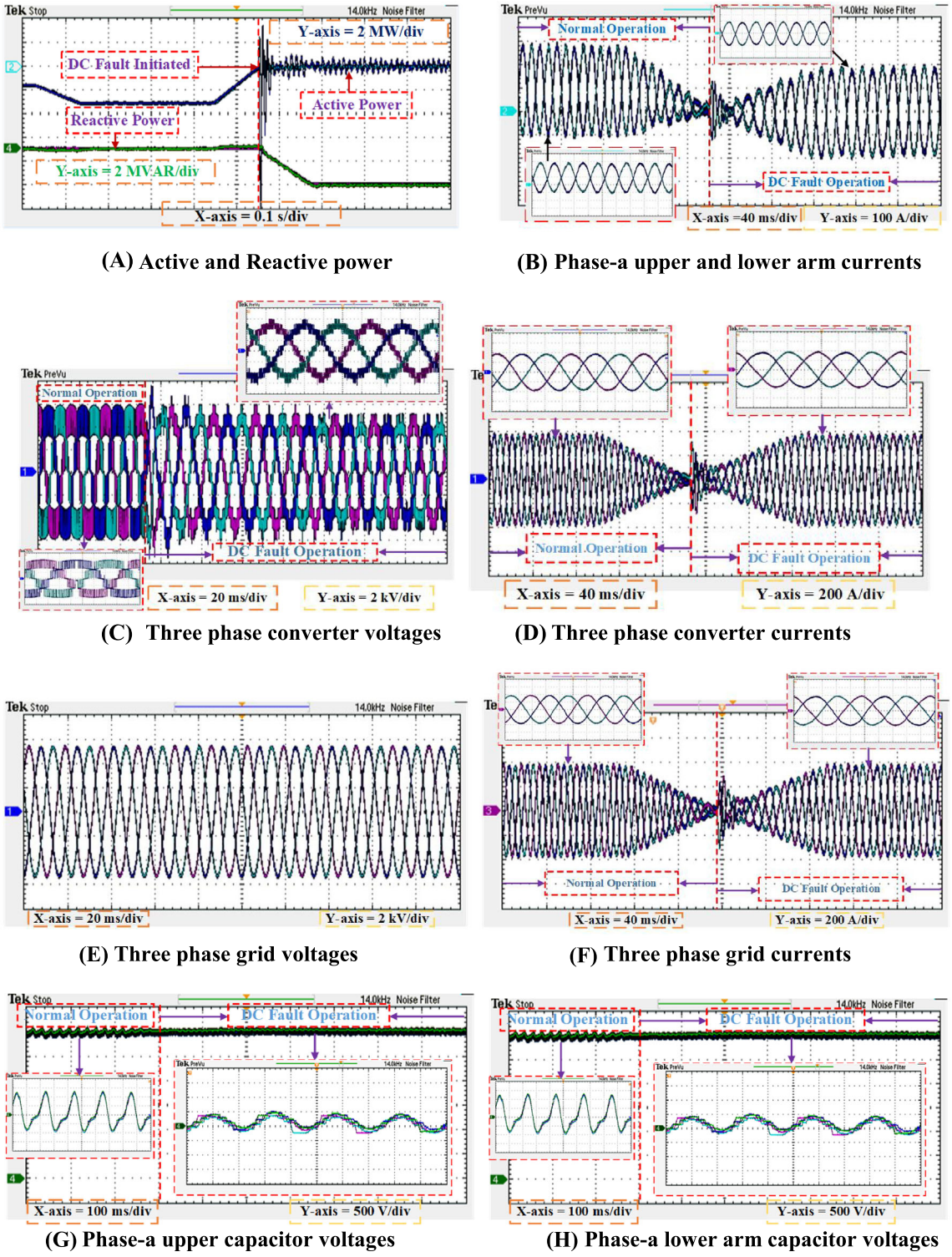

FIGURE 13 OPAL-RT results during both normal and fault operation. (A) Active and reactive power. (B) Phase-a upper and lower arm currents. (C) Three phase converter voltages. (D) Three phase converter currents. (E) Three phase grid voltages. (F) Three phase grid currents. (G) Phase-a upper capacitor voltages. (H) Phase-a lower arm capacitor voltages.

operation, the DC-Bus becomes zero, the arm current consists solely of reactive power current components, and the DC current is eliminated, as depicted in Figure 13B with a scale of (x-axis = 40 ms/div and y-axis = 100 A/div). During normal operation, that is, up to 1.3 s, MMC is able to generate five levels with a steps of 3 kV in the phase voltage measured between one phase leg and midpoint of dc link capacitors. When fault is created, CC cell-MMC restructure

TABLE 2 Comparison between the proposed MMC and the existing state-of-the-art topological configurations.

	HB-MMC[5]	FB-MMC[1]	CDSM-MMC[10]	ZPUC-MMC[11]	Proposed CC cell-MMC
DC-link voltage	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Number of SMs/arm	$2N$	$2N$	N	N	N
Total IGBTs in 3-phases	$24N$	$48N$	$30N$	$36N$	$36N$
Additional diodes in 3-phases	-	-	$12N$	-	-
Output voltage levels during normal operation	$2N+1$	$2N+1$	$2N+1$	$4N+1$	$2N+1$
DC fault blocking capability	No	Yes	Yes	No	Yes
STATCOM operation during DC-Bus fault	No	Yes	Yes	No	Yes
Reactive power (Q) injected during DC-Bus fault	-	Q	$0.5Q$	-	Q

Abbreviations: N, number of sub-modules per arm; Q, rated reactive power.

into cascaded multilevel converter (CMC) configuration with upper and lower arm as parallel units in single phase. Due to this restructure, there will be a significant increase in the number of levels in the phase voltage due to non-availability of ground reference point in CMC. Three phase CMC, Grid voltages with a scale of (x-axis = 20 ms/div and y-axis = 2 kV/div) are exhibited in Figure 13C,E. Three phase CMC, Grid currents with a scale of (x-axis = 40 ms/div and y-axis = 200 A/div) are depicted in Figure 13D,F. Upper and lower arm capacitor voltages ensure that sorting algorithm is successful in balancing the capacitor voltages at desired level with a scale of (x-axis = 100 ms/div and y-axis = 500 V/div) as shown in Figure 13G,H.

A comprehensive comparison between the proposed cross connected cell-based MMC and the existing state-of-the-art topological configurations, in terms of various indices, is presented in Table 2. It is noted from Table 2 that the proposed CC cell-MMC stands out due to its optimized design with 36 N total IGBTs, offering a cost-effective solution compared to the high IGBT count in FB-MMC (48 N). Additionally, the CC cell-MMC retains essential features like STATCOM operation during DC-Bus fault, overcoming limitations found in HB-MMC. Unlike CDSM-MMC, the proposed CC cell-MMC avoids additional diodes in 3-phases that results in increase in conduction losses compared to a discrete IGBT switch. Furthermore, its ability to inject rated reactive power (Q) during DC-Bus fault enhances flexibility, a feature lacking in CDSM-MMC. In ZPUC-MMC 36 N total IGBTs are required and produces $4N+1$ level, however, it may not supress the current during DC fault. These advantages collectively position the proposed CC cell-MMC as a balanced and efficient solution, outperforming the drawbacks of existing configurations.

6 | CONCLUSION

In this paper, a Cross Connected Cell (CC cell) based MMC handy in generating a greater number of levels in the output voltage involving a smaller number of power semiconductor devices has been presented. To suit HVDC application, capacitor voltage balancing using sorting algorithm and circulating current control has been performed. STATCOM operation of CC cell-MMC during DC-Bus fault implemented using decoupled current control and zero sequence voltage injection. The simulation results show dynamic performance of CC cell-MMC during normal operation and STATCOM operation during pole to pole fault. A comprehensive comparative analysis between the proposed MMC and existing state-of-the-art configurations has been conducted, highlighting its distinct advantages.

CONFLICT OF INTEREST STATEMENT

No potential competing interest was reported by the authors.

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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