International Journal of Electronics

ISSN: 0020-7217 (Print) 1362-3060 (Online) Journal homepage: www.tandfonline.com/journals/tetn20

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To cite this article: V. Hari Priya, D. Sreenivasarao & G. Siva Kumar (2024) An improved PWM with simplified unified switched logic (USL) for RSC MLIs, International Journal of Electronics, 111:9, 1517-1540, DOI: 10.1080/00207217.2023.2235724

To link to this article: https://doi.org/10.1080/00207217.2023.2235724

Published online: 17 Jul 2023.

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INTERNATIONAL JOURNAL OF ELECTRONICS
2024, VOL. 111, NO. 9, 1517–1540
https://doi.org/10.1080/00207217.2023.2235724

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An improved PWM with simplified unified switched logic (USL) for RSC MLIs

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ABSTRACT

Inevitability to reduce the size, cost and complexity of multilevel inverter (MLI) to evolve simplified RSC (Reduced switch count) MLIs has created diversified effects such as limited switching redundancies which further restricted modularity and flexibility of implementing PWM schemes. Among the PWM schemes of RSC-MLIs, modified reduced carrier (MRC) PWM with unified switching logic (USL) is the simplest and claims to be superior with the state of art in terms of implementation, line harmonic performance, imposing least controller computational burden (of 6.5 µS to realise a three-phase seven-level RSC-MLI) by adapting minimal carrier constraints. However, this is valid for sophisticated digital controllers such as dSPACE MicroLabBox, but not for low-end cost-effective controllers such as dSPACE1104 (imposing a computational burden of nearly 25 µS to control a single-phase RSC-MLI). Thus, this paper proposes an improved USL which adopts no carrier constraints and operates with less computational burden over the conventional USL. The proposed USL gives flexibility to the user to implement a part of the switching logic with analogue circuits and thereby avoid the requirement of high-end digital controller. The scalability and superiority of the proposed USL is demonstrated for symmetrical and asymmetrical configurations of popular cascaded T-type RSC-MLI. Efficacy of the proposed USL is demonstrated with dSPACE 1104 controller and dSPACE FPGA R&D Micro-lab Box.

ARTICLE HISTORY
Received 25 August 2022
Accepted 30 May 2023

KEYWORDS
Reduced Switching Count (RSC); Reduced carrier PWM; Unified Switching Logic (USL); Multilevel Inverter (MLI); T–type topology

I. Introduction

Multilevel inverters (MLI) are widely used for various high-power medium-voltage applications such as adjustable speed drives, PV/grid connected systems, active front end converters, active filters, electric vehicle (EV), battery energy storage systems (BESS) and custom power devices. Though classical MLI configurations i.e. cascaded H-bridge (CHB), diode clamped (DCMLI) and flying capacitor (FCMLI) gathered wide popularity, their increased device count for higher levels acted as restriction (Franquelo et al., 2008). Adapting asymmetrical dc sources in modular classical MLIs such as CHB has reduced their device count enormously; however, this created unequal device ratings, restricted modularity, reduced switching redundancies and effected fault tolerant ability (C. Rech &

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Pinheiro, 2007). On the other hand, to reduce the device count with preserving the simplified scalable topological structure, various reduced switch count (RSC) MLI configurations also reported are under various categories such as generalised, unit based, stacked, three-phase, switched capacitor and transformer-based configurations (Gupta et al., 2015; Omer et al., 2020; Salem et al., 2022; Vemuganti et al., 2021; Vijayaraja et al., 2016). However, it is to be noted that the topological and operational features of any RSC-MLI configuration depends on their physical arrangements. Considering the topological features of simplified structure, high scalability, presence of redundancies, modularity and asymmetric ability, various RSC-MLI configurations such as MLDCL, T-T-type, Switched series parallel sources (SPS), Series connected switched sources (SCSS), Hexagonal switched cell (HSC) based are reported in generalised configurations category (Vemuganti et al., 2021).

Investigating the RSC-MLI reported under various categories, T-type is one of the most simplified configurations with appreciable reduction in switch count (Odeh, 2014; Odeh et al., 2016; Park et al., 2003; Rahim et al., 2011, 2013). The T-connection of this configuration is formed by clamping the multiple nodes of dc-link with bi-directional switches. Further integrating T-connection with Full/Half bridge structure, this configuration is well reported for various stand-alone and grid connected applications. A three-phase three-level T-type with half-bridge is more efficient over the NPC and is well reported for PV-based grid connected systems. However, at higher level this configuration turns bulky and less impressive (Ceglia et al., 2006; U. M. Choi et al., 2015). On the other hand, T-type with full bridge structure offers simplified topological structure with appreciable reduction in switch count (J.-S. Choi & Kang, 2015; Park et al., 2003). However, absence of redundancies, unequal device ratings, limited modularity and in-ability to operate with asymmetrical sources acted as its limitations. In addition, absence of redundancies limited the feasibility of the configuration to achieve equal utilisation of dc sources, which further acted as a key limitation of T-type for energy storage applications. Thus, to over these limitations, cascading is adopted, where multiple T modules are connected in cascade. Cascaded T-type configuration promotes scalability preserving modularity (i.e. with-out effecting device ratings) and switching redundancies. Feasibility to achieve uniform performance of T-type modules enables it to serve as a viable alternative to CHB for PV, Energy storage and grid connected applications. However, operating cascaded T-type RSC-MLI with uniform power distribution of cascaded T-type modules with simplified control approach is quite challenging task.

On the other hand, topological arrangement to reduce the switch count in RSC-MLIs effected their switching operation such that popular PWM schemes of classical MLIs such as Level shifted PWM (LSPWM) and Phase shifted (PSPWM) are directly applicable for RSC-MLIs (Malinowski et al., 2009; Naderi & Rahmati, 2008; Sreenivasarao et al., 2013). Therefore, to implement RSC-MLIs, various low frequency schemes such as selective harmonic elimination (SHE) (Li et al., 2000; M. Wu et al., 2020), space vector modulation (SVM) (dos Santos et al., 2015; A. Masaoud, Ping, Mekhilef, & Taallah, 2014; A. Masaoud, H. W. Ping, S. Mekhilef, & A. S. Taallah, 2014; Sanjeevan et al., 2016; B. Wu, 2006), and 100 Hz carrier methods (Gautam et al., 2015,2016; Salem et al., 2022); Mixed frequency switching schemes such as Hybrid PWM and various carrier frequency PWM such as multireference and multicarrier are reported for RSC-MLIs (Kouro et al., 2010; McGrath & Holmes, 2002; B. Wu, 2006).

Selective Harmonic Elimination is a popular low frequency (modulating frequency) switching scheme reported for various symmetrical asymmetrical configurations of RSC-MLI such as MLDCL, SSPS, CBSC and HSC configurations (Babaei, 2008; Babaei & Gowgani, 2014; Li et al., 2000; Su, 2005; M. Wu et al., 2020). However, involvement of look-up tables and elusive mathematical calculations to determine the switching instants complicated its implementation for closed loop applications (Alishah et al., 2015). Space Vector modulation is another widely popular low frequency switching scheme reported for RSC-MLI configurations such as T-type and PUC (dos Santos et al., 2015; A. Masaoud, Ping, Mekhilef, & Taallah, 2014; A. Masaoud, H. W. Ping, S. Mekhilef, & A. S. Taallah, 2014; Sanjeevan et al., 2016). However imposing carriers on the modulating signal at the PWM stage, SVM can operate at carrier frequency. Though various unified/non-unified approaches are reported for implementing SVM, most of them involve complex trigonometric calculations to determine the switching instants and faces greater complexity at higher levels. In contrast, a simple low frequency carrier-based PWM using 100 Hz carrier is reported for various symmetrical and asymmetrical RSC-MLIs such as MLDCL, CBSC, basic unit, T-type and hybrid T-type (Alishah et al., 2015; Babaei, 2008; Babaei et al., 2015; Barzegarkhoo et al., 2016; Gautam et al., 2015,2016; A. Masaoud, Ping, Mekhilef, & Taallah, 2014; Su, 2005). Though low frequency switching schemes effectively reduce the switching losses, the presence of dominant lower order harmonic components in the output increases the filter size requirements.

Hybrid PWM is a mixed frequency switching scheme used to realise asymmetrical configuration of cascaded topologies (Babaei et al., 2013; Barzegarkhoo et al., 2016; C. Rech & J. R. J. I. T. O. I. E. Pinheiro, 2007). Cascading H-bridge to SSPS module, a 11-level asymmetrical configuration with hybrid PWM is reported in (Hinago & Koizumi, 2010). Though this scheme is simplified, asynchronization among low and high frequency operating modules produces sudden/unacceptable voltage spikes in output voltage. Among carrier-based modulation schemes of RSC-MLIs, multireference, switching function, reduced carrier and logical-expression-based PWMs are popular (J.-S. Choi & Kang, 2015; W. K. Choi & Kang, 2009; Goel et al., 2022; Gupta & Jain, 2014; Najafi & Yatim, 2012; Odeh, 2014; Odeh et al., 2016; Park et al., 2003; Rahim et al., 2011,2013; Salem et al., 2015). Further to support fault tolerant ability of few RSC-MLI, PWM schemes with non-uniform carriers are also reported (Peddapati & Prasadarao, 2022); however, they cannot support carrier rotation schemes. Multireference PWM is a generalised scheme reported for T-type configuration. This scheme is easily scalable and possesses unified switching logic to support any RSC-MLI configuration but produces degraded line THD performance (Odeh, 2014; Odeh et al., 2016; Rahim et al., 2011,2013). Switching function PWM using level shifted carrier arrangement is reported for RSC-MLI topologies such as switched dc sources (SDS) and reverse voltage (RV) (W. K. Choi & Kang, 2009; Gupta & Jain, 2014). This scheme is easily scalable and produces good line-voltage harmonic profile but, involvement of carrier constraints increases the computational burden on the controller for higher levels. Reduced carrier PWM involves a unipolar level shifted carrier arrangement where (n-1)/2 carrier is involved to control an n-level inverter (Singh et al., 2022). The poor line-voltage harmonic performance of the conventional reduced carrier (CRC) is addressed with modified reduced carrier (MRC) arrangement (J.-S. Choi & Kang, 2015; Najafi & Yatim, 2012; Park et al., 2003,2003; Salem et al., 2015). However, to produce good line-voltage

harmonic profile MRC forces the PWM to operate in synchronous mode and restricts the carrier frequency to be 3*n* multiple of modulating frequency (Park et al., 2003). However, the scalability of the reduced carrier PWM depends on the switching logic applied.

Various multi-carrier (Hinago & Koizumi, 2012) and reduced carrier (RC) PWM schemes (J.-S. Choi & Kang, 2015; Najafi & Yatim, 2012; Park et al., 2003; Salem et al., 2015) involving logical expressions are reported for T-type and reverse voltage RSC-MLI configurations (Babaei, 2008; Babaei et al., 2013,2015; Barzegarkhoo et al., 2016; Gautam et al., 2015,2016; A. Masaoud, Ping, Mekhilef, & Taallah, 2014; Su, 2005) 48 (Zhao et al., 2022). PWM schemes involving level shifted carrier arrangement followed by logical expressions to meet the desired switching operation are also reported (Jakkula et al., 2022; Kishore et al., 2022; Varesi et al., 2022). However, these schemes operate the switching pulses extracted from conventional logic with logical expressions such that final pulses extracted produces the desired operation of the inverter. However, in most of the cases, the reported logical expressions are not unified and vary with topological arrangement and output levels. In (dos Santos et al., 2015), a unified switch logic (USL) with logical expressions using reduced carrier arrangement is reported. The reported logical expression remains unified for any level, irrespective of the topology and dc voltage ratios (Vemuganti et al., 2018). This scheme reduces the involved carrier constraints (reduces comparators) and claims to be superior with respect to switching function PWM scheme in terms of computational burden. Nevertheless, this reported USL contributes to computational burden at higher level and necessitates the requirement of a sophisticated controller (Jakkula et al., 2022; Kishore et al., 2022; Varesi et al., 2022).

To simplify the switching logic and reduce comparator requirement, this work proposes an improved unified switching logic (USL) with no carrier constraints. To implement a n-level inverter, the proposed USL involves (*n*-1)/2 comparators where, the conventional USL requires (*n*-1) (Vemuganti et al., 2018). Further the proposed USL gives a flexibility to implement the switching logic by integrating analogue circuits and reduce the requirement of high-end micro controller. The proposed USL adopt a simplest approach and operate with less computation burden than the conventional USL reported in (Vemuganti et al., 2018). Irrespective of the topology, this scheme is scalable and generalisable for any symmetrical and asymmetrical RSC-MLI configuration. Further, with few modifications, the proposed USL supports conventional level shifted carrier arrangement and also facilitates uniform power/voltage distribution among the operating/cascaded modules.

This paper is organised as follows: Section-II presents the topology, operation, merits and limitations of cascaded T-type configuration. Section-III presents the proposed USL and demonstrates its implementation for nine-level cascaded T-type configuration. Further, the computation burden of proposed and conventional USL (for both CRC and MRC arrangements) on dSPACE low and high-end micro-controller is demonstrated for various levels, and superiority of the proposed USL is analysed. Sec-IV presents the ability of the proposed USL to realise symmetrical and asymmetrical configurations of cascaded T-type RSC-MLI in Simulink and hardware environment. Also, the ability of the proposed USL to facilitate uniform voltage distribution among the cascaded T-type modules is presented. Finally, conclusions are discussed in Sec-V.

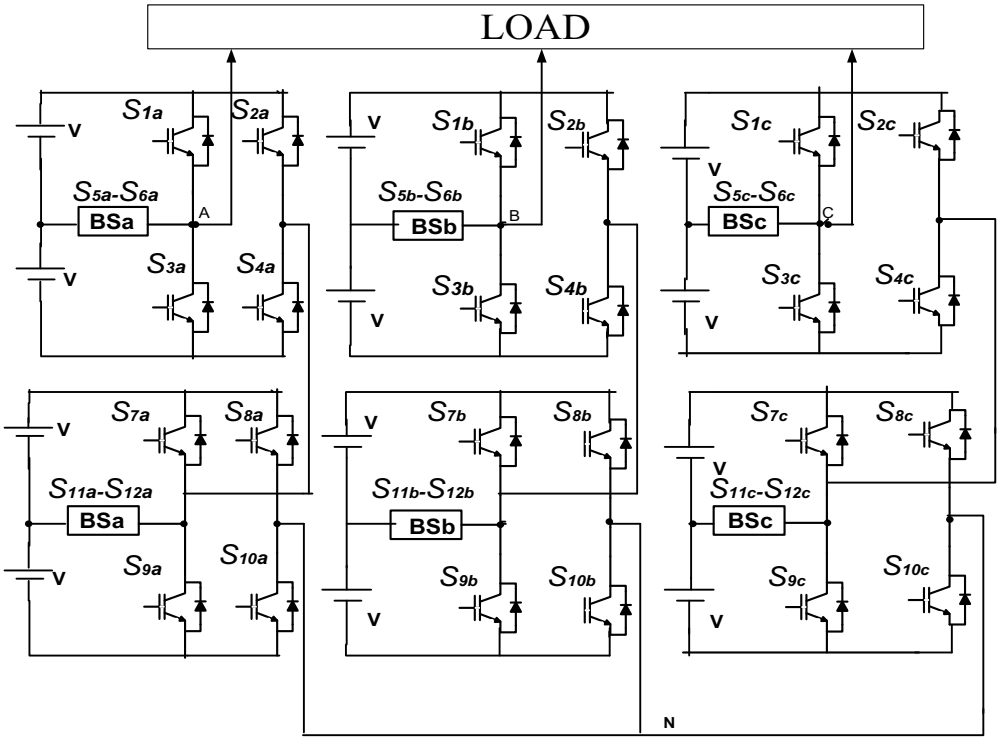


Figure 1. Three-phase cascaded T-type RSC-MLI with m=2, n=5.

II. Cascaded T-type RSC-MLI: topology and operation

T-type is popularly reported for five-level, and cascading two (k) five-level (m) T-type modules, Figure 1 shows the topological arrangement of cascaded T-type configuration. It is to be noted that dc-link voltages in individual T-type modules should always be identical. Operating Figure 1 with identical voltage ratios produces nine-level phase-voltage. Similarly, operating Figure 1 with binary and trinary voltage ratios produce 13-levels and 17-levels in phase-voltage. The comparison of device count and total standing voltage of this configuration (Figure 1) with CHB and T-type is shown in Figure 2.

Figure 2 shows the potential ability of cascaded T-type to serve as viable alternative to CHB. Scaling cascaded T-type configuration can be carried out either by increasing number of cascaded modules (k) or by increasing the levels (m) produced by each T-type module. Connecting an additional five-level T-type to Figure 1, i.e. selecting $k = 3$ and $m = 5$ and operating with symmetrical voltages produces 13-level phase-voltages. On the other hand, scaling each five-level T-type to seven-level of Figure 1, i.e. selecting with $k = 2$ and $n = 7$, and operating with symmetrical voltages also produces 13-level phase-voltage. Though both the configurations produce 13-level phase-voltage, their device count requirement and total standing voltage differ as given in Table 1.

Table 1 concludes that less device count requirement is less for *case*-2, i.e. $k = 2$ and $m = 7$, but *case*-1, i.e. $k = 3$ and $m = 5$, operates with less device ratings. Also, the available switching redundancies for $k = 3$, $m = 5$ promotes its ability to achieve fault tolerant operation and superiority over $k = 2$ and $m = 7$. Finally, referring to the phase-

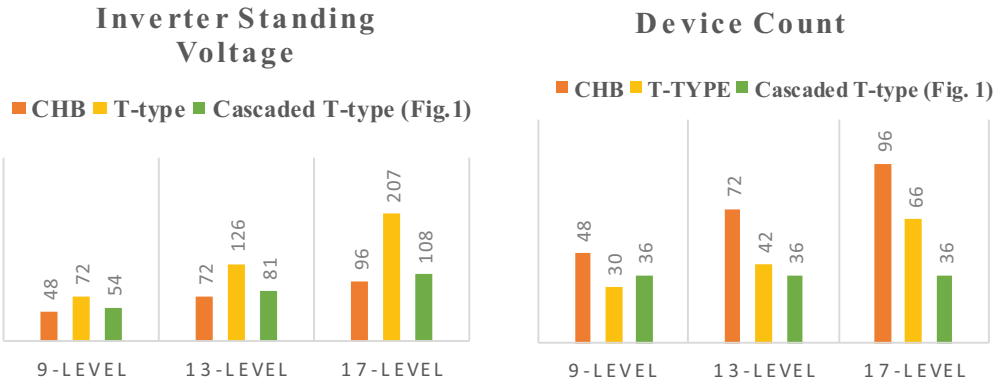


Figure 2. Comparison of device count and standing voltage of cascaded T-type with CHB and T-type.

Table 1. Device count and standing voltage of 13-level configurations of Cascaded T-type.

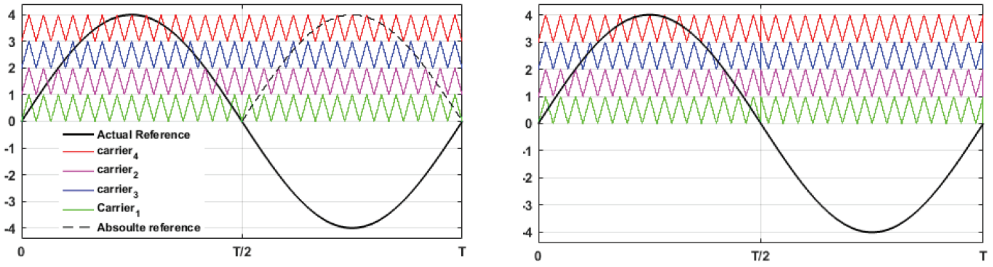
Topology (identical voltage ratios)	Switch count	Inverter standing voltage	Phase voltage levels produced	Max device blocking voltage
Case-1: k = 3, *m* = 5	15 × 3	30 × 3 Vdc	13-level	2 Vdc
Case-2: k = 2, *m* = 7	12 × 3	40 × 3 Vdc	13-level	3 Vdc

voltage levels obtained from Figure 1, it can be stated that cascading '*k*' number of '*m*-level' T-type modules produces *k*(*m*-1) +1 level in phase-voltage. However, operating the cascading T-type MLI to achieve the desired output voltage is a challenging task.

Literature reports multireference modulation scheme as a popular scheme to realise T-type configuration. However, involvement of multiple references creates difficulty to implement with digital controllers for closed loop applications. In addition, the degraded line THD performance and inability to directly apply for cascaded T-type configurations act as other limitations. On the other hand, though reduced carrier PWM is the simplified scheme, its conventional switching logic is not suitable for realising cascaded T-type configuration. The proposed modulation scheme to realise considered configuration RSC-MLI is presented in yjr next section.

III. Proposed modulation scheme

To implement RSC-MLI, this section proposes a simple unified switching logic (USL) which can support conventional reduced carrier (CRC), modified reduced carrier (MRC) and LSPWM carrier arrangements. The implementation of the proposed logic is explained here considering the CRC arrangement. Figure 3(a) shows CRC arrangement to control a nine-level inverter; however, to attain good line-voltage THD performance, modified reduced carrier (MRC) arrangement shown in Figure 3(b) can be used (Vemuganti et al., 2018). Switching pulses obtained by comparing each carrier with rectified reference of Figure 3 are shown in Figure 4, where each pulse is responsible for attaining specific voltage level. The overlapped nature of these pulse shows their inability to directly control an RSC-MLI with least/no redundancies. To extract desired non overlapped switching



(a) Conventional reduced carrier (CRC) arrangement

(b) Modified Reduced carrier (MRC) arrangement

Figure 3. Carrier arrangement of reduced carrier PWM for Nine-level.

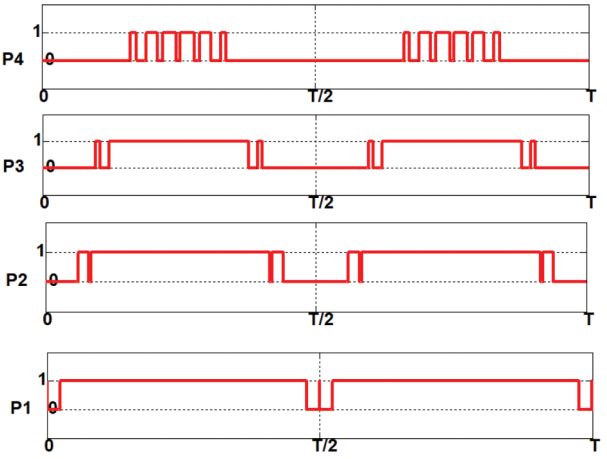


Figure 4. Conventional (overlapped switching pulses).

pulses shown in Figure 5, a unified switching logic adapting a generalised logic expression is reported in (Vemuganti et al., 2018).

Implementation of this conventional USL to control single-phase nine-level inverter is shown in Figure 6. The involved carrier constraints in this conventional USL shown in Figure 6 increases controller computational burden at higher levels. Thus, this section proposes an improved USL which adapts no carrier constraints to produce desired switching operation of the inverter. The objective of the proposed USL is to operate overlapped switching pulses shown in Figure 4 with a generalised logical expression such that it produces non-overlapped pulses shown in Figure 5. Analyzing Figure 5 reveals that the desired non-overlapped pulse P_1* is responsible to obtain V-level of voltage 0-V and V-2 V voltage bands in phase-voltage. In detail P_1* is active for reference greater than carrier$_1$ i.e. V-level in 0-V band and, for reference less than carrier$_2$, i.e. V-level of V-2 V voltage band. Similarly, P_2* is responsible to obtain 2 V-level of V-2 V and 2 V-3 V voltage bands in phase-voltage. Similarly, P_3* and P_4* are responsible to attain 3 V and 4 V levels respectively. Thus, it can be stated that the desired pulse P_1* can be obtained by operating P_1 and P_2 with logical expression. To derive this logical expression, Figure 7 (a) presents the switching states of P_1, P_2 and P_1* and shows a two-variable k-map of P_1

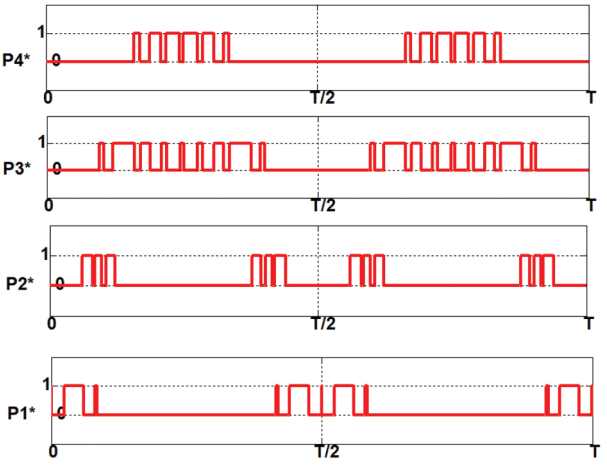


Figure 5. Desired non-overlapped switching pulses.

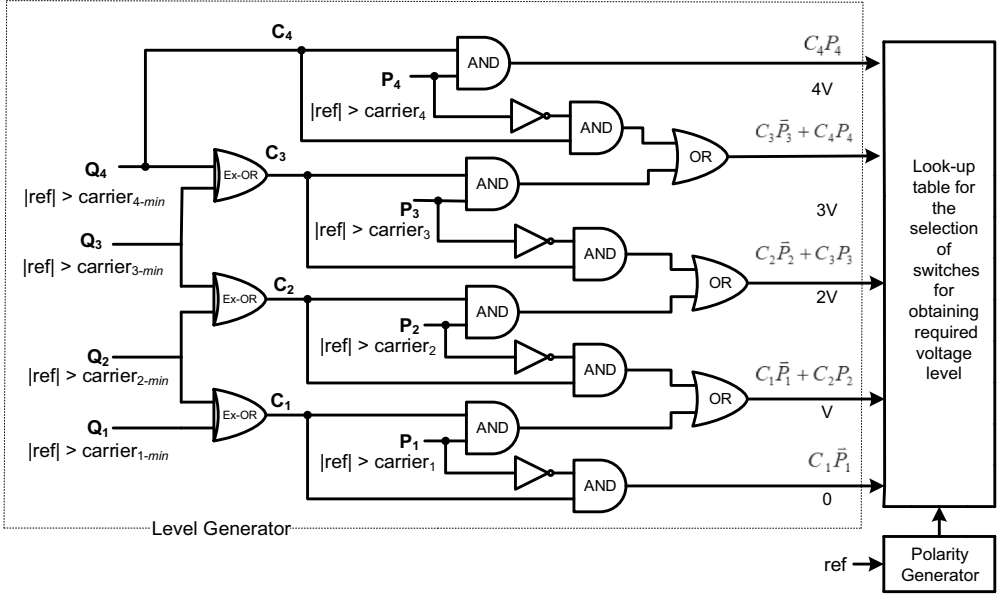
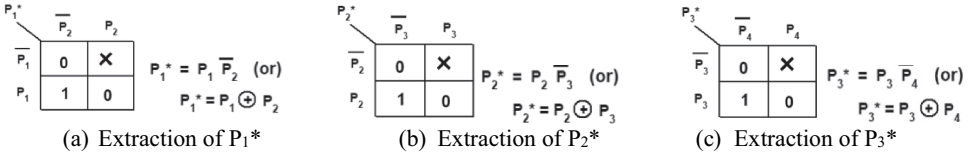


Figure 6. Schematic diagram of conventional USL for nine-level.



(a) Extraction of P_1* (b) Extraction of P_2* (c) Extraction of P_3*

Figure 7. Switching states and two-variable K-map for obtaining desired switching pulses for nine-level with proposed USL.

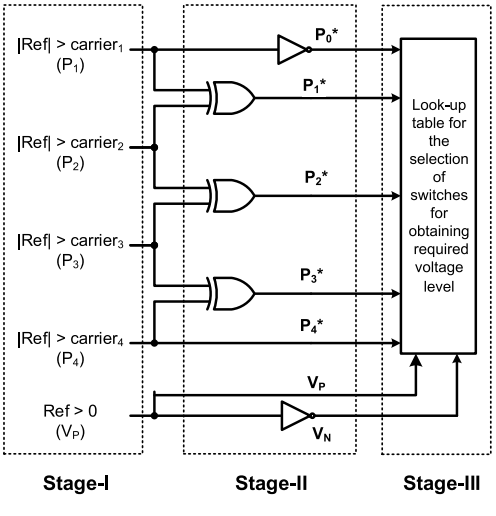
and P_2 to produce P_1*. Similarly, two variable K-maps to obtain logic expression of P_2*, P_3* are given in Figure 7 (b) and (c) respectively. However, no k-map is required for P_4*, as P_4* is identical to P_4 and can be directly obtained. Similarly switching pulse to attain zero-level in phase-voltage can be directly obtained complimentary pulse P_1, i.e. from (1-P_1).

The proposed switching scheme and application of extracted desired switching pulses to control a nine-level cascaded T-type inverter is shown in Figure 8. Each comparator produces a switching pulse by directly comparing the rectified reference and carrier signal, which is further given an XOR gate to extract the desired non-overlapped switching pulses. These XOR gates of stage-II and look-up table of stage-III can be included in micro controller or realised in external hardware using analogue circuits/logical gates (IC). Realization of look up table with analogue IC to exact switching pulses for nine-level cascaded T-type configuration is also shown in Figure 8.

Implementing stage-II and stage-III using analogue circuits avoids the requirement of high-end micro-controller. Thus, the proposed scheme gives a flexibility to the user to realise the partial switching logic in external hardware (logic gates), which is very much beneficial if the available micro-controller is not of high-end. In addition, the proposed unified switch logic supports both the reduced carrier and level shifted carrier arrangements. Thus in terms of computational burden the proposed unified switching logic is superior to the conventional unified switching logic reported in (Vemuganti et al., 2018). The proposed scheme can easily be generalised and scalable to control any level (odd) inverter. The generalised logical expression to exact switching pulses from the proposed switching logic for controlling a n-level inverter is shown in equation (1-5). Equation of the generalized switching logic for n-level inverter is shown in equation (6).

$$P_4{}^* = P_4 \tag{1}$$

$$P_3{}^* = P_3\,\bar{P}_4 \Rightarrow P_3 \oplus P_4 \tag{2}$$



Look-up table implementation (with AND -OR gates) for 9-level cascaded T-type of Fig.1

Switch	Corresponding Pulse
S_1	$(V_P \bullet P_4^*) + (V_N \bullet (P_0^* + P_1^* + P_2^*))$
S_2	V_N
S_3	$(V_N \bullet P_4^*) + (V_P \bullet (P_0^* + P_1^* + P_2^*))$
S_4	V_P
S_5	$(V_P \bullet P_3^*)$
S_6	$(V_N \bullet P_3^*)$
S_7	$(V_P \bullet (P_2^* + P_3^* + P_4^*)) + (V_N \bullet P_0^*)$
S_8	V_N
S_9	$(V_N \bullet (P_2^* + P_3^* + P_4^*)) + (V_P \bullet P_0^*)$
S_{10}	V_P
S_{11}	$(V_P \bullet P_1^*)$
S_{12}	$(V_N \bullet P_1^*)$

Figure 8. Schematic diagram of proposed USL for nine-level.

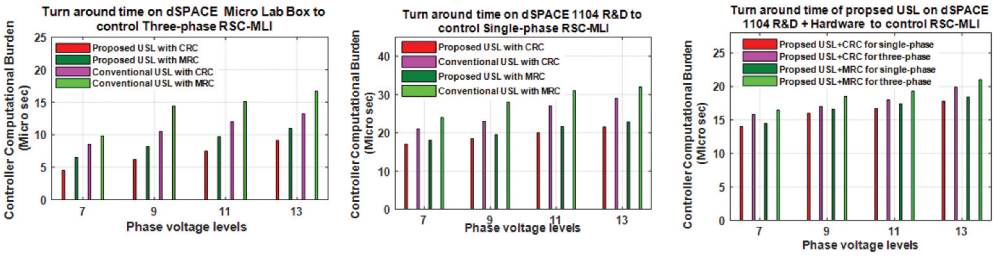


Figure 9. Computational burden imposed by the proposed USL on the dSPACE controller.

$$P_2{}^* = P_2\,\bar{P}_3 \Rightarrow P_2 \oplus P_3 \tag{3}$$

$$P_1{}^* = P_1\,\bar{P}_2 \Rightarrow P_1 \oplus P_2 \tag{4}$$

$$P_0{}^* = \bar{P}_1 \tag{5}$$

$$\begin{aligned} &P_{(n-1)/2}{}^* = P_{(n-1)/2} \\ &P_i{}^* = P_i \oplus P_{i+1} \;\; ; \;\; 1 \le i < (n-1)/2 \\ &P_0{}^* = \bar{P}_1 \;\; ; \end{aligned} \tag{6}$$

Furthermore, imposing few more modifications, the proposed unified logic can successfully support conventional level shifted carrier arrangement. It is to be noted that as the proposed switching logic minimises comparator requirement as it avoids imposing minimum and maximum constraints on the carrier. The superiority and easiness of the proposed USL is well understood comparing to the conventional USL 9-level shown in Figure 6. Comparing the schematic diagram of Figures 8 with 6 clearly verifies the superiority and less computation burden to implement proposed USL. Adopting conventional reduced carrier (CRC) and modified reduced carrier (MRC) arrangements, the recorded computational burden of conventional and proposed USL on dSPACE 1104 and dSPACE Micro-lab Box controller is given in Figure 9. The computational burden is determined in terms of turnaround times (***μs***) and is recorded for 7, 9, 11 and 13-level T-type RSC-MLI configuration, for carrier frequency 3000 Hz. Further, to ensure the comparison more specific, Figure 9 is quantified and depicted in Table 2. Thus, Figure 9 and Table 2 reveal that turnaround time required to implement proposed USL is slightly less than conventional USL the sophisticated dSPACE MICROLAB Box controller.

However, this difference turns dominant with low end controller such as dSPACE 1104 controller at higher levels. Further implementing stage-II and III of the proposed USL with analogue circuits to realise the single-phase RSC-MLI, the recorded computational burden reduces effectively to 18 μs (for thirteen-level), where the conventional USL requires 32 μs. Further to analyse the harmonic performance and scalability of the proposed USL in obtaining desired output, its Simulink implementation for cascaded T-type configuration is presented in the next section.

Table 2. Computational burden of proposed and conventional USL on dSPACE controller.

		Computational burden or Turnaround times (μs) on dSPACE					
		Micro Lab Box to control three-phase RSC-MLI		*1104 R&D* to control single-phase RSC-MLI		*1104 R&D* + Hardware to control RSC-MLI	
						single-phase	*Three-phase*
Ph-volt levels	Carrier arrangement	Proposed USL	Conventional USL	Proposed USL	Conventional USL	Proposed USL	Proposed USL
7-level	CRC	4.5	6.5	17	22	14	15.8
	MRC	8.5	9.8	18	24	14.5	16.5
9-level	CRC	6.2	8.2	18.5	23	16	17
	MRC	10.5	14.4	19.5	28	16.6	18.5
11-level	CRC	7.5	`9.7	20	27	16.7	18
	MRC	12	15.1	21.6	31	17.4	19.3
13-level	CRC	9.1	11	21.5	29	17.8	19.9
	MRC	13.2	16.7	22	32	18.1	21

IV. Implementation and performance validation of the proposed scheme

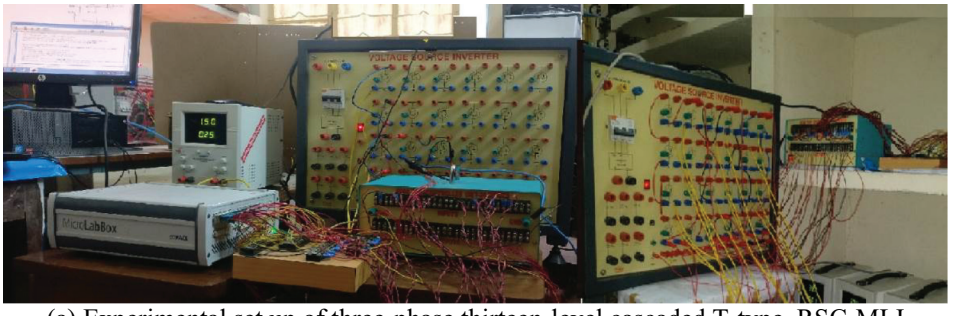
This section presents the implementation of proposed switching logic for cascaded T-type topology adapting MRC carrier shown in Figure 3(b) and LSPWM carrier arrangements. Performance of the proposed scheme is investigated on cascaded T-type configuration (shown in Figure 1) for symmetrical and asymmetrical voltage ratios in MATLAB and Experimental environment. Considered parameters for simulation and experimentation are given in Table 3. To present hardware validation of the demonstrated simulation results, a downscaled prototype of considered topology is developed using 24-switch IGBT module shown in Figure 10 is considered., and two of such IGBT modules are deployed for experimental prototype.

The isolated IGBTS in Figure 10 promotes the ability to support any topological arrangement with in the device rating. To serve the requirement of each input dc-source, dual channel regulated power dc supplies of 30 V/5A are used. Each of the multiple RPS used in the three-phase structure is further controlled to provide the required dc source voltage of 15 V and 30 V. To control the developed inverter module, its corresponding switching scheme is loaded on dSPACE 1104 R&D controller, and required switching pulses are extracted. Also, a time delay of 2 μS is considered in dead band circuit. It is to be noted that the simulation and experimental performance of the proposed and conventional USL are recorded adapting MRC arrangement.

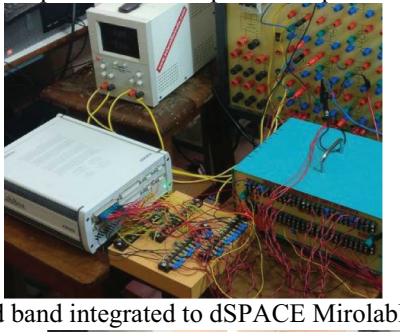
The recorded phase voltage, line voltage and voltage contributed of each T-type module in phase-a of Figure 1 for symmetrical voltage ratios are shown in Figure 11. Though Figure 11 demonstrates satisfactory phase and line voltage

Table 3. Simulation and experimental parameters.

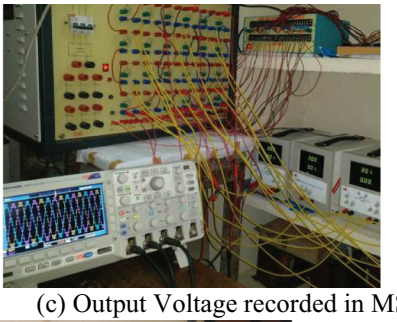
Components-Parameter	Simulation	Experimental	
Regulated dc-power supply (each)	100V	30V/5A single channel and 30V/3A dual channel RPS used to obtain 15V/30V dc Input	
Amplitude modulation index (m_a)	0.96	0.96	
Carrier frequency (fsw)	3000 Hz	30000 Hz & 2000 Hz	
Dead band	—	2 μS	
Measurement	—	4 channel MSO & Fluke metre	
Sample time	1 μS	50 μS (dS1104)	20 μS (Microlab Box)



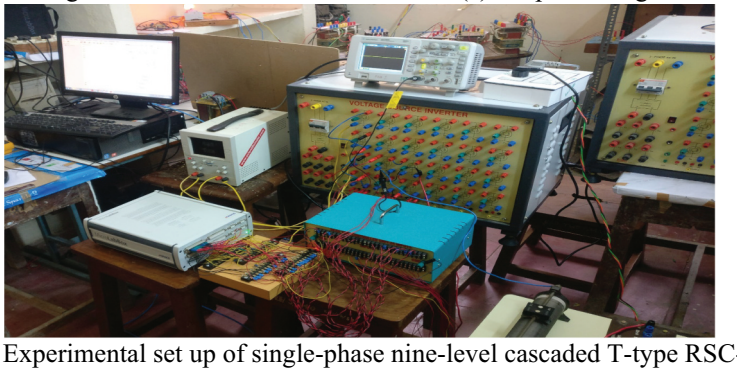
(a) Experimental set up of three-phase thirteen-level cascaded T-type RSC-MLI



(b) Dead band integrated to dSPACE MirolabBox



(c) Output Voltage recorded in MSO



(d) Experimental set up of single-phase nine-level cascaded T-type RSC-MLI

Figure 10. Experimental set-up developed to realize considered RSC-MLI configurations.

performance, the depicted output voltage of each module of phase-*a* claims their dis-similar performance with low order harmonics and dominant harmonic m_f , where 'm_f' is the frequency modulation index defined as ratio of the carrier frequency to the modulating frequency. This dissimilar and non-uniform performance of the cascaded modules (in phase-a) can further be validated referring their corresponding voltage THD, i.e. 28.9% and 19.2%, RMS voltage, i.e. 130 V and 162 V, and load power contribution of each module, i.e. 2340W and 2780W respectively.

For uniform power distribution: To facilitate uniform load power contribution and identical performance of the cascaded modules, the switching pulses obtained from the proposed scheme are exchanged among the cascaded modules (per-phase) for every carrier cycle. However, the pulse rotation among the fundamental frequency switching

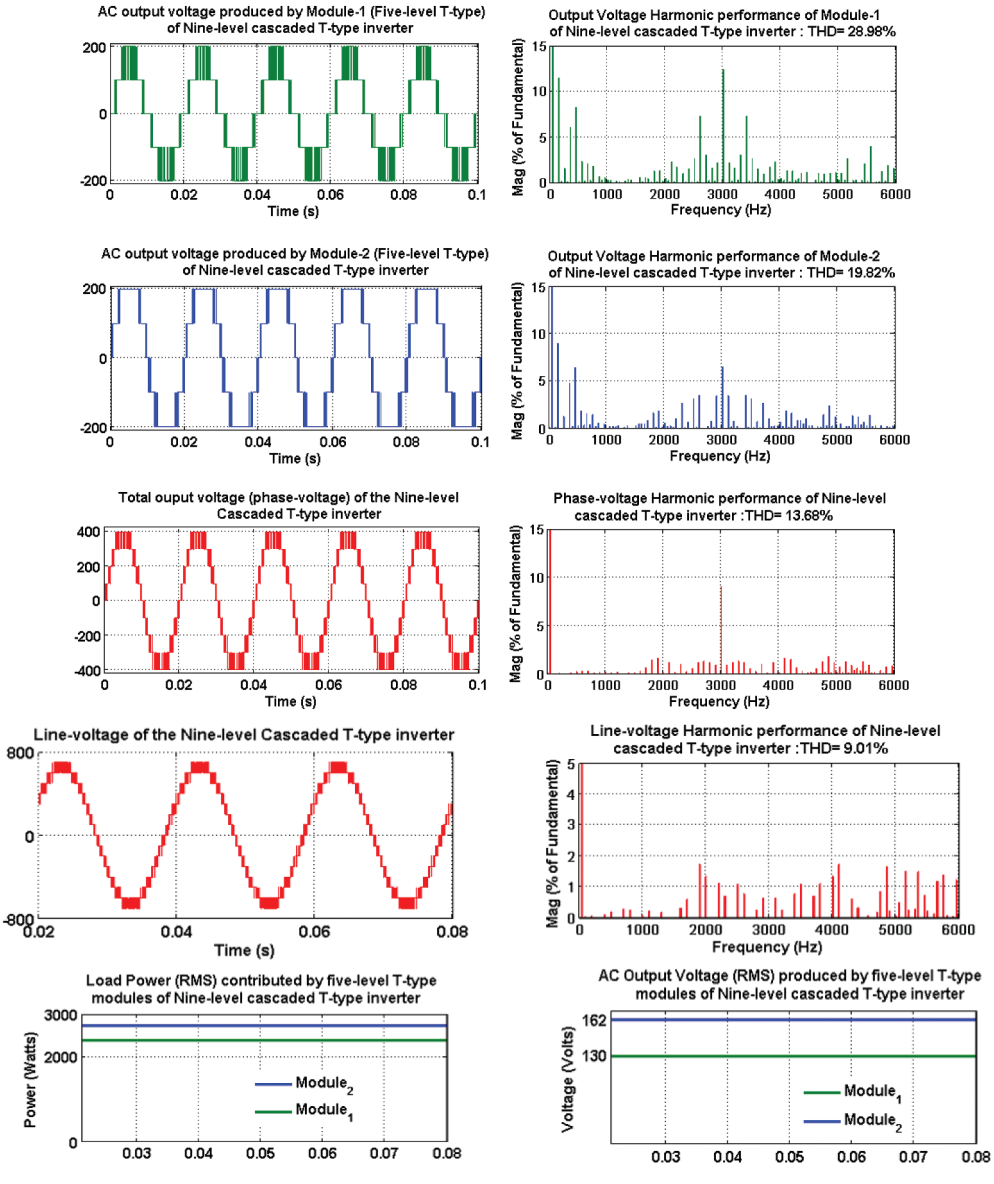


Figure 11. Simulink performance of Nine-level cascaded T-type Inverter with proposed PWM (non-uniform power distribution).

devices is not necessary, and switching pulse rotation among the the carrier frequency devices need to be mandatorily carried out.

The simulation results corresponding to proposed switching scheme to facilitate uniform power distribution of Figure 1 for nine-level are shown in Figure 12. The similar wave shape, identical performance of each cascaded T-modules (of phase-a) in terms of their corresponding output voltage THD, i.e. 26.98% and 26.87%, output voltage RMS, i.e. 146.5 V and 146.4 V, and load power contribution, i.e. 2559 W and 2559W, respectively, shown in Figure 12, demonstrate the ability of the proposed USL to achieve uniform power

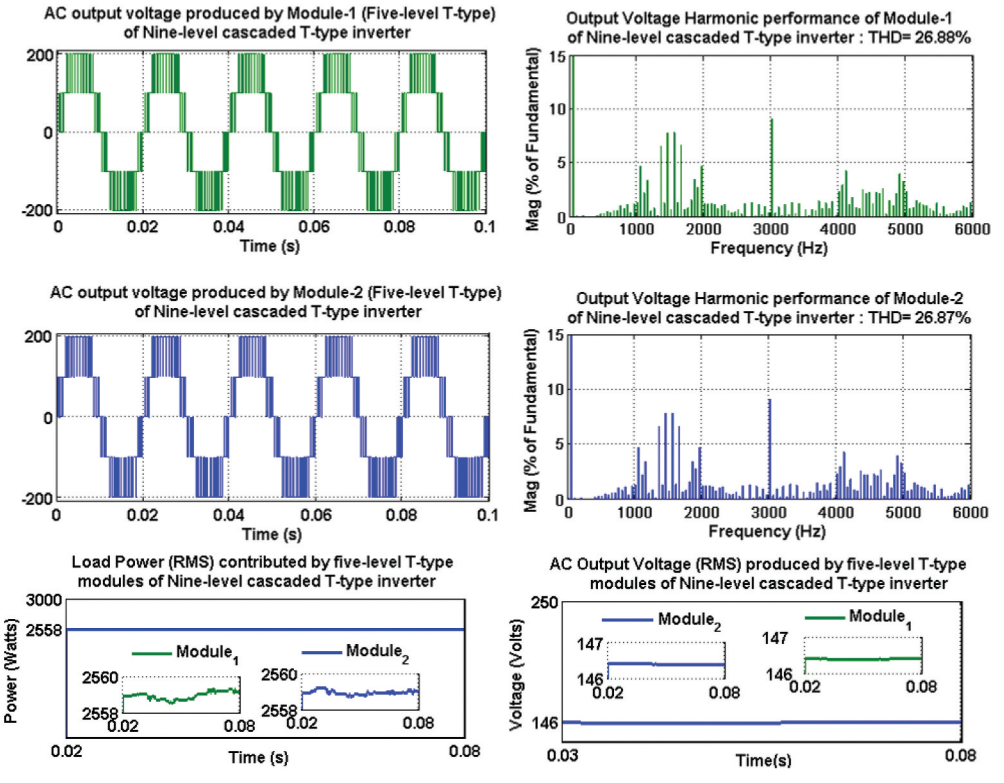


Figure 12. Uniform power distribution among five-level T-modules in nine-level cascaded T-type inverter.

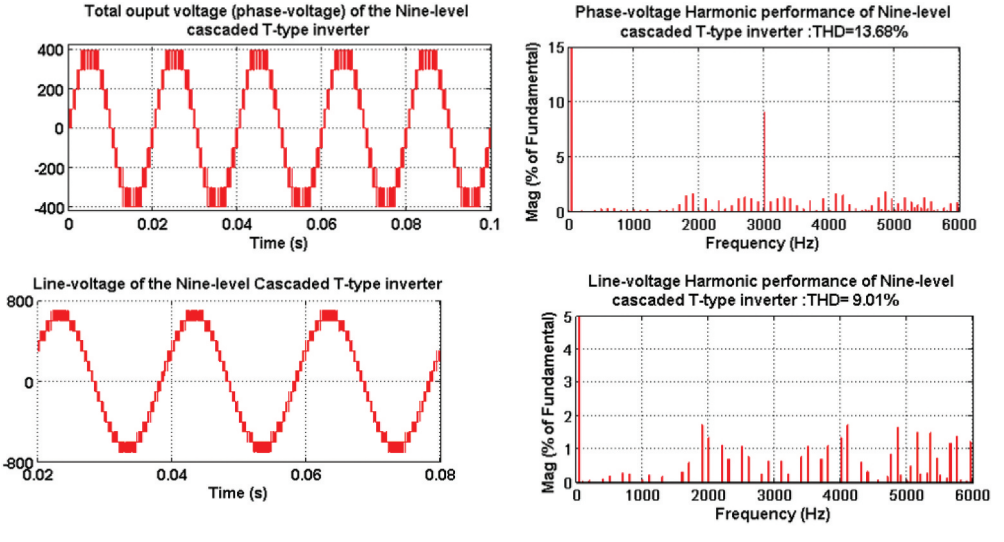


Figure 13. Simulink performance of nine-level cascaded T-type Inverter with proposed PWM facilitating uniform power distribution.

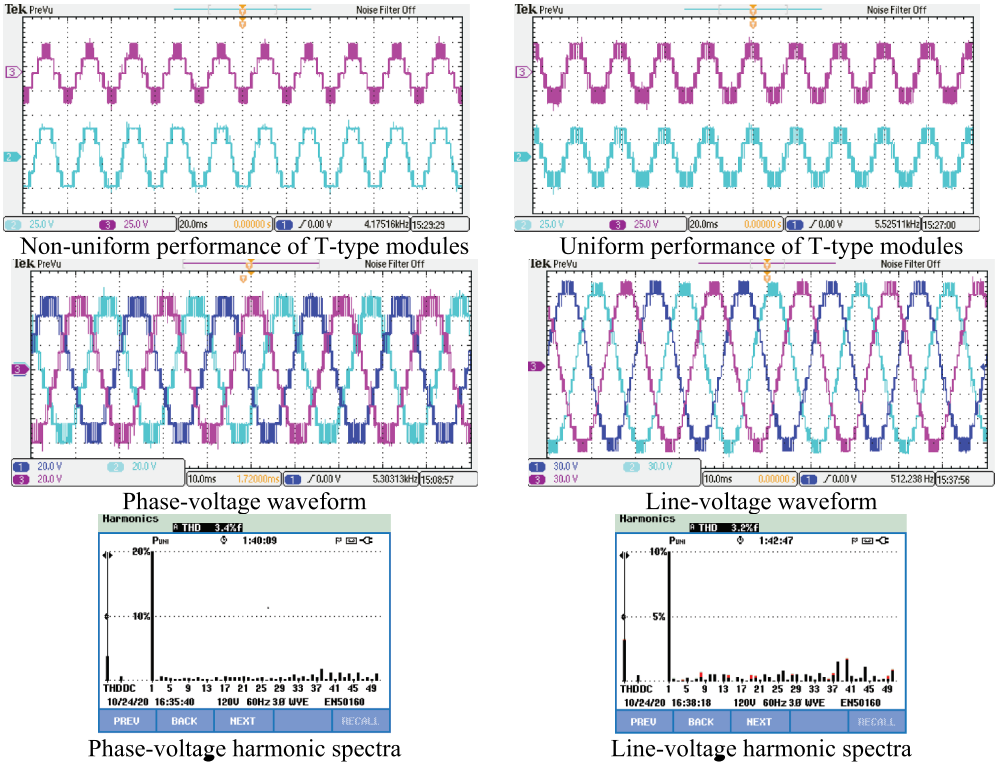
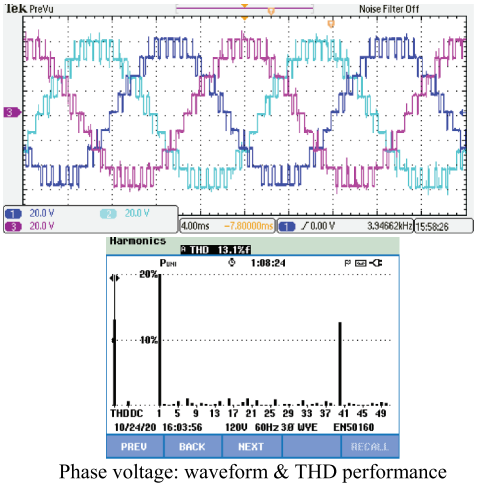


Figure 14. Experimental performance of proposed USL on nine-level cascaded T-type RSC-MLI (f_{sw} =3kHz).

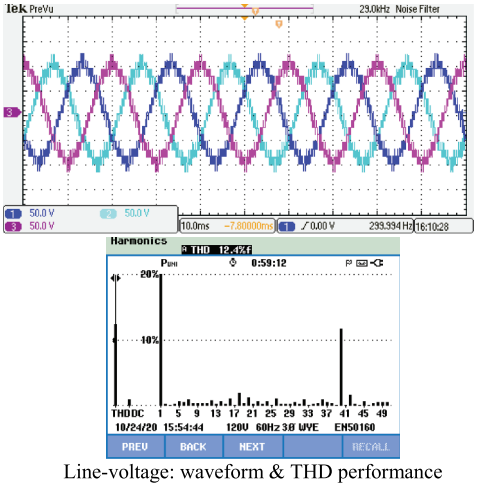
distribution of the cascaded T-type modules. Also comparing its corresponding phase and line-voltage shown in Figures 13 with 11 verifies the ability of the proposed scheme to facilitate uniform distribution without effecting phase (13%) and line voltage (9%) performance.

The hardware validation of Figures 13 and 11, is depicted in Figure 14 for 3 kHz, where Figure 14 demonstrates the ability of proposed PWM to facilitate uniform power distribution without effecting phase (3.4%) and line voltage (3.2%) harmonic performance. However, the performance of the MRC PWM degrades for frequencies other than triple-*n* multiples of modulating frequencies. This can be validated referring to Figure 15.

Imposing carrier frequency of 2000 Hz, the recorded phase and line-voltage harmonic performance of nine-level inverter cascaded T-type configuration with the conventional USL adapting MRC arrangement are shown in Figure 15. The waveform and harmonic performance of conventional USL with MRC for carrier frequency 2000 Hz shown in Figure 15 (a) depicts the presence of dominant harmonic component at m_f with line voltage THD of 12%. This degraded line-voltage performance of the MRC-based PWM forced is due to the effect of imposed switching frequency forcing MRC to operate as asynchronized PWM. This inability limits MRC to operate as synchronised PWM and is not suitable for deriving a three-phase inverter, if inverter switching frequency/carrier frequency is not 3n multiples of fundamental. This can be addressed by implementing the proposed USL with LSPWM carrier arrangement. Figure 15 (b) shows the phase and line

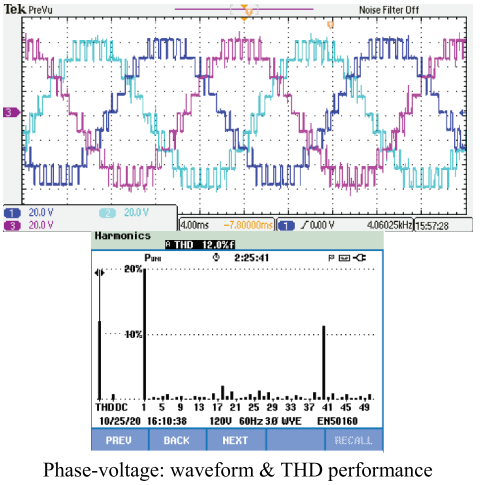


Phase voltage: waveform & THD performance

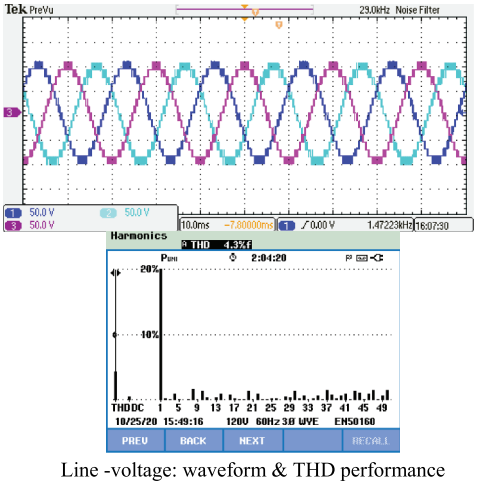


Line-voltage: waveform & THD performance

(a) Conventional USL with MRC arrangement



Phase-voltage: waveform & THD performance



Line -voltage: waveform & THD performance

(b) Proposed USL with LSPWM carrier arrangement

Figure 15. Experimental Performance of nine-level inverter for ma=0.95, and f_{sw}=2000 Hz.

voltage performance of the proposed USL adapting LSPWM carrier arrangement to control nine-level cascaded T-type RSC-MLI, for $f_{cr} = 2000$ Hz. The improved harmonic performance with THD of 4.3% and clean wave shape of line-voltages of Figure 15(b) clearly validates the superiority of the proposed USL to support LSPWM carrier arrangement producing satisfactory performance.

Further, to validate the saleability of the proposed USL, its implementation for asymmetrical configuration is considered. Three-phase cascaded T-type configuration shown in Figure 1 operated with binary and trinary voltage ratios to produce thirteen- and seventeen-level phase-voltage is carried out and its corresponding results are given in Figures 17 and 18 respectively.

The three-phase nine-level RSC-MLI are given Figures 16 and 17 and presents the simulation results of the proposed USL to control asymmetrical cascaded T-type RSC-MLI

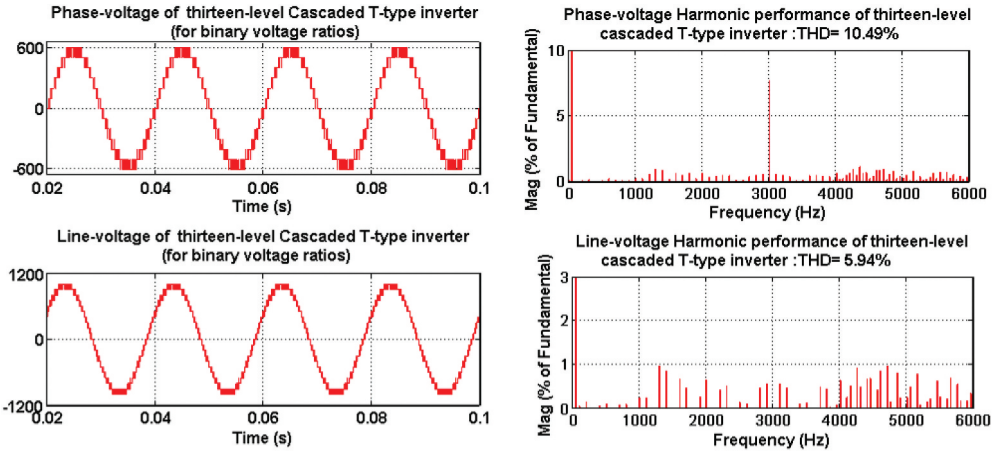


Figure 16. Simulink performance of Thirteen-level cascaded T-type Inverter with proposed PWM (f_{sw} =3000).

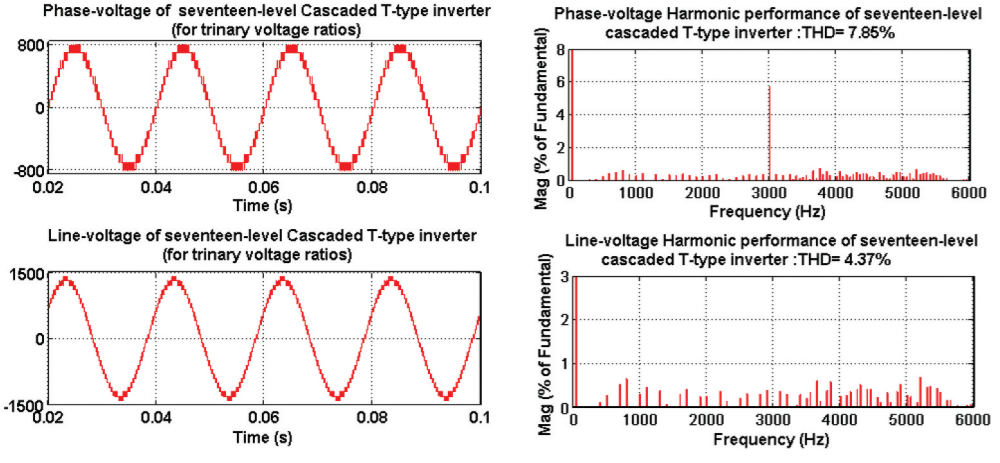


Figure 17. Simulink performance of seventeen-level cascaded T-type inverter with proposed USL (f_{sw} =3000).

to produce thirteen-level (operating Figure 1 with binary voltage ratios) and seventeen-level (operating Figure 1 with trinary voltage ratios) phase-voltage respectively. The experimental validation of the simulation results depicted in Figure 16 is shown in Figure 18, considered a downscaled prototype. The key objective of involving MRC is to achieve good line-voltage harmonic performance as similar to LSPWM-IPD. Observing the phase and line-voltage harmonic profile of Figure 11, Figure 13 , 16 and Figure 17 shows the presence of dominant harmonic around, i.e. 3000 Hz. This shows the ability and proposed scheme to produce harmonic around carrier switching frequency as similar to LSPWM-IPD. Thus simulations results (Figures 11, Figures 13 , Figures 16 and 17) of the proposed scheme produces a phase-voltage THD of 13.68%, 10.49% and 7.85% and line voltage THD of 9.01%, 5.94% and 4.37% for nine-, thirteen- and seventeen-level cascaded T-type inverter respectively.

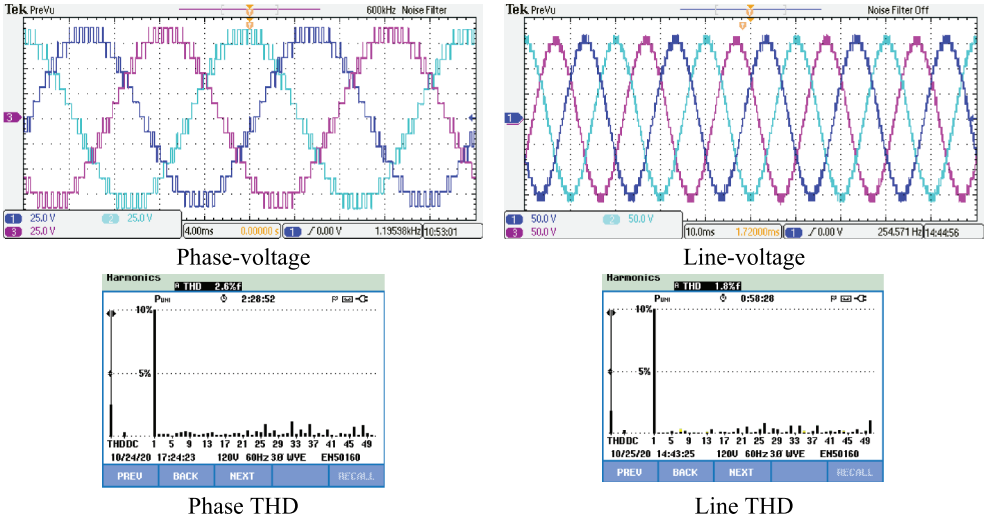


Figure 18. Experimental performance of USL to control 13-level cascaded T-type RSC-MLI (f_{sw}=3000).

Similarly, the obtained experimental results shown in Figures 14 and 18 depict that proposed USL with MRC records a phase THD of 3.4%, 3.2% and Line THD of 2.6% and 1.8%, for nine- and thirteen-level cascaded T-type RSC-MLI respectively. However, these THD values recorded in experimental and Simulink THD show considerable difference. This is due to the power quality analyser (Fluke metre) used to measure experimental THD records harmonics/THD only till 49th order of fundamental frequency, i.e. 2450, whereas the simulation THD recorded in the MATLAB environment records the harmonics/THD till Nyquist frequency, i.e. 499th order of fundamental frequency.

Further, superiority of the proposed USL over the conventional schemes is quantified and presented in Figure 19, where the performance of the proposed USL imposing MRC and level shifted carrier arrangements is recorded and compared with the conventional

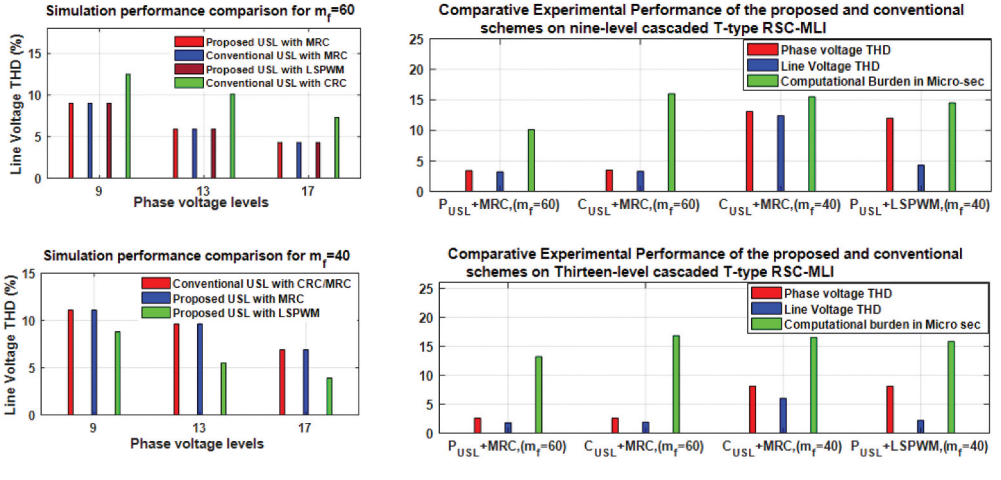


Figure 19. Performance comparison of the proposed USL with conventional USL.

Table 4. Comparative performance of proposed and conventional USL.

Cascaded T-type topology	Simulation performance						Experimental performance with dSPACE Micro Lab Box controller					
	9-level		13-level		17-level		9-level			13-level		
Imposed Scheme	Ph.	Line	Ph.	Line	Ph.	Line	Ph.	line	burden	Ph	line	Burden
Proposed USL with MRC (f_{sw} = 3000 Hz)	13.6%	9.0%	10.4%	5.9%	7.8%	4.3%	3.4%	3.2%	10.1 µS	2.6%	1.8%	12.3 µS
Conventional USL with MRC (f_{sw} = 3000 Hz)	13.6%	9.0%	10.4%	5.9%	7.8%	4.3%	3.5%	3.3%	16 µS	2.6%	1.9%	18 µS
Conventional USL with CRC (f_{sw} = 2000 Hz)	12.9%	11.1%	10.1%	9.63%	7.5%	6.9%	13.1%	12.4%	15.5 µS	8.1%	6.0%	17.5 µS
Proposed USL with LSPWM (f_{sw} = 2000 Hz)	13.1%	8.8%	10.2%	5.5%	7.5%	3.9%	12.0%	4.3%	14.5 µS	8.1%	2.2%	15.8 µS

Table 5. Performance comparison of proposed USL with conventional carrier-based PWM schemes for their state of art reported using dSPACE Micro Lab Box.

		Performance on the state of art reported			*Performance of MRC PWM with proposed USL for the state of art of conventional PWM schemes*		
		Output voltage THD			Output voltage THD		
PWM reported	*Topology involved*	Phase (%)	Line (%)	Turnaround time	Phase (%)	Line (%)	Turnaround time
Hybrid PWM (Babaei, 2008; Babaei & Gowgani, 2014; Gupta et al., 2015; A. Masaoud, Ping, Mekhilef, & Taallah, 2014)	Eleven-level SSPS (Babaei, 2008)	9.9	3.1	7.4 µS	9.6	2.9	6.2 µS
Multi-reference	Seven-levelT-type	14.8	15.7	6.5 µS	15.5	4.8	5.2 µS
Reduced carrier with logical gates	Modified seven-level T-type (Rahim et al., 2013)	15	15.8	19 µS	15.6	4.9	5.2 µS
Switching function	Seven-level SDS MLI	15.6	4.8	8.1 µS	15.6	4.8	5.3 µS
Modified Multi- reference	Seven-level T-type	15.7	4.9	6.3 µS	15.7	4.9	5.2 µS
Reduced carrier	Sevenl-evel RV	15.7	14.9	5.6 µS	15.6	4.8	5.2 µS
MRC with conventional USL	Seven-level T-type	15.7	4.9	6.4 µS	15.7	4.9	5.1 µS

USL. From Figure 19, for $f_{sw} = 3000$, i.e. $m_f = 60$, it is noted that proposed USL with MRC produces improved line voltage THD over the conventional, and also operates with less computational burden on the controller. Similarly, for $f_{sw} = 2000$, i.e. $m_f = 40$ (non-integer multiples of fundamental frequency), proposed USL with LSPWM produces improved line THD performance over the conventional.

To quantify the comparative performance, the tabulation of Figure 19 is depicted in Table 4, where the superiority of the proposed USL over the conventional can be very well analysed referring to its corresponding computational burden imposed on the controller. The experimental results depicted in Table 4 conclude that proposed USL with MRC operates with least computational burden (10 µS and 12.3 µS) over the conventional USL (16 µS and 13 µS) in controlling 9-level and 13-level T-type RSC-MLI respectively. Further the superior performance of the proposed USL over the conventional carrier-based schemes for the reported state of art is demonstrated in Table 5.

Table 5 presents the comparative performance of the proposed USL over the popular conventional carrier-based PWM schemes of RSC-MLI, for their reported state of art. The comparison is carried out in terms of phase-THD, line THD and recorded computation burden, considering the carrier frequency of 3000 Hz and loading the considered PWM on dSPACE MicroLabBox controller in experimental environment. Interestingly the quantified results of Table 5 show that the proposed USL imposes a nearly uniform computational burden of 4.9 µS to implement a seven-level RSC-MLI irrespective of the topological arrangement of the considered RSC-MLI. This can also be validated with the similar phase and line THD of 15.6% and 4.8**%** produced by proposed PWM in controlling a seven-level RSC-MLI. Further comparing the performance of the proposed USL with conventional USL with MRC, shows the superiority less computational burden of 4.9 µS of the proposed over the conventional with 6.4 µS. Thus, qualified values in the Figure 19, Table 4 and Table 5 validate the superiority of the proposed controller in terms of simplified switching logic and reduced complexity.

V. Conclusion

This paper presented an improved unified switching logic (USL)-based PWM to control RSC-MLI topologies. The superiority of the proposed scheme over the conventional in terms flexibility in implementation and reduced computational burden is demonstrated in experimental environment with ds1104 controller and dSPACE Micro Lab Box. The scalability of the proposed scheme and its ability to implement any RSC-MLI with satisfactory line-voltage harmonic performance are validated both on simulation and on experimental environment considering symmetrical and asymmetrical configurations of cascaded T-type RSC-MLI. The feature of the proposed USL to facilitate uniform load power distribution and operate with reduced controller computational burden supports its application of PV/Grid connected systems, battery charging and active front end converters.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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