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Modified Dual PWM-Controlled Boost Converter with Reduced Input Current Ripple for High Gain Applications

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***Abstract*— High gain boost converters are used widely in automobile industry in powertrain unit to transfer energy from batteries to various modules of system. Improvements in the areas of gain and input current ripple will improve the converter performance. This paper proposes a modified control logic for higher output voltage with reducing input current ripple. Boosting the converter gain is achieved through dual PWM technique and ripple reduction is obtained by properly selecting the frequencies of high and low frequency carrier waves. To confirm the effectiveness of the proposed design, simulation studies and the implementation of a 90 V, 90 W hardware prototype circuit have been carried out. The proposed scheme yields satisfactory performance in ripple reduction.**

Keywords—PWM, Dual frequency, Boost converter.

I. INTRODUCTION

In renewable energy systems (RES), where varying input voltages are common, a high gain boost converter can efficiently convert the fluctuating input voltage to a stable and usable output, improving the overall system performance. Renewable energy sources such as PV panels, fuel cells have their output as low voltage level. Hence, it is needed to be boosted before connecting it to DC microgrid [1], [2], [3]. DC-DC boost converters act as a bridge between RES and DC microgrid. Conventional boost converter is not able to achieve high voltage gain of 10 to 20 times with high overall efficiency due to its parasitic parameters [4]. In order to achieve high gain, various techniques are used such as switched capacitor, coupled inductor (CI), voltage multiplier, voltage lift technique, cascaded boost converters, Hybrid structures etc.

Among these, CI is highly used by utilizing high turns ratio to meet high voltage gain. It also increases the size requirement and losses (winding and core loss) [5]. Another drawback of CI is large leakage inductance which causes high voltage stress on switch, high conduction loss and reduced converter efficiency. Switched capacitor high gain boost converters are valuable in applications where size, efficiency and moderate power requirements are critical. Achieving high gain in switched capacitor boost converters often involves more complex circuit designs and precise component matching, increasing the design complexity compared to conventional boost converter [6], [7], [8]. Voltage multiplier circuit uses diode-capacitor networks [9]. Scaling up the voltage lift technique for extremely high voltage gains is impractical due to increased complexity, diminishing efficiency and component limitations. Cascaded boost converters subject components such as inductors, capacitors and switches, to higher voltage stresses across multiple stages. This can be a limiting factor in applications where space is a critical consideration.

The main requirements of high gain boost converters are

1. Improved dynamic response for wide range of input level.
2. Reduced input current ripple.
3. Easy control and compact design

After analyzing various voltage boost techniques, it has been observed that most high-gain converters are essentially modifications of the conventional boost converter. While these modifications meet design requirements, they also increase the cost and introduce lossy components to the system. Instead of modifying the existing circuit topologies, a more cost-effective solution could be the development of advanced PWM control mechanisms. With this in mind, a new dual PWM-controlled high-gain boost converter has been proposed in [10]. This design involves comparing a high-frequency carrier wave and a low-frequency carrier wave with a constant DC control signal. The resulting pulses are then passed through an OR gate to produce PWM control signal for converter switch. In this design, the operational cycle is determined by low frequency PWM signal time period. The main condition to achieve quadratic boost is to maintain $(1 - D_L)T_L = nT_H$, where T_L and T_H are time periods of low and high frequency signals respectively. D_L is duty cycle of low frequency PWM and 'n' is any integer value. This demands for high frequency carrier wave to be at least 4 times greater than low frequency carrier wave if $D_L = 0.5$. Hence, with this dual PWM scheme, the ripple in inductor current and also switching losses are increasing due to a greater number of switching in each cycle.

In this paper, a modified dual PWM control scheme is proposed which can reduce the input current ripple with

reduced number of switching in each cycle. The analysis includes consideration of four different operation modes when D is less than or equal to 0.5, and two modes when D is greater than 0.5, in each operational cycle.

The proposed modified dual PWM control uses two frequency carrier waves which are integer multiples of each other. PWM signals are generated by comparing constant reference signal with each carrier wave. Both PWM signals are passed through OR gate to generate gate control signal for the switch. The voltage gain is evaluated under two different conditions.

1. $D \leq 0.5$
2. $D > 0.5$

The proposed modification in dual PWM control minimizes ripple in inductor current.

This paper is structured as follows. Section II describes overview of proposed scheme follows by voltage gain analysis. Detailed analysis of proposed scheme through simulation result and hardware implementation is presented in section III. It also contains comparison of dual PWM technique [10] and proposed modified dual PWM technique. Major conclusion is drawn in section IV.

II. Operational Principles

Conventional boost converter consists single low side switch along with Inductor L at the input side as shown in Fig. 1. Diode D provides a path for a inductor to deenergize during switch OFF condition. Capacitor 'C' is placed across resistive load (R_{Load}). Switch Q is operated by providing gating pulses to it.

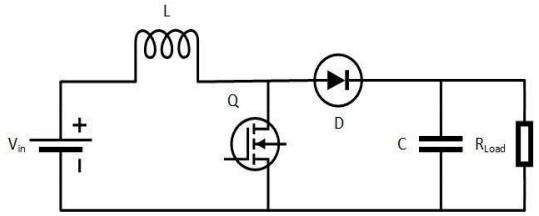

Fig 1: Conventional Boost Converter

Switch Q is conventionally controlled by PWM signal which is generated upon comparing a triangular wave with constant control signal. In the proposed modified dual PWM technique switch Q is controlled by PWM signal which is having two frequency components. Fig. 2 shows a boost circuit operated with the proposed control technique.

In closed loop control, output voltage is always compared with desired output voltage V_{ref}. Error signal ($V_e = V_{out} - V_{ref}$) is used to generate control signal V_{ctrl} through compensator block. V_{ctrl} is used as the reference signal for generating individual PWM signals. In Fig. 3, it can be observed that duty cycle of both PWM_{hf} and PWM_{lf} are same and equal to D (D_L=D_H=D).

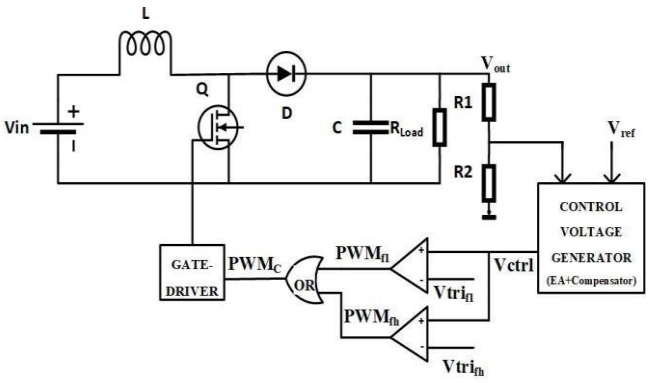

Fig. 2: Block diagram

Two triangular waveforms with frequencies f_h and f_l (V_{trifh} and V_{trifl} respectively) as shown in Fig. 3, are compared with V_{ctrl}. Two sets of PWM signals (PWM_{hf} and PWM_{lf}) are generated with same duty cycle. By logically 'OR'ing the PWM_{hf} and PWM_{lf}, PWM_C is obtained. Detailed waveforms of proposed modified dual PWM control scheme are shown in shown in Fig. 3.

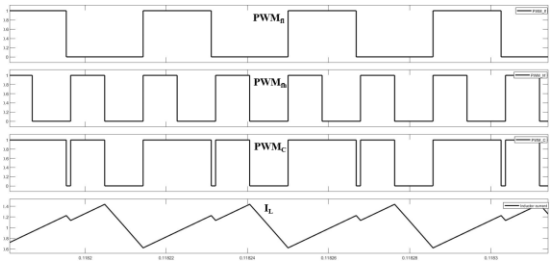

Fig 3. Synthesis of PWM_C

The proposed modified dual PWM scheme emphasis on selecting frequencies of V_{trifh} and V_{trifl} in such a way that Equation (1) holds true.

$$D_L T_L = nT_H \qquad (1)$$

where $n \in N$

The major objective of choosing the PWM frequencies as in Equation (1) is to set frequency of high frequency carrier wave as an integer multiple of low frequency carrier wave. In the proposed modified dual PWM scheme D_L is selected to be 0.5 and hence $f_h = 2f_l$.

Fig. 4 shows PWM pulses and corresponding inductor current waveform when $D \leq 0.5$. Fig. 5 shows the same for $D > 0.5$. Two different frequency carrier waveforms are compared with the control signal which is shown in red.

The period of the PWM_C waveform is equal to T_L. For n=2, proposed technique has four modes of operation (M_1, M_2, M_3 and M_4) for $D \leq 0.5$ and two modes (M_1 and M_2) for $D > 0.5$.

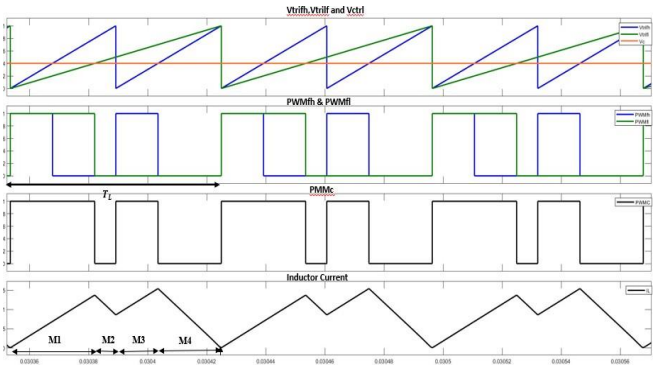

Fig. 4: Modified dual PWM signals and Inductor current waveforms for D ≤ 0.5

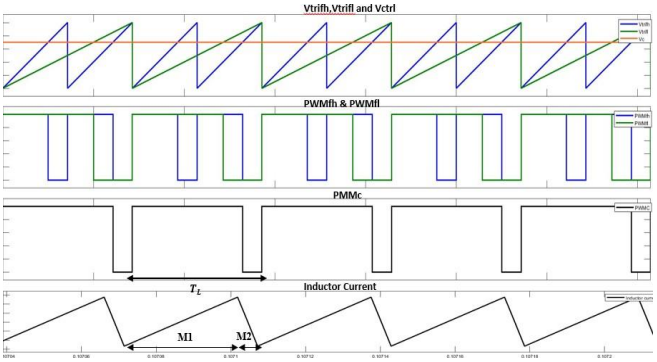

Fig. 5: Modified dual PWM signals and Inductor current waveforms for D > 0.5

A. Modes of operation (D ≤ 0.5)

As indicated in Fig. 2, There are 4 modes of operation under this condition namely M_1, M_2, M_3 and M_4. Let time interval of different modes be t_0-t_1, t_1-t_2, t_2-t_3, and t_3-T_L respectively.

Mode-1 [$t_0 < t < t_1$]:

During mode-1, the MOSFET turns on. As a result of the reverse voltage, diode D turns off and the inductor starts to energize. Voltage across inductor can be expressed as below

$$V_{in} = L\frac{dI_L}{dt} \quad (2)$$

Where L is the inductance. Inductor current I_L is expressed as

$$dI_L = D_L T_L \frac{V_{in}}{L} \quad (3)$$

The inductor is positive now and hence the inductor current increases. Equation (3) is the change in inductor current during mode-1

Mode -2 [$t_1 < t < t_2$]:

During this mode, inductor releases the energy to load. Switch is in OFF state. The change in inductor current is,

$$dI_L = (T_H - D_L T_L)\frac{(V_{Out}-V_{in})}{L} \quad (4)$$

Mode -3 [$t_2 < t < t_3$]:

Switch turns ON and inductor voltage is positive. Hence inductor current is increasing during the period $D_H T_H$.

$$dI_L = D_H T_H \frac{V_{in}}{L} \quad (5)$$

Mode -4 [$t_3 < t < t_4$]:

This mode operation is same as mode-2. Inductor deenergizes during the period of (T_H - $D_L T_L$)

$$dI_L = (T_H - D_L T_L)\frac{(V_{Out}-V_{in})}{L} \quad (6)$$

Hence, one cycle of operation consists of these four modes. According to volt-sec balance principle,

$$\text{Eqn (3)} + \text{Eqn (4)} + \text{Eqn (5)} + \text{Eqn (6)} = 0 \quad (7)$$

Also,

$$T_L = 2T_H \quad (8)$$

From (1), (7) and (8),

$$\text{Voltage gain} \quad G = \frac{2}{2-3D} \quad (9)$$

B. Modes of operation (D > 0.5)

Under this condition, generated PWM signal makes inductor to undergo two modes of operation as shown in Fig. 3.

Mode-1 [$t_0 < t < t_1$]:

During mode-1, MOSFET turns on. The diode D turns off and the inductor starts to energize. Under mode-1, change in inductor current is given by,

$$dI_L = 2D_H T_H \frac{V_{in}}{L} \quad (10)$$

Mode-2 [$t_1 < t < t_2$]:

During this mode, Inductor deenergize to load. Switch remains OFF. Inductor current decreases and change in inductor current is,

$$dI_L = (T_H - D_L T_L)\frac{(V_{Out}-V_{in})}{L} \quad (11)$$

Applying volt-sec balance,

$$\text{Voltage gain} \quad G = \frac{3D}{1-D} \quad (12)$$

C. Critical Inductance

Critical inductance refers to a specific value of inductance that separates two operating modes, CCM and DCM. Since circuit topology is same as conventional boost converter, derivation of critical inductance remains the same. Also, prototype is designed to be operated in CCM, i.e., the inductor current doesn't reach zero during the switching cycle. It continuously flows through the inductor, ensuring a smooth

and continuous energy transfer. The minimum inductance for CCM is expressed as

$$L_{min} = V_{in} \frac{(V_{out} - V_{in})}{dI_L f_s V_{out}} \quad (13)$$

III. Results and Discussion

This section briefs about simulation studies, hardware implementation and results. Fig. 6 shows pulse generation block where 28 kHz and 56 kHz triangular carrier waves are compared with constant 0.2 V control signal thus, generating low and high frequency PWM signals respectively. Logical OR operation is then performed between these generated PWM signals. Resultant PWM signal is then used as gating signal for switch Q of the boost converter as shown in Fig. 2.

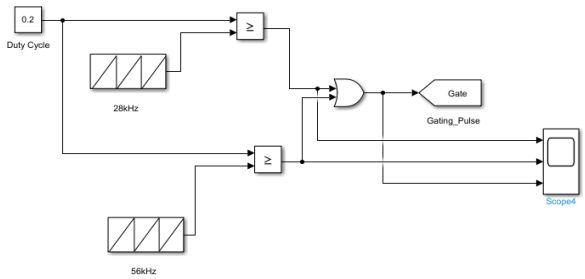

Fig. 6: Simulation model of switching pulse generation

Simulation is run for wide range of inputs. Input is varied from 9V to 33V. Fig. 7 shows the output voltage characteristics of boost converter with proposed modified dual PWM and also with other PWM schemes. A comparison is done between proposed modified dual PWM, dual PWM and conventional PWM techniques by setting input voltage equals to 5V for different duty cycles.

Proposed modified PWM technique has almost similar voltage gain for D < 0.5 as of dual PWM technique. For D > 0.5 proposed technique has slightly lesser voltage gain than [10] but more than conventional PWM technique. Significant increase in output voltage can be seen for dual PWM technique [10] at higher duty cycle values.

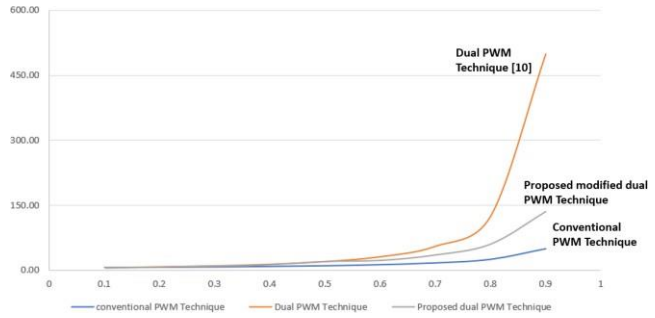

Fig. 7: Comparison of output voltage with conventional PWM, Dual PWM [10] and Modified Dual PWM (proposed) switching scheme

Proposed dual PWM technique is analyzed for wide range inputs and constant output. Fig. 8 shows the change in output voltage for a given change in D for different input voltage.

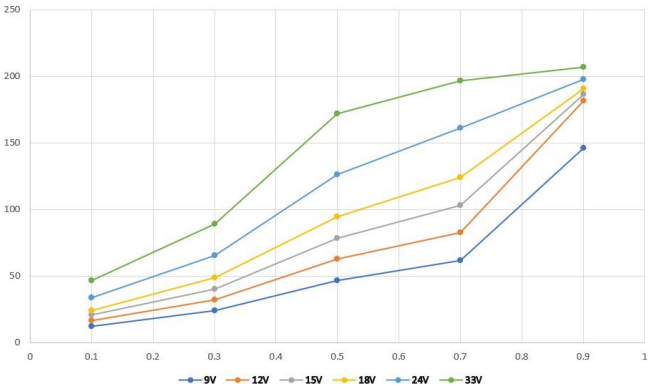

Fig. 8: Voltage gain for wide range input

It can be observed from the characteristics that, as compared with [10] for D < 0.5, inductor current profile is found to be similar and hence similar output voltage is obtained. Fig. 9 and Fig. 10 show the PWM signals and inductor current profiles with D = 0.35 for the proposed modified dual PWM scheme and dual PWM scheme [10] respectively.

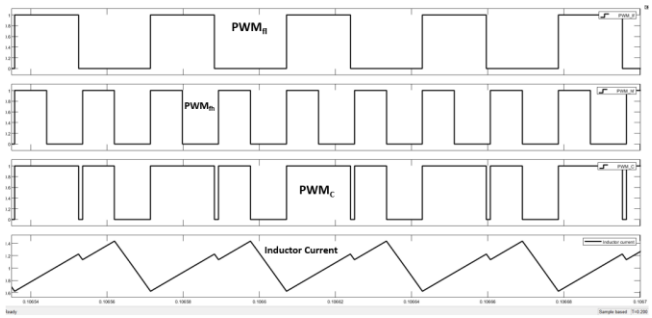

Fig. 9: Inductor current profile for D =35% under proposed modified dual PWM technique

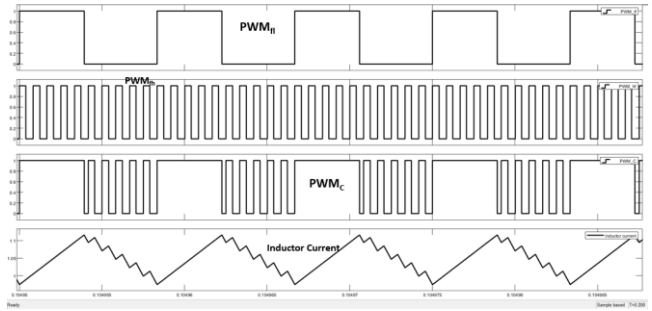

Fig. 10: Inductor current profile for D = 35% under Dual PWM technique [10]

It is observed that the proposed PWM scheme has comparatively less number of switching than [10]. Effect of this advantage can be seen for D > 0.5 case where inductor energizes and deenergizes only once in a cycle whereas in [10] inductor energizes and deenergizes for multiple times.

Fig. 11 and Fig.12 show inductor current profiles for D = 70% for proposed dual PWM technique and dual PWM technique [10] respectively. Multiple switching action in with dual PWM [10] can introduce ripple in inductor current

which is same as the source current. Whereas the proposed modified dual PWM scheme provides reduced number of switching and hence reduced ripple in inductor current. With reduced switching losses, proposed modified dual PWM scheme is a better solution for applications with moderately high gain requirement.

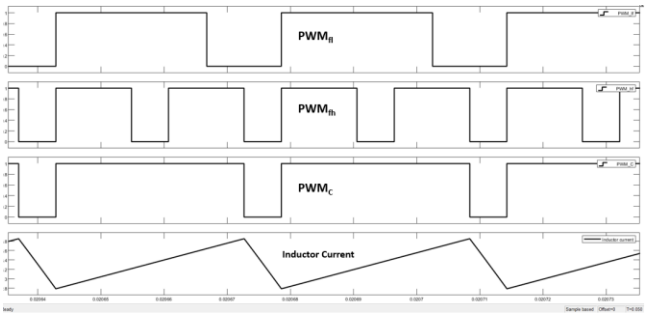

Fig. 11: Inductor current profile for D =70% under proposed modified dual PWM technique

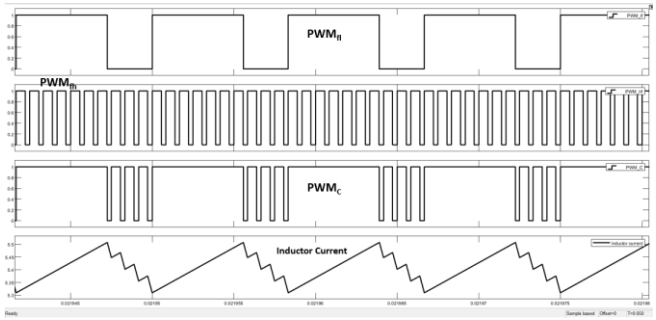

Fig. 12: Inductor current profile for D =70% under Dual PWM Technique [10]

To analyze further, hardware implementation is carried out for 90 W load. The circuit is designed to achieve constant voltage over a wide input range. The prototype was tested at different input voltages. The hardware structure of the prototype is shown in Fig. 13. A TI controller F23879D is used to generate the dual frequency PWM signals. The duty cycle can be controlled using the MATLAB Simulink c2000 library. A 90 Ω rheostat is used as the load. The inductor value of the converter operating in continuous conduction mode is 240uH (240uH, 12A peak, 0.5 ohms) at a load of 90W. IRFP250N switch is used to block 250V. The diode used here is MUR3060PT.

Fig. 11: Experimental Prototype

A. *Results*

The design specification is to achieve 90V output for change in input from 9 V to 33 V. Simulation is verified by setting duty cycle for respective input voltage to bring output to 90 V constant. Fig. 14 shows input voltage of 24 V, duty cycle to achieve 90 V is 0.67. waveform shows nature of inuctor current along with output voltage and current for 90 W load.

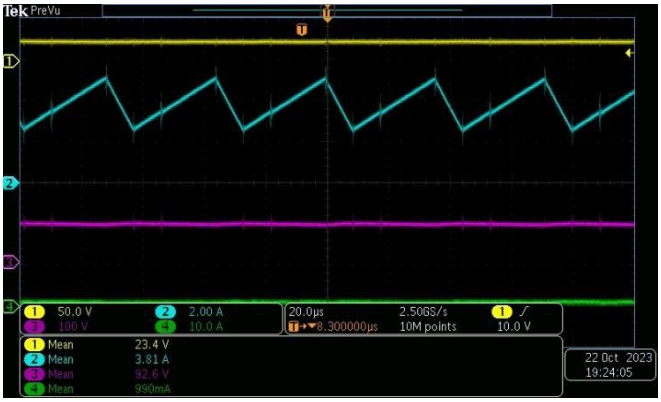

Fig. 14: Input voltage, inductor current and output voltage waveforms with proposed PWM scheme (V_{in} = 24 V& D=0 .67)

Similarly, inductor profile for D < 0.5 can be seen for input voltage equals to 33 V, required duty cycle to keep output voltage constant at 90 V is 0.47. Fig. 15 shows waveforms for 33 V input case.

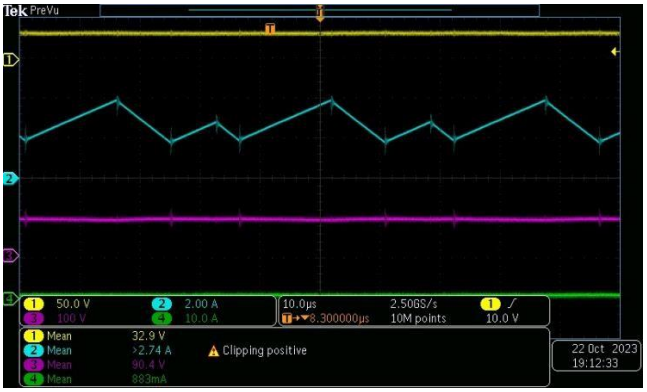

Fig. 12: Input voltage, inductor current and output voltage waveforms with proposed PWM scheme (V_{in} = 33 V& D=0 .47)

B. *Efficiency*

As the circuit topology is not different from the conventional converter topology, the efficiency of the converter remains the same. When the input voltage is 33 V, the maximum efficiency can reach 89%. It can be seen that the efficiency at constant input voltage is better at higher loads. On the other hand, efficiency is more likely to be achieved at maximum input voltage fluctuations and at lower loads. Fig.15 shows efficiency plot of converter with proposed modified dual PWM switching scheme.

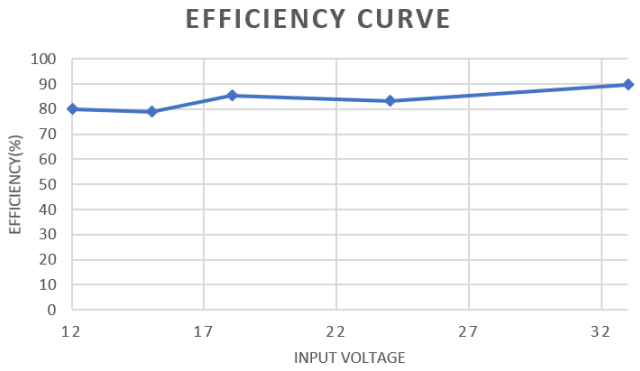

Fig. 15: Efficiency curve of converter with proposed modified dual PWM switching scheme

IV. Conclusion

In this paper, a modified Dual PWM control is proposed for a high-gain boost converter. In comparison with [10], this technique closely follows quadratic boost for D < 0.5 and provides the advantage of reduced number of switching and reduced ripple in inductor current. The PWM control of the boost converter generates two sets of PWM waveforms, one with a higher frequency and the other with a lower frequency. The duty cycle of both waveforms has an impact on the behaviour of the inductor current, ultimately resulting in an improved gain for the boost converter. As compared to [10], proposed switching pattern has less ripple in inductor current because of reduced switching action hence reduced switching losses also. The theoretical analysis of the improved gain aligns with the simulation and hardware results. Two different cases are studied, one for duty cycle (D) less than or equal to 0.5 and the other for D greater than 0.5. A prototype of 90 W converter is tested with varying input voltages ranging from 9 V to 33 V, and the efficiency is calculated. Simulations and experimental studies are conducted for a 90 V output voltage and 90 W output power, with input voltages of 24 V and 33 V. The results from both the simulations and experiments are in agreement. These results clearly demonstrate that the proposed modified dual PWM scheme for high-gain boost converter can effectively meet the design requirements for applications such as fuel cells or PV arrays.

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