Analysis and Design of Switched Inductor-Capacitor based Quasi Z Source analogous Boost Converter

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***Abstract*— This article discusses the design and analysis of a switched inductor-switched capacitor based dc-dc converter. The proposed topology boost factor is akin to a quasi-Z-Source converter in which the load-end switched inductor is preceded by a front-end converter comprising of a single inductor and switched capacitor arrangement. The output capacitor's peak current is significantly abbreviated by incorporating the third switch in the stated topology by retaining the features of continuous-low ripple source current and a common ground. A prototype with 400 V, 300W, and 50 kHz is developed to validate the steady state analysis performance indices.**

Keywords—Boost converter, DC-DC converter, Quasi Z source and Voltage gain.

I. INTRODUCTION

A significant amount of electrical energy in the whole power generation system is shared by green energy renewable sources, specifically a combination of photovoltaic (PV), fuel cell, and wind power. These sources will also play a vital role in high voltage direct current (HVDC) technology. Except for wind power generation, the other two green energy sources are at low output terminal voltage and hence the need of power electronic-based power conditioning converters. The typical solution to the aforementioned problem is to incorporate a boost converter. However, in order to achieve high voltage gains, the boost converter has drawbacks such as elevated duty ratios, which cause increased voltage and current stresses on semiconductor elements and reduced efficiency. One classical alternative remedy for the shortfall of a classic boost converter is to use an isolated dc-dc converter or transformer. These isolated converters has significant drawbacks like voltage spikes at power switches induced by improper usage of leakage flux, which eventually results in equivalent leakage inductance. Another severe difficulty with isolated dc-dc converters is that the source and load will not share a common ground, resulting in electrical isolation and magnetic coupling.

Modern technologies like switched capacitors, switched inductors, and/or combinations [1] of both have evolved to address the shortcomings of isolated dc-dc converters and traditional boost converters along with other technologies that have been developed which include interleaved topologies, split duty-based converters [2], and quadratic converters. Despite all the advantages of the technology outlined above, extended conducting duty ratios are still needed to obtain higher voltage gains. Serious deficiencies including a rise in element stresses and persistently derated efficiency are associated with these excessive ratios.

In recent trends there is good potential for Z-source based DC-DC converters in fuel cell and solar applications. The Z source converter boost factor is 1/1−2D. To further enhance the terminal voltage, Zhu et al. developed a Z-source converter formulated on switching inductor [3]. However, these Z-source converters have severe drawbacks, such as high inrush current, high ripple content in source current, elevated passive component count, absence of common grounding etc. To address the issue of input current ripple, a quasi Z-source (QZS) based converter with voltage multiplier has been reported [4]. However, the number of passive component count is high in the reported topology. To improve converter gain, a combination of charge pump and LCD-quasi network is utilized in a variety of configurations reported in [5] but these configurations have concerns with control complexity, bulk size, and voltage gain. Integration of additional components to Z source and QZS converters also results in improved boosting factors. Two extra capacitors, one additional diode, and one more inducer are required for any Z-source network that is connected in series. An additional switch inductor network, voltage lift unit, and QZS network, respectively, take the place of the inductors in the Z-source or quasi-Z-source network in [6]–[8]. A second boost converter is inserted in [9] in between the QZSC and the voltage supply. In [10]–[12], a second switch capacitor network steps up the QZSC's output voltage. A three-winding transformer is incorporated into the converter in [13]. In [14], a second switch capacitor network steps up the QZSC's input voltage. However, the adverse effects of integrating additional elements are the converter low packaging concerns and less economical aspects which limits the extensive usage of this aspect.

In view of the aforementioned literature, this work proposes a unique topology based on a switched capacitor (C_1) and two switched inductors (L_1 and L_2) as shown in Fig. 1. This converter has a voltage gain similar to a quasi-Z-source converter while maintaining attributes such as low input current ripple, absolute common ground, and nominal voltage-current stresses on switches and diodes.

The following sections of analysis, results and discussion are pertaining to continuous conduction mode (CCM) of the proposed converter.

II. STEADY STATE ANALYSIS

The CCM operation associated with two operating modes, the detailed analysis of these modes are as follows

Mode I: (t_0-t_1)

In this mode of time i.e., ON time DT_S, switches S_1, S_2 and S_3 are at ON state and all the diodes (D_0-D_2) are reverse biased as shown in Fig. 2. The inductors (L_1 and L_2) are magnetized with the voltages as shown in Fig. 3 and the load R_0 is powered by the capacitor (C_0).

The voltage across the inductors (L_1 and L_2) is written as

$$\left.\begin{aligned} v_{L1}&=V_i+v_{C1}\\ v_{L2}&=v_{C1}\end{aligned}\right\} \quad (1)$$

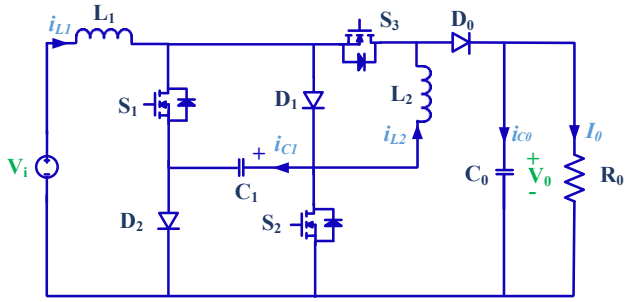


Fig. 1. Proposed Topology

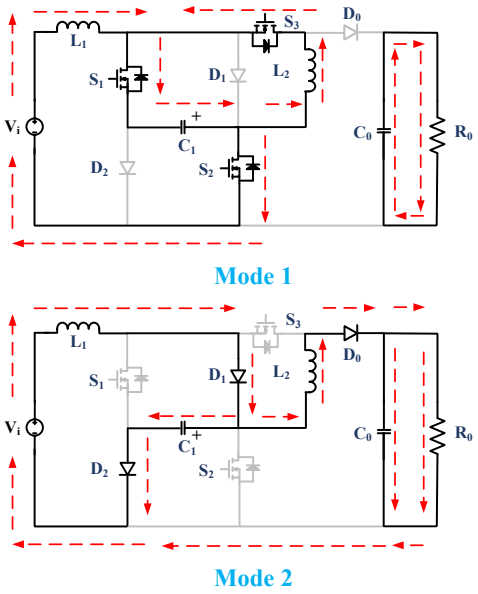


Fig. 2. Operating modes

Mode II: (t_1-t_2)

This mode constitutes of $(1\text{-}D)T_S$ period, in which diodes and switches operation is compliment to mode I as shown in Fig .2. The combination of load R_0 and capacitor C_0 are powered by inductor L_2 whereas a part of inductor L_1 current charges the capacitor C_1 as shown Fig. 2 and 3.

The corresponding inductor voltages are written as

$$\left.\begin{aligned} v_{L1}&=V_i-v_{C1}\\ v_{L2}&=v_{C1}-V_0\end{aligned}\right\} \quad (2)$$

Using (1) and (2) for volt-sec balance on inductors L_1 and L_2 to evaluate V_{C1} and voltage gain.

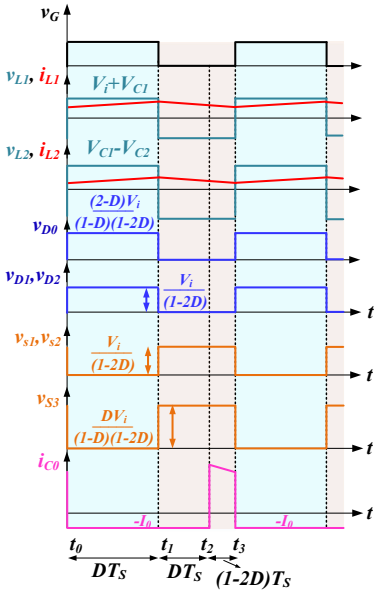


Fig. 3. Key waveforms

$$\left.\begin{aligned} (V_i-v_{C1})D+(V_i+v_{C1})(1-D)&=0\\ (v_{C1})D+(v_{C1}-V_0)(1-D)&\end{aligned}\right\} \quad (3)$$

Therefore

$$V_{C1}=\left(\frac{V_i}{1-2D}\right) \quad (4)$$

$$V_0=\left(\frac{V_{C1}}{1-D}\right) \quad (5)$$

Using (4) in (5), the CCM voltage gain is expressed as

$$G\left(\frac{V_0}{V_i}\,or\,\frac{I_i}{I_0}\right)=\left(\frac{1}{(1-D)(1-2D)}\right) \quad (6)$$

The voltage gain and effectiveness index as defined in [17] variation according to duty ratio is reported in Fig. 4.

The capacitor C_1 current in two operating modes is expressed as

$$\left.\begin{aligned} DT_s\quad &\rightarrow I_{C1\text{-}ON}=-(I_{L1}+I_{L2})\\ (1\text{-}D)T_s&\rightarrow I_{C1\text{-}OFF}=(I_{L1}-I_{L2})\end{aligned}\right\}$$

Upon writing the amp-sec balance for capacitor C_1.

$$I_{L2}=\frac{I_0}{1\text{-}D},\ \because(6)\rightarrow I_{L1}=\frac{I_0}{(1-D)(1-2D)} \quad (7)$$

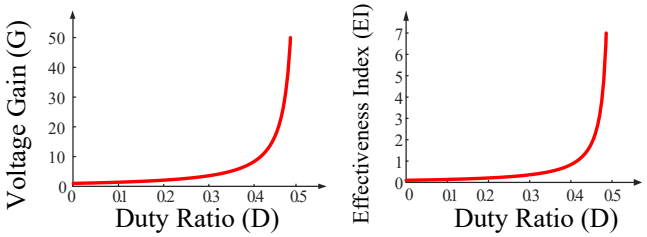


Fig. 4. *G* and *EI* versus duty ratio.

Using KCL and KVL on the selected loops of Fig. 2 the semiconductor element current-voltage stresses are as presented in the Table I.

A. Per Unit Input Current Ripple:

The per unit ripple current ($\Delta I_i/I_i$) as mentioned in [6] is often a quantitative measure for the converter to suit for the renewable applications. In this regard this section deals with

the estimation of per unit ripple current and its variation concerning to duty ratio as shown in Fig. 5.

From mode 1 of operation

$$v_{L1}=(V_i+V_{C1})=V_0\left(2(1-D)^2\right)=\frac{\Delta I_{L1}}{DT_S}$$

$$\Delta I_{L1}=\Delta I_i=\frac{V_0\left(2D(1-D)^2\right)}{L_1 f_S} \quad (8)$$

Using (6) in (8)

$$\frac{\Delta I_i}{I_i}=\left(\frac{V_0}{I_0}(1-D)(1-2D)\right)\frac{2D(1-D)^2}{L_1 f_S}$$

$$\frac{\Delta I_i}{I_i}=\left(\frac{R_O}{L_1 f_S}\right)D(1-D)^3(1-2D) \quad (9)$$

TABLE I. ELEMENT CURRENT-VOLTAGE STRESS

Element	Conducting Period	Average current	Peak current stress	Peak voltage stress
S_1	DT_S	$(I_{L1}+I_{L2})D$	$I_{L1}+I_{L2}+\left(\frac{\Delta I_{L1}+\Delta I_{L2}}{2}\right)$	$V_{C1}=\frac{V_i}{(1-2D)}$
		$\left(\frac{2I_o}{1-D}\right)D$	$\left(\frac{2I_o}{1-D}\right)\left(\frac{V_oD(1-D)^2}{L_1f_s}+\frac{V_oD}{L_2f_s}\right)$	$V_0(1-D)$
$S2$	DT_S	$(I_{L1})D$	$I_{L1}+\left(\frac{\Delta I_{L1}}{2}\right)$	$V_{C1}=\frac{V_i}{(1-2D)}$
		$\left(\frac{I_o}{(1-D)(1-2D)}\right)D$	$\left(\frac{I_o}{(1-D)(1-2D)}\right)\left(\frac{V_oD(1-D)^2}{L_1f_s}\right)$	$V_0(1-D)$
S_3	DT_S	$(I_{L2})D$	$I_{L2}+\left(\frac{\Delta I_{L2}}{2}\right)$	$V_0-V_{C1}=\frac{V_i(2D)}{(1-D)(1-2D)}$
		$\left(\frac{I_o}{(1-D)}\right)D$	$\left(\frac{I_o}{(1-D)}\right)\left(\frac{V_oD}{L_2f_s}\right)$	$V_0(2D)$
D_1	$(1-D)T_S$	$(I_{L1})(1-D)$	$I_{L1}+\left(\frac{\Delta I_{L1}}{2}\right)$	$V_{C1}=\frac{V_i}{(1-2D)}$
		$\left(\frac{I_o}{(1-D)(1-2D)}\right)(1-D)$	$\left(\frac{I_o}{(1-D)(1-2D)}\right)\left(\frac{V_oD(1-D)^2}{L_1f_s}\right)$	$V_0(1-D)$
D_2	$(1-D)T_S$	$(I_{L1}-I_{L2})(1-D)$	$(I_{L1}-I_{L2})+\left(\frac{\Delta I_{L1}-\Delta I_{L2}}{2}\right)$	$V_{C1}=\frac{V_i}{(1-2D)}$
		$\left(\frac{I_o\,2D}{(1-D)(1-2D)}\right)(1-D)$	$\left(\frac{I_o\,2D}{(1-D)(1-2D)}\right)\left(\frac{V_oD(1-D)^2}{L_1f_s}-\frac{V_oD}{L_2f_s}\right)$	$V_0(1-D)$
D_0	$(1-D)T_S$	$(I_{L2})(1-D)$	$(I_{L2})+\left(\frac{\Delta I_{L2}}{2}\right)$	$V_0+V_{C1}=\frac{V_i(2-D)}{(1-D)(1-2D)}$
		$\left(\frac{I_o}{(1-D)}\right)(1-D)$	$\left(\frac{I_o}{(1-D)}\right)\left(\frac{V_oD}{L_2f_s}\right)$	$V_0(2-D)$

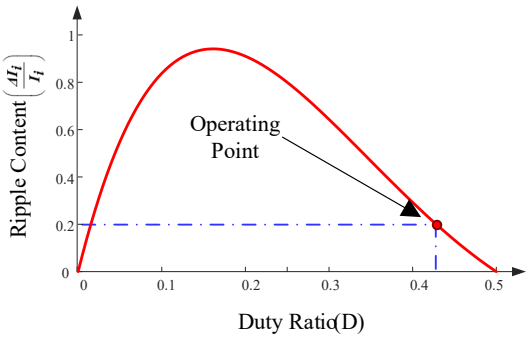


Fig. 5. Ripple current versus duty ratio.

It is observed from the Fig. 5 that at the operating duty ratio the per unit ripple current is 0.2 i.e., 20% of I_{L1}.

B. Inductor-Capacitor Design:

While designing the inductors, a ripple content of 20% to 40% of their average current is considered as %x. Similarly, in capacitors a ripple content of 1% to 5% (%y) of the respective average voltage is assumed. The inductors-capacitors design guide lines are as follows.

$$L_1\geq \frac{(V_i+V_{C1})\,D}{\%X_1\;I_{L1}f_s}\geq\frac{V_i^2\;(2D(1-D))}{(1-2D)\;(\%X_1)\;P_0\;f_s}$$

$$L_2\geq \frac{V_{C1}\;D}{\%X_2\;I_{L2}f_s}\geq\frac{V_i^2\;D}{(1-2D)^2\;(\%X_{21})\;P_0\;f_s} \quad (10)$$

$$C_1\geq\frac{(I_{L1}+I_{L2})\,DT_s}{(\%Y_1)\;V_{C1}}\geq\frac{P_0\;2D\;(1-D)\;(1-2D)}{(\%Y_1)\;V_i^2\;f_s}$$

$$C_0\geq\frac{(I_0)\;(DT_s)}{(\%Y_0)V_0}\geq\frac{P_0\;(D)(1-D)^2\;(1-2D)^2}{(\%Y_0)\;V_i^2\;f_s} \quad (11)$$

C. Elements and parasitics:

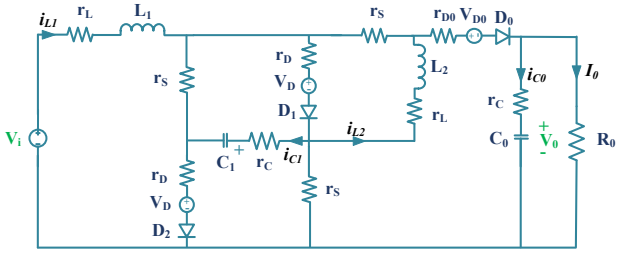


Fig. 6. Proposed converter with parasitics.

The proposed converter's power circuit comprises various parasitic elements, including capacitance with series ESR of r_C, inductors with series ESR of r_L, semiconducting elements like diodes with respective ESR of r_D and forward voltage drop of V_D, and resistance r_S for the switches during the conducting period. The proposed converter is as shown Fig. 6, after incorporating parasitics of the corresponding elements.

Rewriting (1) and (2) for inductor L_1 under the parasitics influence.

$$\left.\begin{aligned} v_{L1}&=(V_i+V_{C1})-I_{L1}(r_L+r_s)-(I_{L1}+I_{L2})(r_c+r_s)\\ v_{L1}&=(V_i-V_{C1})-I_{L1}(r_L+r_D)-(I_{L1}+I_{L2})(r_c+r_D)-2V_D \end{aligned}\right\} \quad (12)$$

Upon adopting volt-sec balance for inductor L_1, the capacitor C_1 voltage is written as

$$V_{C1}=\left(\frac{V_i}{1-2D}\right)-I_0r_L\left\{\frac{1}{(1-D)(1-2D)^2}\right\}-I_0r_s\left\{\frac{D(3-2D)}{(1-D)(1-2D)^2}\right\} - r_CI_0\left\{\frac{4D}{(1-2D)^2}\right\}-r_DI_0\left\{\frac{(1+2D)}{(1-2D)^2}\right\}-\frac{2V_D(1-D)}{(1-2D)^2} \quad (13)$$

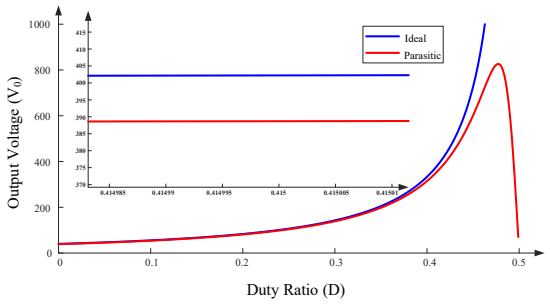
But $V_0=\frac{V_{C1}}{(1-D)}$; Therefore $V_{0\text{-}Parasitic}$ is written as

$$V_{0\text{-}Parasitic}=\frac{\left(\frac{V_i}{(1-D)(1-2D)}\right)-\frac{2V_D}{(1-2D)}}{1+\frac{r_L}{R_0}\left\{\frac{1}{(1-D)(1-2D)}\right\}^2+\frac{r_s}{R_0}\left\{\frac{D(3-2D)}{(1-D)^2(1-2D)^2}\right\}+\frac{r_C}{R_0}\left\{\frac{4D}{(1-D)(1-2D)^2}\right\}+\frac{r_D}{R_0}\left\{\frac{(1+2D)}{(1-D)(1-2D)^2}\right\}} \quad (14)$$

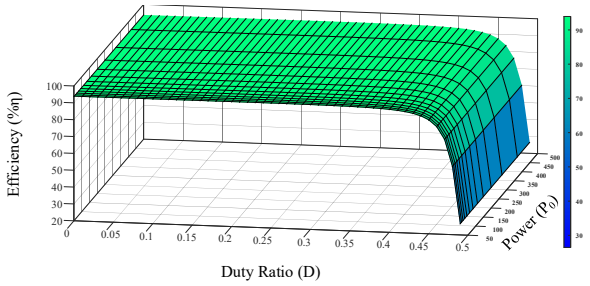
Using (14) the efficiency of the converter is written as

$$\eta=\frac{1-V_D\left(\frac{2(1-2D)}{V_i}\right)}{1+\frac{r_L}{R_0}\left\{\frac{1}{(1-D)(1-2D)}\right\}^2+\frac{r_s}{R_0}\left\{\frac{D(3-2D)}{(1-D)^2(1-2D)^2}\right\}+\frac{r_C}{R_0}\left\{\frac{4D}{(1-D)(1-2D)^2}\right\}+\frac{r_D}{R_0}\left\{\frac{(1+2D)}{(1-D)(1-2D)^2}\right\}} \quad (15)$$

Figure 7 (a) displays the plot of the element parasitics influence on the terminal voltage and its gain. Figure 7 (b) shows a schematic depiction of efficiency-load power against duty ratio. These terminal voltage and efficiency are in good accord with the experimental findings.



(a)



(b)

Fig. 7. Parasitic influence on (a) terminal voltage (b) efficiency.

D. Control Performance:

The proposed converter's control feasibility is analyzed using the state space averaging (SSA) method as in [18]. The suggested converter's steady-state analysis shows that there are two working modes resulting in one set of differential equations for each stage. The converter inductors and capacitors result in four state variables based on respective voltages and currents. The small signal model with the aid of state equations constitutes a fourth order formulation as represented in (16). The control to output transfer function is represented by (17) with stable closed loop bode plot as reported in Fig. 8. A simple PI controller with K_p= 0.00003 and K_i=0.0044 is adopted to regulate the load voltage.

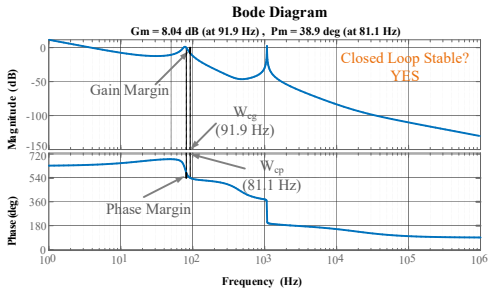
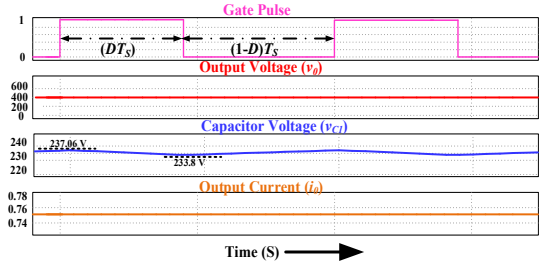


Fig. 8. Closed loop bode plot of proposed converter.

III. Results and Discussion

The feasibility of proposed converter has been validated by means of simulation (PSIM) platform as well as hardware prototype with the specifications as mentioned in Table II. Ideally the converter attains a terminal voltage of 400 V at a duty ratio of 0.415 with the supply voltage being at 40 V. This in fact justify that a voltage gain as in (6) is being achieved for the proposed converter. The next factor of discussion would be capacitor voltage V_{C1}, it has a ripple voltage varying from 233.8 V to 237.06 V (ripple content of 1.4%) with an average of 235.4 V as shown in Fig. 9 (a). The output current is in accord with load power and terminal voltage i.e., 0.75 A as shown in Fig. 9 (a). Inductor voltages and currents justifies (1), (2) and (7), with a source current average of 7.5 A as in Fig. 9 (b). This in turn validates the stated converter operating efficiency as 91.89%. The semiconductor current-voltage stresses are as reported in Fig. 9 (c) and (d), from which it is clear that these results are validating Table I.

The proposed converter experimental validation is also carried out and the results are projected in Fig. 10 (a). The converter attains an output voltage of 388 V followed by the output current of 0.74 A and more importantly the capacitor C_0 peak current stress is very moderate and its in great accord with the ideal wave shape. The terminal voltage regulation by means of a single loop voltage control is experimentally validated as in Fig. 10 (b) for varying input voltage V_i.



(a)

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{c1}(t)}{dt} \\ \frac{d\hat{v}_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-2d)}{L} & 0 \\ 0 & 0 & \frac{1}{L} & \frac{-(1-d)}{L} \\ \frac{1-2d}{C} & \frac{-1}{C} & 0 & 0 \\ 0 & \frac{1-d}{C} & 0 & \frac{-1}{R_0 C} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{c1}(t) \\ \hat{v}_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t) + \begin{bmatrix} 0 & 0 & \frac{2}{L} & 0 \\ 0 & 0 & 0 & \frac{1}{L} \\ \frac{-2}{C} & 0 & 0 & 0 \\ 0 & \frac{-1}{C} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C0} \end{bmatrix} \hat{d}(t) \quad (16)$$

$$\left(\frac{\hat{v}_0(s)}{\hat{d}(s)} \Big/ \hat{v}_i(s)=0 \right) = \frac{-1.021\times10^{14}\, s^4 + 1.24\times10^{19}\, s^3 - 2.509\times10^{22}\, s^2 + 9.035\times10^{25} s + 1.383\times10^{28}}{5.278\times10^{13}\, s^5 + 4.948\times10^{15}\, s^4 + 2.412\times10^{21}\, s^3 + 1.697\times10^{23}\, s^2 + 5.8\times10^{26}\, s} \quad (17)$$

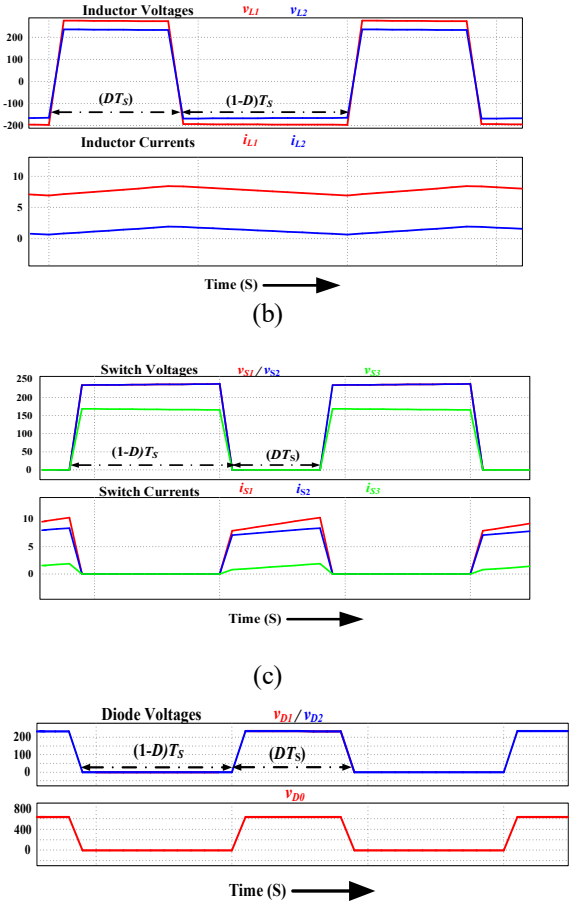


Fig. 9. Simulation Results (a) capacitor C_0-C_1 voltages and load current i_0 (b) inductor voltages-currents (c) switch voltages-currents and (d) diode voltages.

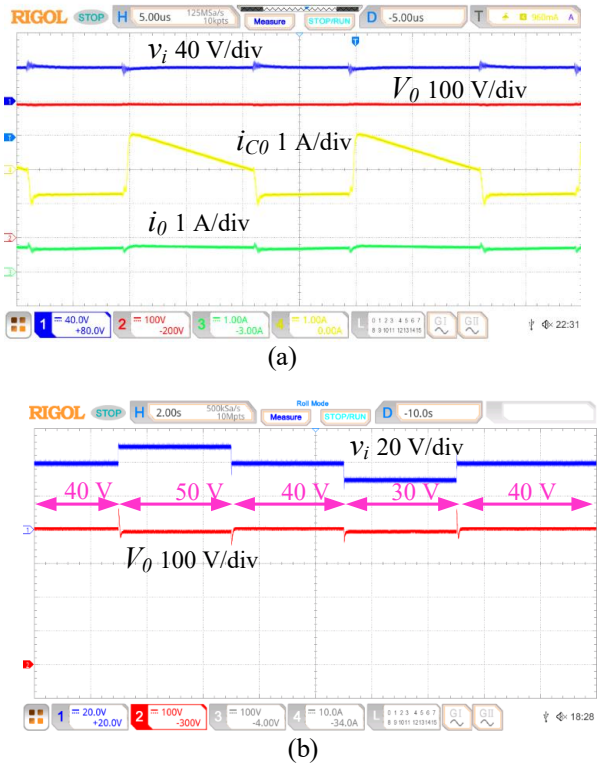


Fig. 10. Experimental Results (a) capacitor C_0 voltage-current and load current (b) Closed loop voltage control.

TABLE II. DESIGN SPECIFICATIONS

Specification	Rating (300 W)	
Inductors	$L_1 = L_2 = 1.5$ mH	
capacitors	$C_1 = C_2 = 22$ µF, $C_0 = 100$ µF	
Diodes	D_0 (STPSC10H065DI)	D_1, D_2 (MUR 1560G)
Switches	S_1, S_2 (FCH072N60F)	

IV. CONCLUSION

In this article, a switched inductor-switched capacitor-based high boost dc-dc converter is proposed. A boosting factor akin to a quasi-Z-Source converter is ensured by the front-end single inductor-switched capacitor arrangement. Moreover, to meet the specified 400V requirement, the boosting factor is further enhanced by adopting the second switched inductor L_2. By means of the decoupling switch

S_3, the load-end capacitor peak current is reduced to greater extent. All the switches and diodes voltage stress are observed to be less than the output voltage (V_0) except the diode D_0 which is having a voltage stress of $V_0(2\text{-}D)$. Since the inductor's charging interval is less because of 50% upper limit on the duty their sizing issues do persist. This concern can be compensated by using the coupled inductor technology with soft switching as a future scope. The key indices of the aforesaid converter are in good accord with their ideal conditions.

REFERENCES

[1] B. Axelrod, Y. Berkovich and A. Ioinovici, "Switched-Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687-696, March 2008, doi: 10.1109/TCSI.2008.916403

[2] Baba, MF, Giridhar, AV, Narasimharaju, BL. Nonisolated high gain hybrid switched-inductor DC-DC converter with common switch grounding. *Int J Circ Theor Appl*. 2022; 50(8): 2810-2828. doi:10.1002/cta.3295.

[3] M. Zhu, K. Yu and F. L. Luo, "Switched Inductor Z-Source Inverter," in *IEEE Transactions on Power Electronics*, vol. 25, no. 8, pp. 2150-2158, Aug. 2010, doi: 10.1109/TPEL.2010.2046676

[4] A. Kumar *et al*., "A High Voltage Gain DC–DC Converter With Common Grounding for Fuel Cell Vehicle," in *IEEE Transactions on Vehicular Technology*, vol. 69, no. 8, pp. 8290-8304, Aug. 2020, doi: 10.1109/TVT.2020.2994618.

[5] M. Veerachary and P. Kumar, "Analysis and Design of Quasi-Z-Source Equivalent DC–DC Boost Converters," in *IEEE Transactions on Industry Applications*, vol. 56, no. 6, pp. 6642-6656, Nov.-Dec. 2020, doi: 10.1109/TIA.2020.3021372.

[6] M. F. Baba, A. V. Giridhar and B. L. Narasimharaju, "A Wide Voltage Range Bidirectional High Voltage Transfer Ratio Quadratic Boost DC-DC converter for EVs with Hybrid Energy Sources," in *IEEE Journal of Emerging and Selected Topics in Industrial* Electronics, doi: 10.1109/JESTIE.2023.3327639.

[7] Baba MF, Giridhar AV, Narasimharaju BL. Active switched-capacitor based ultra-voltage gain quadratic boost DC-DC converters. Int J Circ Theor Appl. 2023; 51(3): 1389-1416. doi:10.1002/cta.3453.

[8] M. Zhu, K. Yu, and F. L. Luo, "Switched-inductor Z-source inverter," IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[9] T. Takiguchi and H. Koizumi, "Quasi-Z-source DC–DC converter with voltage-lift technique," in Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc. (IECON), Vienna, Austria, Nov. 2013, pp. 1191–1196.

[10] H. Shen, B. Zhang, and D. Qiu, "Hybrid Z-source boost DC–DC converters," IEEE Trans. Ind. Electron., vol. 64, no. 1, pp. 310–319, Jan. 2017.

[11] K. Patidar and A. C. Umarikar, "High step-up pulse-width modulation DC–DC converter based on quasi-Z-source topology," IET Power Electron., vol. 8, no. 4, pp. 477–488, Apr. 2015

[12] Y. Zhang et al., "Wide input-voltage range boost three-level DC–DC converter with quasi-Z source for fuel cell vehicles," IEEE Trans. Power Electron., vol. 32, no. 9, pp. 6728–6738, Sep. 2017.

[13] Y. Zhang, C. Fu, M. Sumner, and P. Wang, "A wide input-voltage range quasi-Z-source boost DC–DC converter with high-voltage gain for fuel cell vehicles," IEEE Trans. Ind. Electron., vol. 65, no. 6, pp. 5201–5212, Jun. 2018.

[14] M. M. Haji-Esmaeili, E. Babaei, and M. Sabahi, "High step-up quasi-Zsource DC-DC converter," IEEE Trans. Power Electron., vol. 33, no. 12, pp. 10563–10571, Dec. 2018.

[15] Y. Ji, H. Liu, C. Zhang, and P. Wheeler, "Voltage-double magnetically coupled impedance source networks," IEEE Trans. Power Electron., vol. 33, no. 7, pp. 5983–5994, Jul. 2018.

[16] P. Kumar and M. Veerachary, "Z-network plus switched-capacitor boost DC–DC converter," IEEE J. Emerg. Sel. Topics Power Electron., vol. 9, no. 1, pp. 791–803, Feb. 2021.

APPENDIX

TABLE III. COMPARISON WITH CLASSIC BOOST CONVERTER

Performance Indices	Boost Converter	Proposed Converter
Voltage Gain	$\frac{1}{(1-D)}$	$\frac{1}{(1-D)(1-2D)}$
Element Count	4	10
(L/C/S/D)	(1/1/1/1)	(2/2/3/3)
Peak Switch Voltage Stress	V_0	DV_0
Peak Diode Voltage Stress	V_0	$(2\text{-}D)V_0$
Input Current Ripple Content	Low	Low
Upper Limit on Duty Ratio	100%	50%

TABLE IV. SIMULATED AND EXPERIMENTAL RESULTS COMPARISON

Performance Indices	Simulation	Experimental
Input Current	7.5 A	7.77 A
Output Voltage	400 V	388 V
Output Current	0.75 A	0.74 A