An Ultra High Gain Switched-Capacitor Boost DC-DC Converter with Reduced Ripple Current

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***Abstract*— An ultra high gain quadratic boost converter based on switched-capacitor is proposed in this article. The ultra high gain is achieved with a low duty ratio and a wide range of flexibility. The proposed converter provides significantly reduced device voltage stress and source current ripple. This article presents in detail discussion on the operating principle, continuous conduction mode (CCM) and, discontinuous conduction modes (DCM) and the parasitics effect on the output voltage and efficiency of the proposed converter. Also, the stated converter performance comparison with similar quadratic boost DC-DC converters is presented. The performance indices of the proposed converter are verified by a prototype of 400 V, 50 kHz, 200 W.**

Link to graphical and video abstracts, and to code: https://latamt.ieeer9.org/index.php/transactions/article/view/9018

***Index Terms*— Low voltage stress, Nonisolated converter, Quadratic boost converter, Switched-capacitor, Ultrahigh step-up voltage gain.**

I. Introduction

United Nations Economic Commission for Latin America and the Caribbean in its 2030 agenda (7.1 and 7.2) urges for clean and reliable renewable energy resources technology to transform lives, economics and the planet. To suit this concern of renewable sources power conditioning a plethora of high step-up nonisolated DC-DC converter has been presented in [1], [2] in regard to attaining high voltage gain, power electronic interface to the grid, and micro source applications. Despite having duty ratio flexibility of wide range and high amplification, nonisolated converters have elevated switching intervals, which results in high switching losses and poor efficiency. The coupled inductors are often integrated to the nonisolated converters in which by adjusting the turns ratio high voltage gains are achieved. The flux leakage paths other than the core in the coupled inductor cause leakage inductance and the effect of this leakage inductance in terms of static voltage gain is loss of duty ratio.

The nonisolated DC-DC converters having high voltage conversion ratio at low duty cycles, low input current ripple and are free from coupled inductors is the promising solution for the aforementioned constraints. A three-switching state split duty nonisolated DC-DC converter is proposed in [3]. Here, one additional switch is used to avoid long conducting intervals for the interleaved switches but still the output capacitor must support the load voltage profile for longer intervals. The converters in [4], [5] suggested an alternate approach to have high dc static gain at a low duty ratio. The inductor charging profile in [4] is improved with the aid of a dc source and capacitor (C_1) but the problems of high source current ripple and absence of common ground persist in the stated converter. The elevated ripple content can be reduced by having an inductor as stated in [5] at the input port. Although the converter in [5] has improved voltage gain at low duty ratio with moderate component count, the peak switch current stress is substantially higher.

The passive and active switched inductors (PSL and ASL) are integrated into a single converter [6] to form a hybrid switched inductor (HSL). Here symmetrical and asymmetrical HSL configurations are reported to attain high voltage gain. The converter in [7] used HSL arrangement with tri-switching states to enhance the voltage gain and to avoid extended duty intervals for the switches. The above stated two converters are having high component count and the number of devices acting in the forward path is significantly high. A Zeta derived converters with and without output inversion are proposed in [8]. Although these converters acquire significant voltage gain, the problem of discontinuity in the input current persists. In recent trends [9-12], modified SEPIC converters or integration of SEPIC converters to the existing DC-DC converters is gaining attraction with improved voltage gain and other performance indices. The converter in [9] used a capacitor (C_M) which is in the previous state charged by a boost converter to power the second inductor. Like the previous case, the converter in [10] is proposed but here the only difference is instead of a boost converter at the primary end an active switched-interleaved DC-DC converter is used. The converter in [9] has low voltage gain than that of the converter in [10], although it is having enhanced voltage gain lack of common ground overpowers all its merits. The improved SEPIC converters with diode-capacitor voltage lift arrangement [11] and with quadratic voltage gain are reported in and [12]. The converter in [12] synthesized by integrating SEPIC and conventional PSL

The associate editor coordinating the review of this manuscript and approving it for publication was Julio C. Rosas-Caro (*Corresponding author: M. F. Baba*).

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arrangement at front end to obtain quadratic voltage gain. The converter in [11] attains a noticeable voltage gain but its component count is high and the converter in [12] has a DC static gain of $\left(d/(1-d)^2 ; d=duty\ ratio\right)$, with a high number of inductors which makes the power density to be low.

The aforementioned discussion emphasizes that high dc static gain at moderate duty ratio as well as with low component count is only realizable with a quadratic boost converter. A switched-capacitor cell integrated quadratic boost converter is proposed in [13] in which voltage gain is enhanced with a diode-capacitor voltage lift arrangement. The shortfalls of the converter in [13] are high switch current stress and the absence of common ground.

In light of the aforementioned causes, a quadratic boost converter with the major contributions being low input current ripple with the aid of series inductor at the input and constituting of an absolute common ground is proposed in this article. The stated converter is suitable for the green energy micro source powered dc microgrid application, in which low dc input voltage in the range of 12 V-48 V to be boosted in the range of 400 V, 600 V and 800 V. The proposed converter is also suitable for hybrid energy source powered EV vehicle, where in which the low dc voltage after rectification to be stepped up to the required voltage level at the inverter side.

The following are the crucial features of the proposed converter.

- Improved step-up gain at a modest duty ratio and with moderate component count
- Only one element (D_0) in the forward flow path
- Further to improve the step-up gain and lower the voltage stress on semiconducting elements, a basic capacitor voltage lift (D_3-C_3) is used.

The rest of the article is organized as; the topological key synthesis is reflected in section II, steady state operation, design of elements, parasitics effect and closed loop performance is reported in section III, section IV comprises of key comparison metrics, the experimental validation of performance indices is discussed in section V and finally the conclusive remarks are described in section VI.

II. Topological Derivation

A three-stage cascade connection is used to derive the proposed topology i.e., boost stage 1, boost stage 2 and switched capacitor voltage lift stage as shown in Table I. The boost stage 1 and 2 loads are assumed to be R_{01} and R_{02}. Further in cascading these loads are replaced by respective capacitors (C_i) followed by their voltages (VMi). The third stage i.e., voltage lift stage can be integrated with in stage 1 and stage 2 because it uses internal switches of aforementioned stages in charging process. Here, capacitor C_2 posture in the final derived topology is altered in such a way that the total input current passes through the inductor L_1 as a result its ripple content is low.

III. Steady State Operation and Analysis

The following analysis consists of the discussion on CCM, DCM, border conduction mode (BCM) and effect of element parasitics on output voltage, and efficiency of switched capacitor based quadratic boost DC-DC converter (SCQBC) converter as shown in Fig. 1.

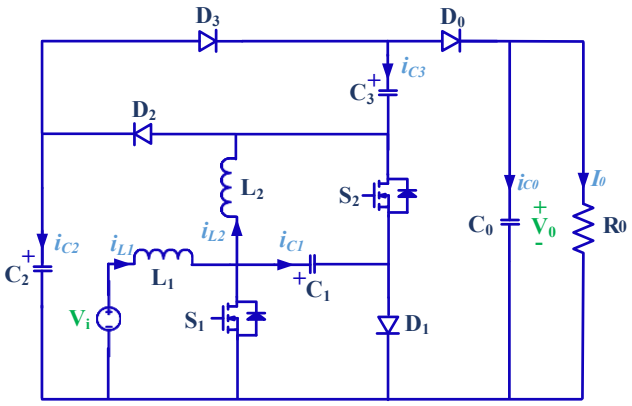


Fig. 1. Proposed switched capacitor based quadratic boost converter topology.

A. CCM and DCM Operation:

The CCM operation comprises two modes i.e., mode 1 and 2 depending on the switching instants (t_0 and t_1) of S_1 and S_2, and the key waveforms are as shown in Fig. 2.

Mode 1: The SCQBC converter mode 1 of operation is initiated at instant t_0 as shown in *Fig. 3*, when a gate pulse is applied to both switches. The applied voltage across inductor L_1 is V_i, that of inductor L_2 and capacitor C_3 is V_{C1}, $V_{C1}+V_{C2}$.

The reverse biased diode D_0 makes the load R_0 to be powered by capacitor C_0. Hence, V_{L1} and V_{L2} are expressed as

$$V_{L1}=V_i\ ;\ V_{L2}=V_{C1} \tag{1}$$

Mode 2: This mode of operation is initiated upon the withdrawal of gate pulse for the two switches at instant t_1. The inductor L_1 along with source V_i charges the capacitors C_1. Since the diode D_0 is conducting, the two inductors along with the source and capacitor C_3 powers load R_0 as well as capacitor C_0. The inductor voltage profile is expressed as

$$V_{L1}=V_i-V_{C1}\ ;\ V_{L2}=V_{C1}+V_{C3}-V_0 \tag{2}$$

Using (1) and (2) for the inductors L_1 and L_2 volt-sec balance, the voltages of three capacitors are as follows

$$V_{C1}=\frac{V_i}{1-D},\ V_{C2}=\frac{V_i}{(1-D)^2};\ V_{C3}=\frac{V_i\,(2-D)}{(1-D)^2} \tag{3}$$

Using (1) to (3) the step-up voltage gain is as follows

$$G_{CCM}\left(\frac{V_0}{V_i}\right)=\frac{3-D}{(1-D)^2} \tag{4}$$

The inductor L_2 peak current (I_{L2P}) for mode 1 and mode 2 is written as

$$\left.\begin{aligned}(I_{L2p})^{I}&=\left(\frac{V_{C1}}{L_2}\right)DT_s\\ (I_{L2p})^{II}&=\left(\frac{V_0-V_{C1}-V_{C3}}{L_2}\right)D_xT_s\end{aligned}\right\} \tag{5}$$

At the instant t_1, the above-stated inductor peak currents are equal as shown in Fig. 4 (a).

$$(I_{L2p})^{I}=(I_{L2p})^{II} \tag{6}$$

Using (5) in (6), the duty ratio D_x is written as

$$D_x=\frac{D\,(1-D)}{\left(\frac{V_0}{V_i}\right)(1-D)^2-(3-2D)} \tag{7}$$

From Fig. 4 (b) in the mode 3 of DCM operation the load is powered by capacitor C_0 only, hence I_{C0} is represented as

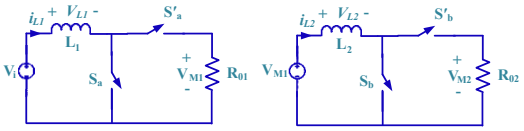
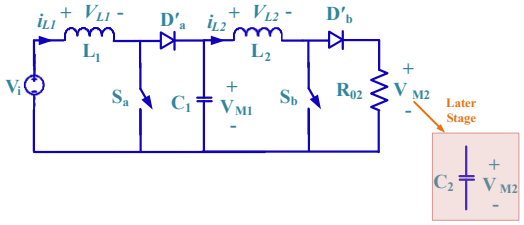
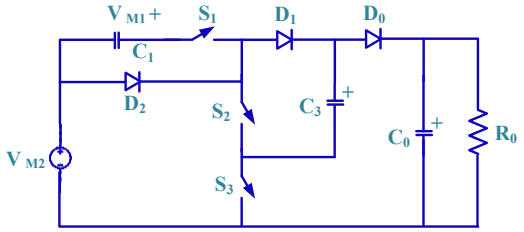
$$I_{C0}=\left(\frac{1}{2}D_x\frac{I_{L2P}}{2}\right)-I_0 \tag{8}$$

Using (5) and (7) in (8), and making the average value of I_{C0} in (8) zero to evaluate the DCM voltage gain

$$G_{DCM}=\frac{(3\text{-}2D)\ \pm\ \sqrt{(3\text{-}2D)^2+\left(\left(D(1\text{-}D)\right)^2/\tau_L\right)}}{2(1\text{-}D)^2}\ ;\ \tau_L=\frac{L_2 f_s}{R_0} \qquad (9)$$

TABLE I

SYNTHESIS OF PROPOSED SWITCHED CAPACITOR BASED QUADRATIC BOOST DC-DC CONVERTER (SCQBC)

Step	Methodology	Analysis
1	Preferred voltage gain is restructured in single inductor converters (SIC) and voltage lift stage to create a cascade form	$V_0=\frac{3\text{-}D}{(1\text{-}D)^2}\ V_i=\underbrace{\left\{\frac{1}{1\text{-}D}\right\}\left\{\frac{1}{1\text{-}D}\right\}}_{\frac{1}{f_D'(D)}\rightarrow\text{SIC form}}\ \underbrace{\{3\text{-}D\}}_{\frac{f_N'(D)}{1}\rightarrow\text{Voltage lift stage}}$ $V_{M1}=\left(\frac{1}{1\text{-}D}\right)V_i \xleftrightarrow{\text{Cascade Connection}} V_{M2}=\left(\frac{1}{1\text{-}D}\right)V_{M1}$
2	Individual stage voltage gains are decomposed to obtain volt-sec balance equations. There by inductor voltages are obtained in each switching sub interval of operation.	$V_i(DT_s)+((1\text{-}D)T_s)\ (V_i\text{-}V_{M1})=0$ $v_{L1}/DT_s=V_i$ $v_{L1}/(1\text{-}D)\ T_s=V_i\text{-}V_{M1}$ $V_{M1}(DT_s)+((1-D)T_s)\ (V_{M1}\text{-}V_{M2})=0$ $v_{L2}/DT_s=V_{M1}$ $v_{L2}/(1-D)\ T_s=V_{M1}\text{-}V_{M2}$
3	Synthesize the equivalent sub-circuits of SIC's as represented in [14] and [15]	 $\left\{\begin{matrix} S_a,S_b\rightarrow DT_s \\ S'_a,S'_b\rightarrow (1\text{-}D)T_s \end{matrix}\right\}$
4	Merge the individual SIC's voltage loops by considering the previous stage output as input next stage. Here the load $R_{0,1}$ is replaced by a capacitor C_1 and the switches S'_a and S'_b are replaced by diodes.	
5	Synthesize the voltage lift stage i.e., the final stage by considering V_{M1} and V_{M2} as the voltages across the respective capacitors in step-4.	 $\left\{\begin{matrix} S_1,S_3 \text{and } D_1\rightarrow DT_s\rightarrow V_{C3}=V_{M1}+V_{M2} \\ D_0,D_2 \text{and } S_2\rightarrow (1\text{-}D)T_s\rightarrow V_0=V_{M1}+2V_{M2}=\frac{3\text{-}D}{(1\text{-}D)^2}\ V_i \end{matrix}\right\}$
6	Integrate all the individual sub-circuits to construct the overall cascade form. Here $R_{0,2}$ is replaced by a capacitor C_2, and the positions of C_1 and D'_a are interchanged for better synthesis of the proposed topology. The switches and diodes in voltage lift stage are also optimized to get the same outcome as shown in step-5.	The proposed SCQBC converter

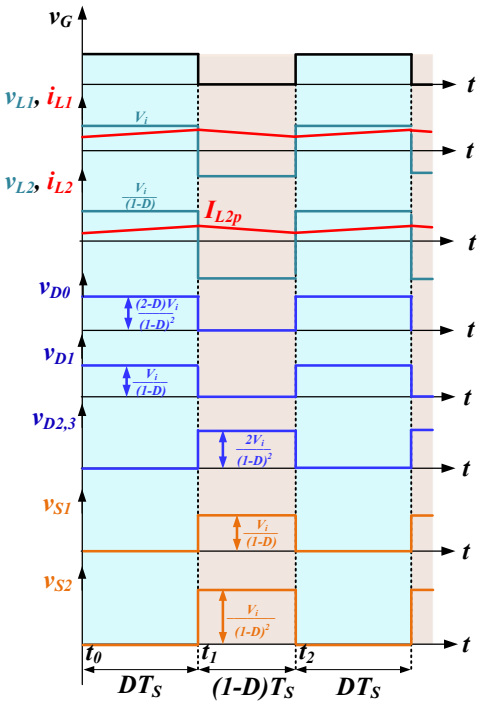


Fig. 2. Ideal operating waveforms of the SCQBC converter in one switching cycle (t_0-t_2).

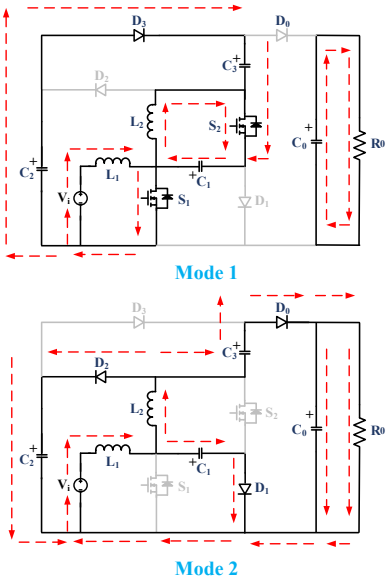


Fig. 3. Operating modes of SCQBC converter in continuous conduction mode.

Numerous crucial parameters are discussed in the aforementioned analysis i.e., capacitor voltage stresses, voltage gain in CCM and DCM operations. Furthermore, upon using KVL equations for mode 1 of operation the diode voltage stresses v_{D0}, v_{D1} and v_{D2} are primarily equal to V_0+V_{C1}-V_{C3}, V_{C1} and V_{C3} respectively. Similarly, from mode 2 of operation the semiconductor elements D_3, S_1 and S_2 are at a voltage stress of V_{C3}, V_{C1} and V_0-V_{C3}. The DCM voltage gain which is obtained by (9) is experimentally validated in the section V of the manuscript.

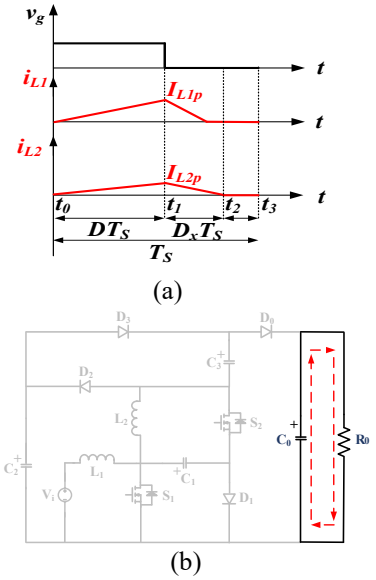


Fig. 4. DCM operation of SCQBC converter (a) key waveforms (b) mode 3 of operation.

B. BCM Operation:

The boundary condition is a common trace between CCM and DCM operations at which respective voltage gains are equal. Using G_{CCM} and G_{DCM} or by equating the ripple current of inductors to twice their average values, the inductor time constants at the boundary are represented as

$$\tau_{L1B}=\frac{D(1-D)^4}{2\,(3-D)^2},\ \tau_{L2B}=\frac{D(1-D)^2}{4\,(3-D)} \tag{10}$$

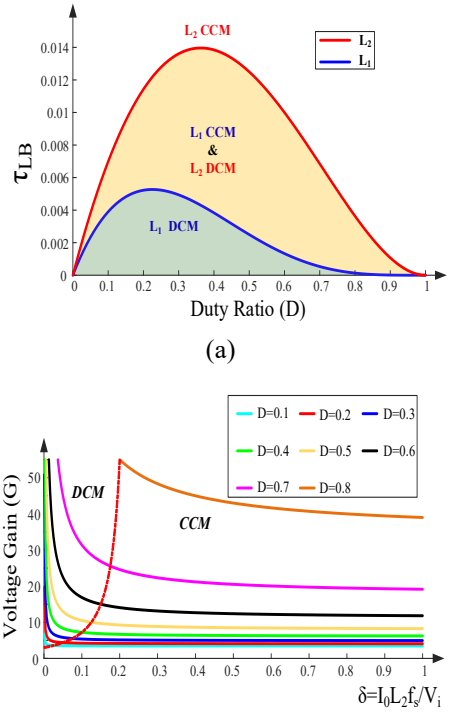


Fig. 5. SCQBC converter (a) boundary inductor time constant versus duty ratio (b) external characteristics.

Fig. 5 (a) depicts the plot of τ_{LB} concerning the variations in duty ratio (D).

By using (8), the critical load is expressed as

$$R_{0\text{-}cr}=\frac{4\,L_2 f_s}{D\,(1\text{-}D)^2}(3\text{-}D) \tag{11}$$

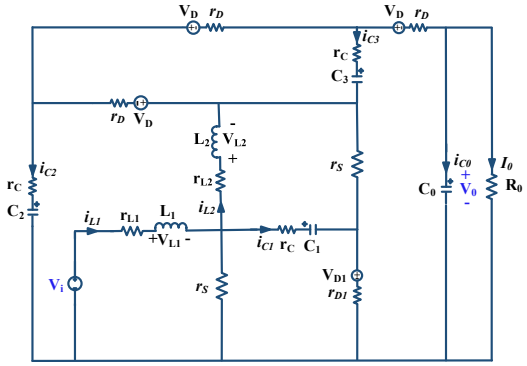
A dimensionless factor (δ) is used to represent the output current of SCQBC converter, which is expressed as follows

$$\delta=\frac{I_0 L_2 f_s}{V_i}$$

Using (10) in (8), the critical value of δ is expressed as

$$\delta_{cr}=\frac{D^2}{4(G(1\text{-}D)^2\text{-}(3\text{-}2D))} \tag{12}$$

The external characteristics of the SCQBC converter for different duty ratios are given by (12) and as shown in Fig. 5 (b).



C. Effect of Element Parasitics:

Fig. 6. Schematic representation of element parasitics in SCQBC converter.

The proposed converter semiconductor and energy storage elements are considered with the respective parasitic parameters i.e., the capacitors and inductors are now consists of equivalent series resistance (ESR), diodes have resembled with series connection of forward voltage drop and its internal resistance, and the switches are replaced with its on-state resistance as shown in Fig.6 for the following analysis in terms of output voltage and efficiency. A similar analysis as in the case of CCM operation is carried out for the inductors L_1 and L_2 voltages to evaluate the output voltage of SCQBC converter (with the same operating conditions that are considered for CCM operation) which is as follows

$$V_0=\frac{V_i\left(\frac{3\text{-}D}{(1\text{-}D)^2}\right)\text{-}V_{D1}\left(\frac{3\text{-}D}{1\text{-}D}\right)}{1+a\left(\frac{r_{L1}}{R_0}\right)+b\left(\frac{r_S}{R_0}\right)+c\left(\frac{r_C+r_{D1}}{R_0}\right)} \tag{13}$$

Where

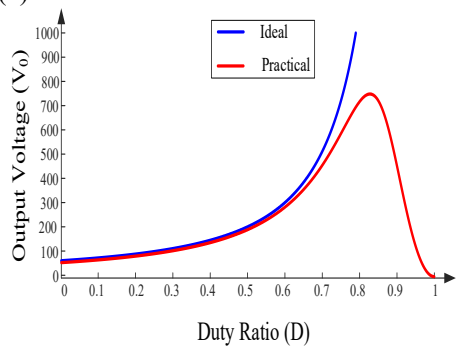
$$a=b=\frac{(3\text{-}D)^2}{(1\text{-}D)^4}\quad c=\frac{2D\,(3\text{-}D)}{(1\text{-}D)^3}$$

The plot representing converter terminal voltage V_0 is shown in Fig. 7 (a) (at V_i=20 V), in which voltage V_0 tends to zero as the duty nears unity.

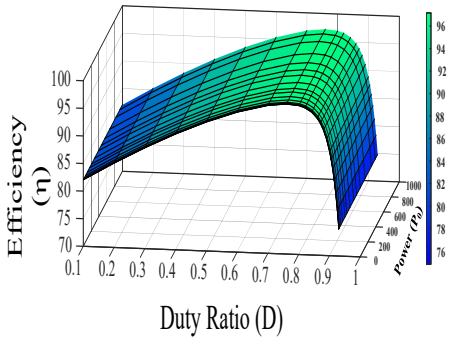
Using (13) the efficiency of SCQBC converter with element parasitics is evaluated as

$$\eta=\frac{1\text{-}\frac{V_{D1}}{V_i}(1\text{-}D)}{1+\left(\frac{(3\text{-}D)^2}{(1\text{-}D)^4}\right)\left(\left(\frac{r_{L1}}{R_0}\right)+\left(\frac{r_S}{R_0}\right)\right)+\left(\frac{2D\,(3\text{-}D)}{(1\text{-}D)^3}\right)\left(\frac{r_C+r_{D1}}{R_0}\right)} \tag{14}$$

The switching losses must be deducted from the above expression to include this portion of losses. The variation of efficiency, output power, versus duty ratio plots are shown in Fig.7 (b).



(a)



(b)

Fig. 7. SCQBC converter (a) V_0 versus D (b) 3-D plot of efficiency, power versus duty ratio with element parasitics.

D. Design Specifications:

The inductors are designed by keeping the ripple content between 20% to 40% of their average currents. The inductor L_2 is designed for an upper limit in the ripple current (40%) so that its size is effectively reduced. Similarly, the capacitors are designed to have a ripple content of less than 5% of their steady-state voltages.

The following expressions are design considerations for inductors and capacitors.

$$\left.\begin{aligned} L_1&\geq\frac{V_i\,D}{(0.2\,I_{L1})f_s}\\ L_2&\geq\frac{V_{C1}\,D}{(0.4\,I_{L2})f_s}\\ (C_X)&\geq\frac{I_{C1off}\,D}{(0.05\,V_{CX})f_s},\ X=1\text{-}3\\ C_0&\geq\frac{I_0\,D}{(0.05\,V_0)f_s}\end{aligned}\right\} \tag{15}$$

Where

$$\left.I_{L1}=\frac{I_o(3\text{-}D)}{(1\text{-}D)^2},I_{L2}=\frac{2I_o}{1\text{-}D},I_{C1off}=I_{L1}\text{-}I_{L2}\right\}$$

E. Control Performance:

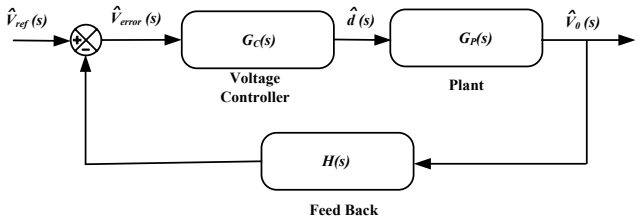


Fig. 8. Single loop voltage control scheme for SCQBC converter.

The proposed converter is designed with a system of single loop voltage control with feedback $H(s)$ (=1) as shown in Fig. 8. It can be observed from the Fig. 8 that $G_P(s)$ represents the plant or the proposed converter preceding by a voltage controller $G_C(s)$ to obtain stable output voltage against perturbation in load current and source voltage. The control performance of SCQBC converter is evaluated by standard small signal modeling. The converter voltage variables are $v_i(t)$ and $v_0(t)$, the control variable is $d(t)$, and the state variables for inductors (L_1 and L_2) and capacitors (C_1, C_2, and C_3) are $i_{L1}(t)$, $i_{L2}(t)$, $v_{c1}(t)$, $v_{c2}(t)$ and $v_{c3}(t)$ respectively.

The SCQBC converter state equations for the durations DTs and $(1\text{-}D)Ts$ with the assumption of each capacitor has an ESR are written as

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{Cr} & \frac{-1}{Cr} & \frac{1}{Cr} & 0 \\ 0 & 0 & \frac{1}{Cr} & \frac{1}{Cr} & \frac{-1}{Cr} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{R_0C_0} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i(t) \quad (16)$$

$$v_{c0}(t) = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 1][i_{L1}(t) \;\; i_{L2}(t) \;\; v_{c1}(t) \;\; v_{c2}(t) \;\; v_{c3}(t) \;\; v_{c0}(t)]^T$$

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ \frac{1}{C} & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & \frac{-1}{Cr} & \frac{-1}{Cr} & \frac{1}{Cr} \\ 0 & 0 & 0 & \frac{-1}{Cr} & \frac{-1}{Cr} & \frac{1}{Cr} \\ 0 & 0 & 0 & \frac{1}{C_0r} & \frac{1}{C_0r} & -\left(\frac{R_0+r}{C_0rR_0}\right) \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i(t) \quad (17)$$

$$v_{c0}(t) = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 1][i_{L1}(t) \;\; i_{L2}(t) \;\; v_{c1}(t) \;\; v_{c2}(t) \;\; v_{c3}(t) \;\; v_{c0}(t)]^T$$

Using (16) and (17), average state equation of the SCQBC converter is written as

$$\begin{bmatrix} \frac{di_{L1}(t)}{dt} \\ \frac{di_{L2}(t)}{dt} \\ \frac{dv_{c1}(t)}{dt} \\ \frac{dv_{c2}(t)}{dt} \\ \frac{dv_{c3}(t)}{dt} \\ \frac{dv_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d(t))}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{-(1-2d(t))}{L_2} & \frac{(1-d(t))}{L_2} & 0 & 0 \\ \frac{1-d(t)}{C} & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-d(t)}{C} & \frac{-d(t)}{Cr} & \frac{-1}{Cr} & \frac{-(1-2d(t))}{Cr} & \frac{(1-d(t))}{Cr} \\ 0 & 0 & \frac{d(t)}{Cr} & \frac{-(1-2d(t))}{Cr} & \frac{-1}{Cr} & \frac{(1-d(t))}{Cr} \\ 0 & 0 & 0 & \frac{(1-d(t))}{C_0r} & \frac{(1-d(t))}{C_0r} & \frac{-(1-(1-r)d(t))}{C_0rR_0} \end{bmatrix} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{c1}(t) \\ v_{c2}(t) \\ v_{c3}(t) \\ v_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i(t) \quad (18)$$

$$v_{c0}(t) = [0 \;\; 0 \;\; 0 \;\; 0 \;\; 0 \;\; 1][i_{L1}(t) \;\; i_{L2}(t) \;\; v_{c1}(t) \;\; v_{c2}(t) \;\; v_{c3}(t) \;\; v_{c0}(t)]^T$$

Assuming small signal perturbations are applied to the converter and with the aid of steady-state and small signal variables the SCQBC converter small signal model is obtained as in (19).

The open loop duty to output voltage (V_0) transfer function of the proposed converter is expressed in (20) assuming the perturbations at the input side are zero.

The PI controller is used to acquire a stiff voltage V_0 concerning the aforementioned perturbances. The SCQBC converter open loop bode plot for (20) is as shown in Fig 9.

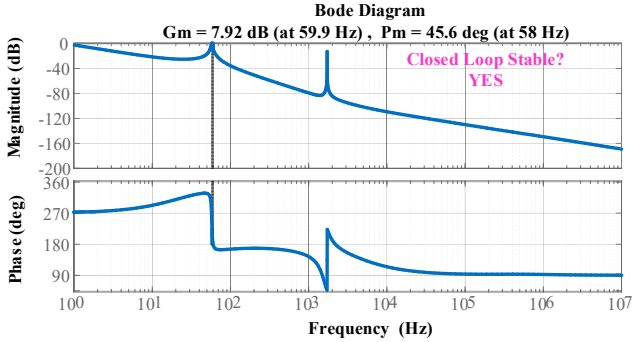


Fig. 9. Bode plot of SCQBC converter (open loop).

IV. Performance Comparison

The performance comparison of similar quadratic boost topologies with the proposed converter in terms of voltage gain, normalized voltage stress, component count, and ripple content in the input current is presented in Table II. Fig. 10 (a) shows the voltage gain comparison, in which among all the converters only the converters in [23]-[25] performance is superior to SCQBC but these converters have an overall component count of 16 and 14 respectively, thereby making the energy storage element count high. The SCQBC converter attains an output voltage of 400 V operating at a duty ratio of 0.658 featuring a superior voltage gain of 20 whereas the converter in [17] is operating at a dc static gain near 14 and that of converter [16], [18] and [19] are operating at a voltage gain about 10-12. Among all the stated converters, the converters in [20], [21] are observed to be providing the least voltage gain of 8.5 for the aforementioned duty ratio. In order to bring the uniformity between the topologies chosen for comparison a parameter known as effectiveness index (EI) is selected such that it will indicate the voltage gain per component at the given duty ratio. Thus, effectively connecting the respective voltage gain with the overall component count. Though the converters in [24] and [25] are having high EI value of 2.2 at 0.658 duty ratio but the proposed SCQBC converter also has improved EI at 1.62 as shown in Fig. 10 (b), which concludes that the proposed converter is still in par with the aforementioned converters in terms of voltage gain and EI comparison.

TABLE II
COMPARISON OF SCQBC CONVERTER WITH OTHER QUADRATIC BOOST CONVERTERS

Topology	Voltage Gain	NDVS ($\sum V_D/V_0$)	NSVS ($\sum V_S/V_0$)	NTVS (NDVS+NSVS)	ΔI_i	S/C/L/D (Total)
Ref [16]	$\frac{2-D}{(1-D)^2}$	1	1	2	Low	2/3/2/3 (10)
Ref [17]	$\frac{1+D}{(1-D)^2}$	$\frac{3}{1+D}$	$\frac{1}{1+D}$ $D=\frac{(2G+1)-\sqrt{8G+1}}{2G}$	$\frac{4}{1+D}$	Low	1/4/3/4 (12)
Ref [18]	$\frac{2-D}{(1-D)^2}$	$\frac{3}{2-D}$	$\frac{1}{2-D}$ $D=1-\frac{1}{2G}-\sqrt{\frac{1}{4G^2}+\frac{1}{G}}$	$\frac{4}{2-D}$	High	1/3/2/4 (10)
Ref [19]	$\frac{1+D-D^2}{(1-D)^2}$	1	$\frac{2-D}{1+D-D^2}$ $D=\frac{(2G+1)-\sqrt{4G+5}}{2(G+5)}$	$\frac{3-D^2}{1+D-D^2}$	High	2/2/2/2 (8)
Ref [20]	$\frac{1}{(1-D)^2}$	$\frac{1+2(1+\sqrt{G})}{G}$	$\frac{1+2(1+\sqrt{G})}{G}$	$\frac{2(1+2(1+\sqrt{G}))}{G}$	High	2/2/2/2 (8)
Ref [21]	$\frac{1}{(1-D)^2}$	$2-\frac{1}{G}$	1	$3-\frac{1}{G}$	Low	1/2/2/3 (8)
Ref [22]	$\frac{3-D}{(1-D)^2}$	$\frac{6-D}{3-D}$	$\frac{1}{3-D}$ $D=\frac{(2G+1)-\sqrt{8G+5}}{2G}$	$\frac{7-D}{3-D}$	High	1/6/3/6 (16)
Ref [23]	$\frac{3}{(1-D)^2}$	$\frac{10-3D-2D^2}{3}$	$\frac{2}{3}$ $D=1-\frac{\sqrt{3}}{G}$	$\frac{12-3D-2D^2}{3}$	High	1/5/3/7 (16)
Ref [24], [25]	$\frac{3+D}{(1-D)^2}$	$\frac{8-2D}{3+D}$	$\frac{2}{3+D}$ $D=\frac{(2G+1)-\sqrt{16G+1}}{2G}$	$\frac{10-2D}{3+D}$	Low	2/5/2/5 (14)
SCQBC	$\frac{3-D}{(1-D)^2}$	$\frac{7-3D}{3-D}$	$\frac{2-D}{3-D}$ $D=\frac{(2G+1)-\sqrt{8G+5}}{2G}$	$\frac{9-4D}{3-D}$	Low	2/4/2/4 (12)

$$\begin{bmatrix} \frac{d\hat{i}_{L1}(t)}{dt} \\ \frac{d\hat{i}_{L2}(t)}{dt} \\ \frac{d\hat{v}_{c1}(t)}{dt} \\ \frac{d\hat{v}_{c2}(t)}{dt} \\ \frac{d\hat{v}_{c3}(t)}{dt} \\ \frac{d\hat{v}_{c0}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-d)}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{-(1-2d)}{L_2} & \frac{(1-d)}{L_2} & 0 & 0 \\ \frac{1-d}{C} & \frac{-1}{C} & 0 & 0 & 0 & 0 \\ 0 & \frac{1-d}{C} & \frac{-d}{Cr} & \frac{-1}{Cr} & \frac{-(1-2d)}{Cr} & \frac{(1-d)}{Cr} \\ 0 & 0 & \frac{d}{Cr} & \frac{-(1-2d)}{Cr} & \frac{-1}{Cr} & \frac{(1-d)}{Cr} \\ 0 & 0 & 0 & \frac{(1-d)}{C_0 r} & \frac{(1-d)}{C_0 r} & \frac{-(1-(1-r)d)}{C_0 r R_0} \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{v}_{c1}(t) \\ \hat{v}_{c2}(t) \\ \hat{v}_{c3}(t) \\ \hat{v}_{c0}(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{v}_i(t) + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & \frac{2}{L_2} & \frac{-1}{L_2} & 0 & 0 \\ \frac{-1}{C} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C} & \frac{-1}{Cr} & 0 & \frac{2}{Cr} & \frac{-1}{Cr} \\ 0 & 0 & \frac{1}{Cr} & \frac{2}{Cr} & 0 & \frac{-1}{Cr} \\ 0 & 0 & 0 & \frac{-1}{C_0 r} & \frac{-1}{C_0 r} & \frac{-1}{R_0 C_0} + \left(\frac{R_0+r}{C_0 r R_0}\right) \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C0} \end{bmatrix} \hat{d}(t) \quad (19)$$

$$\left(\frac{\hat{v}_0(s)}{\hat{d}(s)} \Big/ \hat{v}_i(s)=0 \right) = \frac{-4.983\times10^{56}\, s^5 - 4.53\times10^{63}\, s^4 - 9.224\times10^{69}\, s^3 + 2.639\times10^{74}\, s^2 - 1.785\times10^{78}\, s + 2.348\times10^{82}}{3.405\times10^{52}\, s^6 + 3.212\times10^{59}\, s^5 + 7.209\times10^{65}\, s^4 + 4.543\times10^{67}\, s^3 + 8.245\times10^{73}\, s^2 + 9.772\times10^{74}\, s + 1.802\times10^{79}} \quad (20)$$

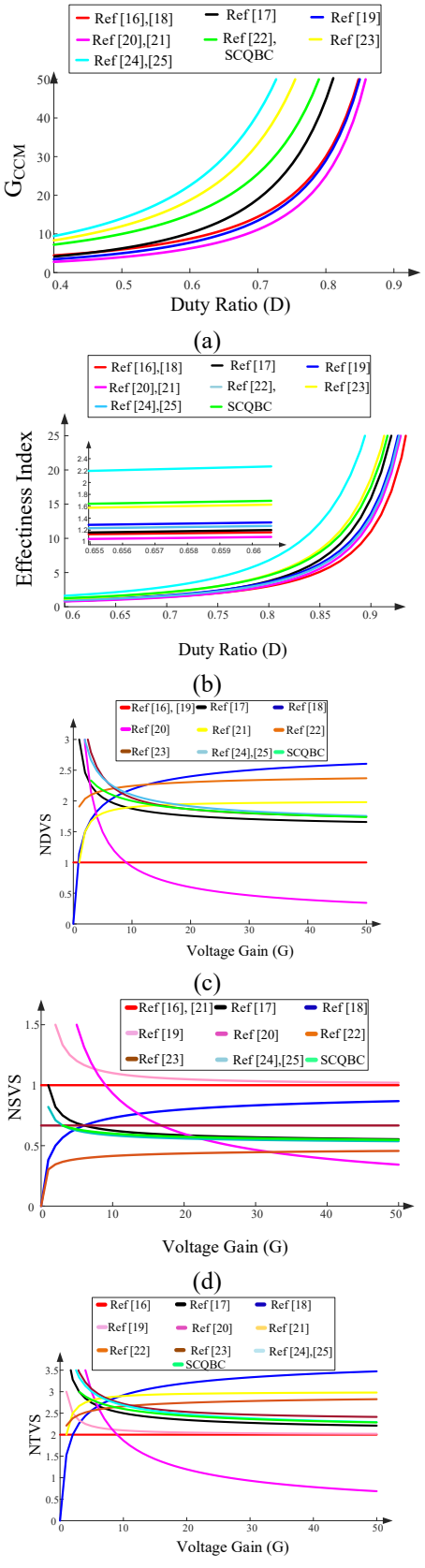


Fig. 10. Performance comparison of SCQBC converter with other quadratic boost DC-DC converters in terms of (a) voltage gain (G_{CCM}) (b) EI (c) NDVS (d) NSVS and (e) NTVS.

The semiconductor voltage stress is also one of the prominent features to evaluate the performance of any DC-DC converter. To understand the semiconductor voltage stress comparison, the particular type of the semiconducting element voltage stress are added and the cumulative is normalized with respect to the output voltage as expressed by the following NDVS, NSVS, and NTVS equations.

$$\left.\begin{aligned} \textit{Normalized Diode Voltage Stress } (NDVS) &= \frac{V_{D1}+V_{D2}+\ldots+V_{Dn}}{V_0} = \frac{\sum V_{Dx}}{V_0} \\ \textit{Normalized Switch Voltage Stress } (NSVS) &= \frac{V_{S1}+V_{S2}+\ldots+V_{Sn}}{V_0} = \frac{\sum V_{Sx}}{V_0} \\ \textit{Normalized Total Voltage Standing } (NSVS) &= NDVS+NSVS \end{aligned}\right\}$$

The NDVS of SCQBC converter is at 2.2 for a voltage gain of 20, which is observed to be moderate from Fig. 10 (c). Here in this aspect of NDVS, the converter in [20] performance is superior at an NDVS of 0.6 but the dc voltage gain attained is low. The converters in [18], [22] are having high NDVS thereby high diode voltage stress compared to all other converters. The succeeding parameter of discussion is NSVS and it is observed to be 0.57 for the SCQBC converter from Fig. 10 (d), this NSVS is lowest among all other converters. The converters in [17], [20] are having the same NSVS of 0.6, the converter in [17] has a voltage gain that is similarly comparable to the SCQBC converter, and for the converter in [20] source current ripple content is large. The NTVS of the stated SCQBC converter is observed to be 2.74 from Fig. 10 (e). Except for the converter in [20] remaining all converters NTVS is high, for which the voltage gain is very low (8.5), and hence its performance evaluation in this aspect is not relatable to the SCQBC converter. Although the NDVS and NSVS of the proposed converter are moderate but in the end the NTVS is substantially improved. This NTVS for the converters whose voltage gain is near the proposed converter is also crucial for comparison because it indicates the effective surface voltage stress of the converter. In this aspect, the converters in [21], [22] performances are not superior but the converters in [23]-[25] are having a NTVS which is closer to the stated SCQBC converter. The SCQBC converter is also having the features like moderate component count, low ripple content in input current and common ground for source and load, and minimum components in the forward path.

V. Experimental Validation

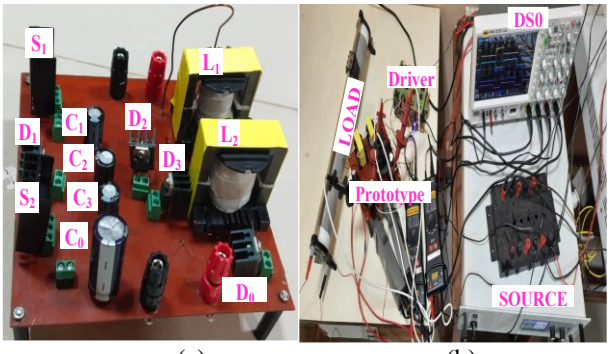


Fig. 11. SCQBC converter (a) prototype of (b) Experimental setup.

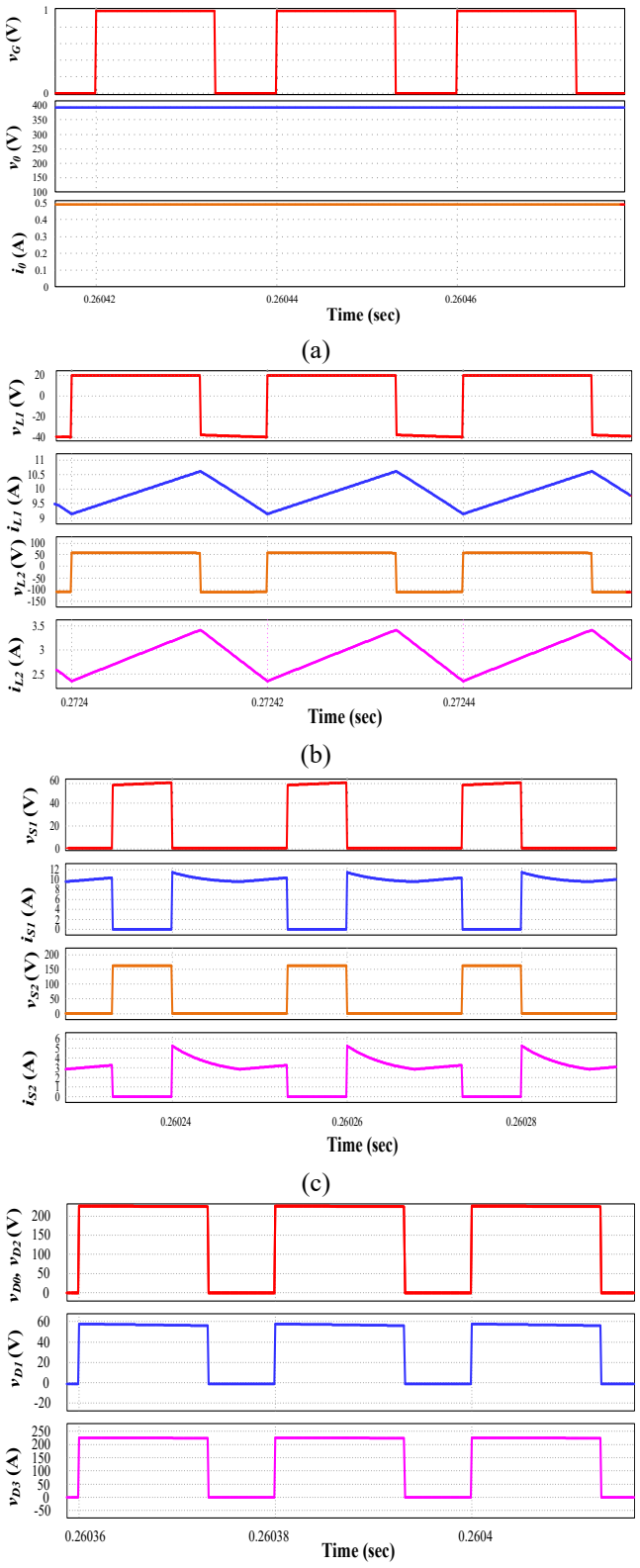


Fig. 12. Simulated results for SCQBC converter (a) input and output voltages v_i and v_0, load current i_0 (b) inductor voltages (v_{L1} and v_{L2}) and currents (i_{L1} and i_{L2}) (c) switch voltages (v_{S1} and v_{S2}) and currents (i_{S1} and i_{S2}) (d) diode voltages (V_{D0}–V_{D3}).

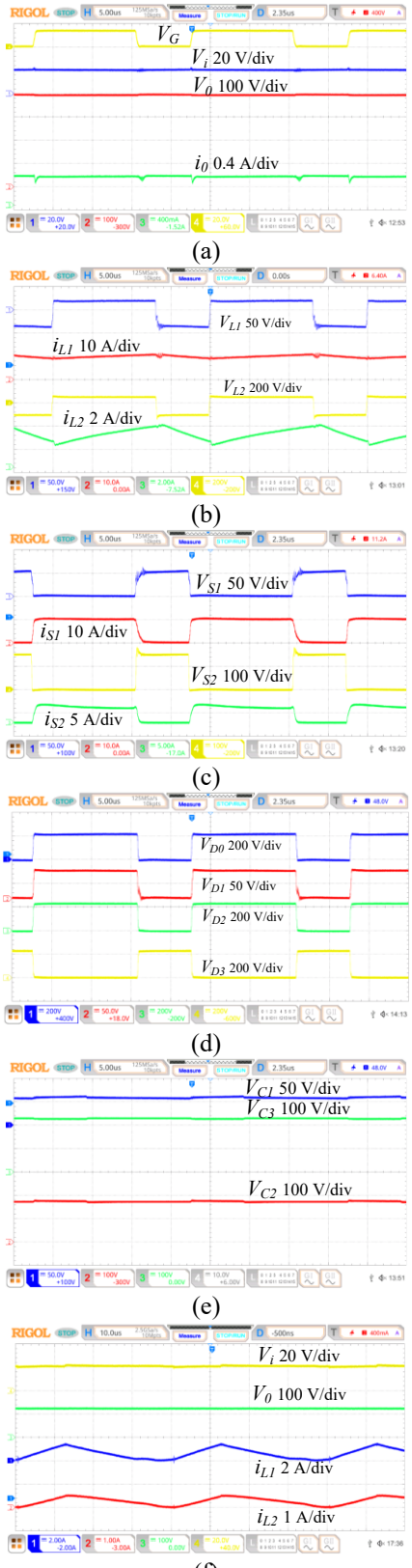


Fig. 13. SCQBC converter experimental validation (a) input and output voltages v_i-v_0, load current i_0 (b) inductor voltages (v_{L1}-v_{L2}) and currents (i_{L1}-i_{L2}) (c) switch voltages (v_{S1} and v_{S2}) and currents (i_{S1}-i_{S2}) (d) diode voltages (V_{D0}–V_{D3}) (e) capacitor Voltages (V_{C1}–V_{C3})and (f) DCM operation.

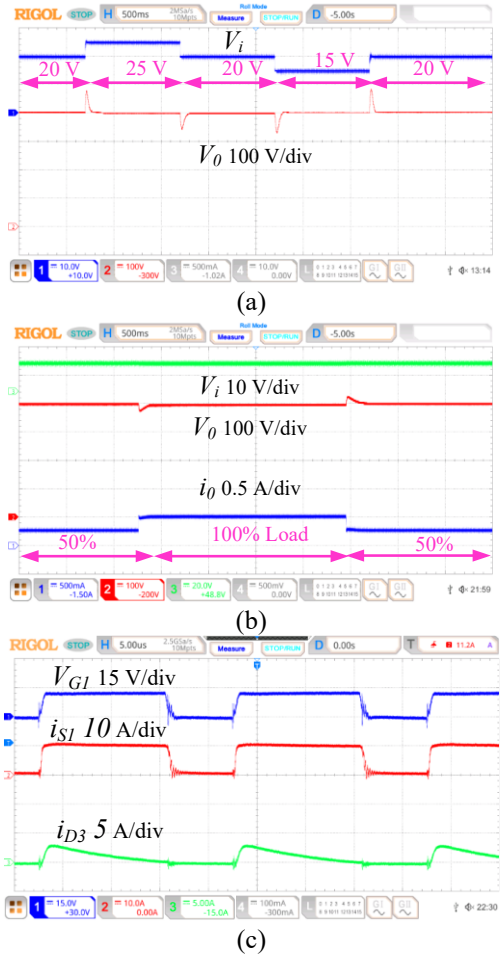


Fig. 14. Closed loop performance of SCQBC (a) stepped V_i (b) stepped load; and (c) diode D_3 and switch S_1 currents.

The simulated and experimental validation of the proposed SCQBC converter performance indices for a power rating of 200 W is shown in Fig. 11, with the prototype specifications as in Table III. All the simulated results from i.e., Fig. 12 (a), (b), (c) and (d) are in good accord with the ideal operating waveforms and the following experimental studies. The proposed converter attains an output voltage of 391 V at a load current of 489 mA for an applied voltage of 20 V as shown in Fig. 13 (a). The inductor voltages and currents are resembling their ideal wave shapes and are as shown in Fig. 13 (b). Since the entire input current passes through the inductor L_1, its ripple content will be low. The input current of the SCQBC converter is observed to be 10.08 A, making the converter's operating efficiency 94.84%.

The blocking voltage of switch S_1 is low and it is equal to the voltage stress of V_{C1}. The voltage stress on switch S_2 is greatly reduced and it is 43% of V_0 as shown in Fig. 13 (c). The diode D_1 blocking voltage is equal to switch S_1, and that of diodes D_0, D_2, and D_3 are at a voltage of $\frac{(2-D)V_0}{3-D}$, making the diode operating voltage stress 15% and 57% of V_0 as shown in Fig. 13 (d). It is evident from the aforementioned discussion that diodes and switches peak voltage stresses are always less than V_0. The capacitor voltage stresses (V_{C1}-V_{C3}) are as shown in Fig. 13 (e), in which as discussed earlier capacitors C_1, C_2, and C_3 are having a voltage stress of $\frac{V_0(1-D)}{(3-D)}$, $\frac{V_0}{(3-D)}$, and $\frac{V_0(2-D)}{(3-D)}$ i.e., the capacitors C_1, C_2 and C_3 are at a voltage stress of 15%, 43% and 57% of output voltage. A case study of proposed SCQBC converter with L_1=130 µH, L_2=700 µH, Switching frequency (f_s)= 25 kHz, load (R_0)=1300 Ω at a duty ratio of 34% is carried out to validate DCM performance indices as shown in Fig. 13 (f). The voltage gain G_{DCM} for an applied input voltage of 20 V is observed to be '6', which is in good accord with its ideal value as derived from (9).

The open loop control to output transfer function [26-28] of the SCQBC converter preceded by a PI controller of K_P=0.000015 and K_I=0.004 acquired a stable output voltage against source voltage and load current perturbations. The control performance of the SCQBC converter for a stepped voltage V_i from 15 V- 20 V- 25 V at a stable V_0 of 400 V is shown in Fig. 14 (a). In addition to the step changes in input voltage, a 50% step change in load is also considered to verify the SCQBC control performance as shown in Fig. 14 (b) and Fig. 14 (c) validates the peak currents caused by switched capacitor structure in mode I. Moreover, the feasibility of the proposed SCQBC converter is also demonstrated for different loading conditions and key results are presented in the Fig. 15. The theoretical and experimental efficiency variation concerning to load power is as shown in Fig. 16 (a) and the power loss distribution wheel of various elements for experimental case is as shown in Fig. 16 (b).

TABLE III
DESIGN SPECIFICATIONS

Specification	Rating	Simulation Details
Input voltage	20 V	
Output Voltage	400 V	
Power	200 W	
Inductors	L_1=130 µH, L_2=700 µH	
Capacitors	C_0=100 µF, C_1-C_3=22 µF	PSIM software Time Step 10E-7 sec
Diodes	D_0, D_2, D_3 (STPSC10H065)	
	D_1 (MBR10100)	
Switches	S_1 (FDPF3860T)	
	S_2 (STW28N65M2)	

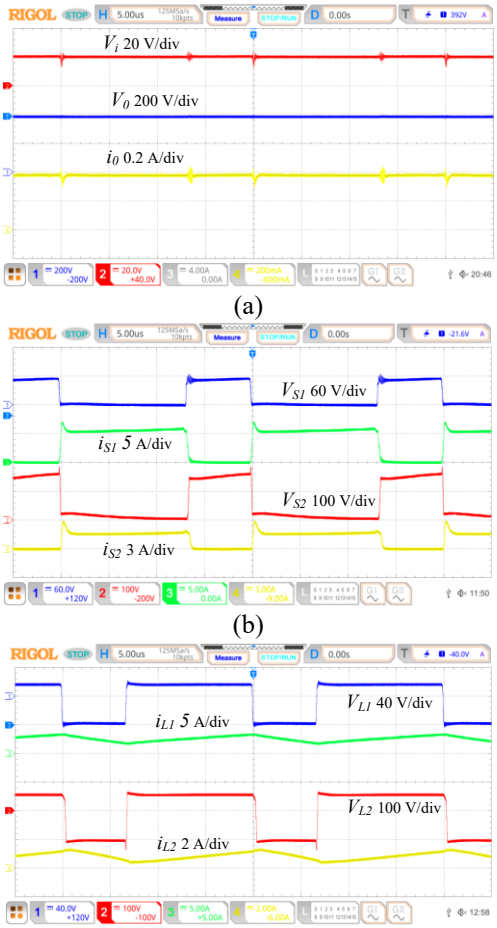


Fig. 15. Performance of SCQBC converter for load disturbance (a) input and output voltages v_i and v_0, load current i_0 at 3/4th load (b) switch voltages (v_{S1} and v_{S2}) and currents (i_{S1} and i_{S2}) at 1/2 load and (c) inductor voltages (v_{L1} and v_{L2}) and currents (i_{L1} and i_{L2}) at 1/4th load.

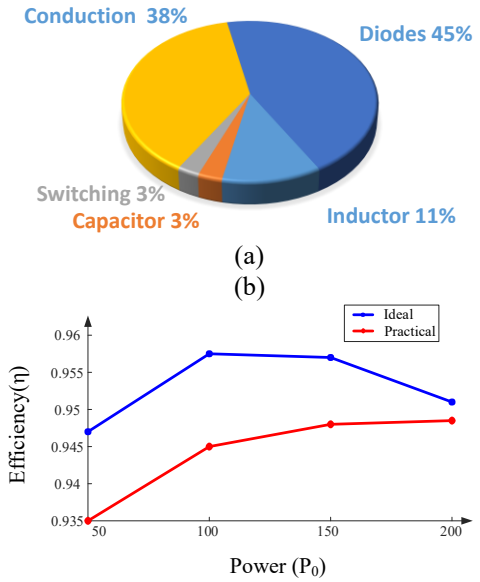


Fig. 16. SCQBC converter (a) efficiency and (b) loss distribution among various elements.

VI. Conclusion

A switched-capacitor-based quadratic boost converter is presented in this article. The major contributions proposed SCQBC converter are low ripple content in the input current and retaining an absolute common ground with other features being ultrahigh step-up gain at a moderate duty cycle, low semiconductor voltage stress, and minimum components in the forward path. The operating principle of SCQBC converter with CCM and DCM analyses is presented in this article. The proposed converter performance indices comparison with other similar quadratic boost converters is also presented in this article. In view of the voltage gain and energy storage element count the conclusive remarks of performance comparison are that the proposed SCQBC converter possess improved effectiveness index and switch voltage stress profile. Furthermore, to demonstrate the feasibility of the SCQBC converter a scaled laboratory prototype of 200 W, 400 V, 50 kHz operating with a peak efficiency of 95.4% is developed. The proposed converter feasibility for its performance indices under DCM mode of operation is also demonstrated.

VII. Appendix

By applying the KCL and amp-sec balance principle for all the capacitors in SCQBC converter the steady state peak current stresses of the semiconductors are as presented in Table IV.

Apart from the mentioned peak currents in Table IV, additional currents are also practically exist because of the instantaneous voltage difference in the ripple voltages of various capacitors especially in the forward path of mode 1 operation. Prior to the switching instant there exist a difference of ripple voltage $\Delta v_c(0)$ among the capacitors of SC structure (C_1-S_1-C_2-D_3-C_3-S_2) as shown in Fig. 1. Due to which semiconductors in this path experiences peak inrush currents, the analysis of aforesaid peak currents is as follows

$$\Delta v_c(0)=\frac{\Delta v_{c1}(0)}{2}+\frac{\Delta v_{c2}(0)}{2}-\frac{\Delta v_{c3}(0)}{2}$$

$$\Delta v_c(0)=\frac{1}{2C}\int_{DT_S}^{T_S}\overbrace{\{I_{C1\text{-}OFF}\}}^{\Delta v_{c1}(0)}+\overbrace{\{I_{C2\text{-}OFF}\}}^{\Delta v_{c2}(0)}-\overbrace{\{I_{C3\text{-}OFF}\}}^{\Delta v_{c3}(0)}$$

Further rearranging and simplifying, the $\Delta v_c(0)$ is expressed as

$$\Delta v_c(0)=\frac{1}{2Cf_S}\left(\frac{3\text{-}D}{1\text{-}D}\right)\frac{V_0}{R_0} \tag{21}$$

Assuming the overall SC structure ESR as R'

$$R'=(3r_c+2r_s+r_D)$$

Using (21) the additional instantaneous current that the switches (S_1 & S_2) and diode D_3 have to carry is expressed as

$$i_{D3}(0)=i_{s1,2}(0)=\frac{\Delta v_c(0)}{R'}=\frac{1}{2Cf_S}\left(\frac{3\text{-}D}{1\text{-}D}\right)\frac{V_0}{R_0}\times\frac{1}{(3r_c+2r_s+r_D)}$$

TABLE IV
SEMICONDUCTOR ELEMENT PEAK CURRENT STRESS

$$\hat{I}_{S1}=\frac{(1+D)I_0}{D\,(1\text{-}D)^2}$$

$$\hat{I}_{S2}=\frac{(1+D)I_0}{D\,(1\text{-}D)}$$

$$\hat{I}_{D1}=\frac{(1+D)I_0}{(1-D)^2}$$

$$\hat{I}_{D0}=\hat{I}_{D2}=\frac{I_0}{(1-D)}$$

$$\hat{I}_{D3}=\frac{I_0}{D}$$

ACKNOWLEDGEMENTS

The authors express their gratitude to Mr. P. Ravi Teja for helping to conduct the additional experimentation required for the revised manuscript.

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