Stability Assessment and Simplified Control Strategy for DC Microgrids with Constant Power Load

Ram Krishan, Senior Member, IEEE, Rohith Y., M Pavan Kumar
Department of Electrical Engineering
National Institute of Technology Warangal, India
rkrishan@nitw.ac.in

2024 IEEE Power & Energy Society General Meeting (PESGM) | 979-8-3503-8183-2/24/$31.00 ©2024 IEEE | DOI: 10.1109/PESGM51994.2024.10688752

***Abstract*—Dynamic performance of the DC microgrid is seriously affected due to negative impedance characteristics of the constant power loads (CPL). It deteriorates the system damping, especially when network impedance is not negligible. In this condition, stability margin assessment and DC-DC converter control are essential. This paper proposes a novel and straightforward virtual negative impedance-based control loop for analysing the stability and design of the controllers for DC-DC converters connected at both source and load ends to enhance the CPL stabilization. First, a simple pole-zero criterion-based strategy is used to evaluate the virtual negative resistance. Further, small-signal and extended large-signal models of the bidirectional buck/boost are proposed for assessing system stability with CPL. A comparative stability analysis is conducted to illustrate the system's resilience in the face of changes in parameter values. Also, eigenvalue analysis and real-time simulations are performed with the proposed control strategy at the load and source side converters without affecting the load side voltage profile to demonstrate its effectiveness.**

***Index Terms*—Constant power loads, DC microgrid, Negative impedance control, Stability margin, Virtual droop.**

I. Introduction

With increasing demand of energy and environmental concern, DC microgrid is rapidly gaining ground for harnessing renewable energy sources (RES) to establish a sustainable and cost-effective solution. DC microgrids have enhanced efficiency, flexibility and controllability [1] to adopt diversified distributed generators and loads. These diversified components in a system demand efficient control strategies for a smooth and stable operation [2], [3]. Specifically, in DC microgrids (DCMG) that incorporate constant power loads (CPLs), the foremost concern revolves around system stability, primarily because of the adverse impact of CPLs' negative impedance characteristics which deteriorates the system damping. Nowadays, it is essential to assess the CPL stability of the DC microgrid [4].

The modelling of voltage, current and power control loops for the converters connected at sources side is broadly discussed in [5]. It is based on power-sharing among the DGs in islanded DC microgrid, however stability criterion is not verified properly. The authors in [6] deal with the parallel operation of DGs using droop control techniques without sufficient stability margin. Moreover, in [7], the droop control method has been proposed for sharing the power among the inverter-based generators. The stability criterion for AC microgrid with CPL has been given in [8], where physical dampers are introduced to increase the system damping. This is a passive damping method where a large capacitor or resistor is deployed. The damping effect in DCMGs is realized in Aircraft, ships and space shuttles. Research is happening in these domains, but finding the solution for the stabilization and sharing of loads, especially the CPL loads needs to be more comprehensive. The instability caused by CPL is also discussed. The paper [8] discusses the stability criterion used for the DCMGs analysis. The primary stabilization techniques with CPL using small signal stability criteria have been developed in [9]. Almost all methods have been implemented at the source side converter, except, where sufficient stability criteria for the DCMGs are discussed. This criterion can be used to design efficient controllers for AC and DC microgrids. Controlling at the source side may limit the flexibility of the microgrid because the control system only has access to the sources, such as RESs, and cannot directly control the loads. In [10], the author has proposed a controller for the load-side converter. Large signal stabilization techniques are used in [5]. The secondary stabilization techniques are used in [11]. Tertiary control techniques are developed in [12]. A large signal stability analysis of an AC microgrid using a distributed control algorithm is given in the previous researches. In this paper, CPL impacts are ignored. Recently, Machine Learning algorithms have also been proposed for stabilization of CPLs in microgrids.

A. Contributions

Source-side control limits the system's flexibility, voltage regulation and responsiveness to load conditions changes. Since the source-side controllers are centralized, adapting to dynamic load variations or incorporating new loads may be challenging. In contrast, a load-side control enables effective load management and voltage regulation in a DC microgrid. This flexibility in load management improves the overall system efficiency and ensures stable operation. Therefore, this

This research was partially supported by the Department of Science and Technologies (DST), India through the SERB project (grant number SRG/2021/000810) and the NSM project (Reference: DST/NSM/R&D/HPC Applications/2021/03.31.).

paper proposes a load-side control strategy that can effectively be implemented at the load side to enhance the stability margin.

Summarizing, the main contribution of this paper are the following:

- Small-signal modelling and design of a novel virtual resistance-based control loop to ensure the stability of DC microgrid with CPL
- Load side as well as source side control strategies to enhance the CPL stability margin

The remaining paper is organized in 5 sections. Modelling of DC microgrid components is given in Section II. Control and stability criterion are discussed in Section III. Section IV describes the evaluation of controlling parameters and proposed virtual negative inductance control strategies and also, demonstrated through the numerical simulation to validate its effectiveness for CPL stabilization in a DC microgrid. Final conclusions and future scopes are given in Section V.

II. MODELLING OF DC MICROGRID SYSTEM

The effective mathematical modelling of individual microgrid components (loads, converters, sources, etc.) is essential for analysing system behaviour in real-time operating scenarios. There are two types of modelling: small signal and large signal. Small-signal modelling is where the models are linearised around an operating point for stability and control analysis. In contrast, the large signal modelling is non-linear and includes an exact model of the individual components.

A. Small signal model of CPL

Although many types of load can exist in a DCMG system, some loads are tightly controlled by PECs and draw constant power irrespective of the system voltage. These constant power loads (CPL) introduce negative impedance in the system, which may impact the stability margin of the DCMG system. In this paper, the stability of CPL in a DCMG is considered. Mathematical model of the CPL can be given as

$$P_{CPL} = V_{load} \times I_{load} = Constant \tag{1}$$

Where
V_{load} = CPL load terminal voltage
I_{load} = CPL load current
P_{CPL} = Power drawn by CPL

If the operating point is (V_{load},I_{load}), CPL can be defined as,

$$V = slope * I + C \tag{2}$$

$$slope = \frac{\partial V_{load}}{\partial I_{load}} = R_{CPL} = -\frac{V_{load}^2}{P_{CPL}} \tag{3}$$

At the operating point eq (2) can be written as

$$I = \frac{V}{R_{CPL}} + \frac{2P_{CPL}}{V_{load}} \tag{4}$$

This linearised small-signal model of CPL can be used for stability analysis and developing an effective control strategy. A non-linear model of the CPL is derived in the subsequent subsection.

B. Converters modelling

In a DCMG, bi-directional DC-DC converters are used to integrate RES and loads. A simple mathematical model for these converters can be given as follows.

1) Bi-directional boost converter: A simplest bi-directional boost converter circuit consists of input DC voltage sources, two switches operated as per the duty ratio D, a set of resistance R_{in} and inductance L_{in} , and a capacitor C_{in} across the converter terminal. Using fundamental laws Kirchhoff's current (KCL) and voltage (KVL), dynamic model of the converters can be written as - The dynamic equations are given as,

$$L_{in}\frac{di_L}{dt} = V_{dc} - R_{in}i_L - (1-D)V_o \tag{5}$$

$$C_{in}\frac{dV_o}{dt} = (1-D)i_L - i_o \tag{6}$$

For small disturbance around the steady state values, dynamic equations (5) and (6) can be written in following simplified expressions

$$L_{in}\frac{d\hat{i}_L}{dt} = (\hat{V}_{dc}) - R_{in}(\hat{i}_L) - (1-D)\hat{V}_o + \hat{d}V_o \tag{7}$$

$$C_{in}\frac{d(\hat{V}_o)}{dt} = (1-D)\hat{i}_L + \hat{d}(i_L) - (\hat{i}_o) \tag{8}$$

2) Modelling of Controller for DC-DC converters: A dual loop controller is required to regulate the DC-DC converter output voltage. A general controlling structure of the dual loop controller is illustrated in Fig. 1, and its large signal model is expressed in eq (9).

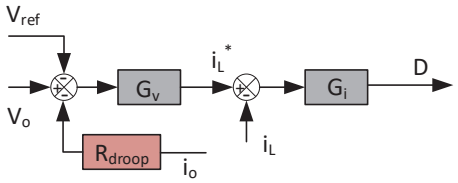


Figure 1: Control structure of converters

$$D = K_{pi}[K_{pv}(V_o^* - V_o) + K_{iv}\int(V_o^* - V_o)dt - i_L] + K_{ii}\int[K_{pv}(V_o^* - V_o) + K_{iv}\int(V_o^* - V_o)dt - i_L]dt \tag{9}$$

where,
G_v = PI voltage controller
G_i = PI current controller
V_o^* = V_{ref} = Reference output voltage
K_{pv} = Proportional gain of voltage controller
K_{pi} = Proportional gain of current controller
K_{iv} = Integral gain of voltage controller
K_{ii} = Integral gain of current controller
i_L = Actual inductor current in converter
V_o = Actual output voltage of controller
i_o = Actual output current of controller
i_L^* = Reference inductor current
R_{droop}= Output voltage and current of converter Droop
D = PWM Duty cycle

Details on linearizing dynamic equations of the converter and the duty cycle given in eq.(9) can be found in [4]. Further, this converter model can be represented by an equivalent source connected with an impedance $Z_o(s)$ (eq.11) and the transfer functions of small signal model can be found as in eq.(10)

$$Z_o(s) = -\frac{\hat{V}_o(s)}{\hat{i}_o(s)} \tag{10}$$

$$Z_o(s) = \frac{Z_{out}(1 + G_i G_{id}) - A_{io} G_i G_{vd} + R_{droop} G_v G_i G_{vd}}{1 + G_i G_{id} + G_v G_i G_{vd}} \tag{11}$$

Here the $A_{vo}(s)$ is derived as

$$A_{vo} = \frac{\hat{V}_o(s)}{\hat{V}_{dc}(s)}\bigg|_{\hat{d}(s),\hat{i}_o(s)=0} = \frac{1-D}{s^2 L_{in} C_{in} + s C_{in} R_{in} + (1-D)^2}$$

The output impedance of boost converter can be calculated from equation (11) with transfer functions derived above. A similar derivation can be done for bidirectional buck converter. The output impedance of the buck converter from eq (11) with transfer functions mentioned above.

III. Stability Criterion and Calculation of Negative Impedance

In this section, concept of the proposed virtual negative impedance loop is described for enhancement of DCMG stability in the presence of CPL. First, the stability of converters is analyzed using the small signal model of the DCMG. Similar to the approach given in [4], a stability criterion-based approach is proposed for the DCMG's PECs.

A. Bi-directional boost converter stability criterion

In the recent research [13], it was seen that the destabilizing impact of CPL is profound when voltage regulation is insufficient, or a smaller DC link capacitor is used. The dynamic model of the converters considered in the DCMG is derived in eqs (5) and (6). The converter output current is dependent to the load connected across its terminal. Let the load current in i_o due the terminal load $R = R_{CPL} \parallel R_{dc}$) where, R_{CPL} = CPL resistance and R_{dc} = Resistive load . This load current can be written as

$$i_o = V_o / R \tag{12}$$

Converter transfer function can be rewritten with substitution of i_o in eqs (7) and(8), and expressed in Laplace transform as

$$s L_{in} \hat{i}_L(s) = \hat{V}_{dc}(s) - R_{in} \hat{i}_L(s) - (1-D)\hat{V}_o(s) + \hat{d}(s) V_o \tag{13}$$

$$s C_{in} \hat{V}_o(s) = (1-D)\hat{i}_L(s) + \hat{d}(s)(i_L) - \frac{\hat{V}_o(s)}{R} \tag{14}$$

From eq (13), the transfer function $\frac{\hat{V}_o(s)}{\hat{d}(s)}$ is derived as shown below

$$i_L(s) = \frac{(s C_{in} + \frac{1}{R})\hat{V}_o(s) + \hat{d}(s) i_L}{1-D} \tag{15}$$

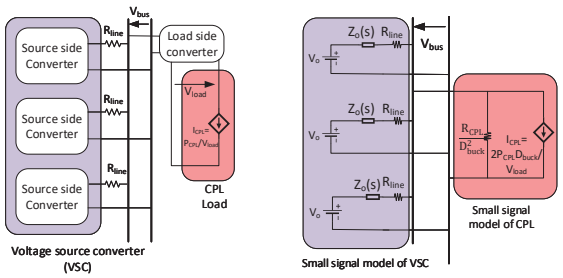


Figure 2: (a) Load side control microgrid (b) Small signal model of microgrid

Substituting equation (15) in equation (13) gives

$$\frac{\hat{V}_o(s)}{\hat{d}(s)} = \frac{(1-D)V_o - (R_{in} + sL_{in})i_L}{L_{in}C_{in}s^2 + s(\frac{L_{in}}{R} + R_{in}C_{in}) + (D-1)^2 + \frac{R_{in}}{R}} \tag{16}$$

In order to have a stable system, roots of the denominator in eq. (16) should be on the left side of $j\omega$ axis. The real part of roots should be negative.The above analysis is done assuming the PI controllers are very fast. Then L_{in}, C_{in}, R_{in} is always positive so,

$$\frac{1}{R} > 0 \implies \frac{R_{dc} - \frac{V^2}{P_{CPL}}}{R_{dc}.(-\frac{V^2}{P_{CPL}})} > 0 \implies R_{dc} < \frac{V^2}{P_{CPL}} \tag{17}$$

P_{CPL} is the CPL power, V is the terminal voltage of the CPL load. If equation (17) is satisfied then the boost converter is stable.

Similar to the analysis of bi-directional boost converter, transfer function for the buck converter can be derived. Similarly, The stability criterion for bi-directional buck converter is derived.

B. Load side converter stability criterion

A control strategy can be employed to the PEC connected at the load end, as shown in Fig. 2 (a). It is important to note that the source-side converters are bi-directional boost converters, whereas the load-side converter is a bi-directional buck converter. The small signal equivalent and its Thevenin equivalent circuit are depicted in Fig. 2 (b) and 3, respectively. This equivalent circuit is designed after referring the loads connected across the converter output to the source side, just like a transformer having a turns ratio $(1 : D)$. In Fig 3,

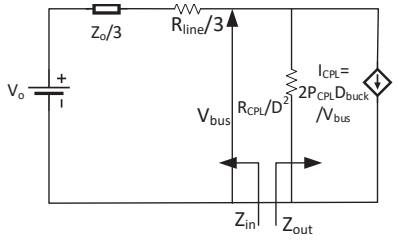


Figure 3: equivalent model of microgrid

Table I: Source side converter parameters

Variable	Description	value
V_{dc}	Source voltage	48
V_{ref}	Bus reference voltage	200 V
L_{in}	Converter Inductance	2 mH
C_{in}	Converter Capacitance	2200 μF
R_{in}	Converter resistance in series with inductance	0.04 ohms
R_{line}	line resistance	0.08 ohms
F_{sw}	switching frequency	10 KHz
R_{droop}	voltage current droop of converter	0.4
Kpv	Proportional gain of PI voltage controller	0.1061
Kiv	Integral gain of PI based voltage controller	50
Kiv	Proportional gain of PI based current controller	18.8495
Kii	Integral gain of PI based current controller	376.991

$$Z_{in} = (Z_o + R_{line})/3 \quad and \quad Z_{out} = (R_{CPL}/D_{buck}^2$$
$$T_m = Z_{in}/Z_{out}$$
$$\frac{1}{T_m + 1} = \frac{1}{\frac{(Z_o+R_{line})/3}{R_{CPL}/D_{buck}^2} + 1} \tag{18}$$

Like the stabilization criterion used in bi-directional boost converter, $\frac{1}{T_m+1}$ should have the roots left to the $j\omega$ axis.

IV. PROPOSED CONTROL STRATEGY AND STABILITY ANALYSIS

This section proposes a novel negative resistance method to stabilize the instability caused by the CPL loads on the grid. The converter control structure discussed above (Fig. 1) is modified with the proposed negative resistance loop as in Fig. 4. This small signal model is used for finding the $Z_o(s)$ for each converter discussed in sections II-B2 and III-B, respectively, with the proposed negative resistance loop. The Fig. 4 is the control structure used for real-time simulation. The following parts discuss the stability margin of MG without the proposed loop using $\frac{1}{1+T_m}$ from section III and the stability margin of the MG with the proposed loop at the source side or load side using $\frac{1}{1+T_m}$ with $Z_o(s)$ calculated from the enhanced small-signal model.

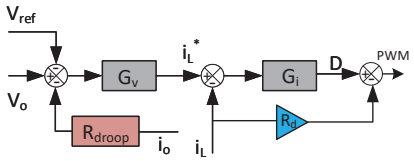
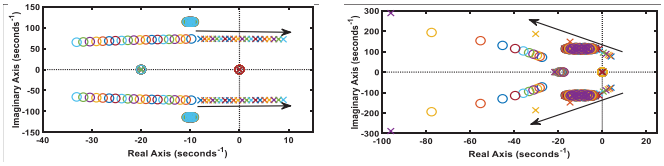


Figure 4: Proposed control loop structure for converters

The Pole-Zero plots are found by varying the 'R_d' in the derived transfer functions. The proposed control strategy selects an optimal value of R_d using these pole-zero plots for the system stability. Detailed stability analysis is given in the following sub-sections.

A. Source side control

1) Bi-directional boost converter as VSC: A voltage source converter (VSC) consisting of the bi-directional boost converter is used to connect the 48V DC source with a common DC bus of the DCMG operating at 200V DC. The source side converter and microgrid parameters are given in Table I. The trial and error method is used to find the gains of the proportional-integral (PI) based controllers. The system stability is analyzed using the eq. $\frac{1}{T_m+1}$ derived from eq. (18).



(a) (b)

Figure 5: (a) Stability margin with source side converter (b) Root-locus when R_d is varied from -1 to -12

a) Stability margin: The stability margin of the system is assessed using a pole-zero plot of the function $\frac{1}{T_m+1}$. The CPL load in the DCMG is increased slowly from 1KW to 20 KW. At around 10kW, the system poles are moved to the right of $j\omega$ axis. It is shown in Fig 5(a). So, the system is stable for the CPL less than 10 KW. Any CPL load greater or equal to 10 KW in the microgrid with a bi-directional boost converter as VSC becomes unstable.

b) Stability margin with proposed control strategy: The proposed negative impedance loop with R_d is now performed to enhance the CPL stability limits up to 15 kW. By varying the R_d value from -1 to -12 in steps of 1, the pole-zero plot of $\frac{1}{T_m+1}$ is drawn to show the movement of poles (eigenvalues) towards the stable region (left of the $j\omega$ axis). This DCMG stability assessment is depicted in Fig. 5 (b). The R_d is chosen to be -10.5 so that stability margin of the grid is increased from 10KW to 15KW of CPL. The stability margin increased by 50%. At $R_d = -10.5$, the droop of converters is changed from 0.05 to 0.2 in steps of 0.05. The pole-zero plot of the grid is shown in Fig. 6 (a). It can be seen that the stability of the DCMG is not much affected by the droop values. Hence, the proposed control strategy is almost independent of droop value R_{droop}.

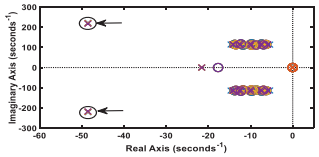


Figure 6: Root locus for R_{droop} = 0.05 to 0.2

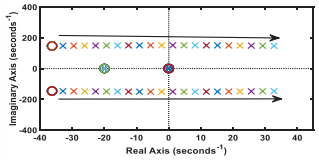


Figure 7: Stability with bidirectional converter

B. Load side control

The micro grid has a bi-directional boost converter at the source side, whereas a bi-directional buck converter at the load-side. If the controlling needs to be done at the load-side, the system dynamics are always decided by the slower response component in the grid. So, the load-side converter dynamics should be slower than the source-side converter. The source side converter parameters are shown in Table II, and the load side converter parameters are shown in Table III and all other parameters are the same as shown in Table I. The stability of the system is analyzed using eq. (18).

Table II: Source side converter parameters for load side control

Variable	Description	Value
Kpv	Proportional gain of PI voltage controller	0.1061
Kiv	Integral gain of PI voltage controller	50
Kpi	Proportional gain of PI current controller	12.5663
Kii	Integral gain of PI current controller	251.3274
Fsw	Switching frequency	15 KHz
Rdroop	Voltage current droop of converter	0.05

Table III: load side converter parameters

Variable	Description	value
Vdc	Bus Voltage	200 V
Vref	load terminal reference voltage	150 V
Rdroop	voltage current droop of Converter	0

1) Stability margin: The CPL is varied from 1KW to 8KW in steps of 1KW the pole zero plot of the $\frac{1}{1+T_m}$ is shown in Fig.7. As, the CPL increases on the grid shown stability decreases and poles are moving to right of jω axis. The stability margin of system is about 4KW. For any CPL load greater than or equal to 4 KW make system unstable as the poles of $\frac{1}{T_m+1}$ lie on the right of jω axis.

2) Negative inductance droop method: At load side, there is no droop but for stabilization a negative inductance droop is incorporated using the proposed controlling structure for load side converter as in Fig. 8. Due to negative droop inductance a differential term sL_{droop} to reduce its effects a filter is used along with it so the total droop is given as $\frac{sL_{droop}}{sT+1}$ appropriate filter design should be used to counter the differential gain produced to the noise in the system. Where, T=Time constant of the filter = 1m sec, L_{droop} = inductance droop.

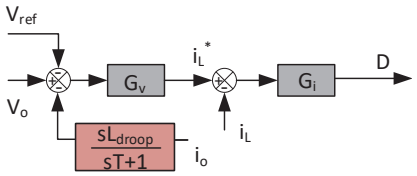


Figure 8: Negative inductance droop control structure

The CPL is maintained at 8KW and the L_{droop} is changed from -1mH to -0.025H, the poles of system $\frac{1}{T_m+1}$ moves to left as shown in Fig. 9

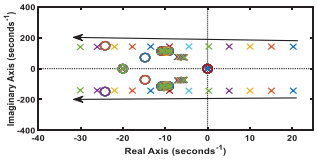


Figure 9: Root locus when L_{droop} is -1mH to -0.025H

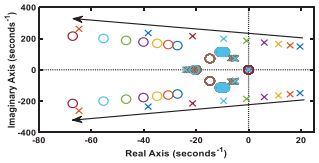


Figure 10: Root locus when R_d is varied from -1 to -10

The L_{droop} is chosen to be -0.025H to have stability margin of system up-to 8KW of CPL.

3) Proposed control strategy: The proposed control strategy is incorporated at load side. The CPL on the grid is maintained at 8KW so that instability is created on the grid. The R_d is varied from -1 to -10 , the poles lying on the right side of jω axis is moves to the left of jω axis as shown in Fig. 10. The R_d is chosen to be -12.5 to have system stability margin till 8KW of CPL. The stability margin increased by 100%.

V. Conclusion

This paper proposes a modified virtual negative impedance-based control loop for the converters connected at both load and source end to enhance the CPL stability margin of a DCMG. Pole-zero-based stabilization criterion is developed and tested with the Small-signal models of DCMG having source side control and load side control techniques. The effectiveness of the proposed control loop is demonstrated with a DCMG, and the results are compared with the existing virtual negative impedance droop method. Sometimes, the existing virtual impedance droop method gives faster control at the cost of complex implementation and filter design. However, the proposed stabilization strategy doesn't require any filter design and is easy to implement with comparable faster stability control.

References

[1] K. Jithin, P. P. Haridev, N. Mayadevi, R. H. Kumar, and V. P. Mini, "A review on challenges in dc microgrid planning and implementation," *Journal of Modern Power Systems and Clean Energy*, pp. 1–21, 2022.

[2] Y. Reddy O, J. J, A. K. Chakraborty, and J. M. Guerrero, "Stability constrained optimal operation of standalone dc microgrids considering load and solar pv uncertainties," *IEEE Transactions on Power Delivery*, pp. 1–9, 2023.

[3] M. S. Alam, F. S. Al-Ismail, S. M. Rahman, M. Shafiullah, and M. A. Hossain, "Planning and protection of dc microgrid: A critical review on recent developments," *Engineering Science and Technology, an International Journal*, vol. 41, p. 101404, 2023.

[4] S. Liu, P. Su, and L. Zhang, "A virtual negative inductor stabilizing strategy for dc microgrid with constant power loads," *IEEE Access*, vol. 6, pp. 59 728–59 741, 2018.

[5] Z. Zhang, X. Yang, S. Zhao, D. Wu, J. Cao, M. Gao, G. Zeng, and Z. Wang, "Large-signal stability analysis of islanded dc microgrids with multiple types of loads," *International Journal of Electrical Power & Energy Systems*, vol. 143, p. 108450, 2022.

[6] N. Pogaku, M. Prodanovic, and T. C. Green, "Modeling, analysis and testing of autonomous operation of an inverter-based microgrid," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 613–625, 2007.

[7] A. Aggarwal, A. S. Siddiqui, and S. Mishra, "State space modelling and stability analysis of ac micro-grids for different configurations," in *2022 IEEE IAS Global Conference on Emerging Technologies (GlobConET)*, 2022, pp. 936–941.

[8] A. Riccobono and E. Santi, "Comprehensive review of stability criteria for dc power distribution systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3525–3535, 2014.

[9] R. Kumar, R. Sharma, and A. Kumar, "Adaptive negative impedance strategy for stability improvement in dc microgrid with constant power loads," *Computers and Electrical Engineering*, vol. 94, p. 107296, 2021.

[10] M. Adly and K. Strunz, "Dc microgrid small-signal stability and control: Sufficient stability criterion and stabilizer design," *Sustainable Energy, Grids and Networks*, vol. 26, p. 100435, 2021.

[11] N. Ghanbari and S. Bhattacharya, "Constant power load challenges in droop controlled dc microgrids," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 3871–3876.

[12] S. Moayedi and A. Davoudi, "Distributed tertiary control of dc microgrid clusters," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1717–1733, 2016.

[13] F. Gao, S. Bozhko, A. Costabeber, C. Patel, P. Wheeler, C. I. Hill, and G. Asher, "Comparative stability analysis of droop control approaches in voltage-source-converter-based dc microgrids," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2395–2415, 2017.